OSPO Plans: Hardware

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Open Hardware at CERN: a bit of history

- See https://www.oshwa.org/research/brief-history-of-open-source-hardware-organizations-and-definitions/ for the history of Open Source Hardware (OSHW) and CERN's place in it
- Pioneering role since 2008
- The Open Hardware Repository
- The CERN Open Hardware Licence (thanks KT, Myriam!)
  - March 2011: version 1.0
  - July 2011: version 1.1
  - September 2013: version 1.2
  - March 2020: version 2.0
    - Only hardware licence approved by the Open Source Initiative (OSI)
    - Recommended for all types of hardware (including gateware) by choosealicense.com (part of GitHub)
    - Recommended by the Open Source Hardware Association (OSHWA) for hardware and gateware
    - Covers gateware well and provides support for three sharing regimes (see later)

A preliminary question

In the following slides, when I say “hardware” I mean electronics. Is there anybody interested in open-source mechanics (or some other hardware) who would like to take a leading role in this domain?

And similarly

Should we include design of Application-Specific Integrated Circuits (ASIC) with open-source Process Design Kits (PDK) in the scope of the OSPO?

The tools issue

When you open-source hardware or gateware, you expect that others can freely open, edit, simulate, etc, your design. The use of FOSS for hardware design and gateware design/simulation is desirable but not always possible. This could be discussed in the frame of the upcoming ELEC committee (and CAEC if we include mechanical CAD in the discussion). Proprietary tools can even be a risk in terms of our ability to fulfil our basic mandate.

The CERN Component Libraries

Can they be open-sourced? Altium, Cadence, KiCad libraries? What would be the cost and who would pay?

Best practices for OSHW at CERN: some initial ideas for discussion

- Working with BE-CEM-EPR (CERN design office)
  - Using CERN component libraries
  - Design rules
  - Storing files in a standardised EDMS structure
- Design reviews (schematics, layout)
- Production readiness review
  - Development of a Production Test System (PTS)
  - Prototypes shown to work in as diverse environments as possible
- Involving companies and Knowledge Transfer (KT) early on. In some cases one might go as far as creating a consortium (e.g. White Rabbit Collaboration, thanks KT!).
- Template for electronic production procurement
- Documentation: user manual, designer manual

Best practices for OSHW at CERN: some initial ideas for discussion

- Licensing
  - CERN Open Hardware Licence and its three variants:
    - Permissive (P)
    - Weakly reciprocal (W)
    - Strongly reciprocal (S)
- Project mandate and milestone plan
- Landing page with short description, status, contact, users, producers, etc. See evolution of the Open Hardware Repository (https://ohwr.org)
- Use of an issue tracking system (GitLab, Jira)

Open question

KT is the entry point for hardware disclosures. To be discussed/decided: is gateware more like hardware or like software when it comes to the default entry point (KT or OSPO)? This will be decided by OSPO/KT but any comments/suggestions from you are very welcome.

Best practices for OS gateware at CERN: some initial ideas for discussion

- Validation
  - Testbenches
  - CI with or without hardware-in-the-loop testing (ongoing discussion/effort in IT, subscribe to ci4fpga-beta egroup if interested)
- HDL style guides (and tools to check)
- Design reviews
- Documentation: user manual, designer manual
- Licensing: CERN OHL v2 and the effect of each of its three variants
- Use of an issue tracking system (GitLab, Jira)
- A common repository of reusable cores at CERN or elsewhere
- Tools for automation: HDLMake, Cheby, Hog...
- Gateware is code. Many questions from the software case apply: REUSE, inbound/outbound contributions, managing a GitHub presence...

The evolution of https://ohwr.org

- Initially a place combining two functions:
  - Collaborative development
  - Window to the world for your designs
- In the future, only the latter (a catalogue)
- Take the opportunity to improve on:
  - Findability of hardware designs
  - Relationships: “this piece of hardware works with this other piece when you use this gateware and software”
  - Curation
- See new website (under development) at https://ohwr.github.io/ohwr.org/ (sources at https://github.com/OHWR/ohwr.org)

Plans for the short term

- Focus on documenting best practices for hardware and gateware in https://ospo.docs.cern.ch/
- ohwr.org evolution:
  - Migration strategies for current content.
  - Release of a first version of the new website.
  - Documentation.

References

- OSHWA best practices to share hardware designs
- OSHWA best practices to share FPGA designs
- OSPO website: https://opensource.cern/
- OSPO documentation site: https://ospo.docs.cern.ch/
- Get in touch!
  - OSPO Forum: https://ospo.web.cern.ch/
  - OSPO Email: Open.Source@cern.ch