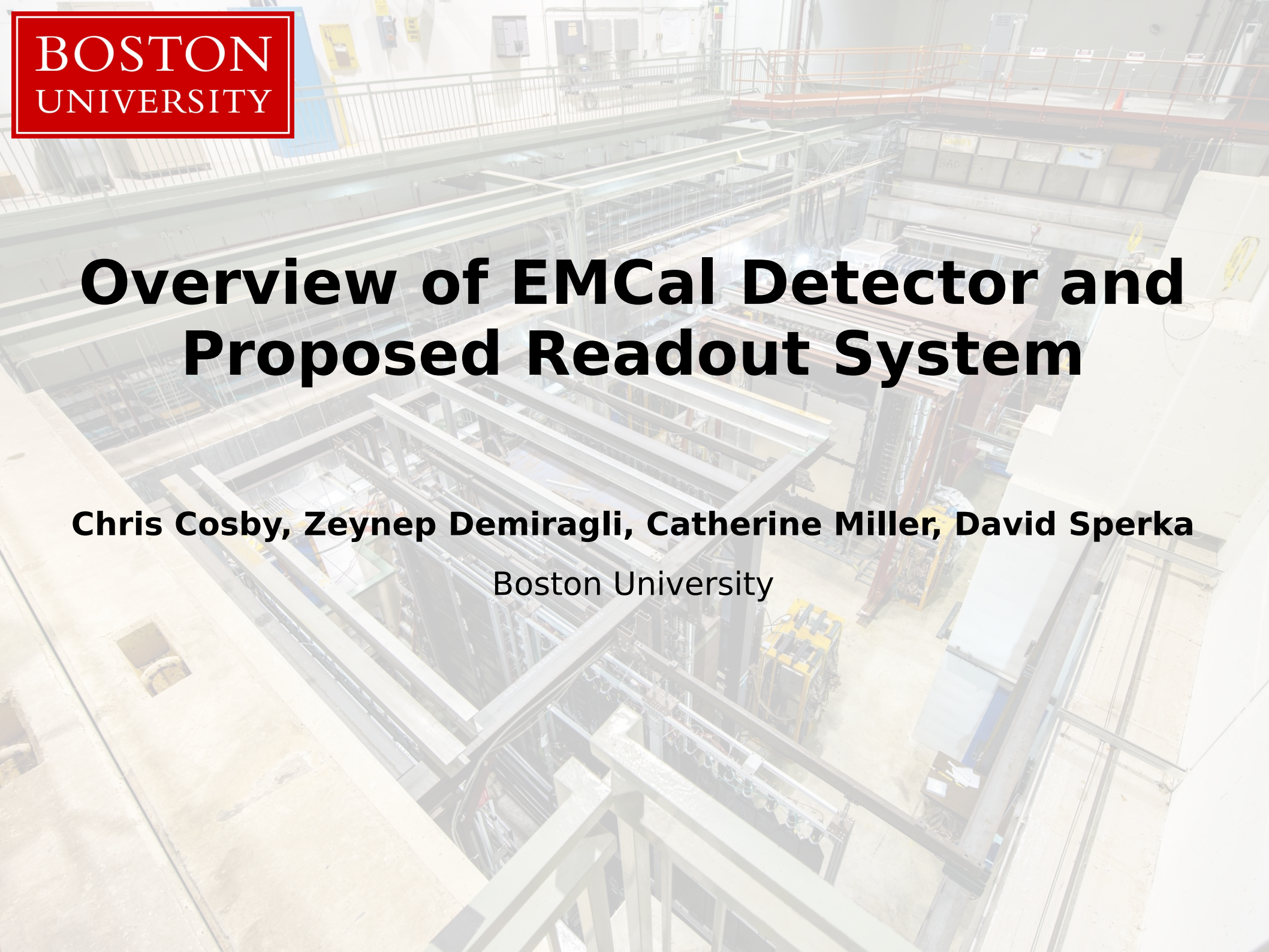
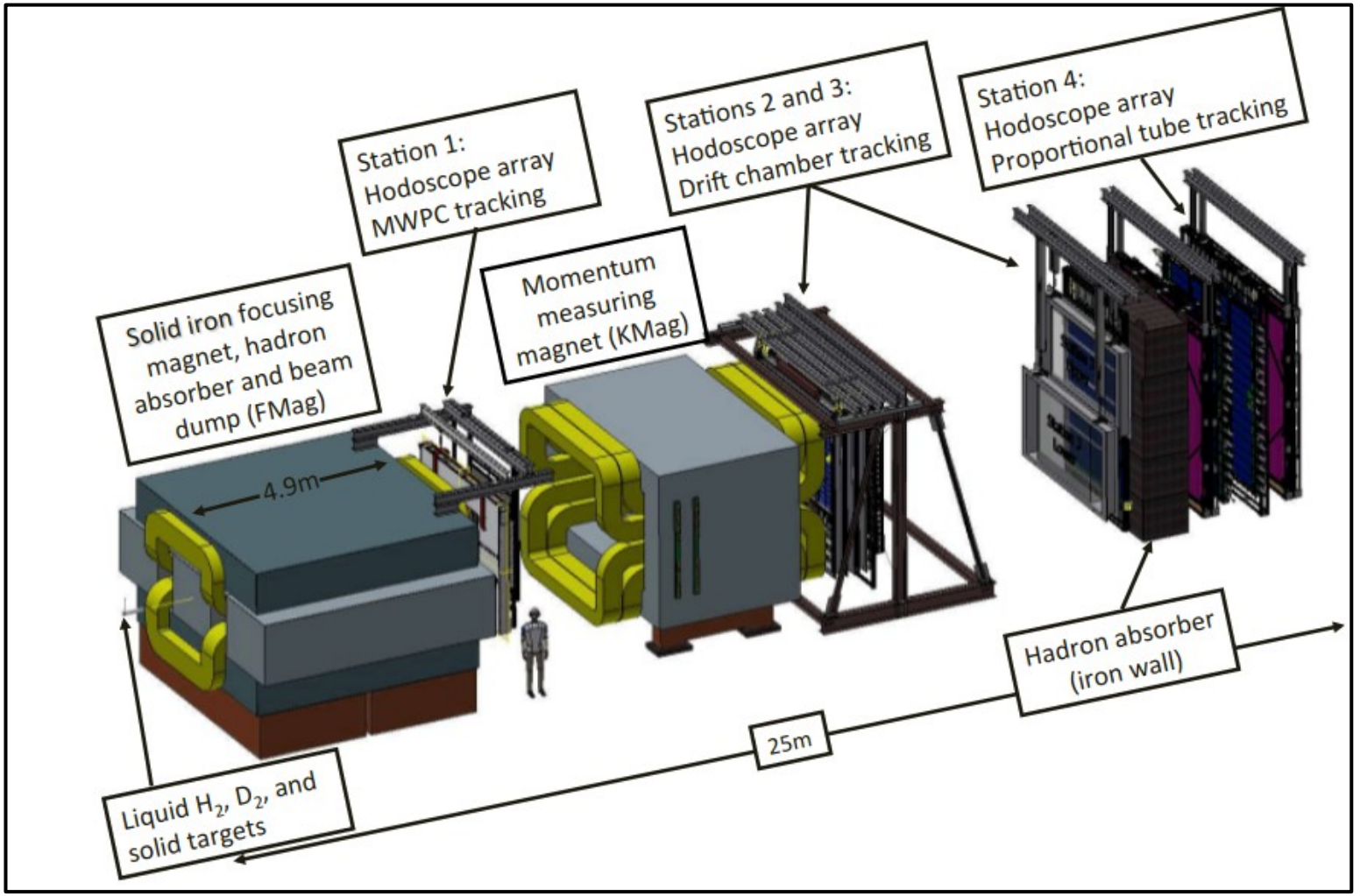


Overview of EMCal Detector and Proposed Readout System

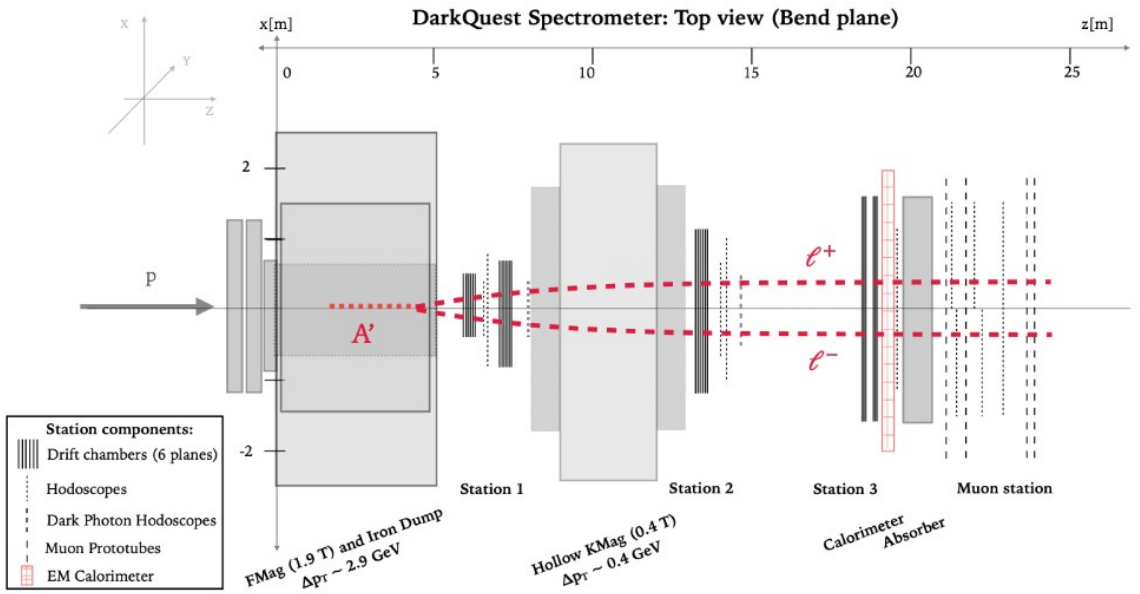
Chris Cosby, Zeynep Demiragli, Catherine Miller, David Sperka

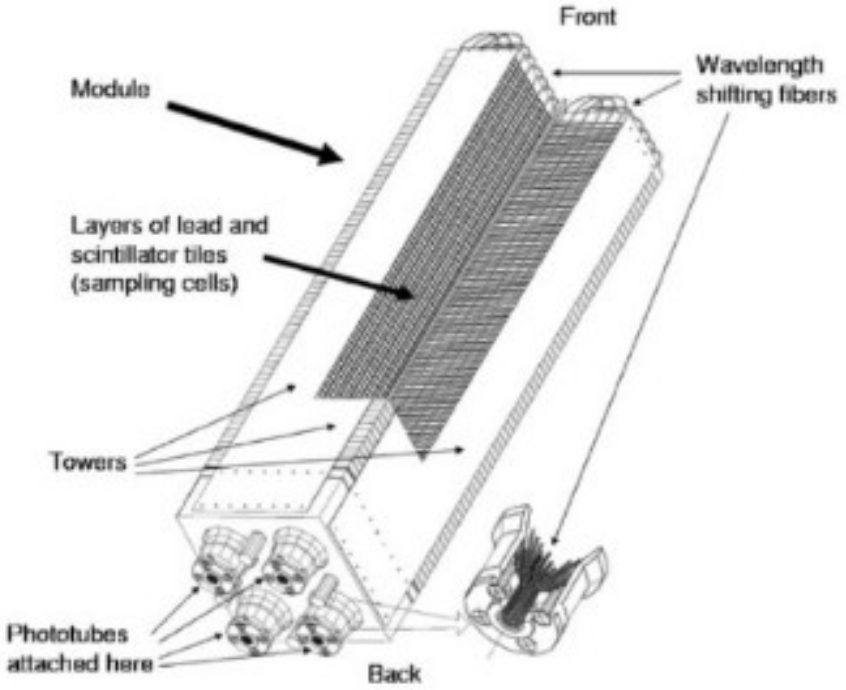
Boston University

SpinQuest


Station 1:
Hodoscope array
MWPC tracking
Stations 2 and 3:
Hodoscope array
Drift chamber tracking
Station 4:
Hodoscope array
Proportional tube tracking
Solid iron focusing magnet, hadron absorber and beam dump (FMag)
Momentum measuring magnet (KMag)
4.9m
Hadron absorber (iron wall)
25m
Liquid H_2, D_2, and solid targets

EMCal Detector

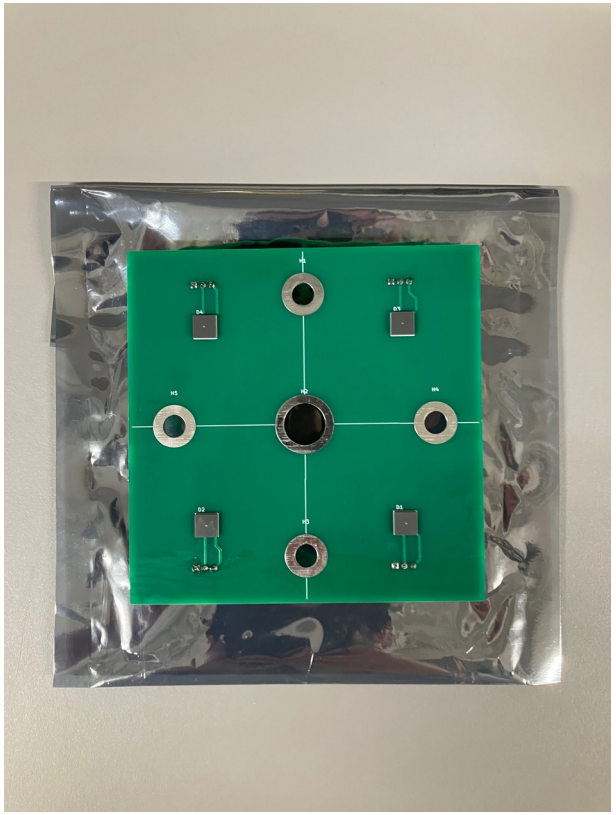


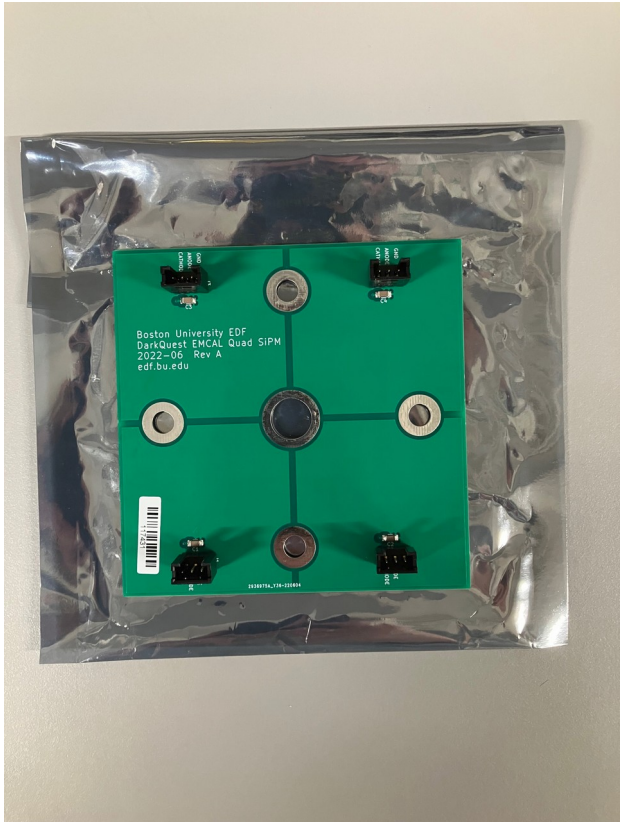


- DarkQuest adds to the spectrometer an Electromagnetic calorimeter decommissioned from PHENIX (BNL)
- Neutral Kaon decays, e.g. $K_L^0 \rightarrow \pi^{\pm} e^{\mp} \nu$n be suppressed
- Opens possibility to search for wider range of dark sector models and masses

EMCal SiPM Readout

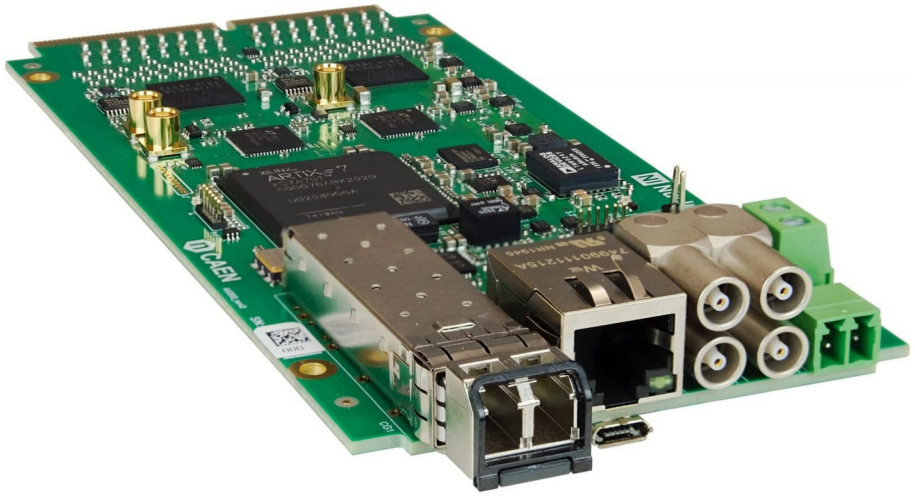
- Light yield of EMCal Module is large, ~12,500 photons/GeV
- Peak emission of the WLS is at 490 nm, 95% of emission is 470-570 nm
- Investigated SiPM readout, compatible with off the shelf electronics systems
- Simple Front End board where the 4 SiPMs are mounted, one per channel
  - Have added a temperature sensor, options for electrical attenuation

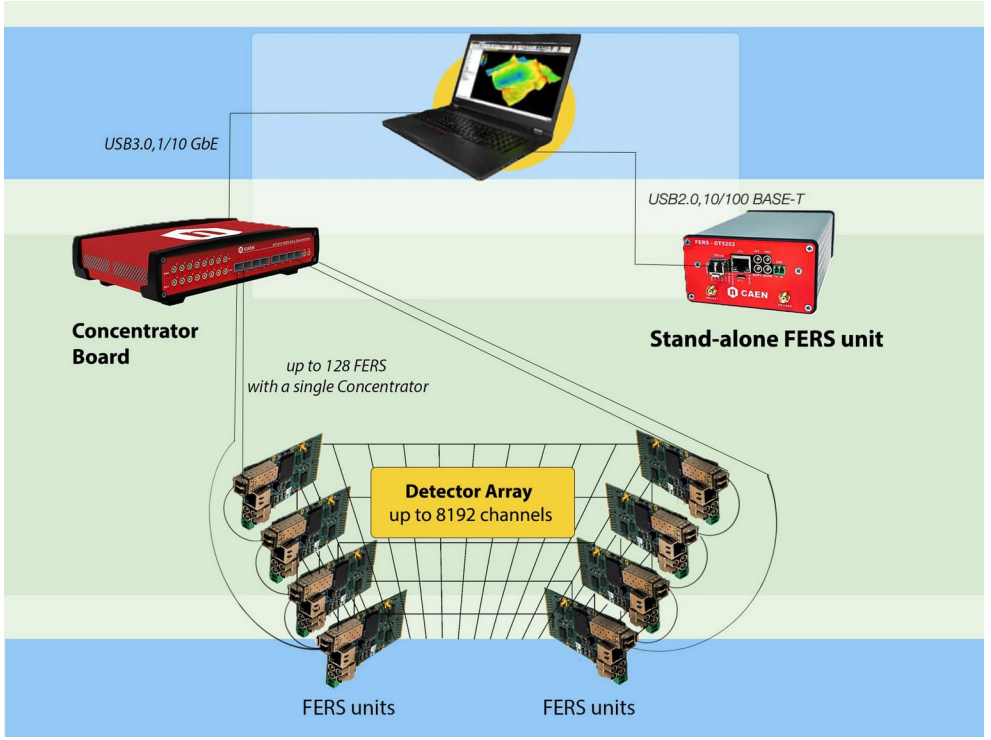




Caen Front End Readout System

- Caen makes an off-the-shelf system designed for readout of large SiPM arrays
- A5202 is a 64 Channel card based on 2 Citiroc-1A, ADC, and FPGA.
  - Up to 16 boards can be synchronized via high speed optical link
- Idea is to connect 2560/64 = 40 boards, controlled by a single “concentrator board”
  - Concentrator board can also distribute clock, not yet tested
- One temperature sensor / board (64 channels)





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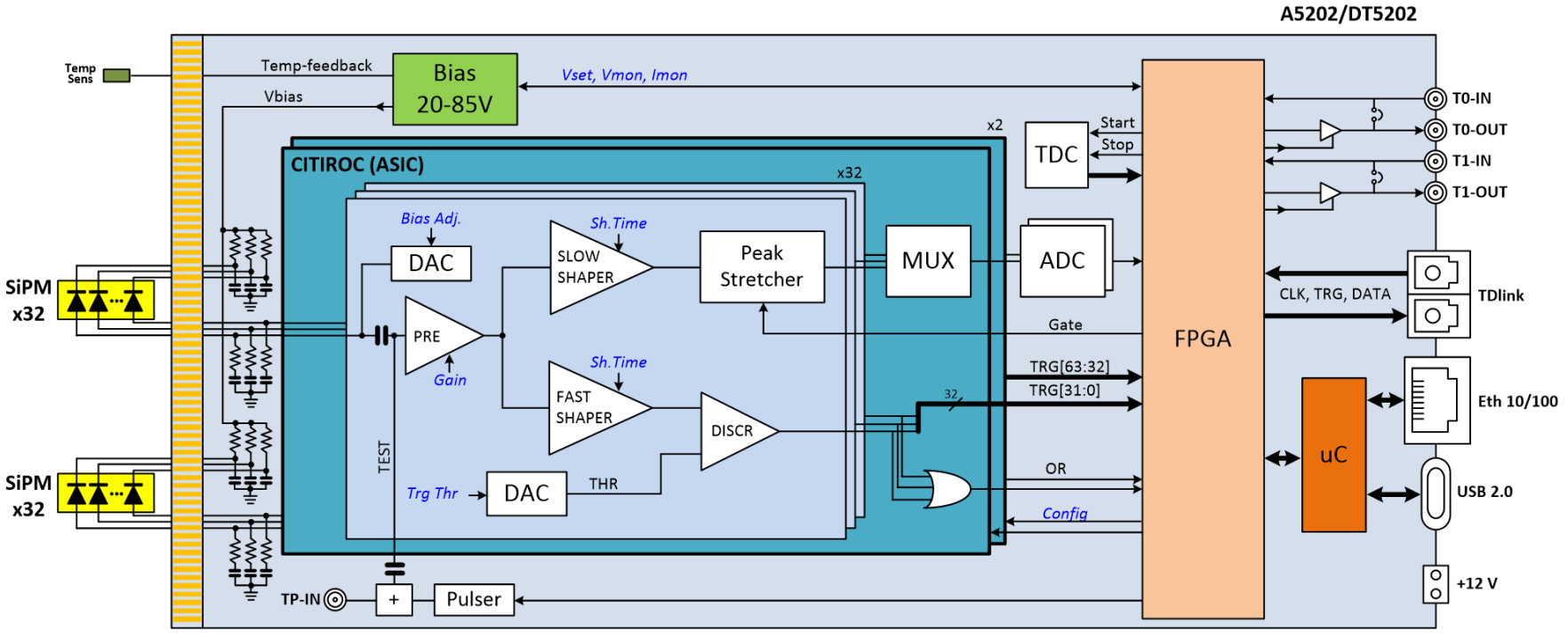
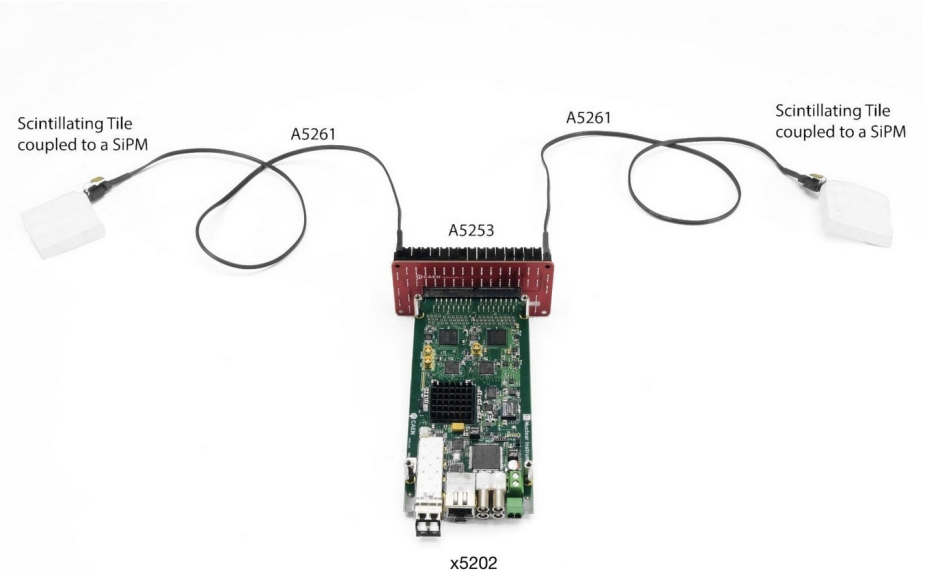
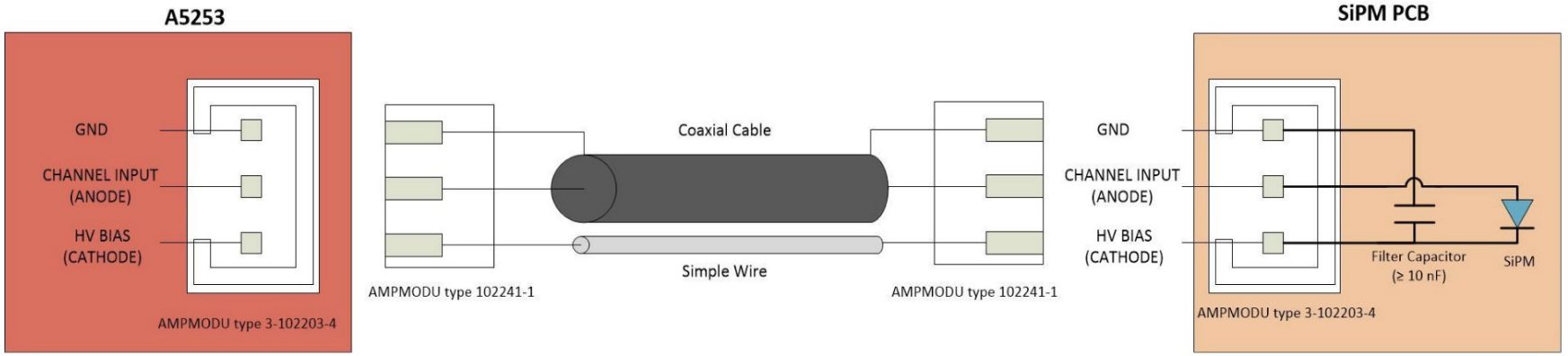


Caen Front End Readout System

- Once concern is whether the SiPM output is strong enough to transport the signal over ~meter distances without any initial amplification
- Our calorimeter has a high light yield, so the SiPM gain by itself is enough
  - In fact the signal is too large
- Using quality cables signal will not be degraded over distances of ~few meters





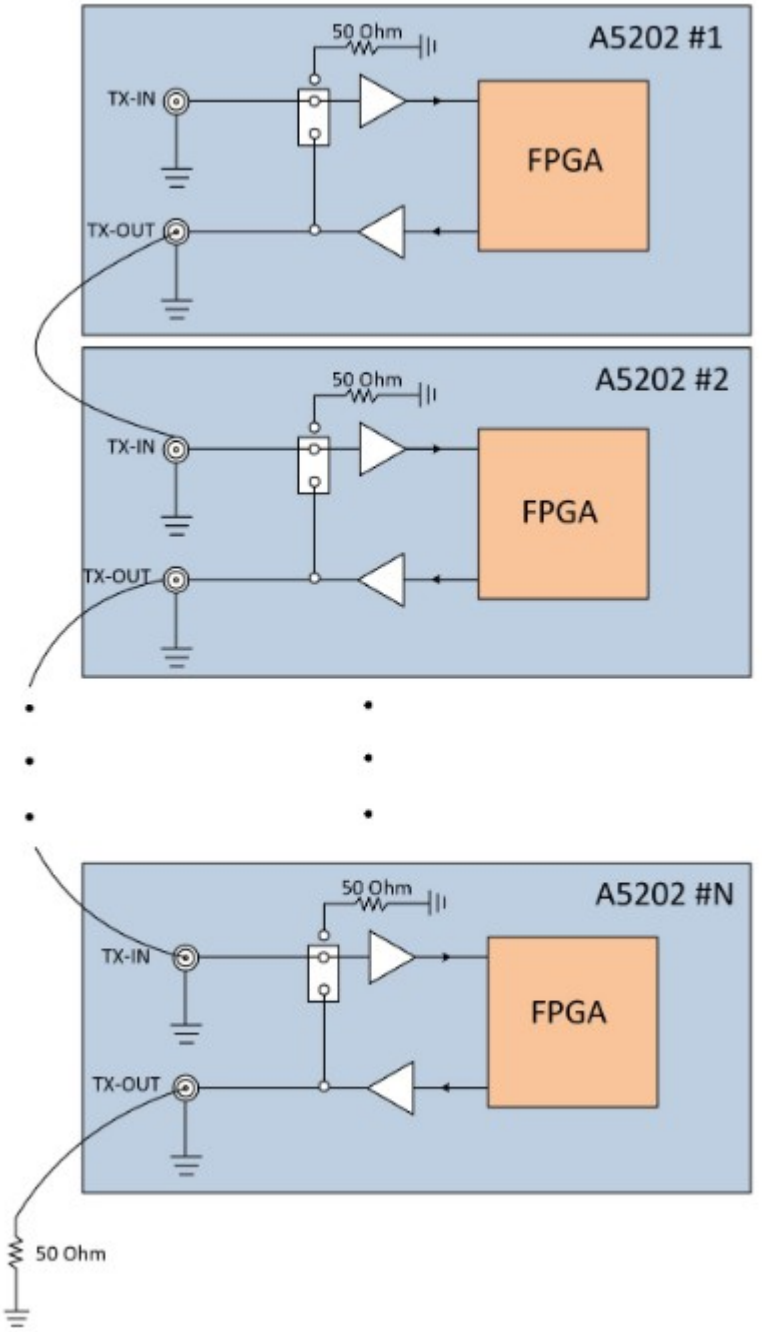
Apart from the connection of the SiPM to the cathode and anode lines, a filter capacitor, with a capacitance of at least 10 nF and a voltage rating of approximately 100 V, should be connected between the ground and cathode lines.

CITIROC Readout Modes

- **Spectroscopy Mode**: This mode (also indicated as Pulse Height Analysis, PHA) works with a global (bunch) trigger, either coming from an external source or generated by a combination of the channel self-triggers. As soon as a trigger is issued, all channels start simultaneously the A/D conversion of the pulse amplitude and create a data packet containing the common trigger time stamp followed by the individual energies. The packet is saved into the local memory buffer of the FERS-5200 unit, waiting for the readout, while a new cycle can start. In Spectroscopy Mode, the A/D conversion causes a systematic dead time and limits the maximum trigger rate. In particular, the dead time due to conversion with Citiroc-1A is about 10 µs.
- **Counting Mode**: In this mode, the self-triggers of each channel are individually counted. The counting intervals (the same for all channels) are defined by an internal periodic gate with programmable width or by an external signal. At the end of each counting interval, the counters are latched and saved in a data packet, while the counting continues in the next interval without any dead time. The maximum counting rate for the Citiroc-1A is 20 Mcps.
- **Timing Mode**: This mode generates a list of individual time stamps, optionally combined with the Time over Threshold (ToT) that gives a rough estimation of the pulse amplitude (energy). The channels run independently and are allowed to push an event (time stamp of the self-triggers and ToT) to a data packet. The timing resolution of both time stamp and ToT is 0.5 ns LSB (≈ 250 ps RMS). When the data packet reaches the programmed size, it becomes available for the readout and the acquisition continues in a new packet. There is not any intrinsic dead time, even though a high input rate might produce huge amounts of data that saturates the readout bandwidth with consequent data loss.

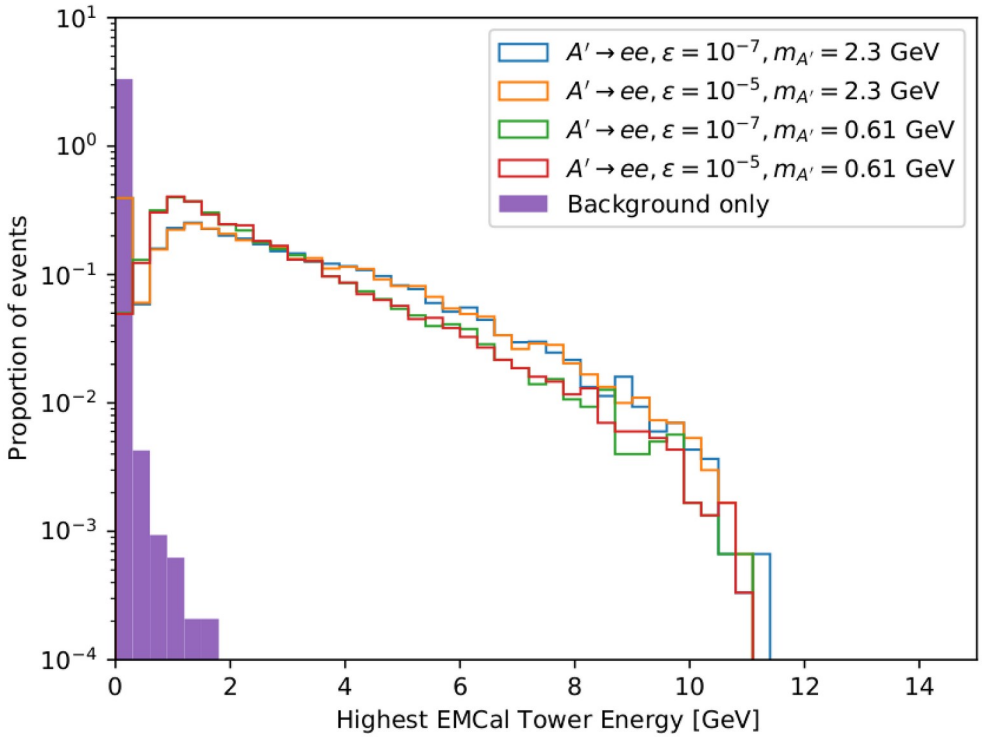
EMCal Trigger

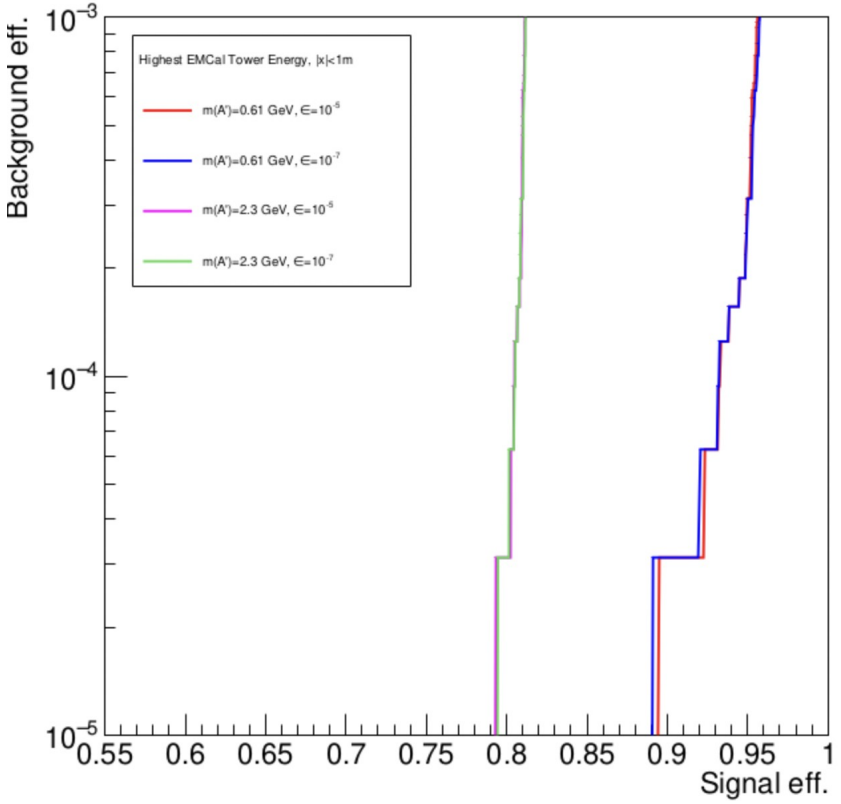
- The simplest way to trigger is to require at least one channel above a large threshold.
  - We can select which channels contribute to the trigger (e.g. central towers only)
- The trigger can by formed using a wired-OR on an LVTTL output.
  - This is similar to current NIM trigger logic, and can form an input to the Trigger Supervisor for triggering the readout of other detectors.
  - The trigger is very fast, ~25 ns, may need to delay it in the actual experiment
- There are two of these ports, so also possible to accept an external trigger (i.e. FPGA trigger, NIM, or DP hodoscopes).
  - However, the external trigger needs to arrive in under ~75ns, probably not feasible



EMCal Trigger Performance

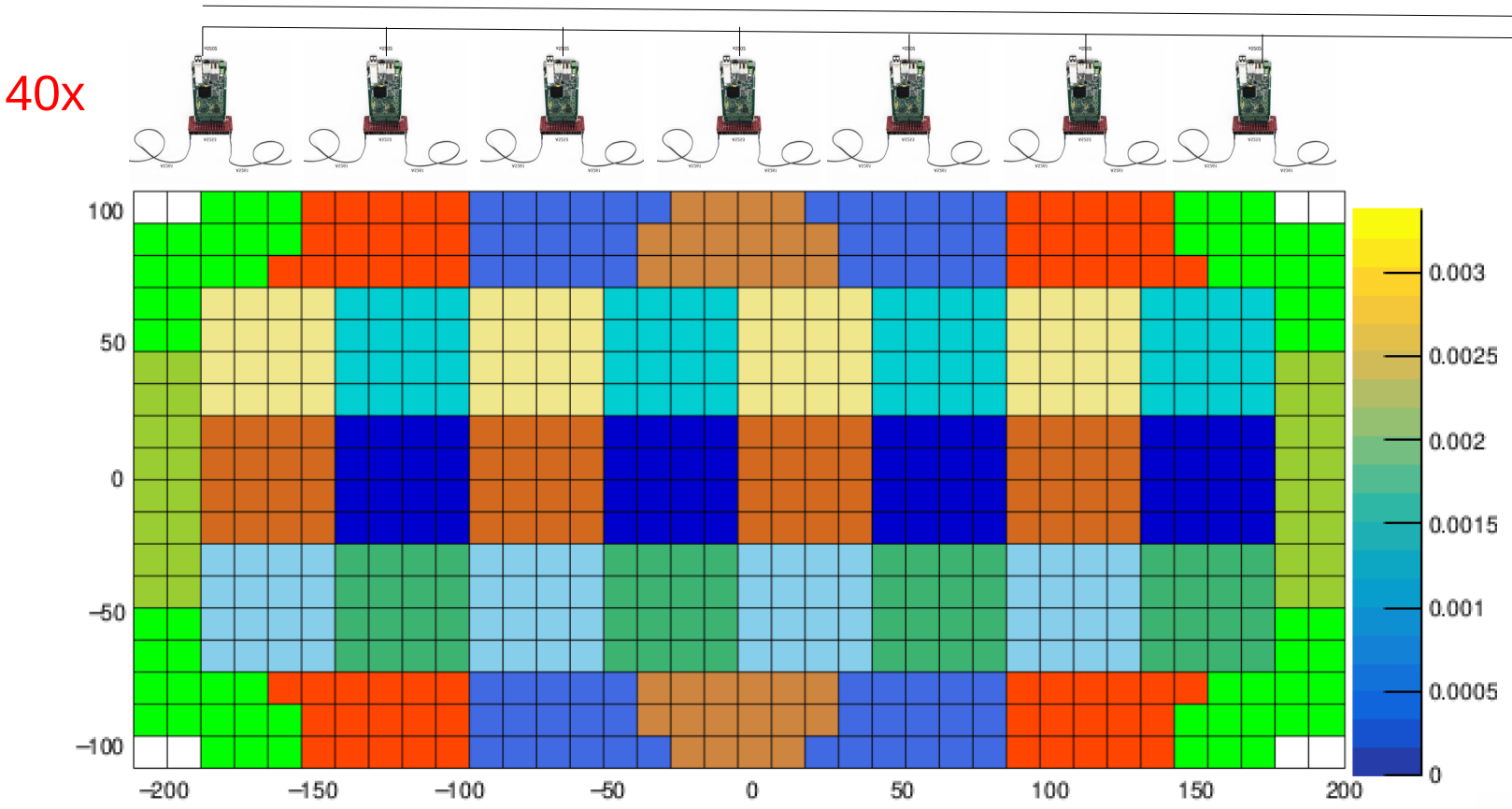
- More of the energy from background is low energy and towards the edge of the calorimeter, which is after Kmag. Only looking at central region has better performance.
- The trigger maintains about 80-90% of the dark photon signal, depending on the mass of the dark photon, for a background rejection of ~1e-5 (~0.5 KHz)





Physical Layout

- It has been raised that we may need to move Station 3 forward a bit to fit the EMCal. Modules can be behind, on top, next to, or below the EMCal structure
- Keep front end cable short, try to keep boards out of highest radiation areas
- Each board reads out 16 Modules (cartoon layout shown)



Wired-OR NIM/TTL to TS

Optical links from FE boards to concentrator

Gigabit ethernet to DAQ PC

Physical Layout

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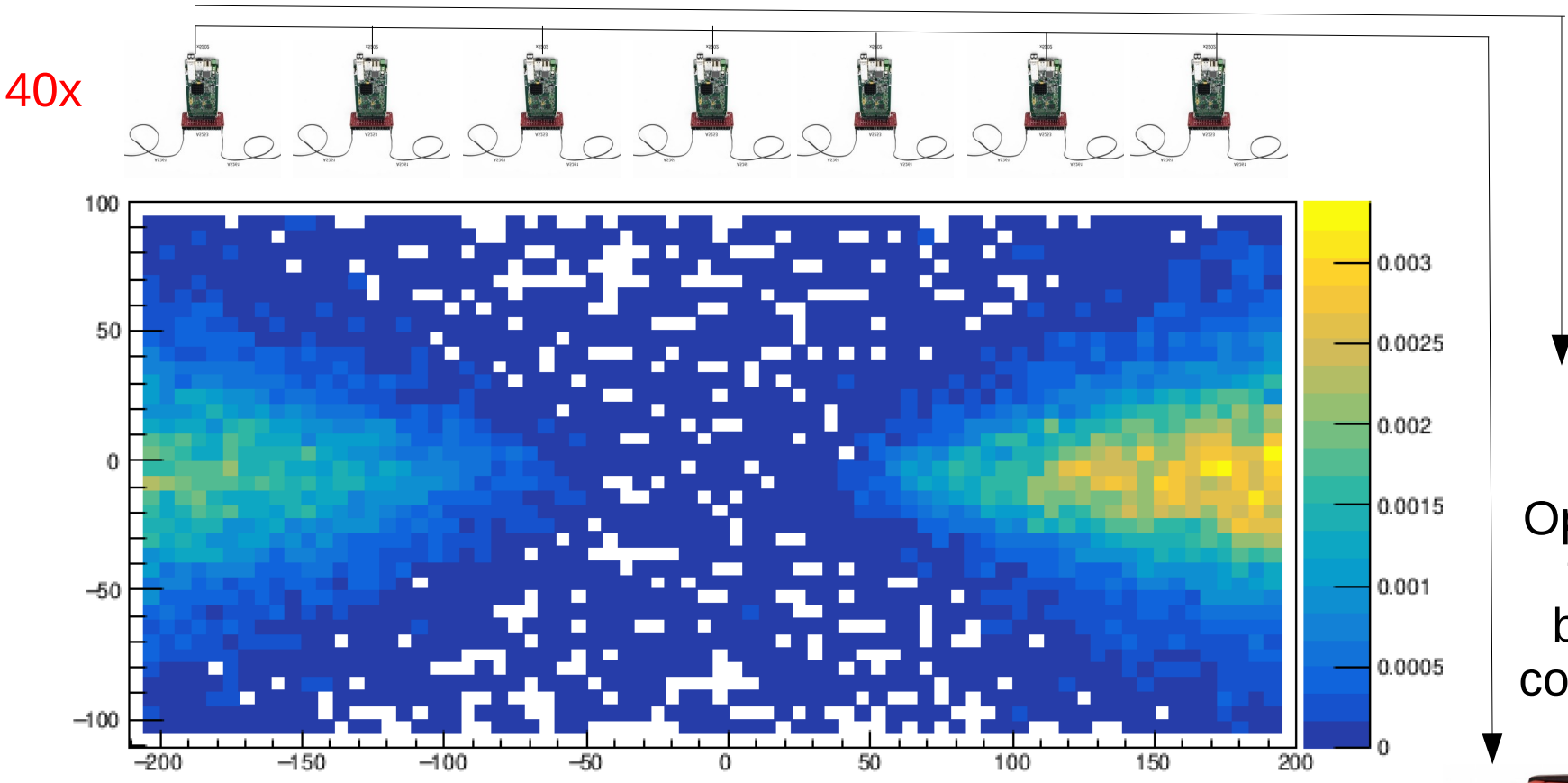
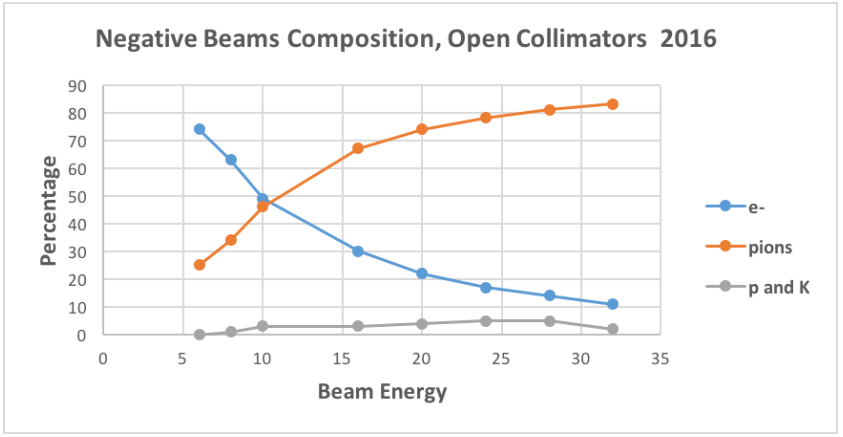
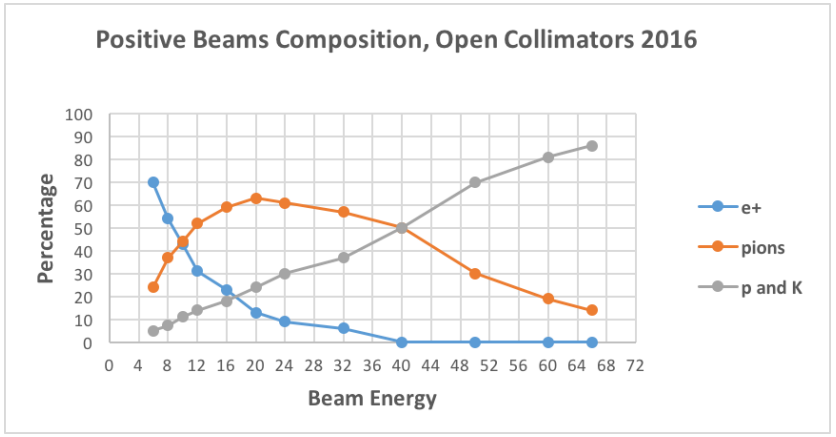
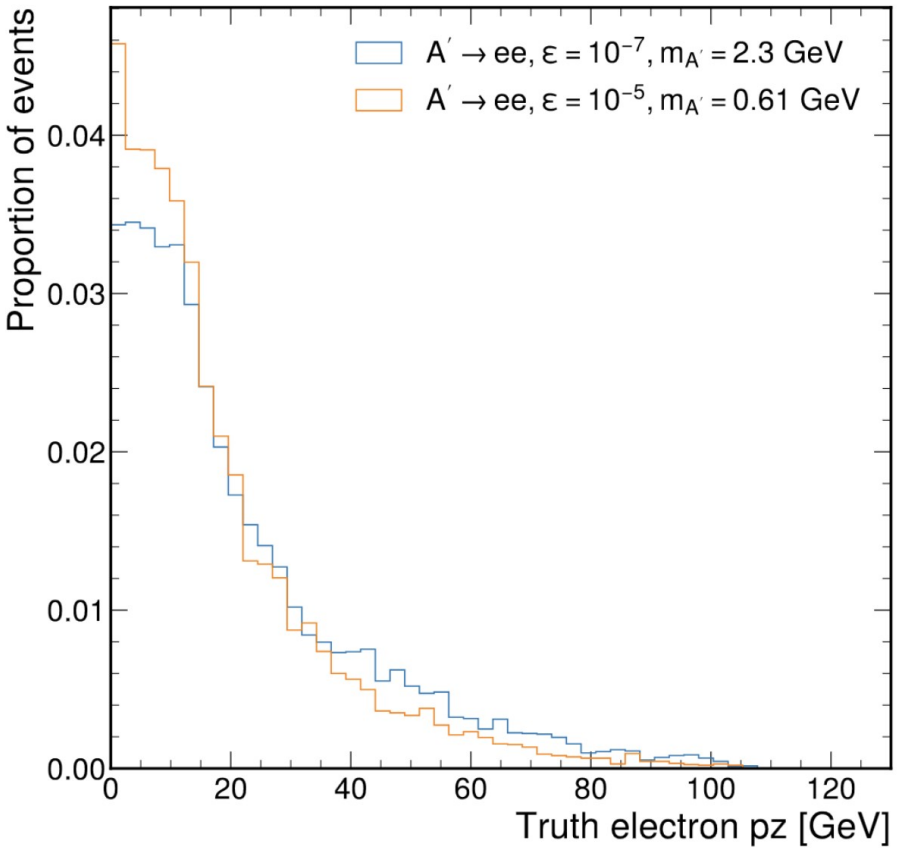


Test Beam Preparations and Plan

- We have studied the performance of the EMCal and our readout system using cosmic rays and LED drivers (see the next two talks)
  - Still need realistic high energy electrons and pions to better with test beam
  - Test beam can provide electrons between 1-32 GeV, mixed in with pions
    - Should be able to distinguish electron peak, but only up to 32 GeV

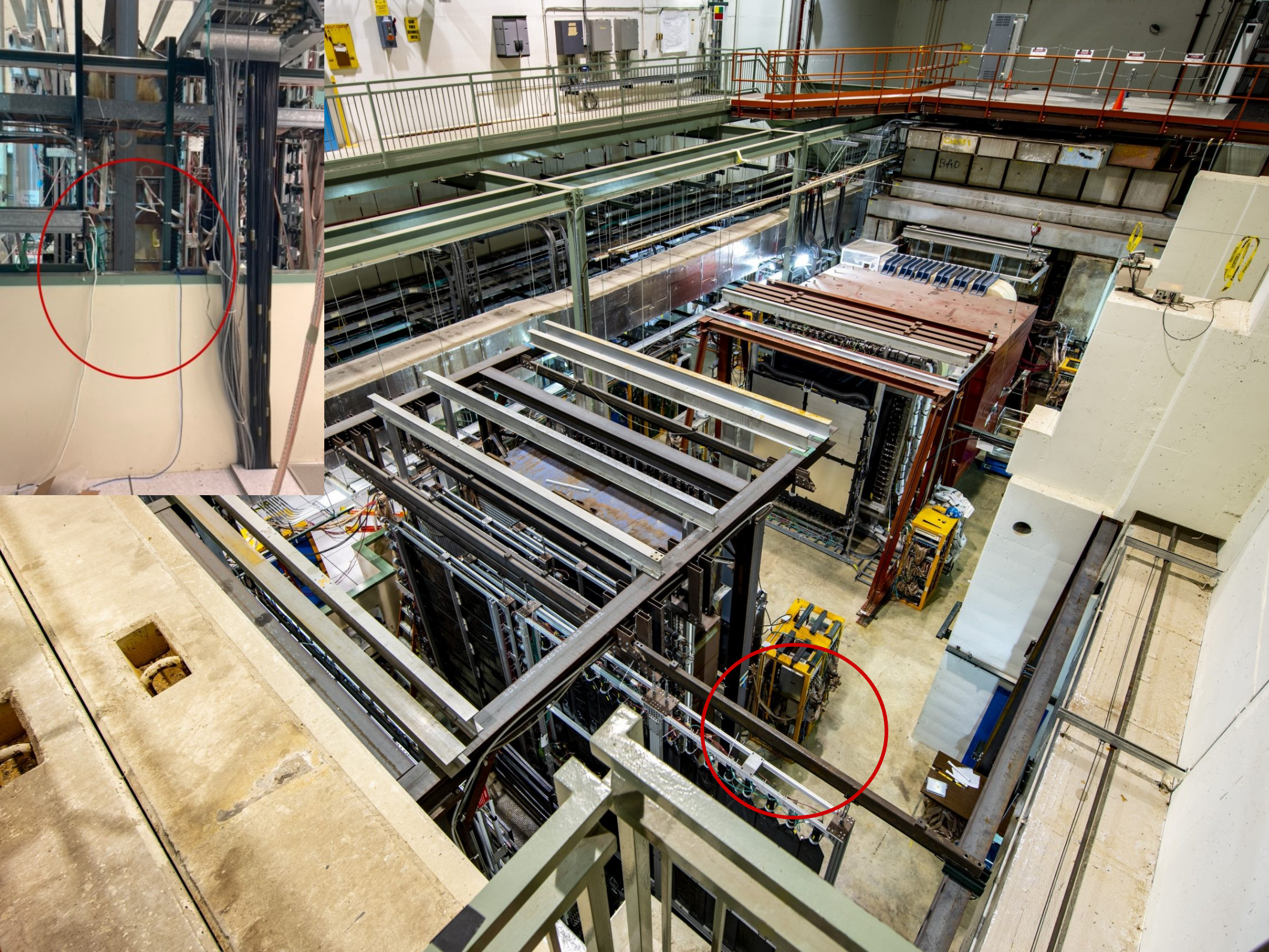






Test Stand in NM4

- We would like to place a small test stand next to the Iron Absorber wall, outside of the Spectrometer acceptance, to measure in situ background rates with beam
  - Should have ~no impact on the SpinQuest data taking
  - It would be nice, if possible, to re-position some electronics crates so that there is minimal material in front of the EMCal modules
  - Ideally, the test stand would be movable to measure rates at different positions
  - We would only need standard power (110-120V AC) and an ethernet connection to a linux machine
- Plan is to first go to test beam, and then transition the detector to NM4


BAD

Other Thoughts And Work in Progress

- Integrating the DAQ of the EMCal with the SpinQuest DAQ is not trivial
  - Two systems based on different hardware, minimal technical support available
  - Started to study this in BU test stand but not there yet
  - Timing in the detector with SpinQuest will also be non-trivial
  - Need to have some dedicated effort on EMCal at Fermilab, many of the technical issues can be circumvented by using the test stands available there
- Right now have access to 4 EMCal modules (3 at FNAL, 1 at BU)
  - Ownership of 1 full supermodule (36 modules) being transferred from BNL to LANL (Ming), not sure the current status of this process
  - We need to better understand this procedure to be able to move the entire detector from BNL to FNAL

Backup

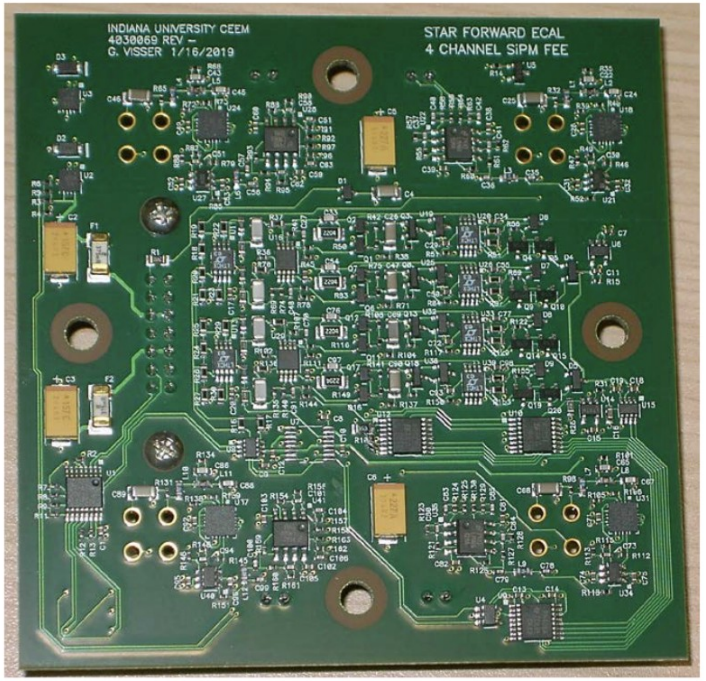
STAR Readout Design

http://npvm2.ceem.indiana.edu/~gvisser/STAR/FCS/STAR_FCS_FEE_and_Readout.pdf

Design goals

- Frontend amplifier and signal shaping on detector
- SiPM bias voltage control on detector
  - Including simple local analog temperature compensation
  - Including SiPM current monitoring
- Separate SiPM/thermistor and FEE boards
  - Production at two sites UCLA / IU
  - Lower cost to replace SiPM (for upgrade or rad. damage)
  - Multichannel FEE with loose tolerance on tower(SiPM) positions
- Services (+/-6 V, +80 V, I^2C controls) on low cost multidrop flat cable
- Differential signal output for reasons of size, cost, and noise immunity
  - Micro-ethernet cable on detector
  - 3M loose pair CL2 cable the rest of the way to ADC's
- Waveform digitizer readout (BNL – "DEP" board)
  - "80" (75.06 = 8×RS) MSPS, 12 bits
  - Pulse arrives already shaped from FEE
    - DEP is **general purpose** (in fact we use also for preshower)
    - Shaping the pulse on detector makes best use of driver/cable dynamic range
  - Triggered readout in STAR, but DEP is also intended as a development platform for streaming readout

FEE Implementation – ECAL



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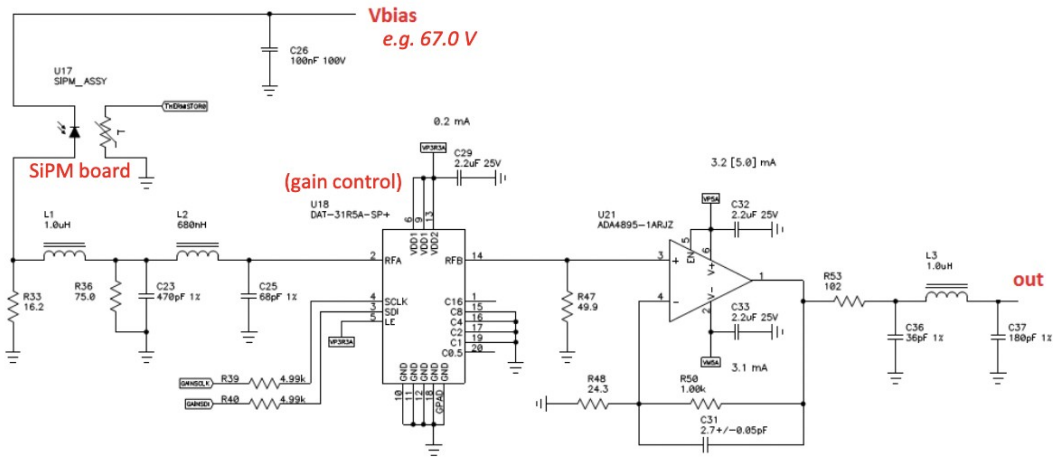
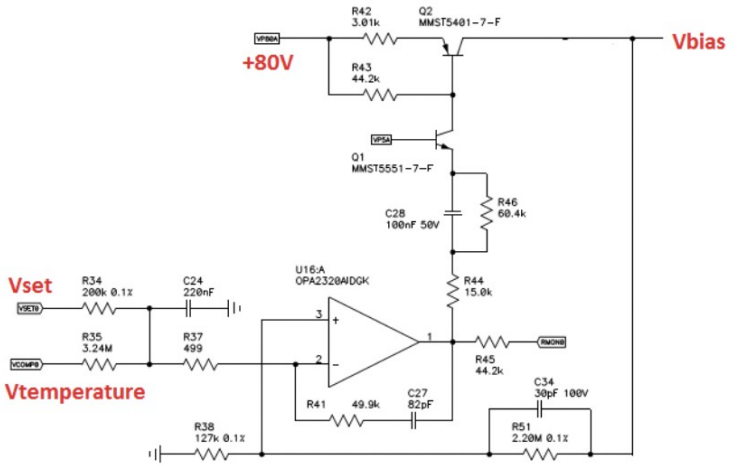
Frontend and bias



- ECAL 4×, HCAL 6× 3×3 mm^2 SiPM's
- SiPM with small load resistor, followed by voltage amplifier
  - for best possible linearity – *speed and linearity of the amplifier are not involved in sweeping charge out of SiPM*
  - load resistance << 50 Ω is best
- some shaping before any amplifier – so that amplifier *does not have to linearly follow pulse as fast as SiPM produces*
- more shaping after amplifier – noise limiting
- for STAR we included gain control as thought necessary for cosmic ray calibration. omit/simplify for EIC application…



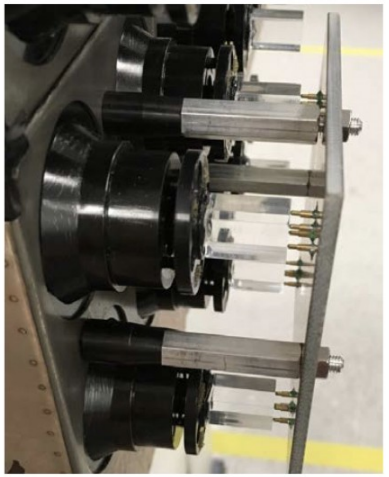
- simple but precise and low noise bias voltage regulator
- inherent current limiting – no series resistor needed to protect SiPM
  - more stable bias voltage → more stable gain
- fast recovery 3 µs to 2 mV after full scale signal pulse
- current monitor (not shown above) – optional, but useful!
- Vset and **slope of** Vtemperature set by DAC's

STAR Readout Design

http://npvm2.ceem.indiana.edu/~gvisser/STAR/FCS/STAR_FCS_FEE_and_Readout.pdf

FEE Connections

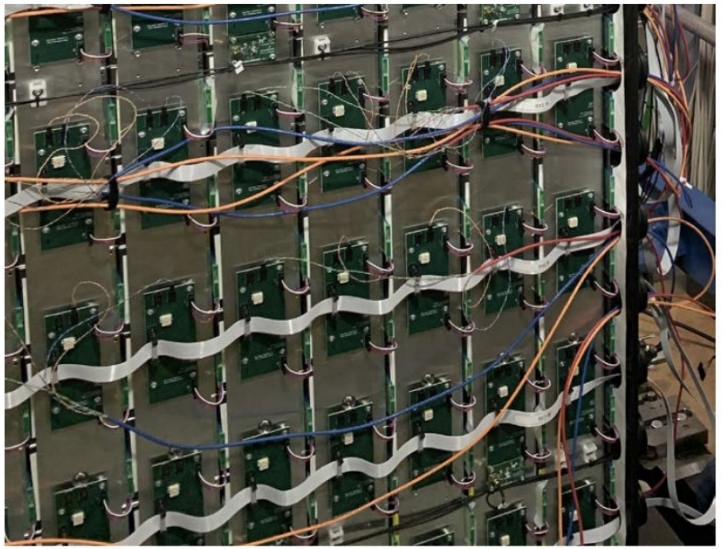
SiPM board per tower, glued to light guide. Connection from FEE by pogo pins. Large tolerance of transverse location (several mm). **Easy blind installation** (*once dimensions verified by fixture*).



Cooling of FEE: Air is drawn out from top of the enclosure. Enters at bottom, through baffles for light tightness.

Power inside detector: 180 mW/ch (e.g. ½ ECAL is 136 W)

Patchpanel boards on sides of detector: Transition to long signal cables. Group power rows into power groups. +80V power supplies.



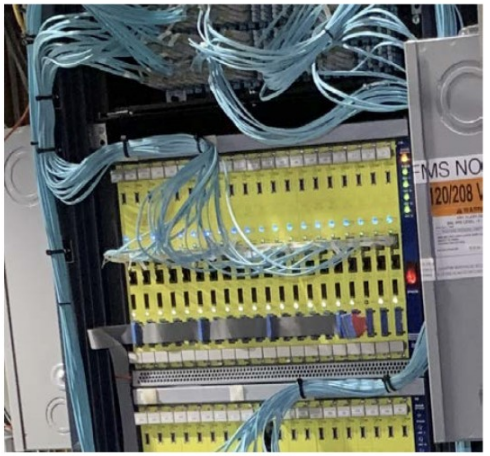
HCAL: Same concepts, except short cable connection to SiPM board instead of pogo pin connection. Much more room than ECAL.

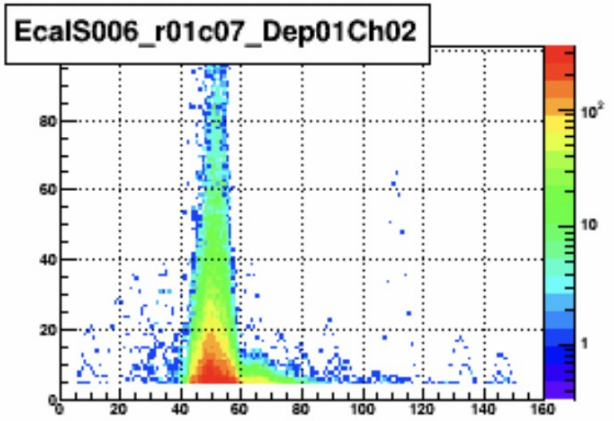
STAR Readout Design

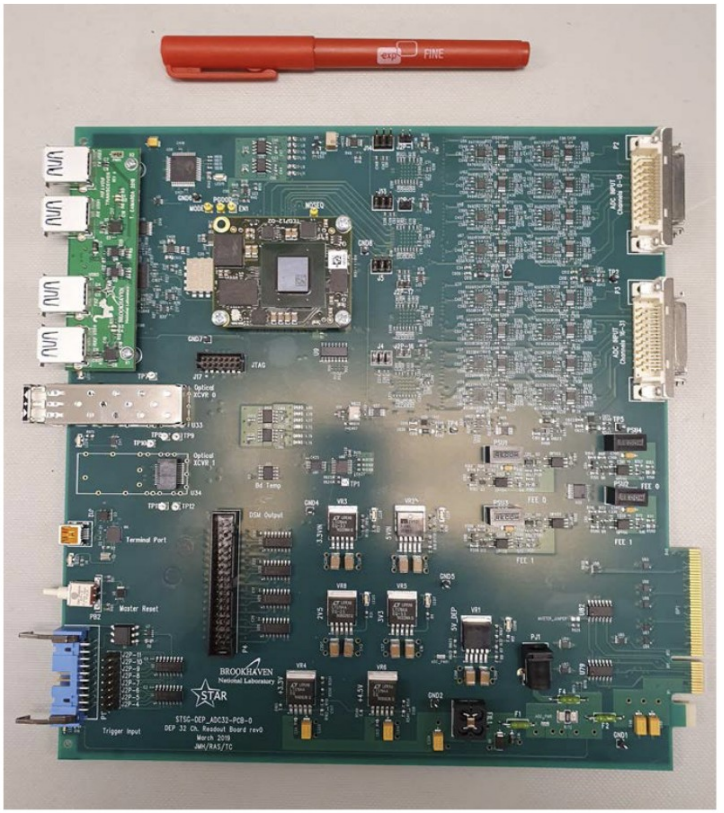
http://npvm2.ceem.indiana.edu/~gvisser/STAR/FCS/STAR_FCS_FEE_and_Readout.pdf

DEP ADC Board

- 32 channel 80 MSPS 12 bit ADC (P/N AD9637); pin compatible 14-bit upgrade
- high CMR line receiver inputs (same as GlueX ADC125)
- FPGA on Trenz Module – upgradeable!
- 2× 3.2 Gb/s fiber links (≈ 512 MB/s) to DAQ PC
  - In practice w/ current receiver/PC we measure ≈ 460 MB/s, plenty for STAR, room for improvement for future
- Expect ≈ 40 bits per hit for summary info (amplitude, time, etc.) for a streaming mode readout
- This is “DEP ADC” – there is also “DEP IO” a trigger processor with fiber input instead of ADC
- DEP ADC also includes 2× opto-isolated I^2C masters for FEE controls







STAR System Limitations (?)

- The STAR Front-End board shapes the pulse to ~50ns, and the ADC board runs at 8x the RHIC clock, i.e. ~75 MHz (RHIC clock is ~9.37 MHz, 107ns)
- This is a only slightly faster than our clock (53 MHz, 19ns)
- It might be ok or could try to modify the design to work with a faster clock