Contribution ID: **35** Type: **Poster**

Boosting CPU Efficiency in ATLAS Inner Detector Reconstruction with Track Overlay

Monday, 11 March 2024 16:15 (30 minutes)

In response to the rising CPU consumption and storage demands, as we enter a new phase in particle physics with the High-Luminosity Large Hadron Collider (HL-LHC), our efforts are centered around enhancing the CPU processing efficiency of reconstruction within the ATLAS inner detector. The track overlay approach involves pre-reconstructing pileup tracks and subsequently running reconstruction exclusively on hard-scatter tracks. This allows us to conserve valuable CPU resources by concentrating on events of interest. Integral to track overlay is the incorporation of machine learning (ML)-based decision processes. ML decisions guide the selection of events suitable for track overlay, while events in denser environments continue to use the standard overlay. This strategy ensures judicious use of resources, balancing efficiency and precision in inner detector reconstruction. This presentation focuses on constructing the ML model and verifying the workflow with ML decisions. The improvement of the track overlay approach on CPU usage and the reduction in the size of standard data format files in the Run 3 detector setup are also demonstrated. Preliminary results in the context of the forthcoming ITk inner detector at HL-LHC will be presented as well.

Significance

This presentation goes beyond traditional status reports by showcasing the results of the track overlay approach, coupled with machine learning-based decision processes and significant advancements in the workflow. We will also present a preliminary result with Run 4 setup, which is a totally different inner detector at HL-LHC from Run 3.

References

Faster simulated track reconstruction in the ATLAS Fast Chain
https://indico.jlab.org/event/459/papers/11440/

Experiment context, if any

This abstract is conducted in the context of the ATLAS experiment at the LHC.

Primary authors: DUDA, Dominik (The University of Edinburgh (GB)); TSAI, Fang-Ying (Stony Brook University (US)); CHAPMAN, John Derek (University of Cambridge (GB)); JAVURKOVA, Martina (University of Massachusetts (US)); JIGGINS, Stephen (Deutsches Elektronen-Synchrotron (DE))

Presenter: TSAI, Fang-Ying (Stony Brook University (US))

Session Classification: Poster session with coffee break

Track Classification: Track 1: Computing Technology for Physics Research