Phase-2 Upgrade of the ATLAS L1 Central Trigger

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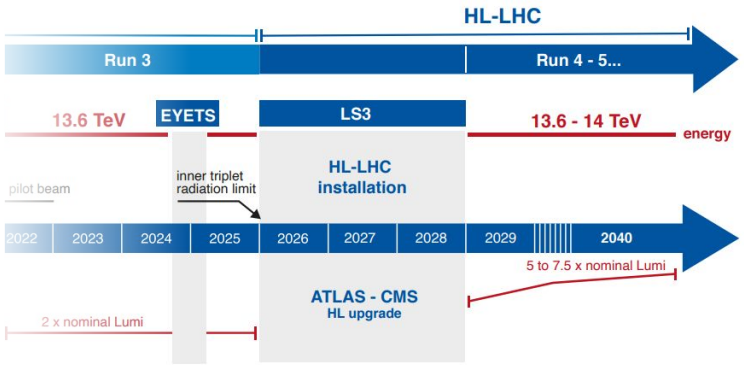
on behalf of the ATLAS Trigger and Data Acquisition (TDAQ) group

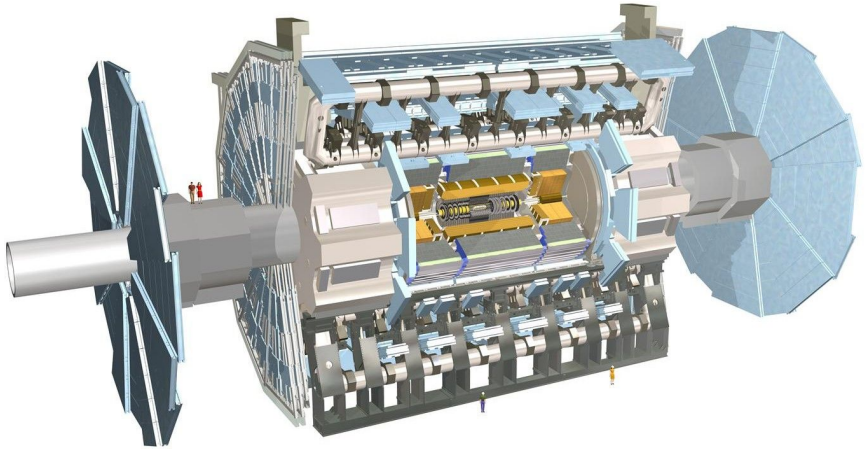
ACAT 2024

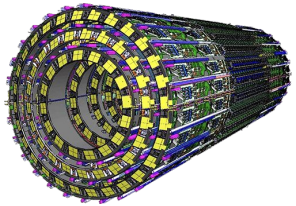
ATLAS Phase 2 upgrade at a glance

More on earlier talk by F. Pastore

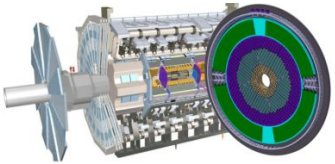
High-Luminosity LHC (phase 2) to start in 2029 after LHC Long Shutdown 3 (LS3)







Inner TracKer (ITk)



High-Granularity Timing Detector (HGTD)

L0Global prototype

More on link

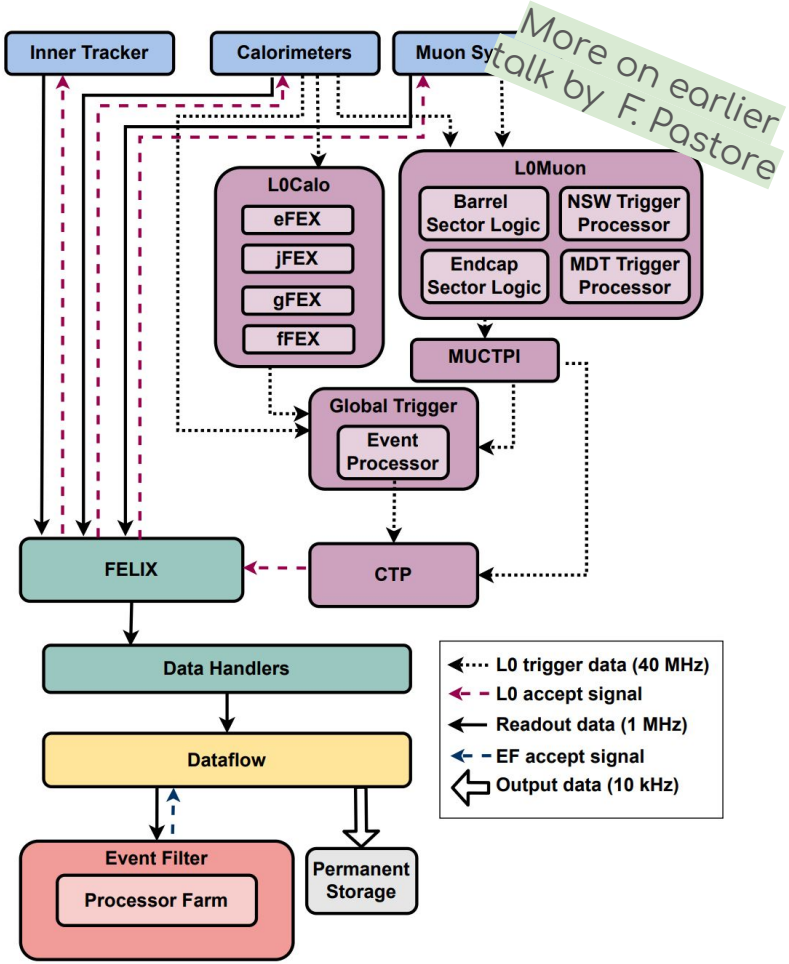
And more projects...

ATLAS TDAQ in Phase 2

- Full detector granularity
- Extended tracking range
- Improved muon trigger efficiency

- Similar architecture - more inputs
- New hardware (ATCA, SoC ...)

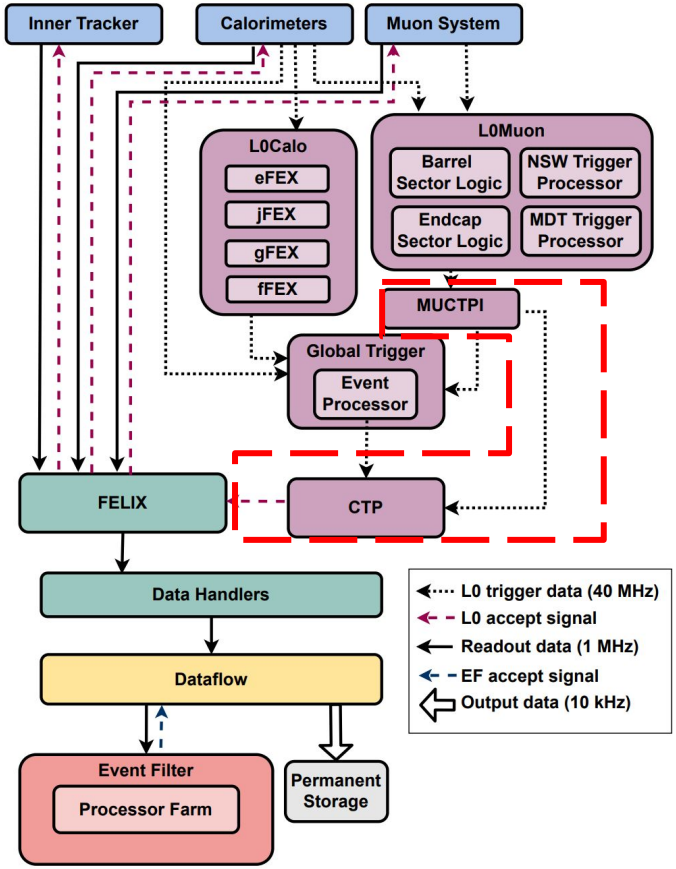
Rates	Phase 1	Phase 2
Trigger inputs	40 MHz	
L0/L1 trigger output	100 kHz	1 MHz
Event farm output	1 kHz	10 kHz



Central Trigger within TDAQ

Includes: Muon trigger interface, final stage of first-level trigger and TTC distribution.

- MUCTPI[1]
  - Muon candidate multiplicities & overlap removal
  - Send info to Global Trigger and the CTP
- CTP[2]
  - L0 trigger logic based on list of trigger requirements ("menu")
  - Prescaling & matching with LHC bunches
  - Deadtime to prevent buffer overflows
- Timing, Trigger & Control (TTC) distribution
  - Receive & fan-out TTC stream from CTP
  - Board(s) per sub-detector
  - Required for running in standalone



[1]MUCTPI: Muon-to-CTP Interface
[2]CTP: Central Trigger Processor

Central Trigger upgrades - hardware timeline

	Before	Phase 1	Phase 2
MUCTPI	Full 9U VME crate	ATCA+SoC	(reuse Phase 1 board)
CTP	Full 9U VME crate	Core module (VME)	ATCA+SoC
TTC board	Legacy TTC (VME)	ALTI (VME)	LTI (ATCA+SoC)

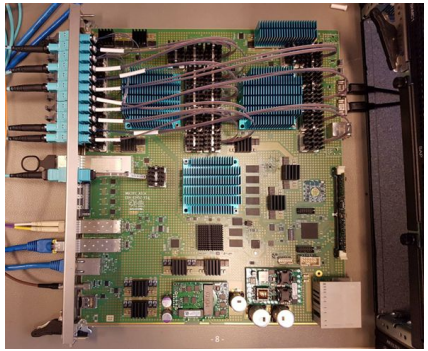
ATCA+SoC components come with optical inputs and additional functionality (monitoring, partitioning).

(A)LTI: (Atlas) Local Trigger Interface

Phase 1

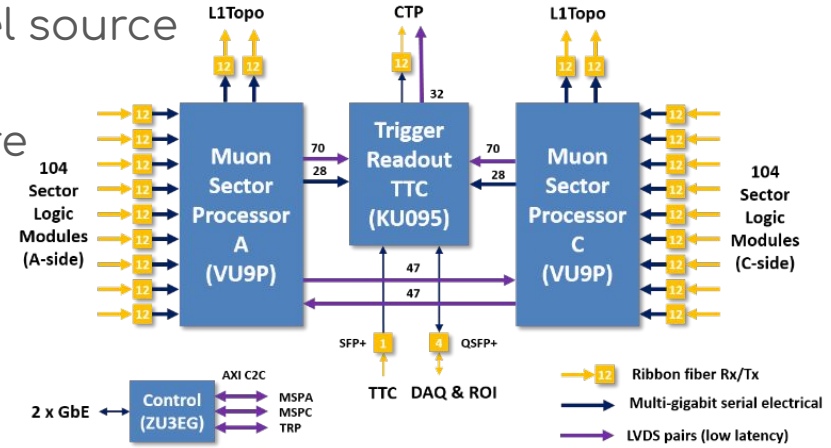
MUCTPI: A Phase 1 upgrade, pilot for Phase 2

- ATCA blade running Linux on a SoC
- Logic implemented on three FPGAs
  - Muon Sector Processor [x2] (MSP)
    - Timing alignment, multiplicity, overlap, Tx to Topo
  - Trigger Readout Processor (TRP)
    - TTC distribution, candidate merging, final readout



- A "hardware compiler" generates low-level source code for both VHDL and C++
- Cross-compilation of run control software
- Gitlab CI for firmware and software release deployment

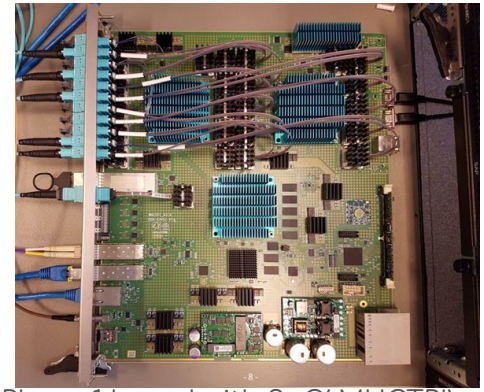
- Operating in ATLAS in Run 3 (2021-)



SoC experience for Phase 2 upgrades

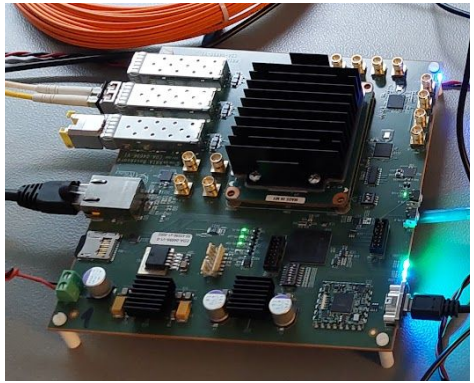
- All future platforms will feature SoC
  - Processing System (PS) will run AlmaLinux
  - Initially cross-installing, now standard `aarch64` images
  - `U-Boot` through `TFTP` to choose kernel and rootfs
  - `rootfs` mounted from "host" server

- System-on-Modules (SoM) for upgradability
  - Platform of choice: Xilinx Kria K26
  - Ongoing work: Adapting workflows
    - Many low-level procedures very similar
    - Need scalability from single system to ~50 LTI[1] boards



Phase 1 board with SoC(MUCTPI)

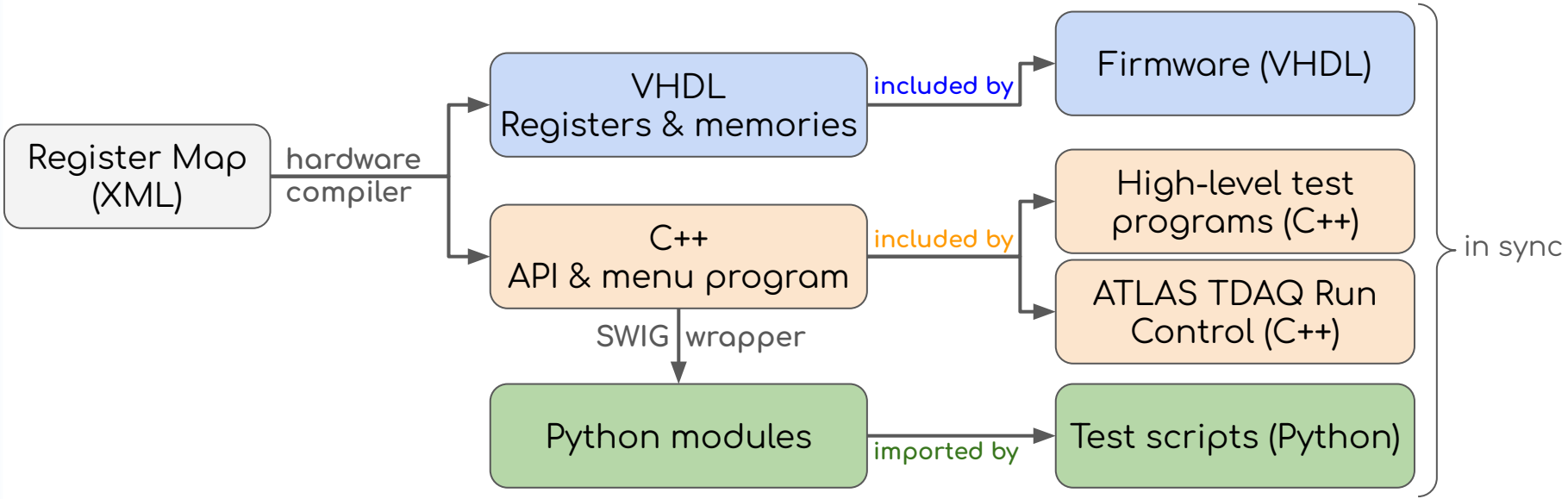
Kria SoM evaluation setup



[1]LTI=Local Trigger Interface; see later slides

MUCTPI experience for Phase 2 upgrades

Well-defined procedures to develop & deploy all components.

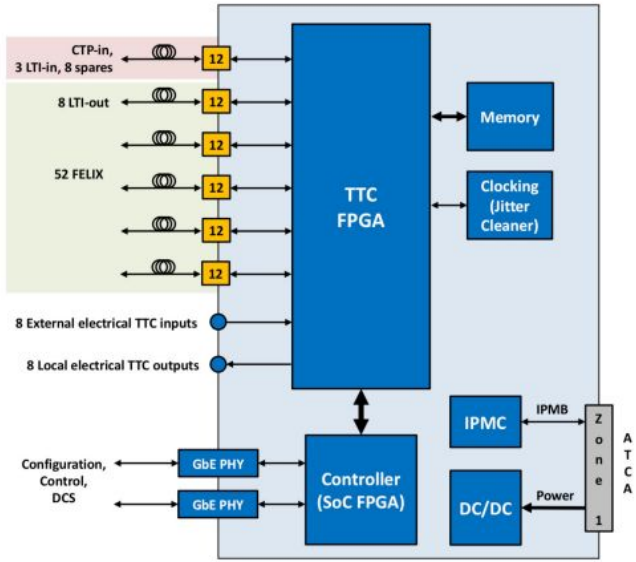


Common practices: CERN SoC interest group

Phase 2

The Local Trigger Interface (LTI) upgrade

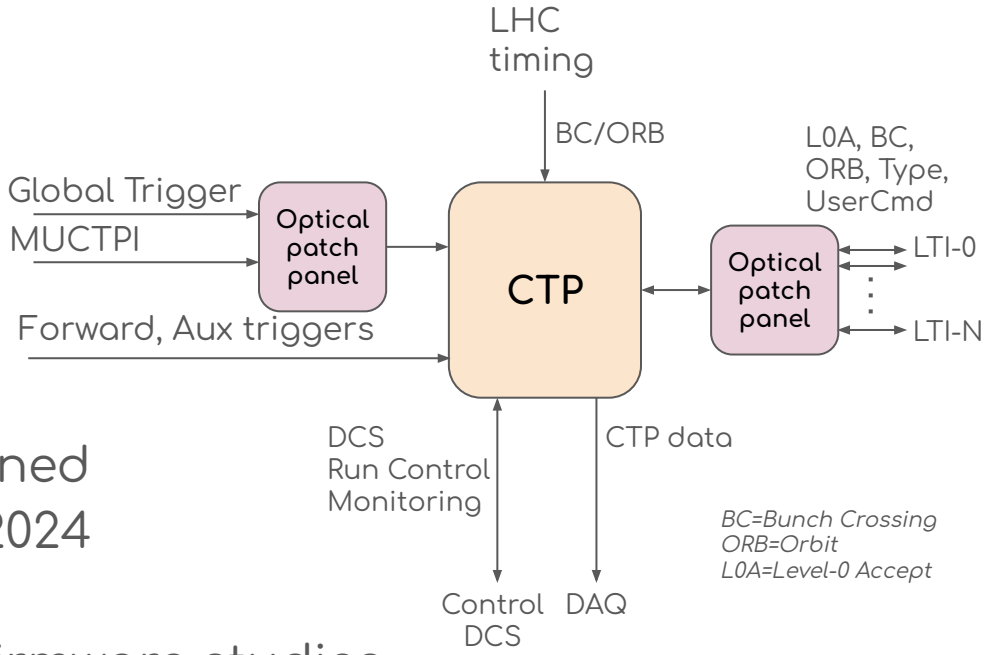
- Distribution of timing (TTC) signals and busy collection
  - Interface to CTP during physics running
  - Standalone trigger unit for sub-detector testing and calibration (master/slave options)
- Single ATCA blade with SoM
  - Kintex UltraScale+ & Zynq UltraScale+
- Prototype in production
- Time-Compensated Link (TCLink)
  - Meet detector requirements
    - clock phase stability <30ps
    - jitter <15ps
  - Allow compensation for temperature differences
  - In-situ phase measurements & external phase interpolator
  - Extensive testing with FPGA Mezzanine Cards (FMC)



- Some features
  - Standalone trigger
  - Per-bunch monitoring
  - Playback & snapshot memory

CTP in Phase 2

- Single ATCA blade with SoM
  - More (optical) inputs
  - More trigger items
  - Completely new software
- Functional specifications defined
- Prototype review & design in 2024
- Using evaluation boards for firmware studies
- Multiple features -existing and new- on trigger logic (next slide)

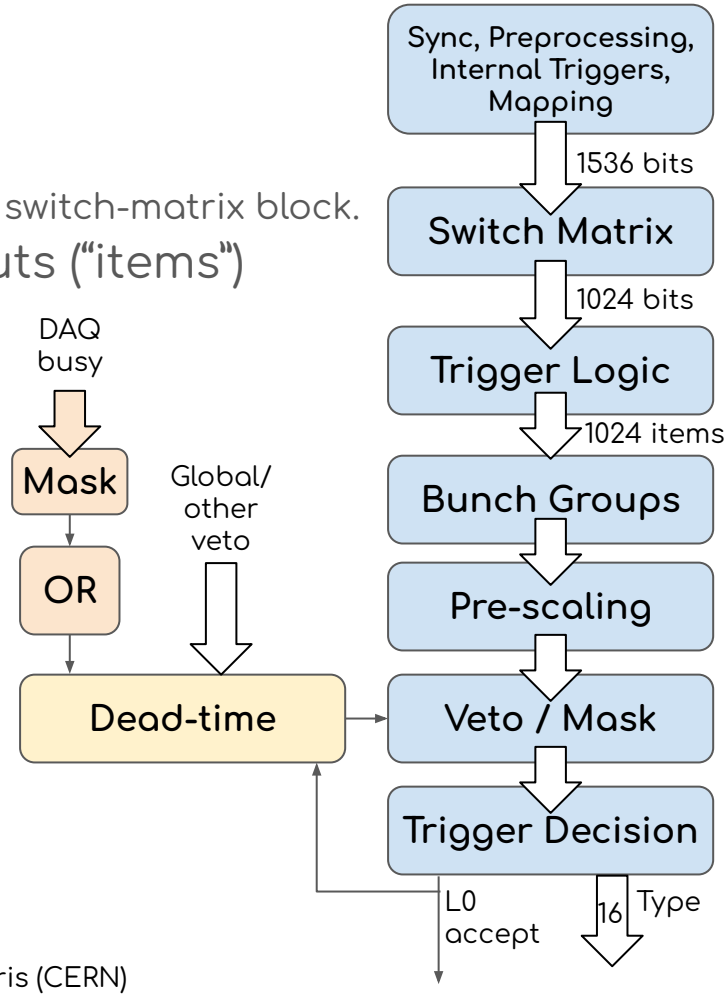


CTP in Phase 2 - features

- Up to 1024 trigger logic input bits
  - Selection from 1536 inputs implemented with a switch-matrix block.
- Up to 1024 logical combinations on inputs (“items”)
  - Expressions with **AND**, **OR**, **NOT** logic
- Run at 1 MHz with burst protection
  - Sliding window
  - Leaky bucket

< 4 in 5 BC
<=8 in 0.5 us
<=128 in 90 us

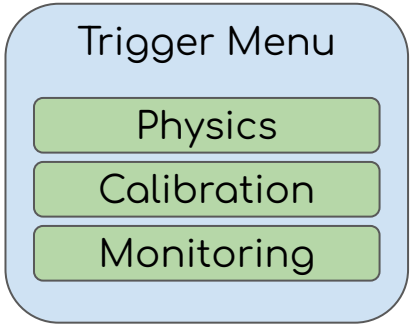
- Delayed triggers
  - New feature for long-lived particles
- More: partitioning, bunch matching, per-bunch monitoring



From physics requirements to trigger logic

Physics requirements are gathered in a “menu of items”, any of which triggers the Level-0 accept signal.

- Lookup tables and a content-addressable memory implement the trigger logic.
- Logical combinations of input bits (20GeV muon, 50GeV jet, etc) are “compiled” into configuration files (as before) by the Trigger Menu Compiler (TMC).
- New TMC implementation with python.

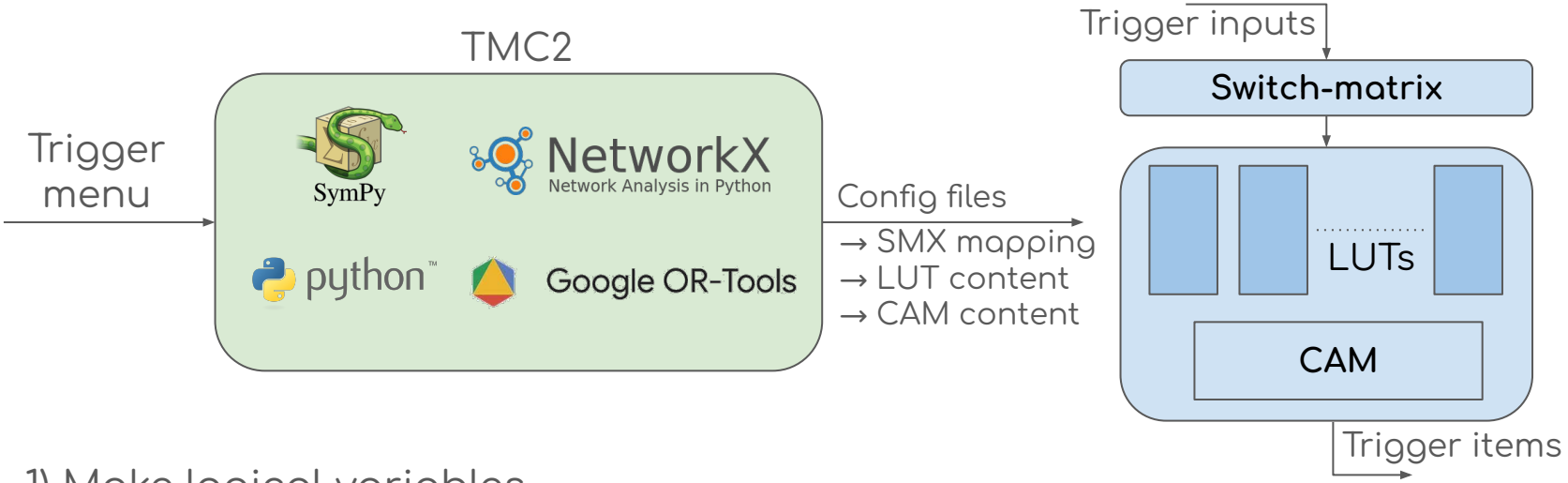


Example items:

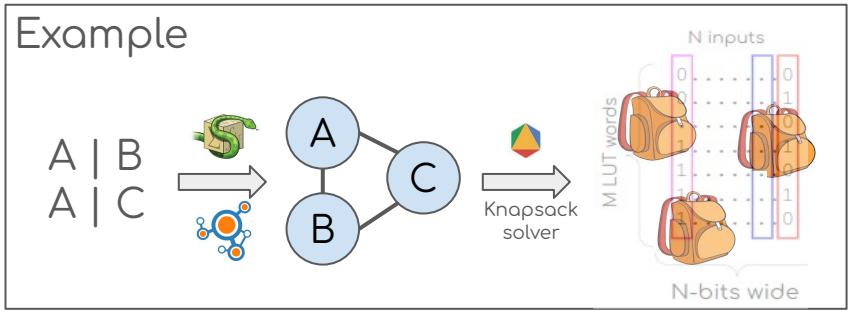
```
"MU5VF[x1] & MU3VF[x3]"
"eEM18M[x2]"
"NSWMon[x1]"
"RNDM0"
```

energy
multiplicity
type
flags

A new Trigger Menu Compiler for the CTP



1) Make logical variables
2) Simplify & CNF-ify[1] expressions
3) Isolate connected nodes
4) Assign groups to LUTs
5) Build configuration files



[1]Conjunctive Normal Form logic (AND of ORs)

Summary

Demanding conditions of HL-LHC require **major upgrades for the ATLAS experiment** in the next long shutdown (2026-2028).

ATLAS TDAQ and L1CT groups preparing for Phase 2 upgrades while ensuring smooth operation of current system.

Phase 1 upgrades serve as pilot for the upcoming ones.

Significant upgrades of key components in Phase 2, using modern techniques in hardware and software.

Thank you

References & links

ATLAS TDAQ Phase 2 Technical Design Report

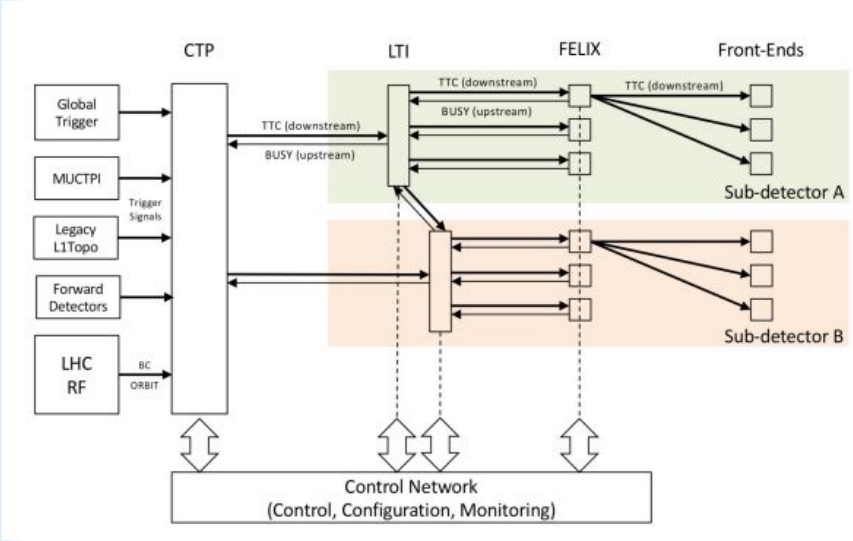
Continuous Integration for the Software and the Firmware of the New ATLAS Muon-Central- Trigger-Processor Interface (MUCTPI)

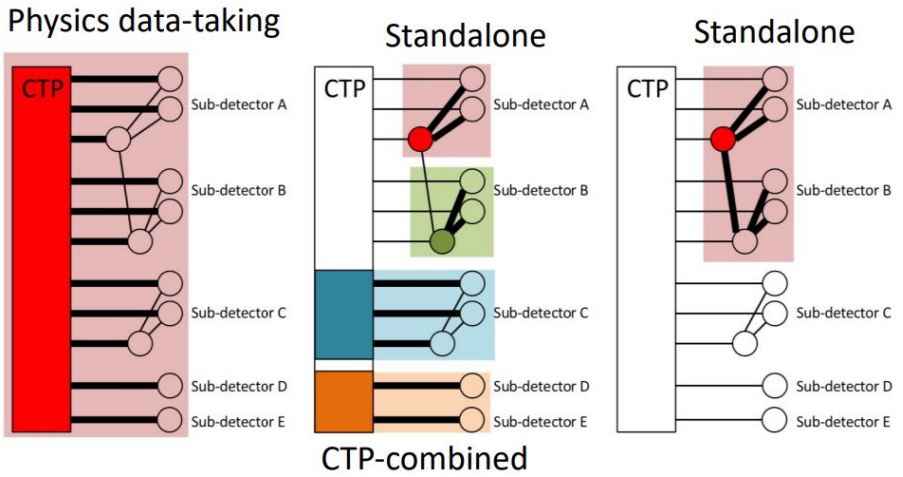
The new Muon-to-Central-Trigger-Processor Interface at ATLAS (ATLAS Note)

sympy | networkx | ortools

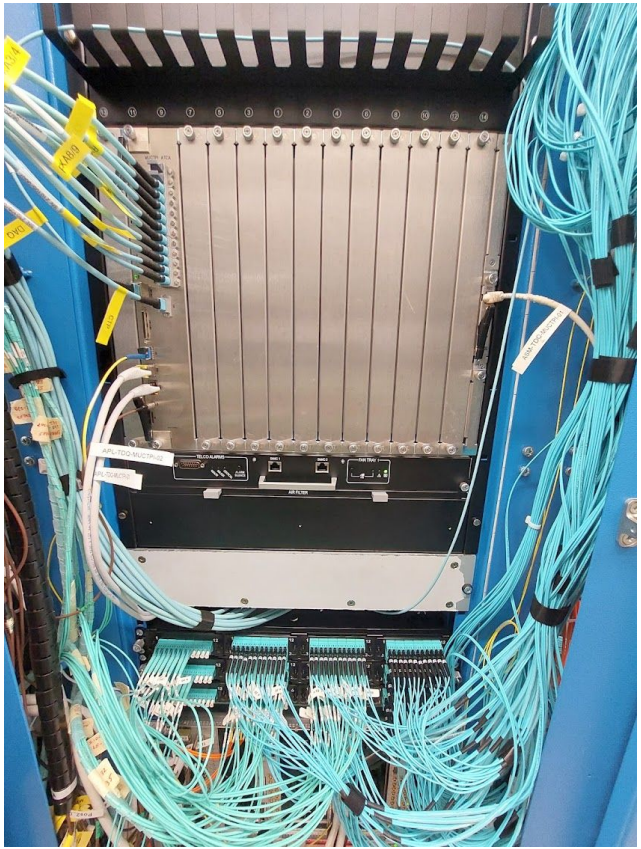
Extra material

TTC stream context





MUCTPI extra



MUCTPI prototypes

	SoC	MSP (fpga)
v1	32-bit Zynq-7000	Virtex Ultrascale
v2	32-bit Zynq-7000	Virtex Ultrascale+
v3	MPSoC: 64-bit Ultascale+	Virtex Ultrascale+

TTC distribution with a Time-Compensated Link (TCLink)

*An FPGA core for **picosecond**-level phase adjustment.*

- Lower **jitter**
- Better **stability** in phase uncertainty - O(ps).

Motivation for using the TCLink

- Compensate for **temperature** variations causing phase drifts
- Possibility to perform fine delay **adjustments**

Phase 2 detector upgrades for “4D” tracking in high pileup require clock phase stability (<30ps) and jitter <15ps

LTI modes

Slave mode:

- CTP Slave: CTP is the TTC Master
- LTI Slave: another LTI is the TTC Master
  - TTC signals and associated information will be taken from the CTP-in or one of the LTI-in dowlinks

TTC Master mode:

  - Each TTC signal is a programmable selection of local resources
  - L0A and associated information is produced in the MiniCTP
  - Parasitic running

Testing TCLink in the lab

- Clock jitter <5ps RMS measured in the lab environment for a single TClink stage.

- Observed phase uncertainty

  - Dependent on ambient temperature
    - Working on calibration scripts to understand behavior, and later evolve into continuous correction.

  - After resetting the board, observe phase shift.
    - Long studies evolved in a correction applied on hardware.