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## Sensor Prototypes for the ALICE ITS3 Upgrade

The ALICE Experiment will upgrade the innermost three layers of its Inner Tracking System (ITS) during the next LHC Long Shutdown (LS3). It is planned to partially replace the existing conventional setup using individual chips on staves by a novel concept, where wafer-scale sensors are bent to half-cylinders allowing for a tracker with an extraordinarily low material budget of  $0.07\% X/X_0$  per layer. The sensor chip will be based on Monolithic Active Pixels and fabricated in 65 nm CMOS technology exploiting stitching. During R&D, two stitched sensor prototypes, MOSS and MOST, were designed, where the first is less densely designed and the latter follows a more densely integrated in-pixel layout combined with a less dense power grid and power switches in the matrix. In the case of in-pixel short circuits, small regions of the matrix can be detached from the power grid restoring the retaining part of the overall functionality. The MOST readout is based on global high-speed lines spanning the entire approximately 25 cm long chip, which have successfully been operated. Procedures have been designed to select detector-grade ITS3 chips on wafer level using impedance measurements, powering tests, and functional tests. For MOSS, above 95% of the chip area can be operated. The majority of faults can be traced down to anomalous cross-connections in the topmost metal layers by correlating the grid design with thermal hotspots during power ramping. Several beam tests have proven efficient operation of MOSS prototypes, also under radiation load. The full size and full functionality prototype for the final production sensor, MOSAIX is currently under development, heavily profiting from studies done on MOSS and MOST prototypes. This contribution gives an overview of latest results including in-beam efficiencies obtained with the two large scale prototypes and an outlook of the next generation prototype.

## Category

Experiment

## **Collaboration (if applicable)**

ALICE

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