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43rd RD50 Workshop

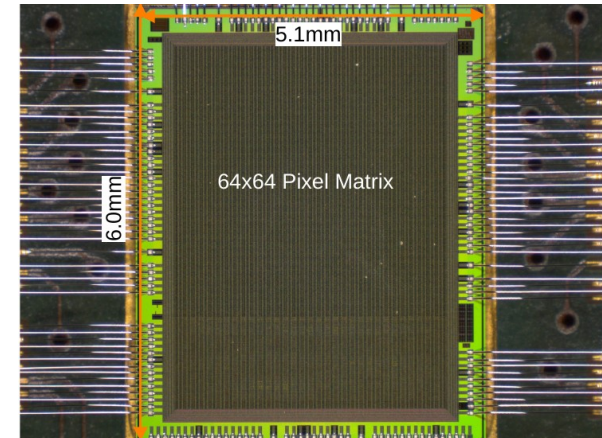
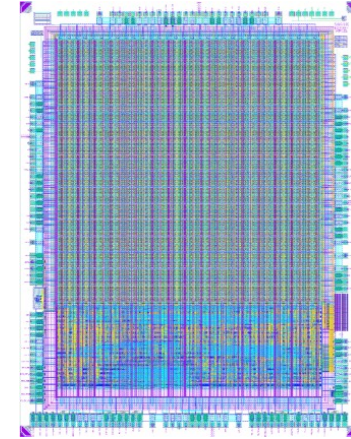
Beam test characterization of RD50-MPW3

Bernhard Pils on behalf of the HV-CMOS working group

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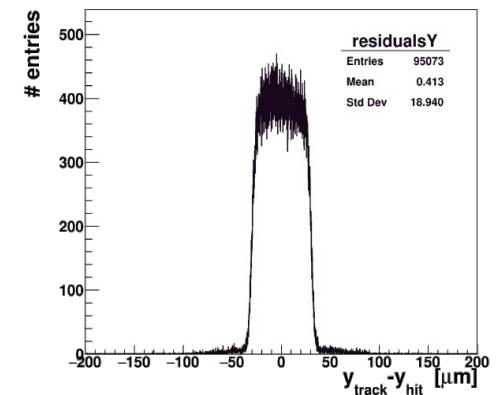
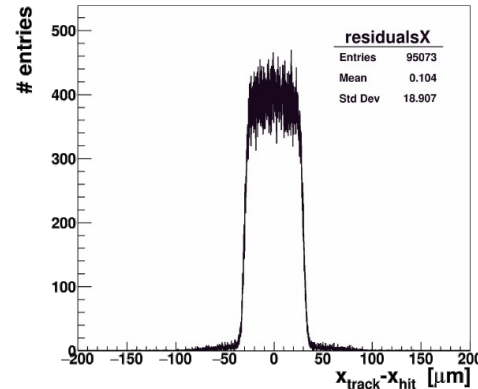
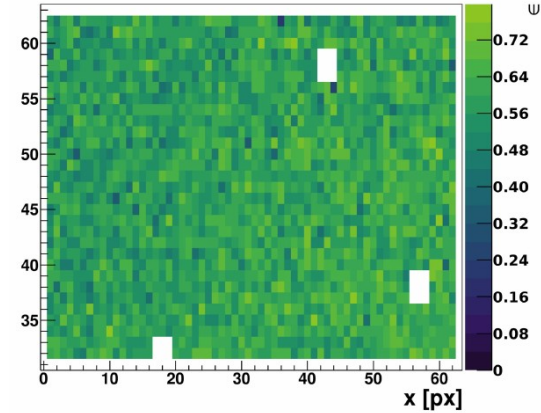
The RD50-MPW3

- *HV-CMOS chip fabricated in LFoundry 150nm process*
- Large collection electrode design
- 64 x 64 Pixel with pitch of 62 μ m
 - Arranged in 32 double columns
- Full analog and digital electronics inside pixel
- Fast clock at 320MHz
- 8 bit 50ns timestamps for ToT
- Digital periphery
 - I2C server for configuration
 - 8 bit per pixel
 - Data FIFO depth of 32 words for each double column



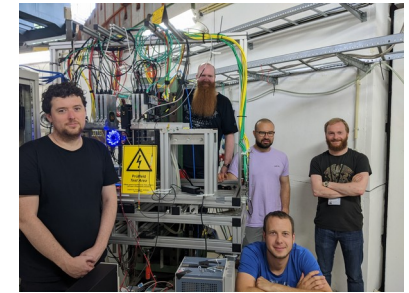
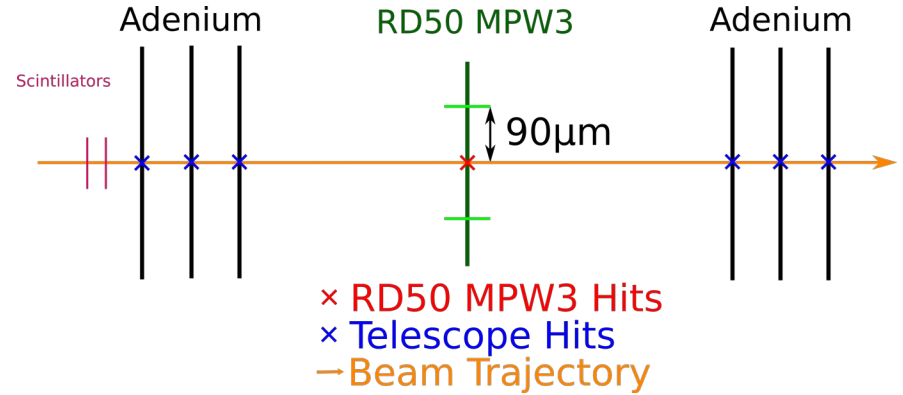
Reminder: Testbeam at CERN SPS

- Beam test at CERN SPS facility in Oct. 2022
- Severe issues with synchronization
- Only low statistic runs taken due to bugs in measurement setup
- Total efficiency of ~60% evaluated
- ~Binary spatial resolution measured
~18.9 μm



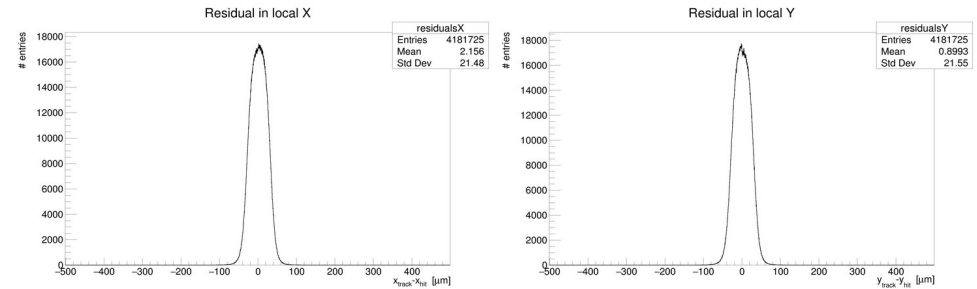
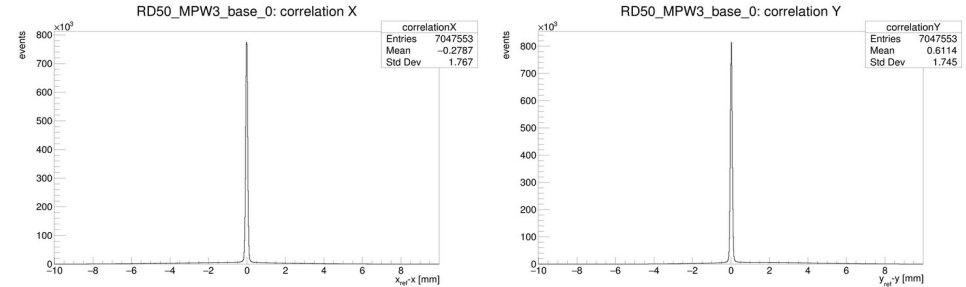
Testbeam Setup *DESY*

- Testbeam done in Jul. 2023 at *DESY* Hamburg
- Utilizing *Adenium* telescope
 - Based on *Alpide* chip
 - Pitch: $29\mu\text{m} \times 26\mu\text{m}$
 - 1024×512 pixel matrix
 - 6 planes
- Setup triggered by 2 scintillators operated in coincidence
- Telescope synchronized via trigger-numbers
- DUT (MPW3) synchronized via time-stamps
- Matching done by AIDA2020-TLU
- Electron beam with (mostly) 4.2 GeV, 6kHz used

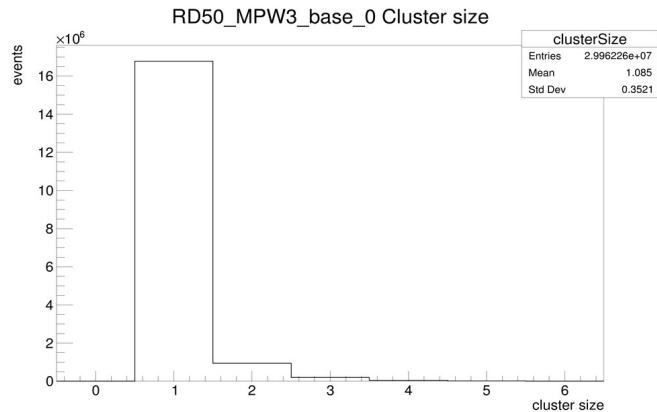
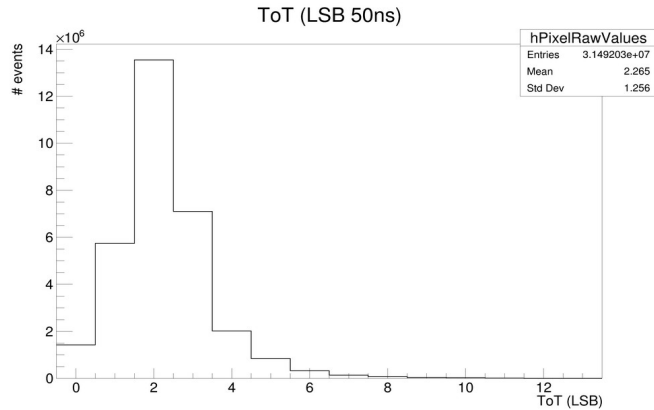


General Results *DESY*

- Correlations with very little background observed
 - Well synchronized
- Std. dev. of residuals show spatial resolution of $\sim 21.5\mu\text{m}$
 - Slightly worse than binary resolution of $\sim 18\mu\text{m}$
 - Reason: pointing resolution of telescope and alignment?

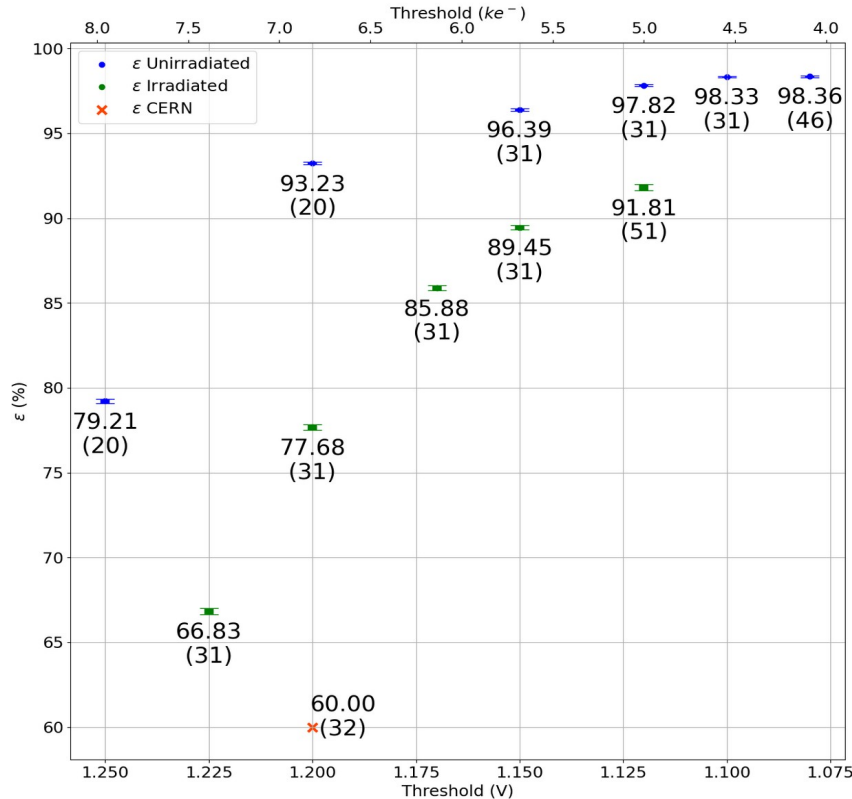


General Results *DESY* (2nd)

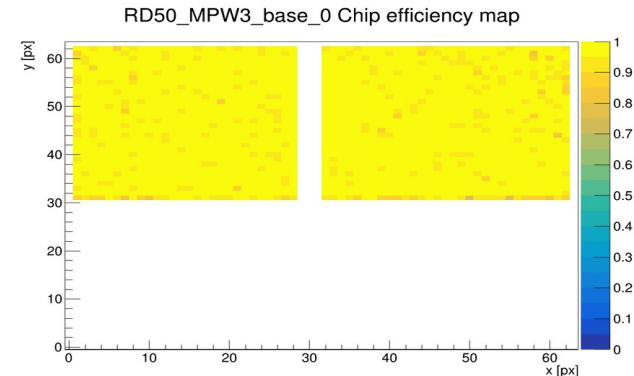


- ToT values of ~ 2.26 LSBs (on 50ns base) measured at 1.25V $\sim 8ke^-$ threshold
- Mean cluster size ~ 1 pixel / cluster
 - Center of gravity approach to increase spatial resolution not possible

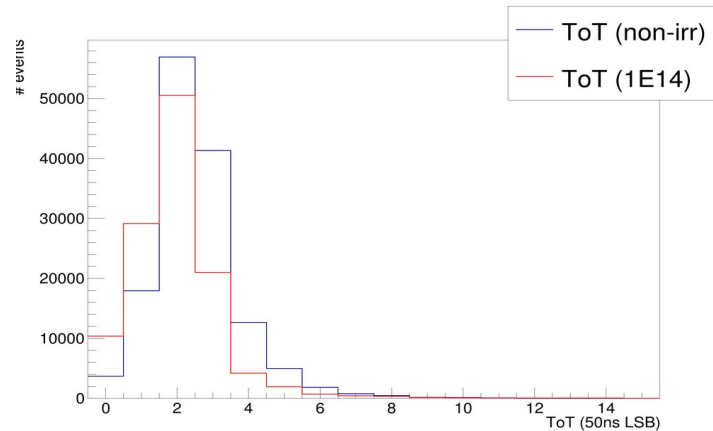
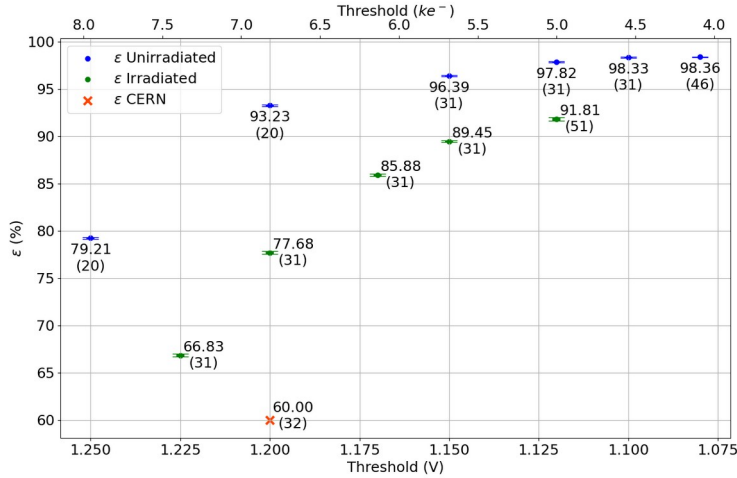
Chip - Efficiency *DESY*



- ~98% total efficiency encountered at threshold of ~4.09ke⁻ for non-irradiated sample
- After *CERN* test beam ~60% was the accepted value
- Due to noise issue ~bottom half of the matrix needed to be masked (number of masked rows indicated by numbers in brackets)



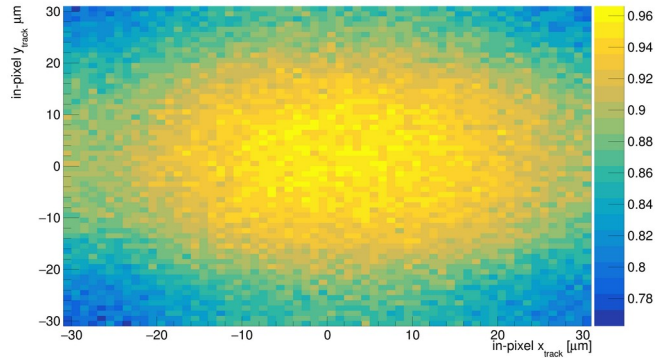
Results irradiated sample *DESY*



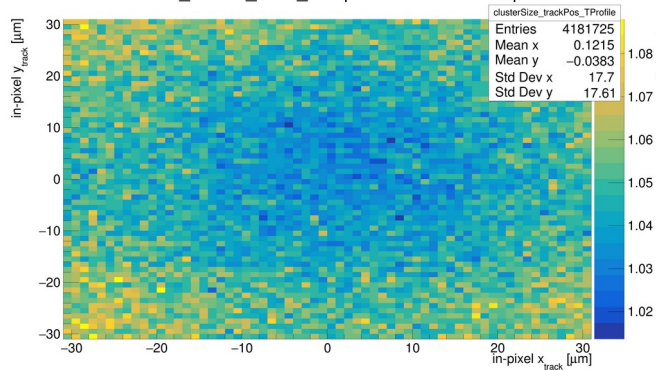
- Samples irradiated with 10^{14} 1MeV n_{eq} at JSI in Ljubljana
- Efficiency values in green correspond to irradiated sample
 - Efficiency decreases after irradiation
- Noise also increases (more rows masked)
- ToT decreases with irradiation (shown at 1.15V ~5600e⁻ thr.)
 - Mean Non-irradiated: 2.53 LSBs
 - Mean Irradiated: 1.98 LSBs
- Cluster-size and spatial resolution basically unchanged

In-Pixel Efficiency *DESY*

RD50_MPW3_base_0 Pixel efficiency map



RD50_MPW3_base_0 in-pixel cluster size map



- In-pixel efficiency (shown for 1.15V ~ 5.6ke⁻ thr.) shows worse efficiency in corners
- Cluster size map shows increased cluster-size in the corners
 - Tracks intersecting pixel corners cause bigger clusters → Charge sharing
- Charge sharing with neighboring pixels attenuated due to high threshold

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

The Piggy Board

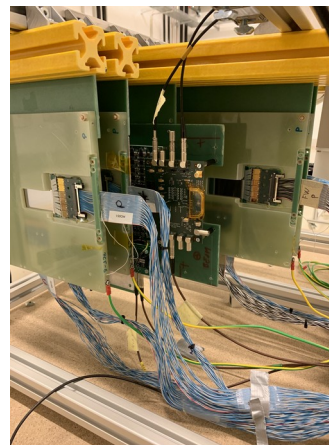
- Additional PCB
- Allows to operate two RD50-MPW3s with only one Caribou system
- High speed signals connected via ethernet cable
- Supply voltages connected via standard ribbon cable
- Was also installed at *DESY*, but DAQ was not able to synchronize data
- Intended use:
 - Easier to install / exchange in a telescope than base board (base needs to be plugged into the CaRboard)



Setup *MedAustron*

- *MedAustron* is a medical facility located close to Vienna
 - 50 km from *HEPHY*, beam time ~once a month
- Telescope with 4 DSSD planes
 - 512 x 512 “quasi” pixel
 - Pitch: 100 μ m x 50 μ m
- Triggered with 2 scintillators operated in coincidence
- 800 MeV proton beam with ~10kHz rate
 - No MIPs
- 2 DUTs
 - Base board 1.9k Ω cm non-irradiated
 - Piggy board 3k Ω cm non-irradiated
 - 32 bottom rows masked
 - Threshold 1.25V ~ 7900e⁻
 - Biased to -90V

MedAustron

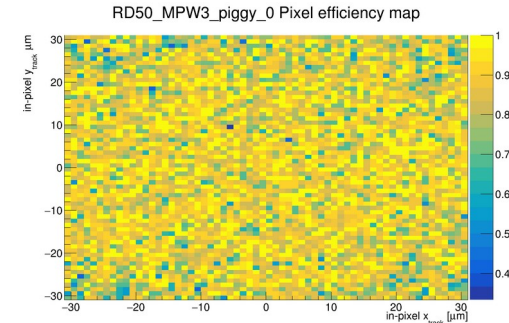
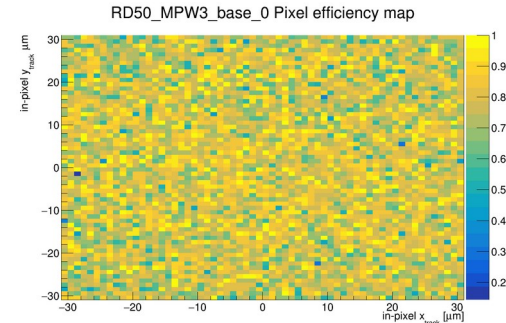
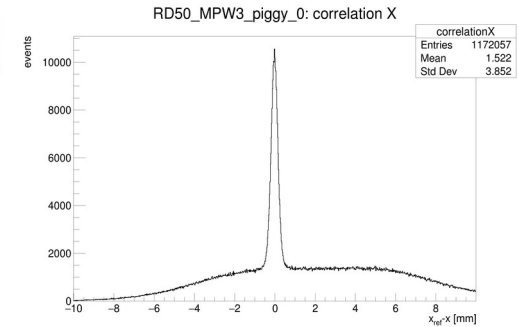
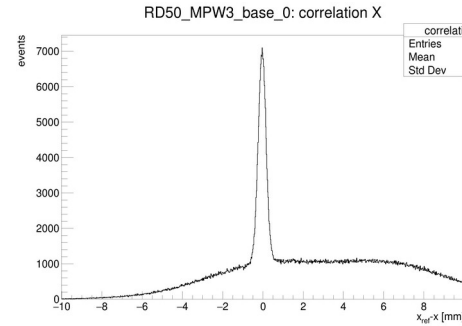


Piggy

Base

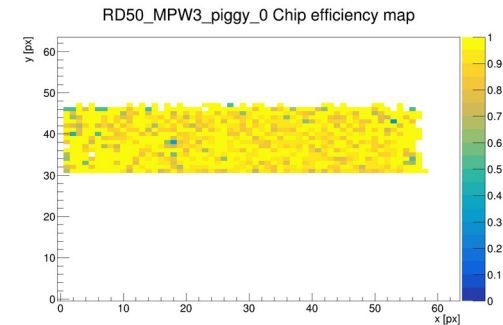
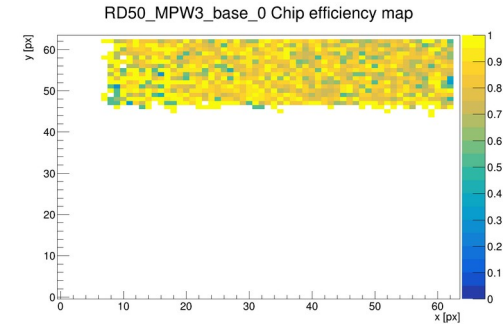
MedAustron Results

- Managed to properly synchronize Piggy board
- Correlations show increased background compared to *DESY* results
 - Synchronization parameters of the DSSD-telescope not known as well
- Total-efficiency Base $74.21(\pm 0.18)\%$
 - Efficiency at this threshold ($\sim 8ke^-$) at *DESY*: $\sim 79.2\%$
- Total-efficiency Piggy $86.33(\pm 0.16)\%$
- Corner effects for in-pixel plots less pronounced, reason: lack of statistics



MedAustron: Extending the telescope

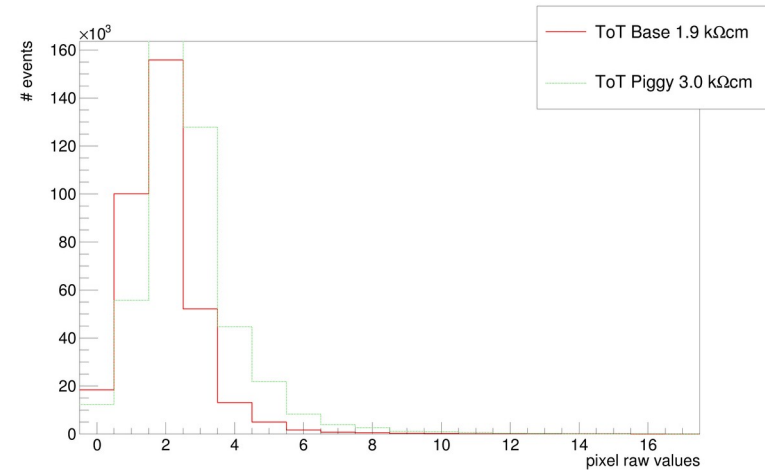
- Sacrificing one DUT in Corryvreckan analysis to act as extra telescope plane
 - Require 5 telescope-hits for each track
 - Yielding ~18 times less tracks
 - Allows to counter systematic (synchronization) errors in the analysis (same DAQ used for both DUTs)
 - Tracks get better resolution
- Efficiency base $81.73(+0.38, -0.39)\%$
 - In better agreement with *DESY*
- Efficiency piggy $92.26(+0.28, -0.29)\%$
- Misalignment of base and piggy → Only small area of chip taken into account



Discrepancies

- Base vs. Piggy:
 - ~10% higher efficiency for MPW3 on Piggy
 - Only significant difference: resistivity of substrate
 - Differences also seen in ToT values
 - 1.9kΩcm: 1.94 LSB
 - 3kΩcm: 2.68 LSB
 - Different threshold behavior?
 - Greater depletion depth for 3kΩcm substrate?
 - Work in progress

- *MedAustron vs. DESY*
 - *Efficiency at MedAustron* ~2% higher at same threshold
 - Lower beam energy at *MedAustron* → More energy deposited in detector



Outlook

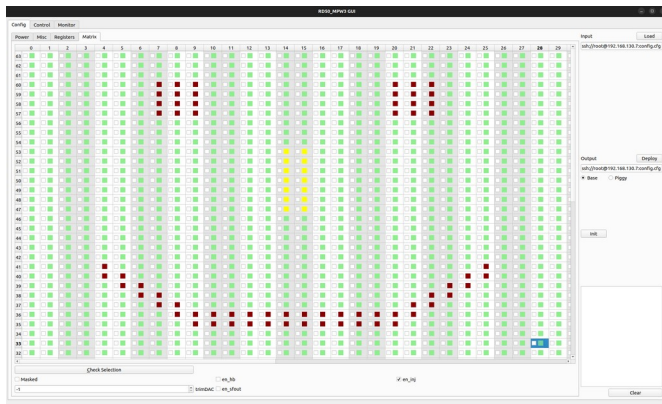
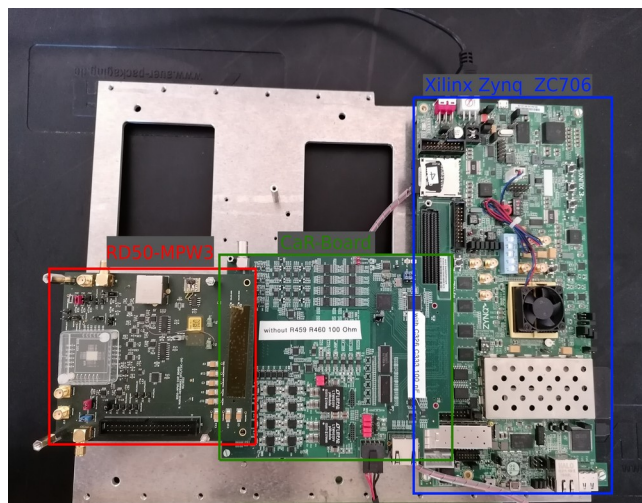
- MPW3:
 - Work on Allpix² simulations started
 - Aiming to reproduce *DESY-TB* results to improve understanding of chip
 - Annealing studies with irradiated samples
- MPW4:
 - Should be delivered by *LFoundry* in the next few weeks
 - Noise issue should (hopefully) be resolved
 - Lab work: I-V measurements, proper calibration with injections
 - 2 Beam test campaigns already scheduled in 2024
 - End of Mar. at *MedAustron*
 - End of Apr. at *DESY*



- Thanks for your attention!
- Questions?


BACKUP

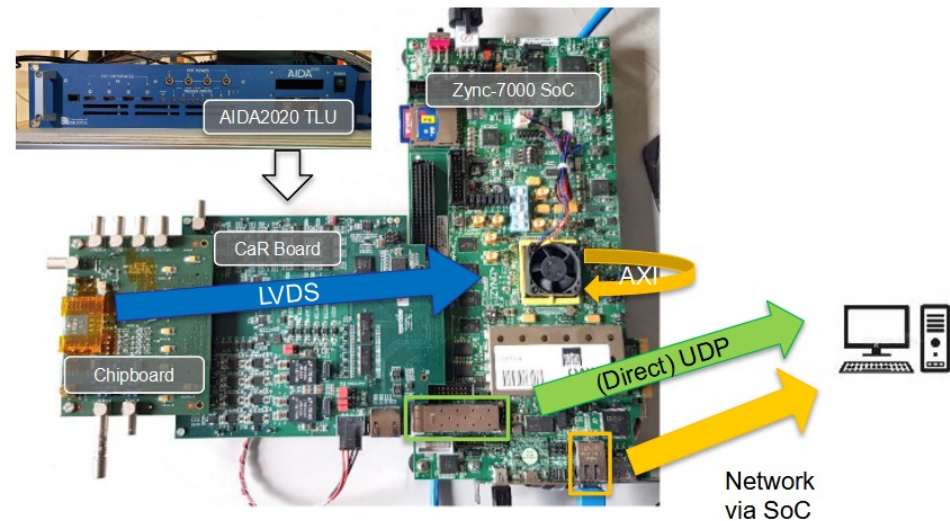
Base DAQ



- Caribou system
- Implemented Peary Device
 - Custom I2C interface (16 bit addresses)
- GUI for configuration
 - Generating Peary config files

Testbeam DAQ

- Fully integrated into EUDAQ2
- CaribouProducer too slow for full read-out rate
 - Only used for run-control commands
- Custom UDP (1 Gbit/s) Data-Collector implemented
 - Multi-threaded approach
 - More like a EUDAQ-producer, but directly storing to disk
- EUDAQ-monitor integrated in GUI
- EUDAQ-Producer for submission of run info to ELog server
- Analysis done with *Corryvreckan* 



DAQ improvements

- Problem at *CERN*: synchronization
 - 1 global timestamp for ~1300 hits
 - Data preprocessor looking for overflows in TS-LE to refine hit-timestamps
- FW adjustments allow for global timestamp for ~each hit

CERN 2022

UDP Pack		64 bit counter 0x005F918A4C0812AF
Frame	SoF 0xAF08A124 Hit 0x10F31210 Hit 0x193E3836 EoS 0xE080A143	8 bit Overflow-counter Overflow of overflow
Frame	SoF 0xAF01F338 Hit 0x1C0C2A29 Hit 0x0B7E4448 EoS 0xE081F331	
Frame	SoF 0xAF0808A8 Hit 0x08084848 EoS 0xE08080A9	
Frame	SoF 0xAF081386 Hit 0x10454F4D Hit 0x1CDA928D EoS 0xE0801387	
Frame	...	
Frame	...	
Frame	...	
Frame	...	

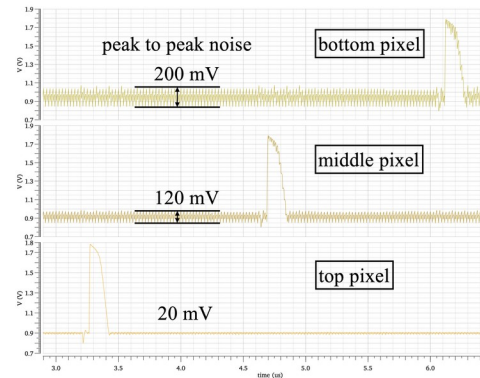
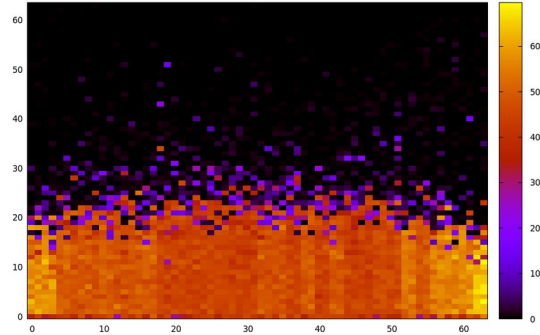
Improved 2023

UDP Pack		
Frame	SoF 0xAF013187 Hit 0x10454F4D EoS 0xE0808088	24 bit LSB global TS
Frame	SoF 0xAF0131E6 Hit 0x1CDA928D EoS 0xE0808088	24 bit MSB global TS
Frame	SoF 0xAF0131E6 Hit 0x1B524848 EoS 0xE0808088	
Frame	SoF 0xAF0131E8 Hit 0x10E64847 Hit 0x1F55E9E7 EoS 0xE0808088	
Frame	...	
Frame	...	
Frame	...	
Frame	...	

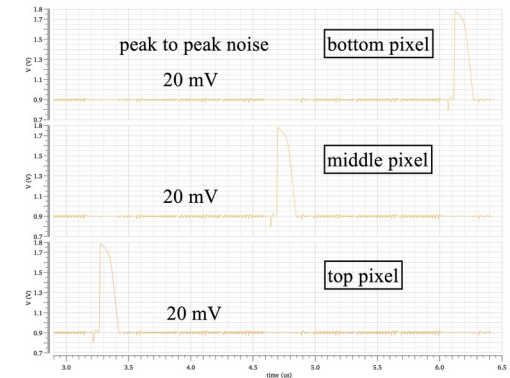
The Noise Issue

- Shared power lines between pixel matrix and digital periphery
 - High noise occurrence in bottom rows correlated to digital activity
- Analog simulations as reported in last RD50 workshop reproduced the measured behavior
- Changes in design of upcoming RD50-MPW4 should (hopefully) fix this behavior

Noise map of the uncalibrated chip at $V_{th} = 1.2V$ and $TDAC = 7$
record time: 10s



Common Power and GND (MPW3)



Separated Power and GND (MPW4)

Efficiency too high?

- According to (Allpix²) simulations MPV of deposited charge $\sim 46\text{ke}^-$ in $300\mu\text{m}$ silicon with DESY beam
- Assuming depletion depth of $100\mu\text{m}$
- (Back of the envelope) calculation yields $\gtrsim 15\text{ke}^-$ transferred to implants
- With threshold of $\sim 5\text{ke}^-$ efficiency of 98% plausible

