

State of the art and future developments

Last 43rd **RD50 Workshop** on Radiation Hard Semiconductor Devices for High Luminosity Colliders

28 Nov – 1 Dec 2023

CERN





on behalf of the ARCADIA Collaboration

¹ INFN Torino

Three main types of **monolithic** sensors

▷ Depleted Field Effect Transistor (DEPFET):

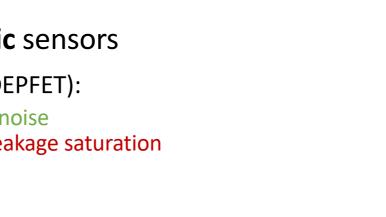
low input $C \Rightarrow$ low noise gate reset due to leakage saturation

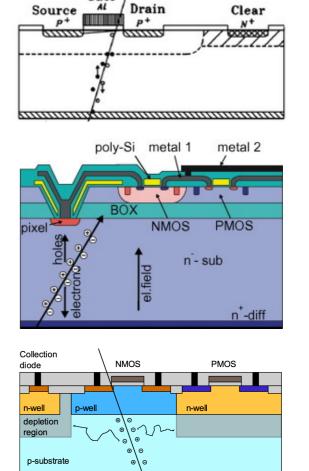
▷ Silicon-on-Insulator (SOI):

low input C \Rightarrow low noise back-gate effect hole accumulation layer after irradiation \Rightarrow low rad-hard

▷ Complementary Metal-Oxide Semiconductor (CMOS):

low power, high-rate capability, low material budget commercial technology \Rightarrow low cost per unit area slow diffusion in undepleted substrate competitive collection by *n*-wells





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Gate

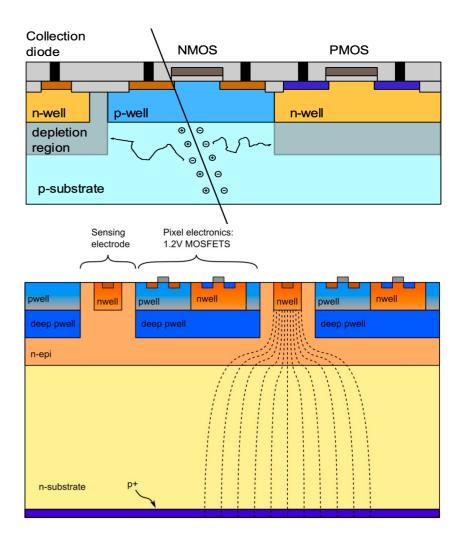
Monolithic particle detectors

Possible solutions in standard CMOS:

- ▷ lowering substrate doping (high resistivity)
- ▷ use high bias voltage
- ▷ isolate the *n*-wells with deep-*p*-wells
- ightarrow put the electronics inside the collection diode
- ▷ isolate the electonics with a buried oxide (SOI)

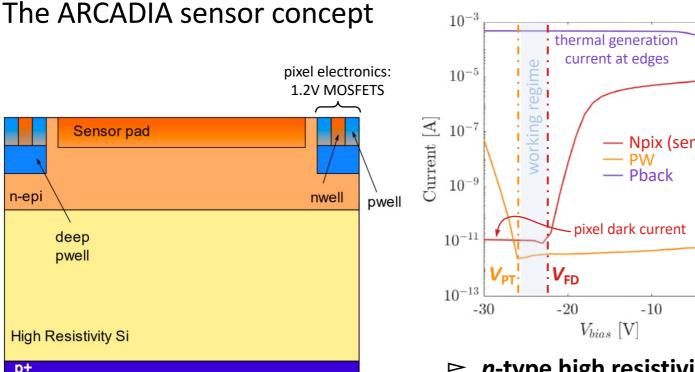
The ARCADIA approach (from SEED project):

- ▷ MAPS, Monolithic Active (integrated amplifier) Pixel Sensor
- ▷ **fully depleted** pixel sensor with integrated electronics
- ▷ use of deep-p-wells
- ▷ *n*-type epitaxial layer to better control the potential barrier
- ▶ 110 nm CMOS process (LFoundry)





Monolithic particle detectors

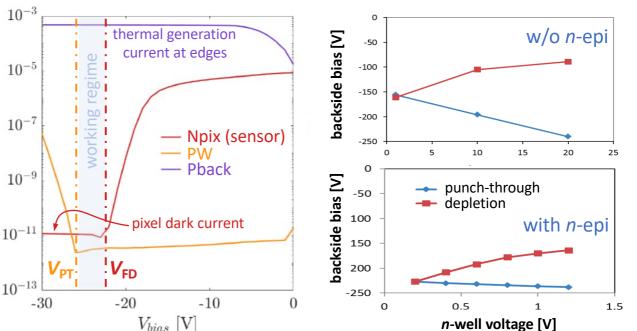


Main limitations:

n-epi

D+

- edge breakdown due to the topside voltage
- punch-through due to the backside bias \triangleright



- *n*-type high resistivity active region
- **deep-***p***-wells** shielding *n*-wells with electronics \triangleright
- **reverse-biased** junction: depletion grows from back to top
- sensing electrodes can be biased at low voltage (< 1 V) \triangleright
- *n*-epi layer delays the onset of punch-through hole current

ARCADIA

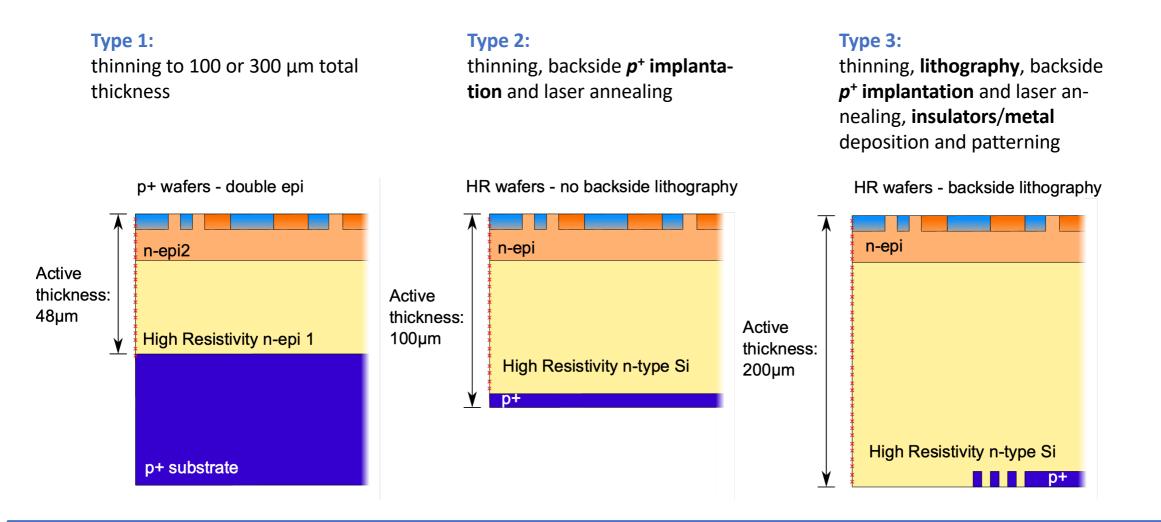
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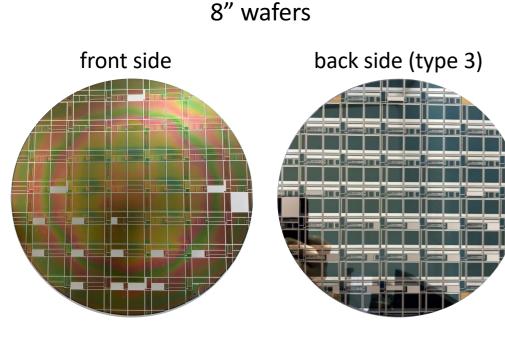
Monolithic particle detectors



The ARCADIA substrates and post-processing

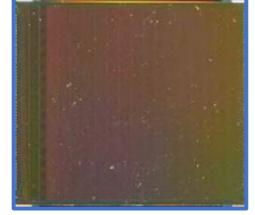






Structures:

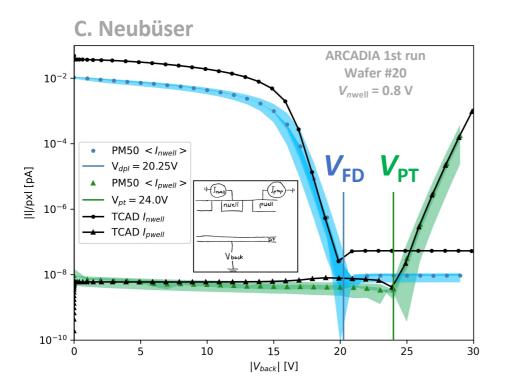
- small pixel arrays with different pitch (10 μm 25 μm 50 μm) with and w/o active readout
- strip detectors with and w/o active readout
- passive test structures for sensors characterization and process qualification
- **Main Demonstrator**: **25-μm-pitch** pixel sensor, **512** × **512** array



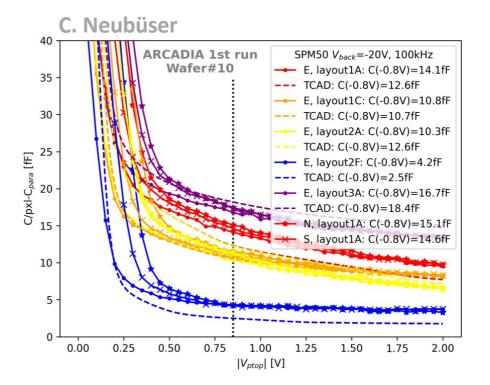
ARCADIA Main Demonstrator

passive test structures block

Electrical characterizations



- ▷ different **pixel layouts** have been tested
- ▷ intra- and inter-wafer uniformity evaluated
- TCAD parameters adjusted on experimental results

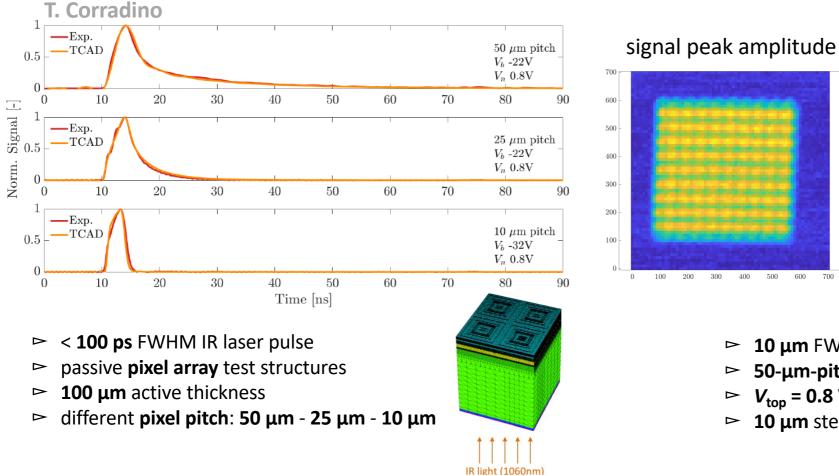


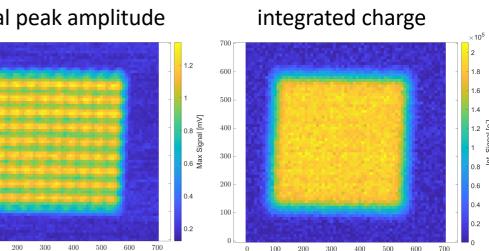
▷ capacitance dominated by the sensor perimeter

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Dynamic response with laser





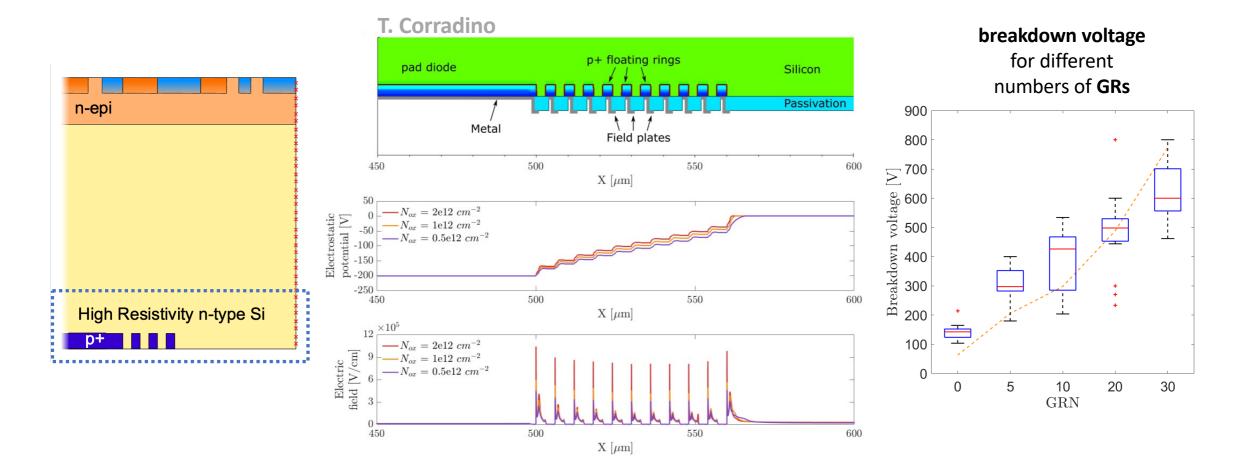
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- 10 μm FWHM focused red laser
- ▶ **50-µm-pitch** test structure
- \triangleright V_{top} = 0.8 V and V_{back} = -22 V
- ▶ **10 µm** steps in *X* and *Y* directions

Backside layout optimization (Type 3)



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static characteristics Active thickness (µm) 200 Pixel pitch (µm) @ 100-µm-thick 48 100

25

48

Type 2

10⁻⁸

10⁻⁹

Current [A]

10^{-11 ⊦}

 10^{-12}

Ē

Type 1

First ARCADIA engineering runs

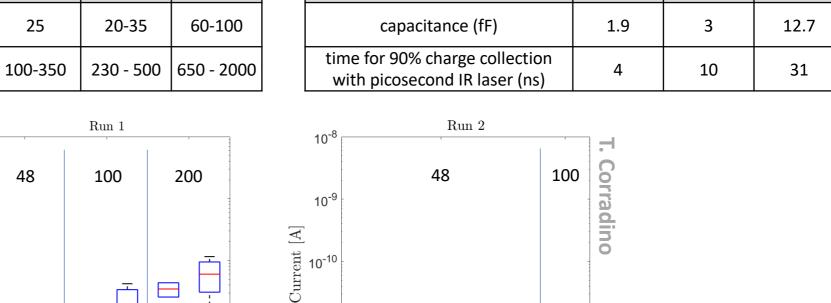
Type 3

dynamic characteristics

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Type 2

<u>–</u>



Type 1

dark currents in 1.5 mm × 1.5 mm **pixel** arrays with different active thicknesses



Pixel characterization

bias voltage (V)

dark current density (pA/cm²)

10⁻¹¹

10⁻¹²

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25

50

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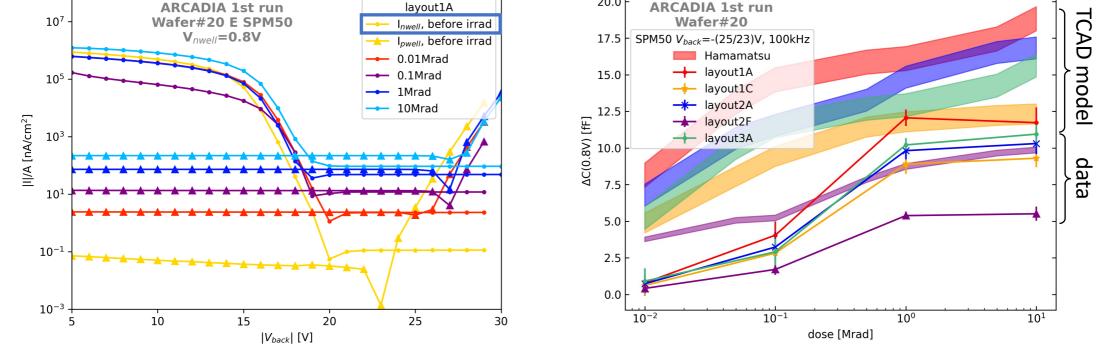
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First ARCADIA engineering runs Pixel radiation hardness: X-rays @ University of Padova, Italy



▷ capacitance post-irradiation overestimated by the Perugia model with Hamamatsu parametrization

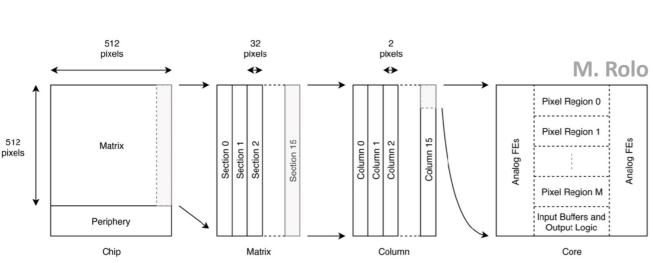
C. Neubüser



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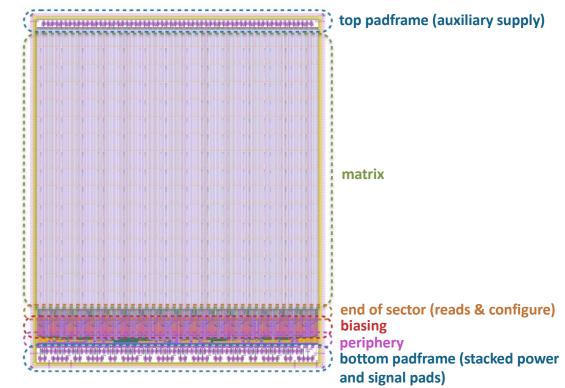
Neubüser



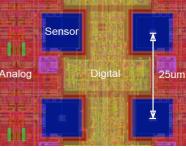


Main Demonstrator - architecture

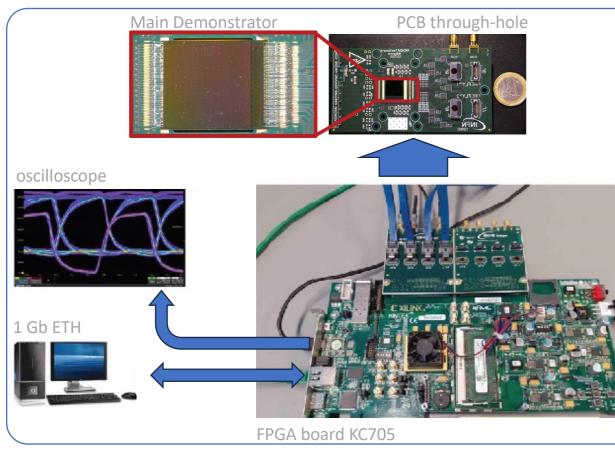
- ⊳ Pixel pitch: 25 μm
- ▷ Array core area: 1.28 cm × 1.28 cm (262144 pixels)
- ▷ Electronics: analog and digital, with in-pixel threshold and data storage
- Architecture: event-driven, with active pixels sending their address to the chip peripheral circuits
- ▷ (Low) power: 20 mW/cm²
- ▷ (High) event rate: 100 MHz/cm²

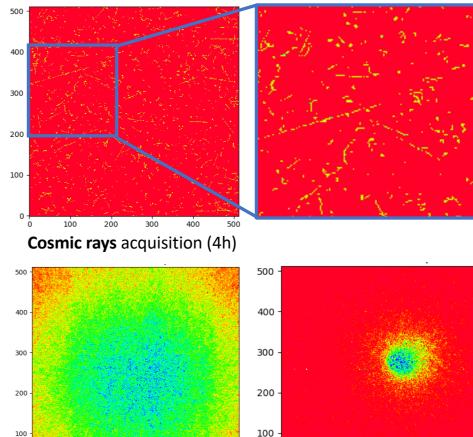






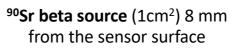
Main Demonstrator - acquisition setup

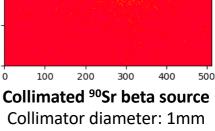




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▶ Total **power consumption**: **10 mW/cm²** at low event rates ▶ **Design specification**: **20 mW/cm²** at rates up to 100 Mevents/cm²





INFN

ECAL Absorber - RICH **Muon chambers** Magnet

ALICE 3 **TOF** detector:

FCT

ALICE

- ▷ high-resolution tracking and vertexing
- ▷ particle ID with low $p_T \Rightarrow \sigma_t \sim 20 \text{ ps}$



Sensor pad

Sensor pad

Gain layer

nwell

nwell

pwell

n-epi

D+

n-epi

- D+

TOF

Tracker

Vertex detector

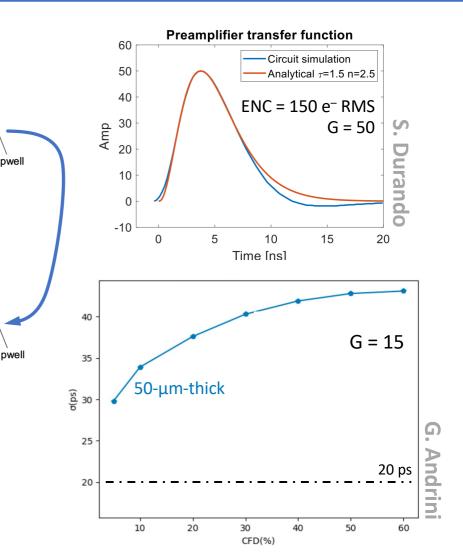
deep pwell

High Resistivity Si

deep

pwell

High Resistivity Si



The ARCADIA run-3



high-resolution tracking and vertexing

ALICE 3 **TOF** detector:

M. Mandurrino, INFN Torino

ALICE

▷ particle ID with low $p_T \Rightarrow \sigma_t \sim 20 \text{ ps}$

Sensor pad

Sensor pad

Gain layer

nwell

nwell

pwell

pwell

n-epi

D+

n-epi

D+

TOF

Tracker

Vertex detector

deep pwell

High Resistivity Si

deep

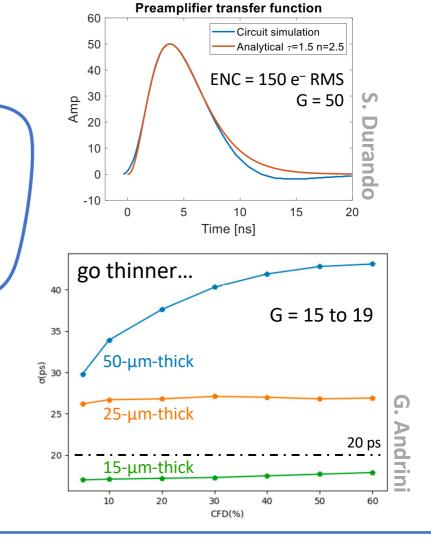
pwell

High Resistivity Si



15

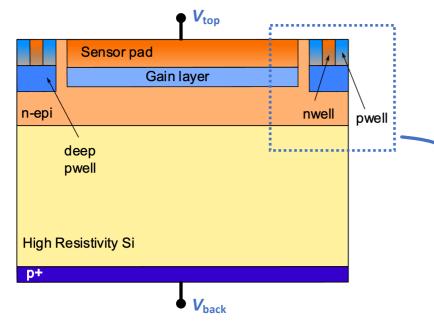
Muon chambers







Sensor structure and layout

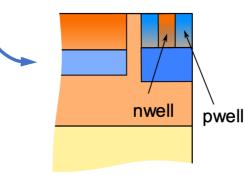


 V_{top} (30-40 V) determines the gain, while V_{back} (-30 V) defines the drift field in the substrate

top voltage limited by edge breakdown backplane bias limited by punch-through

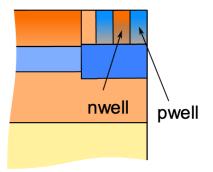
Layout A2:

standard solution \Rightarrow direct path to the n^+ collecting electrode for charges at border



Layout A1:

deep-*p***-wells** are in connection with the *p*-gain implant ⇒ more uniform charge multiplication



- ▷ four **gain dose splittings** to cope with implantation uncertainties
- ▷ target: gain in the range 10 30
- ▷ 50, 100 and 200 µm active thicknesses



MadPix: first small-scale (4 × 16 mm²) demonstrator with gain and integrated electronics

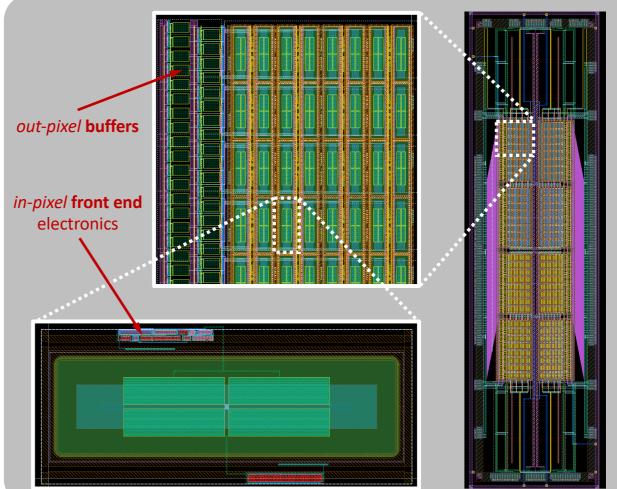
- 8 matrices (64 pixel pads each) implementing different sensor and front-end flavours
- \vartriangleright pads of 250 × 100 μm^2
- ▷ readout: 64 × 2 analog outputs on each side
- ▷ **rolling shutter** of single matrix readout

Front-end (in-pixel)

- Cascoded common source amplifier, followed by a differential buffer (1.2V)
- AC-coupled with sensor (in order to decouple it from the sensor top voltage)
- Power consumption: 0.18 mW/ch

Source follower out-pixel buffers (3.3V)

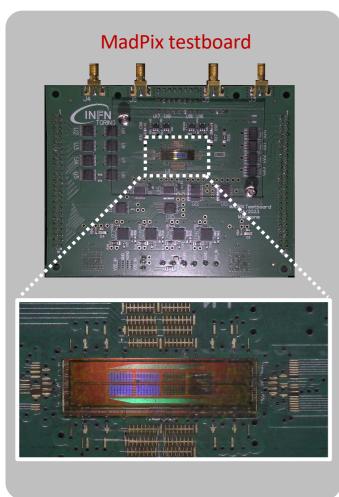
- ▷ AC-coupled with FE
- Power consumption: 1.65 mW/ch

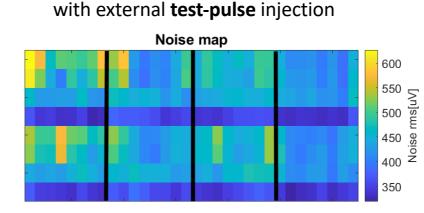




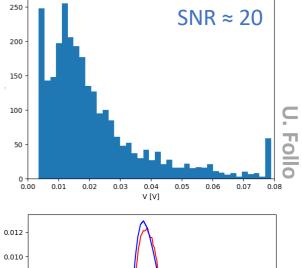
MadPix: first small-scale (4 × 16 mm²) demonstrator with gain and integrated electronics

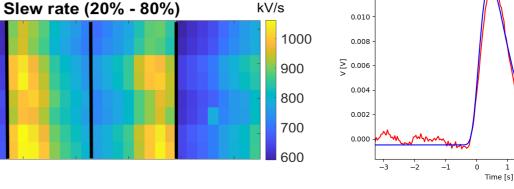
Noise and slew-rate characterization





First data with **beta source** (⁹⁰Sr)





Data

U. Follo

1e-8

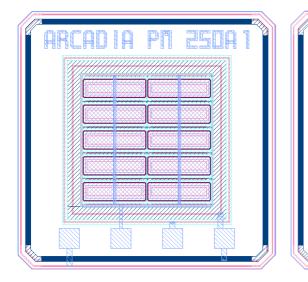
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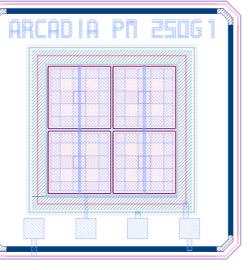


Electrical characterization – standalone passive test-structures

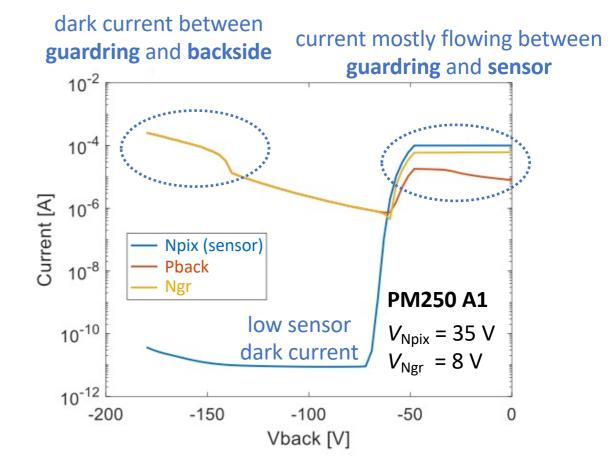
Designed for test at the probe station and with external amplifiers



Rectangular passive pads: $70 \ \mu m \times 250 \ \mu m$

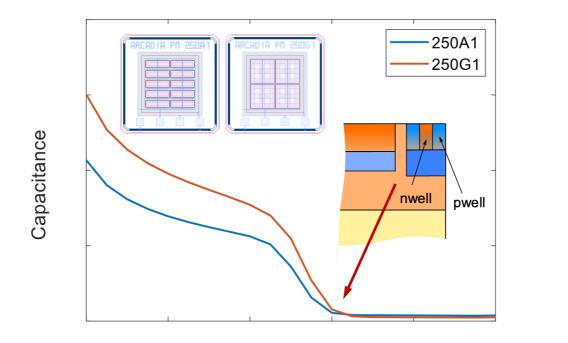


Square passive pads with large fill-factor: 250 μm × 250 μm

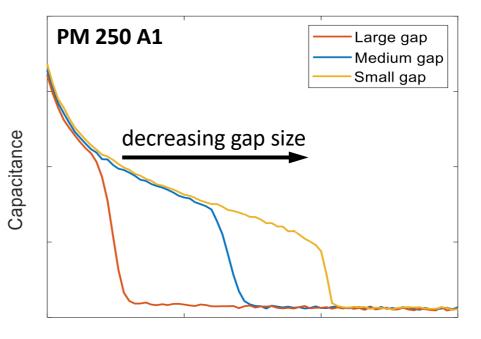




Electrical characterization – standalone **passive test-structures**



Vtop [V]



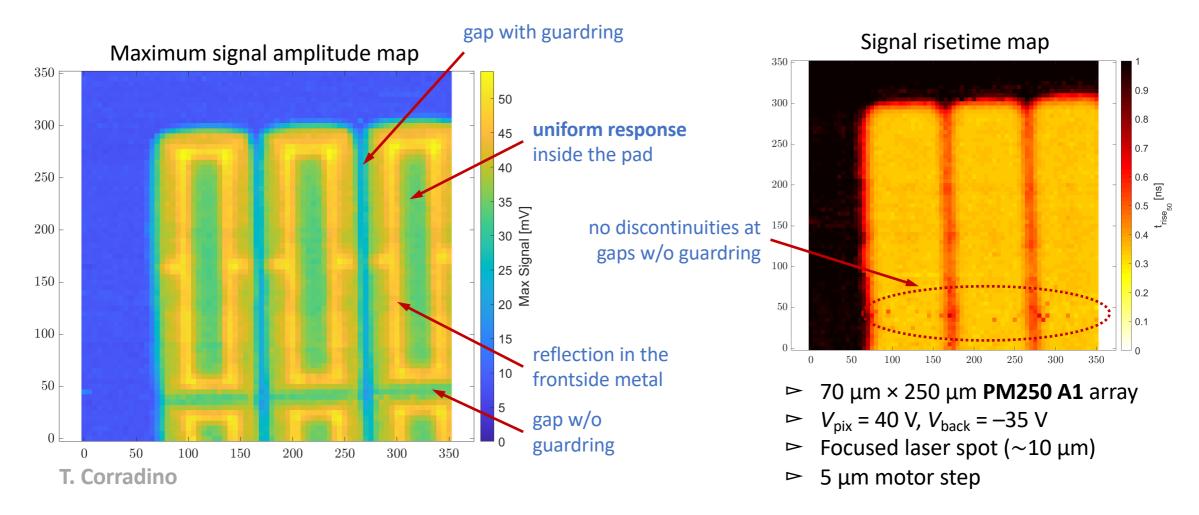
Vtop [V]

Differently from standard LGADs, the *C*(*V*) does not allow to reconstruct the whole gain implant profile, since the **gaps** between **deep-***p***-well** and *p*-gain are depleted earlier

The **knee** observed in the *C*(*V*) curves depends on the **size** of the gap. A **larger gaps** are fully **depleted** at **lower voltage**

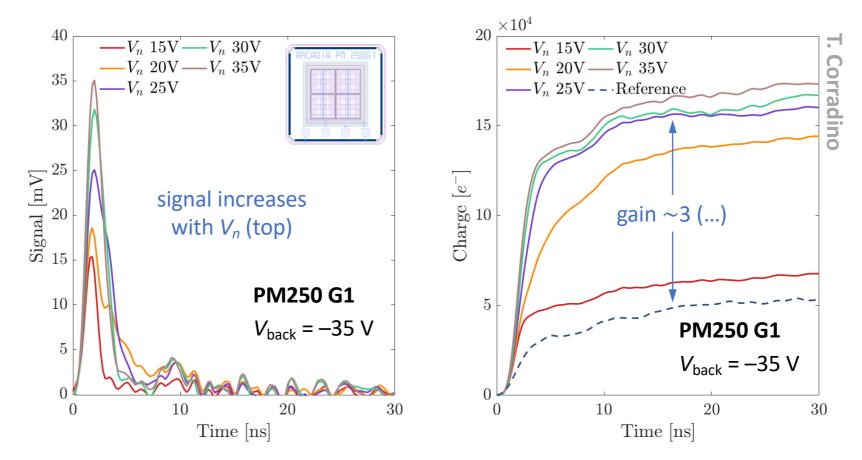


Dynamic characterization – standalone passive test-structures



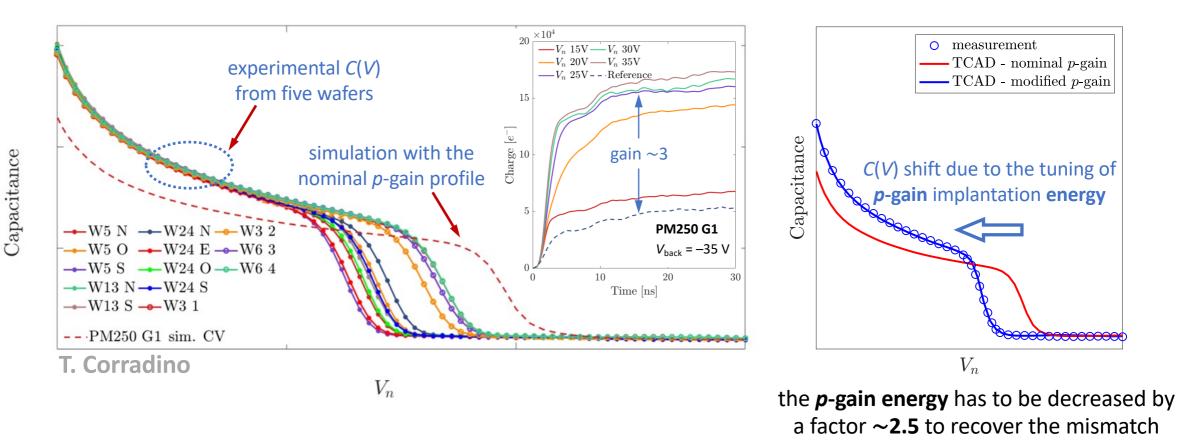


Dynamic characterization – standalone passive test-structures



Backside illumination with a **focused IR laser** spot (\sim 10 µm)

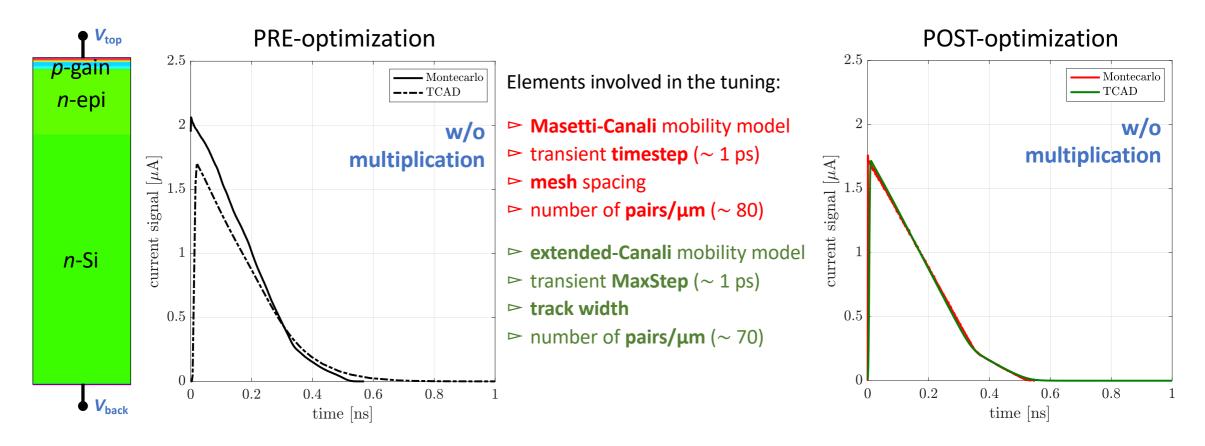
Investigations about the gain (target: 10 – 30)





Optimization of numerical tools

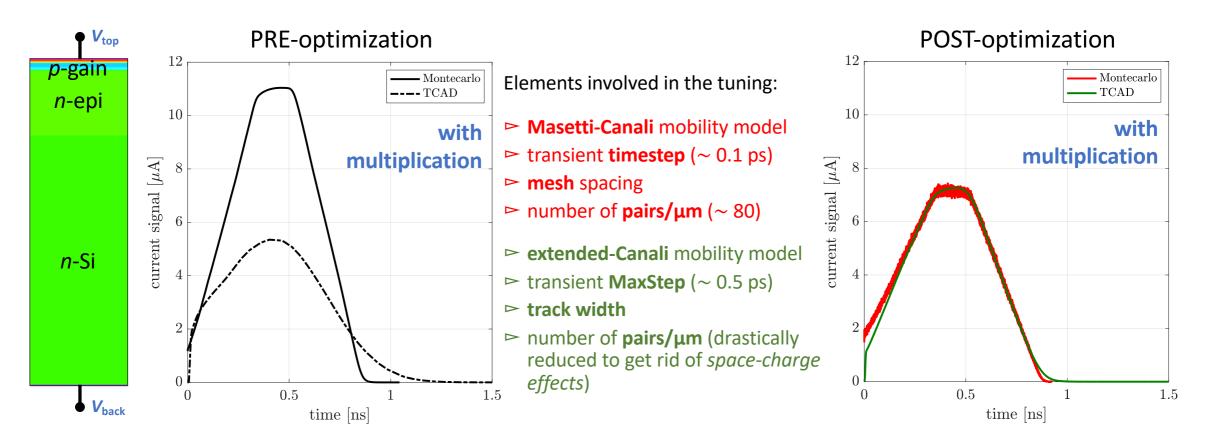
Signal simulations w/ and w/o default models (and parameters) for TCAD and Montecarlo



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Optimization of numerical tools

Signal simulations w/ and w/o default models (and parameters) for TCAD and Montecarlo



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- ▷ we accumulated a lot of experience in the past years in designing and characterizing monolithic CMOS sensors for particle detection produced with the standard (commercial) technological 110-nm-node
- the first two runs demonstrated the robustness of our designing tools (both for electronics and sensor part), the effectiveness of the LFoundry-INFN collaboration and the maturity level of the sensor concept
- with the last production we investigated and proved the compatibility of the LGAD technology with the CMOS process
- ▷ we found the reason behind the low gain we observed in run-3 and we are ready to launch a new short-loop engineering run with a reasonable splitting of *p*-gain implant doses in order to cope with the process uncertainties and achieve the target of having CMOS sensors with an internal gain between 10 and 30

Thanks for your attention!

