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BONN DMAPS DEVELOPMENTS

FABIAN HÜGGING ON BEHALF OF THE BONN CMOS TEAM

LATEST MONOPIX PROTOTYPES

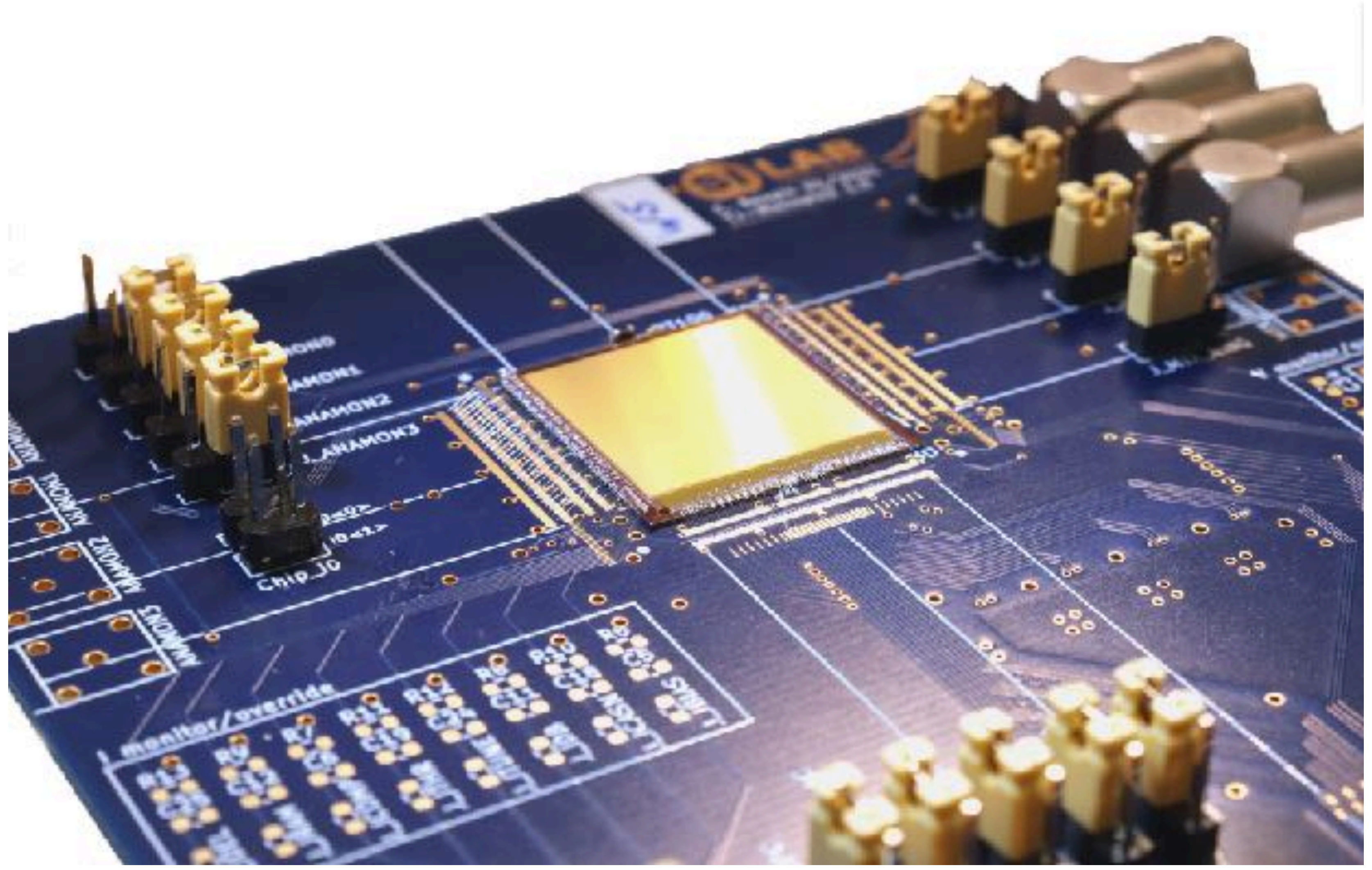
TJ-Monopix2:

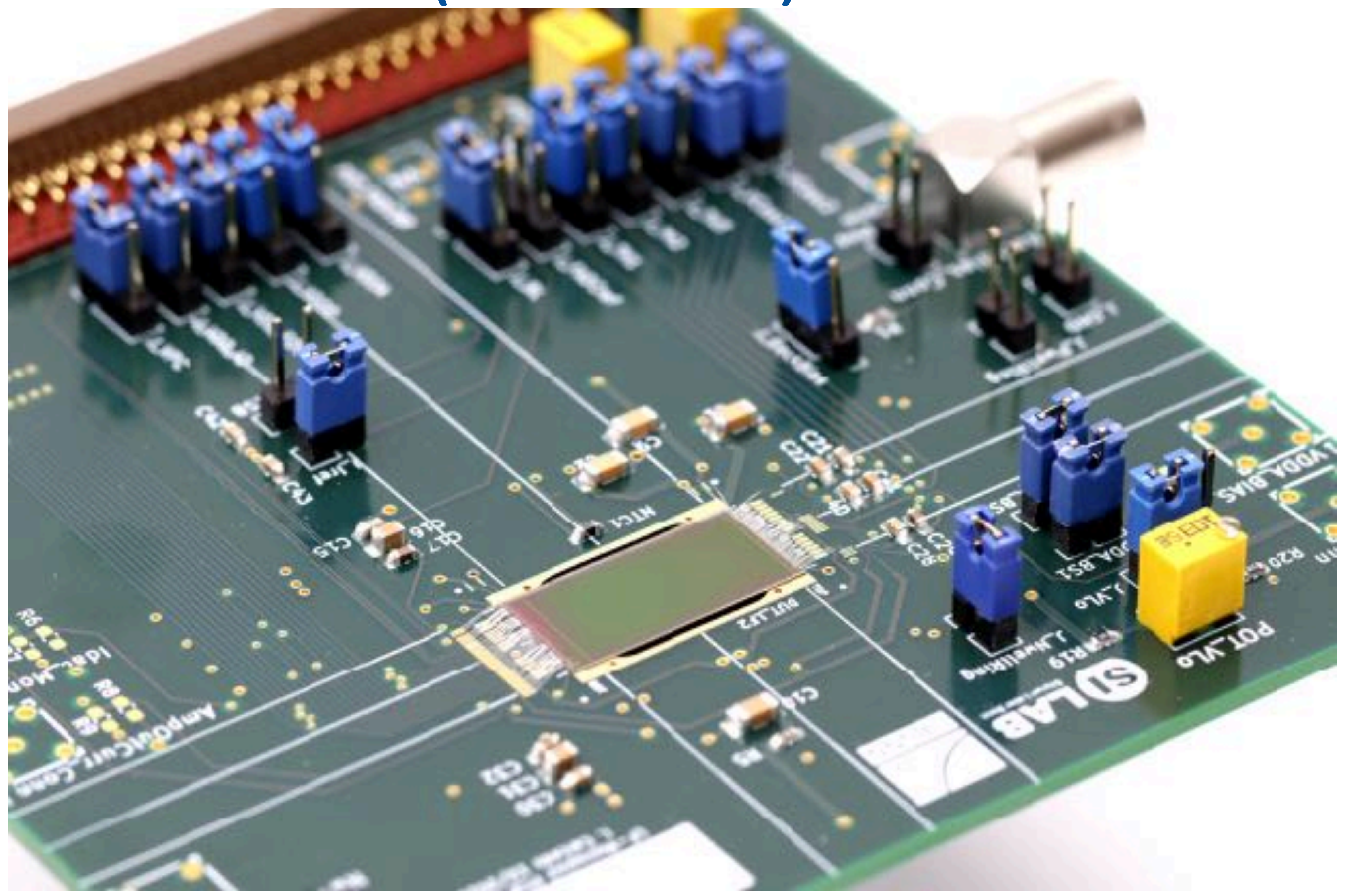
- 180 nm TowerSemi CMOS technology
- Small collection electrode
- 2x2 cm² matrix with **33x33 µm²** pixel pitch
- Substrate resistivity >1 kΩcm

LF-Monopix2:

- 150 nm LFoundry CMOS technology
- Large collection electrode
- 2x1 cm² matrix with **50x150 µm²** pixel pitch
- Substrate resistivity > 2 kΩcm

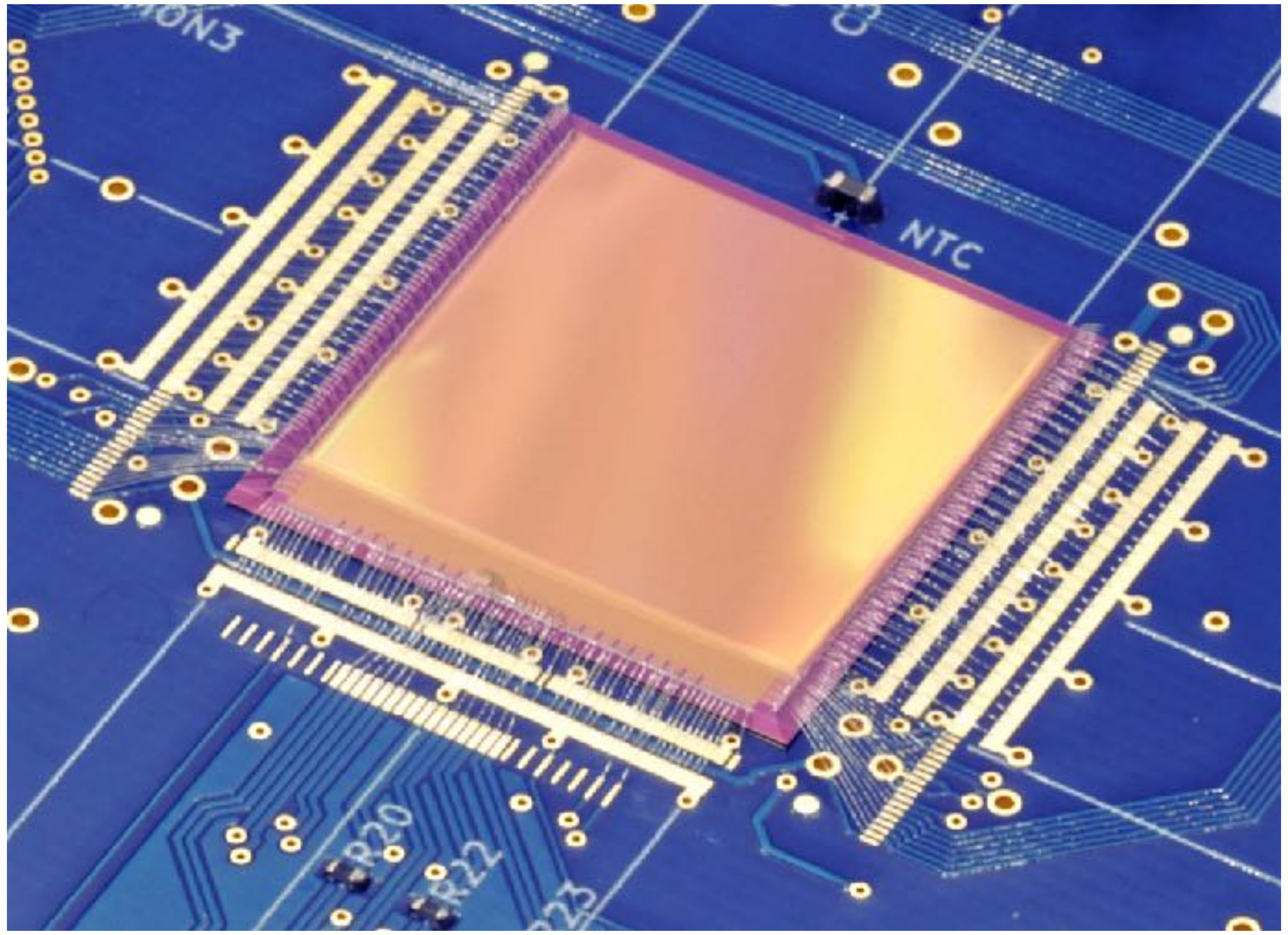
Same fast **column drain readout** architecture (FE-I3 like)





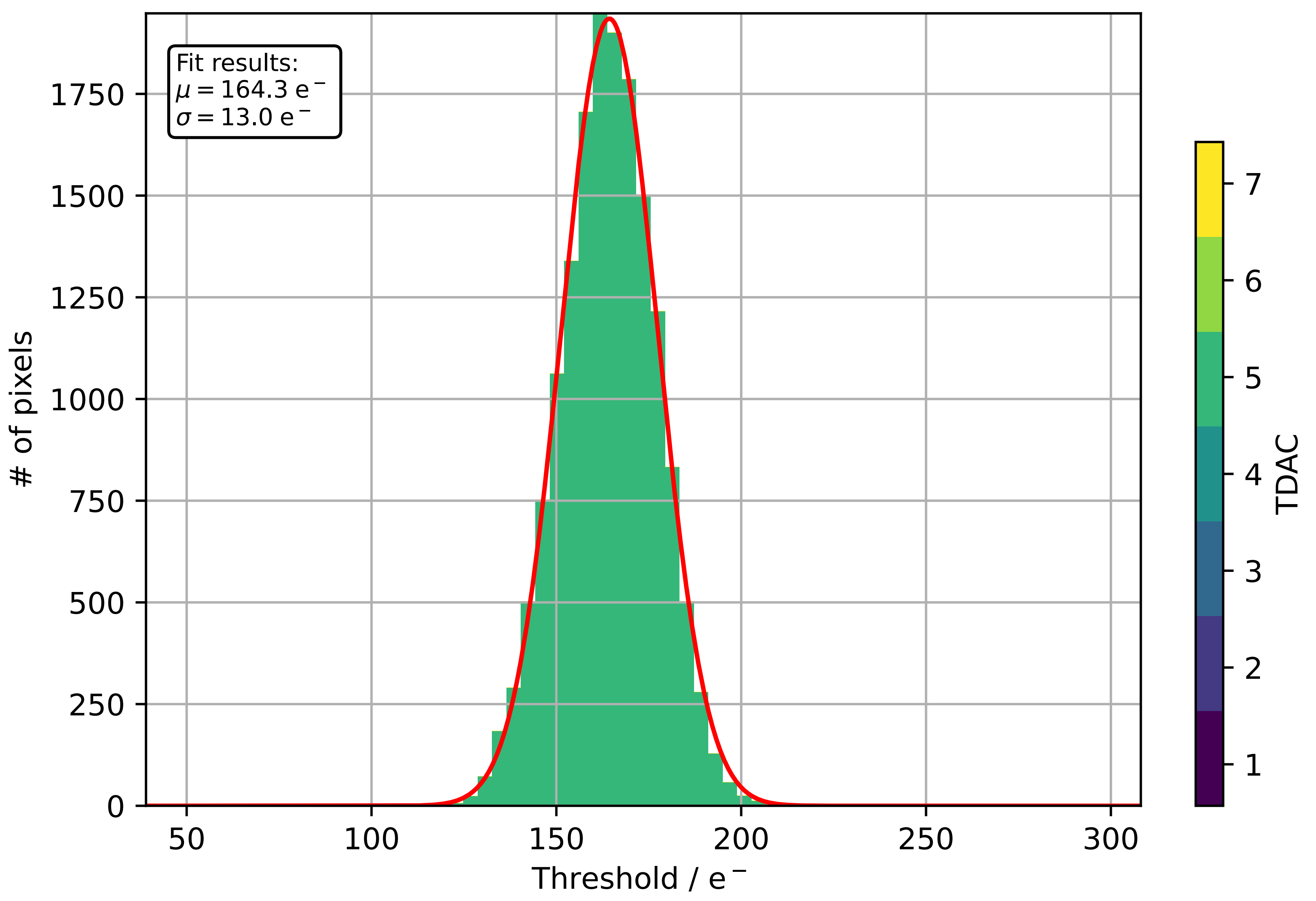
TJ-MONOPIX DESIGN

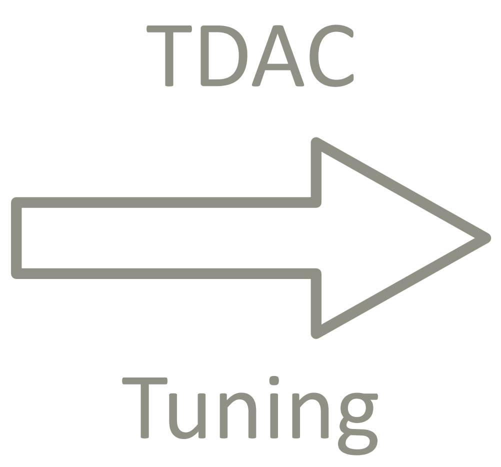
- Latest iteration TJ-Monopix2: 33.04 µm pixel pitch in 512 x 512 pixel matrix (2 x 2 cm^2)
- 7 bit TOT resolution (40 MHz BCID clock - 25 ns timing)
- 3 bit in-pixel threshold tuning
- Communication via four differential lines
  - Command-based slow control (taken from RD53B)
  - 160 MHz data output rate (frame-based 8b10b encoding)
- bdaq53 readout board (from RD53A/B testing)

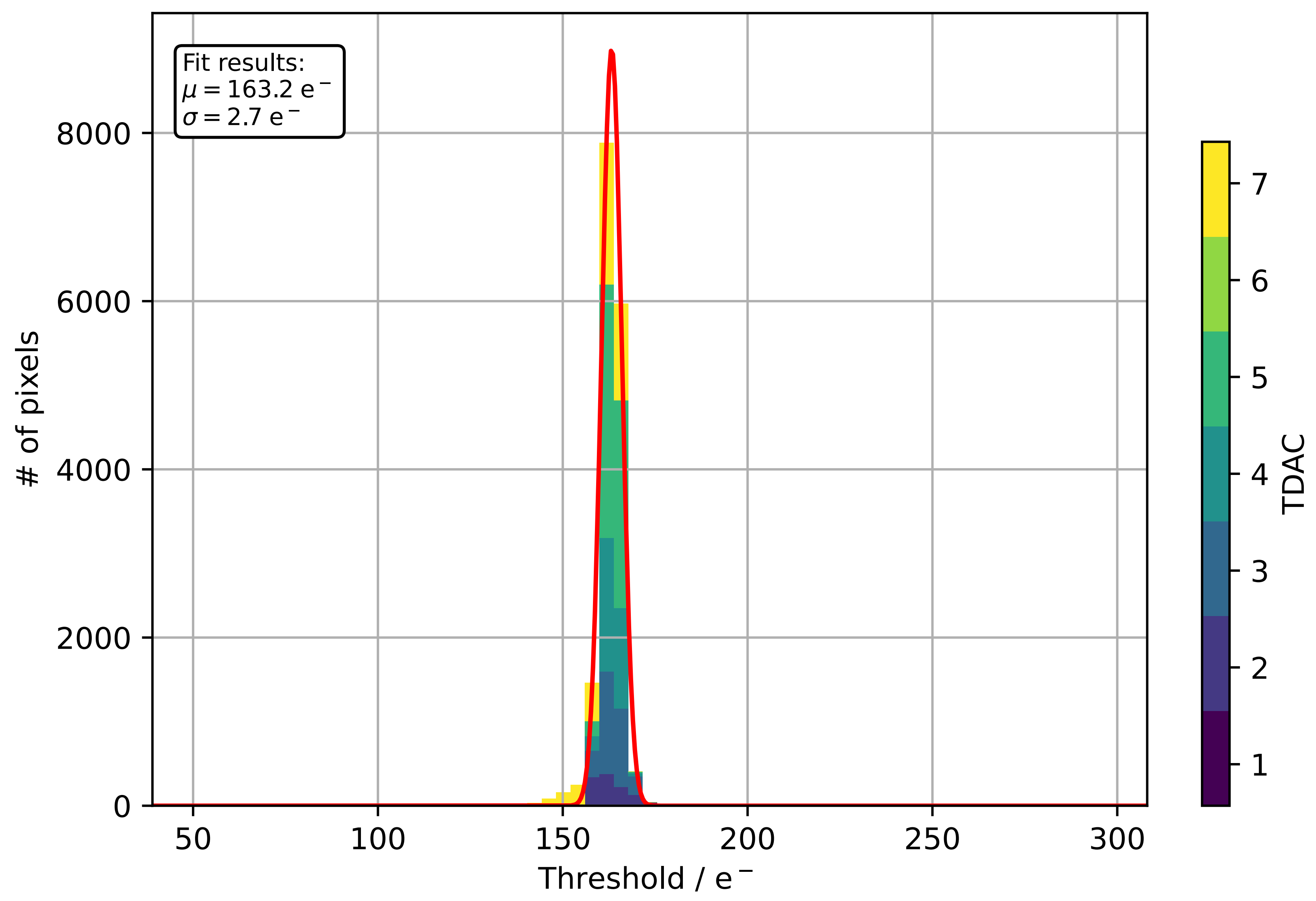


TJ-MONOPIX2 LAB TESTS

- Lab tests conducted for threshold and noise measurements
- Design goals: operational threshold ≈ 100 e^-, threshold dispersion < 10 e^-, ENC ≈ 5 e^-
- In-pixel threshold trimming (3 bit) significantly reduces threshold dispersion to less than design value
- Operational threshold higher than anticipated, but we will see later that it should not be a problem



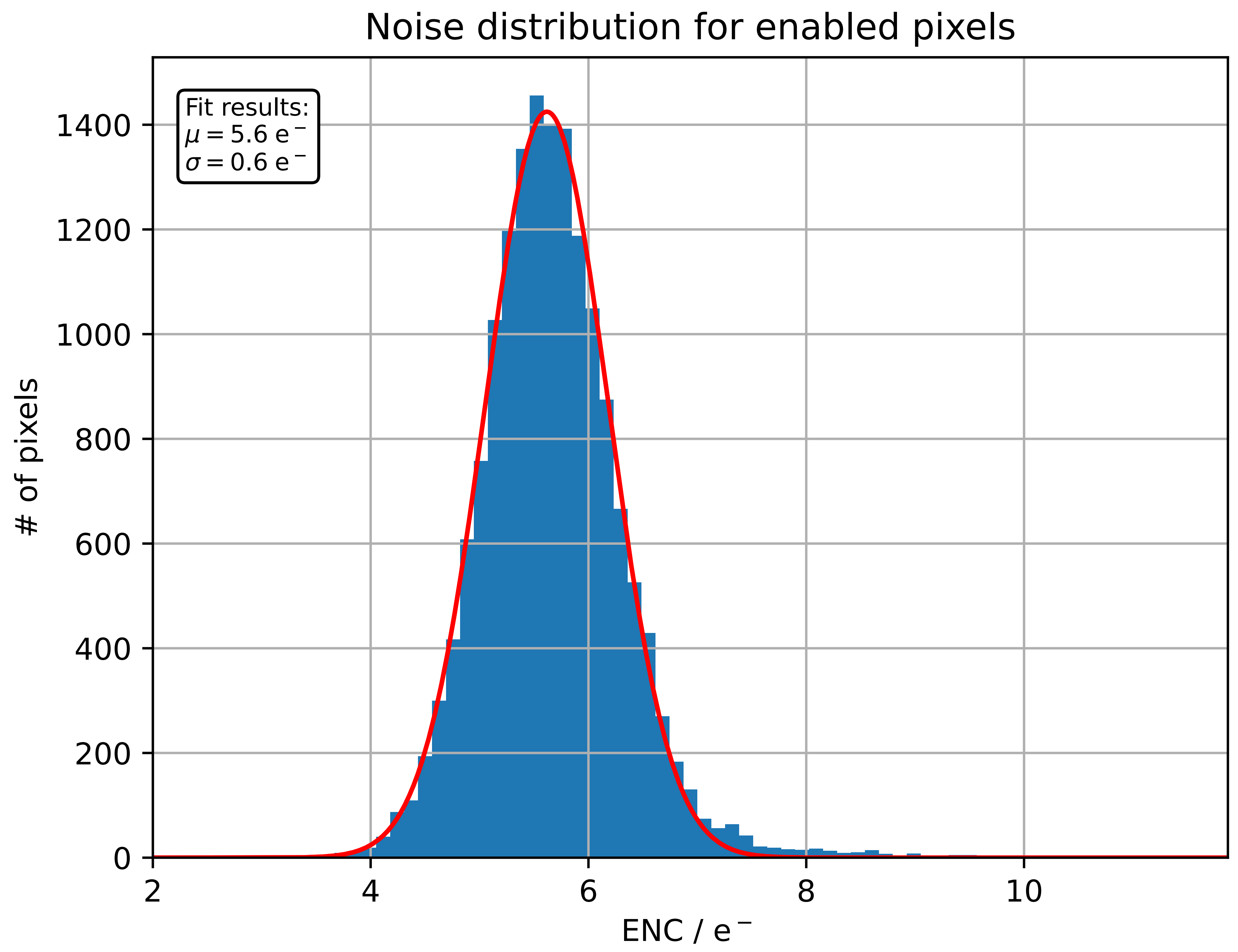




TJ-MONOPIX2 LAB TESTS

- Noise (ENC) measured from steepness of S-curve when injecting varying charges
- Mean noise 5.6 e^- in accordance with design goal
- No RTS noise tail observed as in TJ-Monopix1
- Allows operation at low thresholds thanks to large S/N ratio

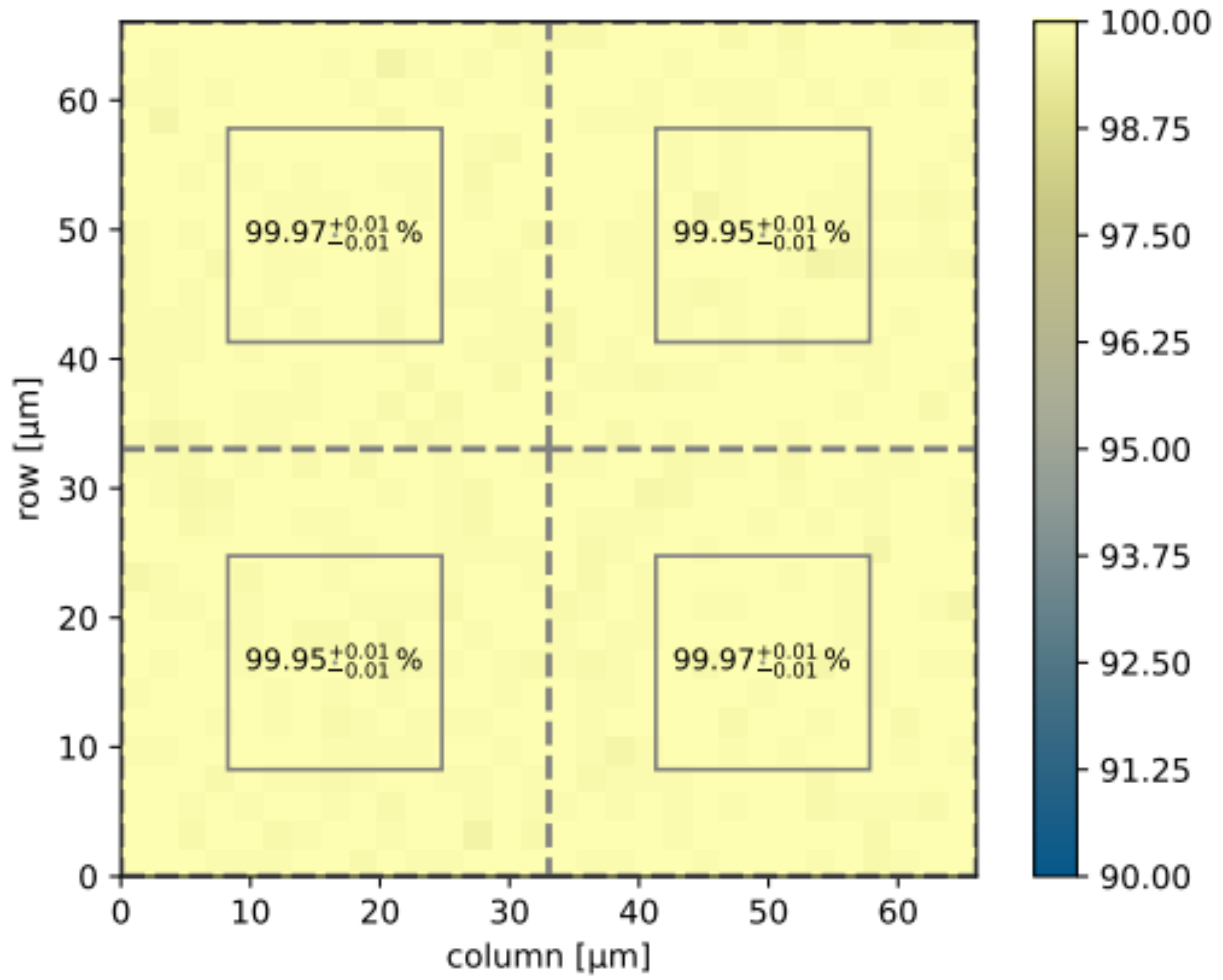
- Reminder: in TJ-Monopix1, operational threshold was O(400 e^-) which lead to efficiency losses in pixel corners, especially after irradiation



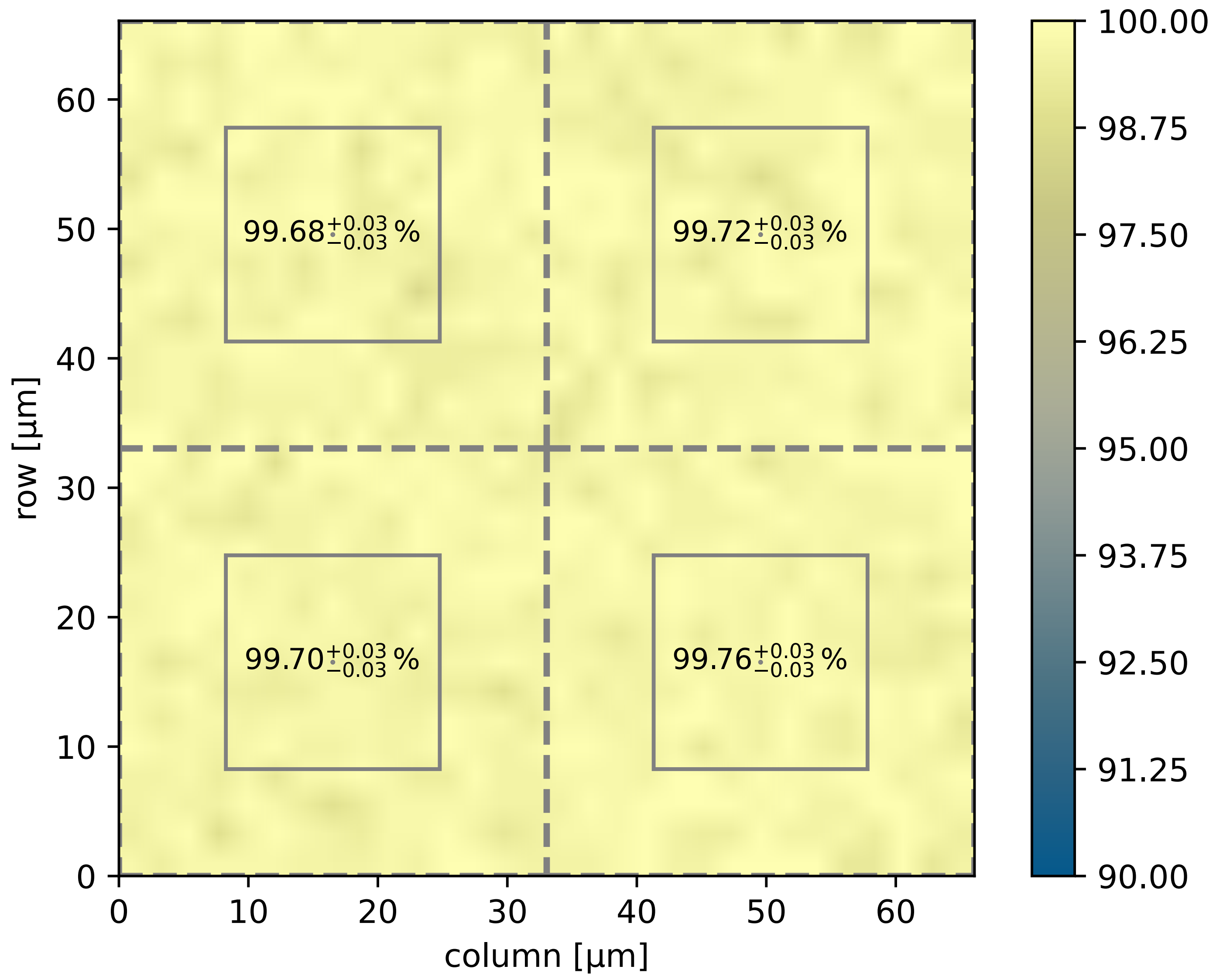
TJ-MONOPIX2 EFFICIENCY

- In-pixel efficiency for standard pixel flavor
- Homogeneous efficiency > 99 % with no losses in the corners, higher than TJ-Monopix1 already
- With ~200 e^- threshold no difference between samples expected for the observed cluster charge, deviation within error (estimated around 0.1 %)

Epi gap in n-layer (30 µm): 99.96 %



Cz gap in n-layer (100 µm): 99.72 %

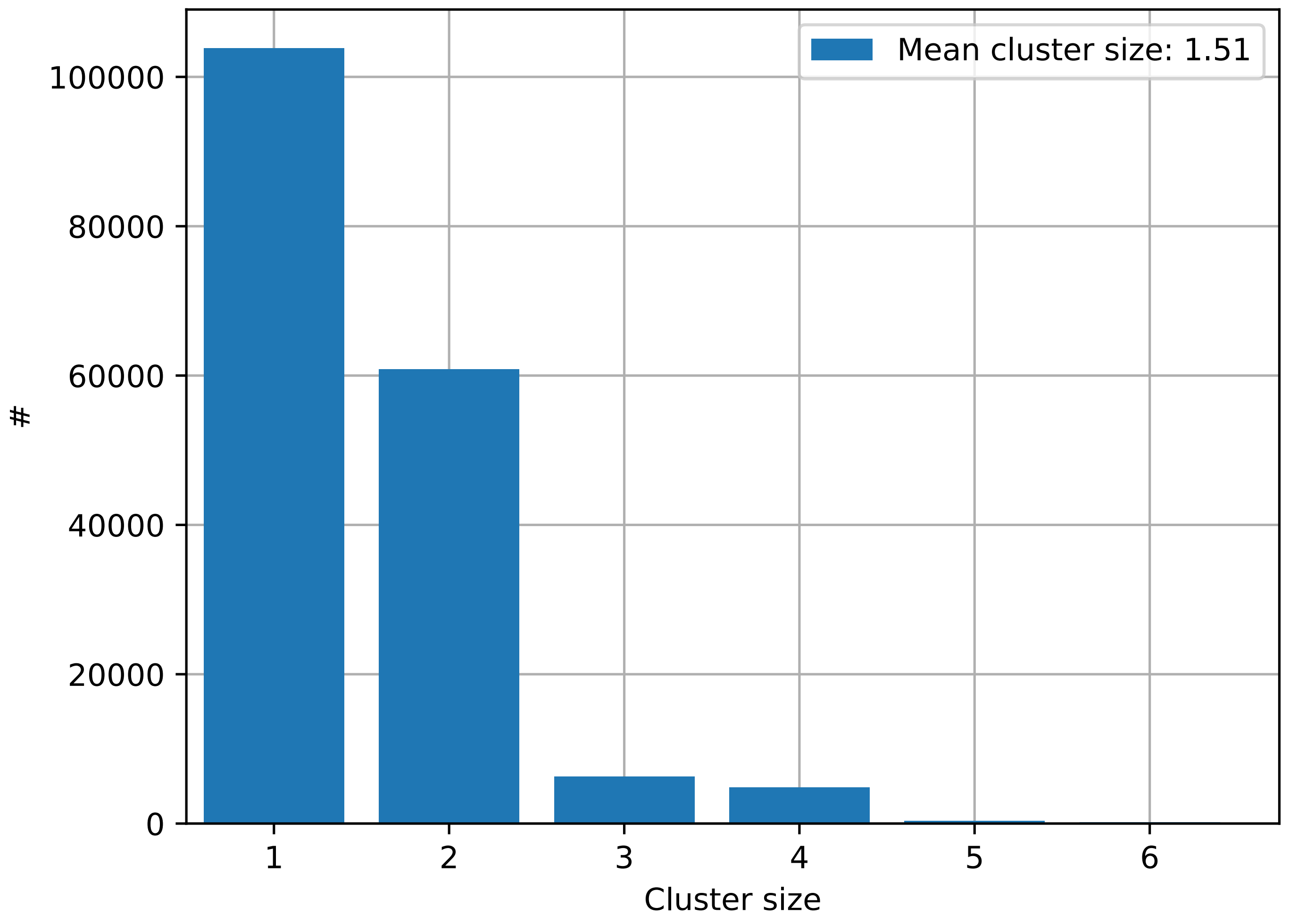


TJ-MONOPIX2 CLUSTER CHARGE

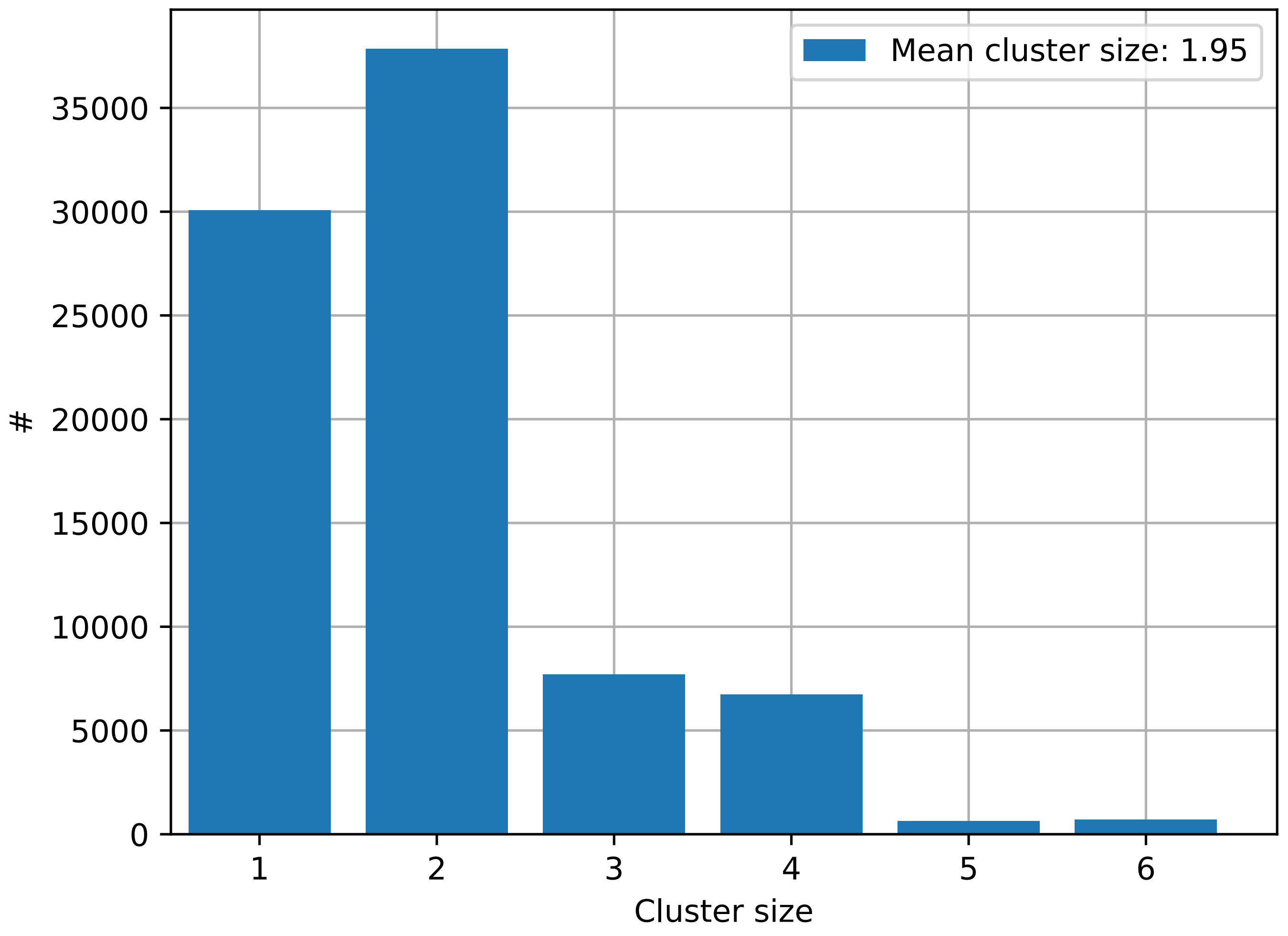
- Compare different sensor materials (epi 30 µm / Cz 100 µm) regarding cluster size
- As expected from accumulated charge and higher depletion than 30 µm cluster size is significantly larger in 100 µm silicon (not fully depleted)

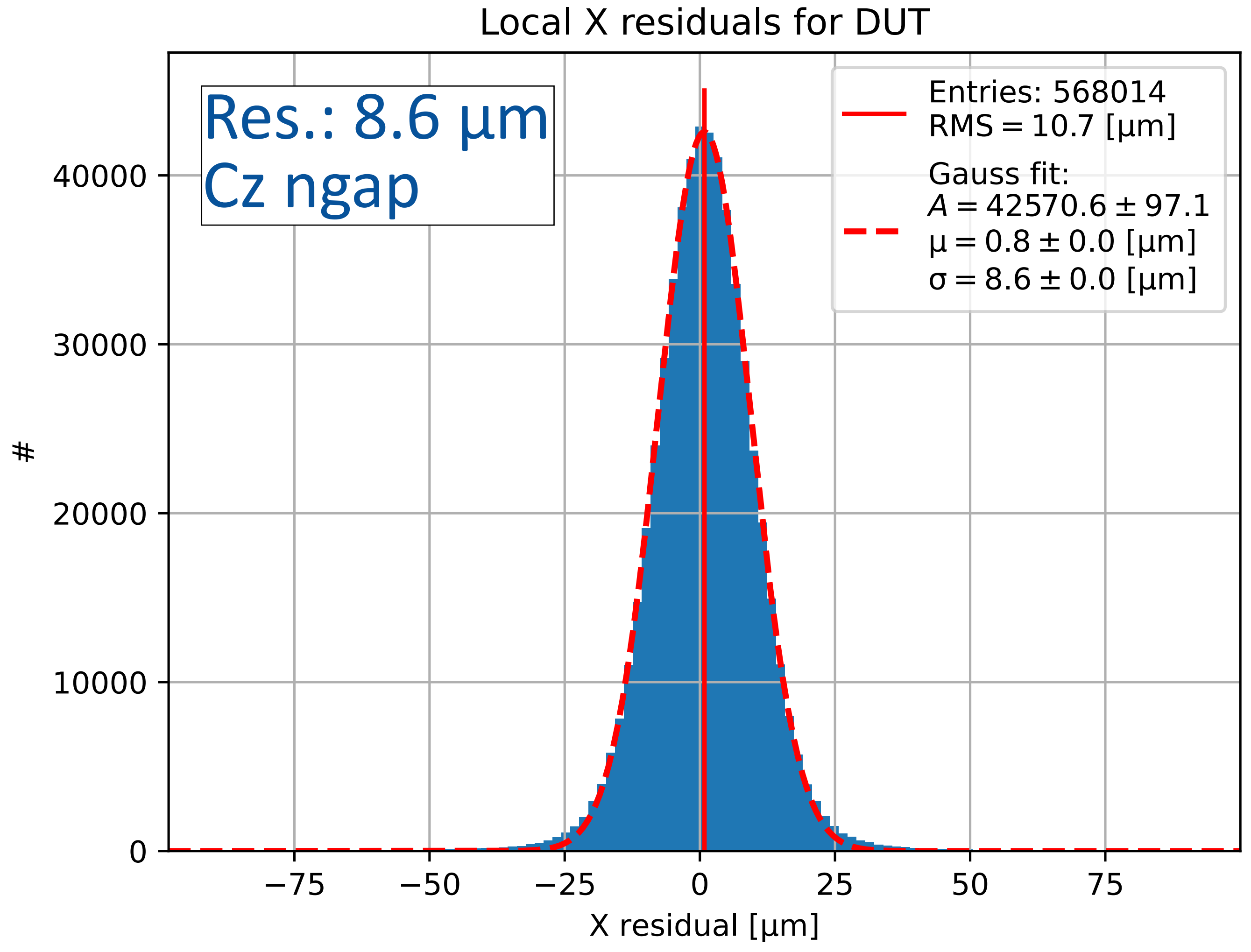
- High (average) cluster size allows for high spatial resolution; better than $\frac{d}{\sqrt{12}}$ in Cz chip

Epi gap in n-layer: 1.51



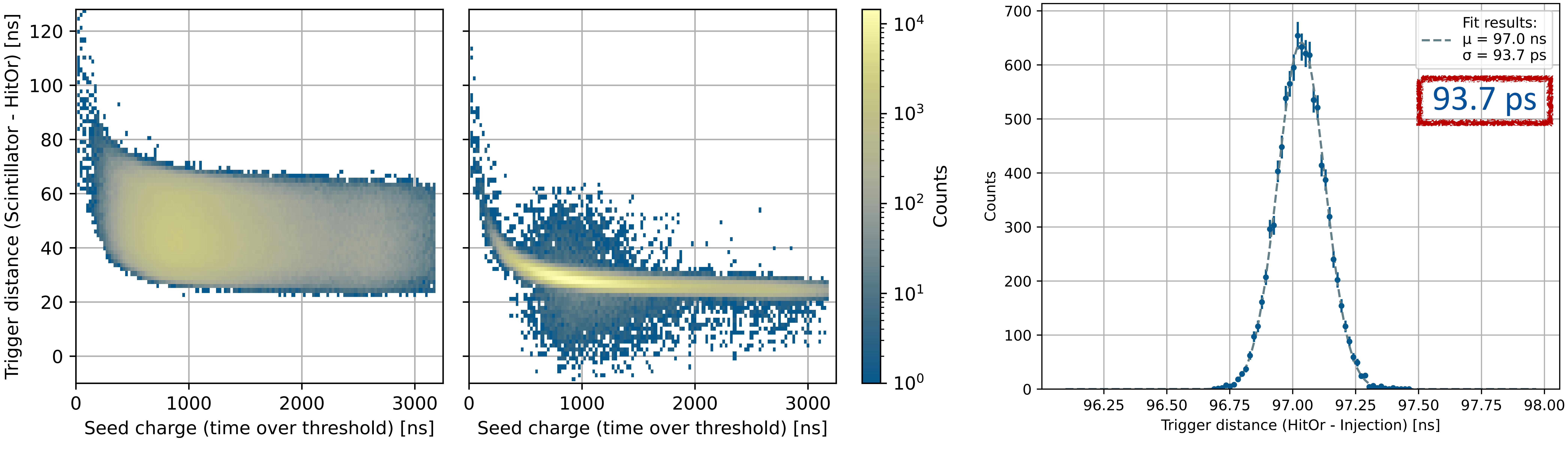
Cz gap in n-layer: 1.95





TIMING IN BEAM

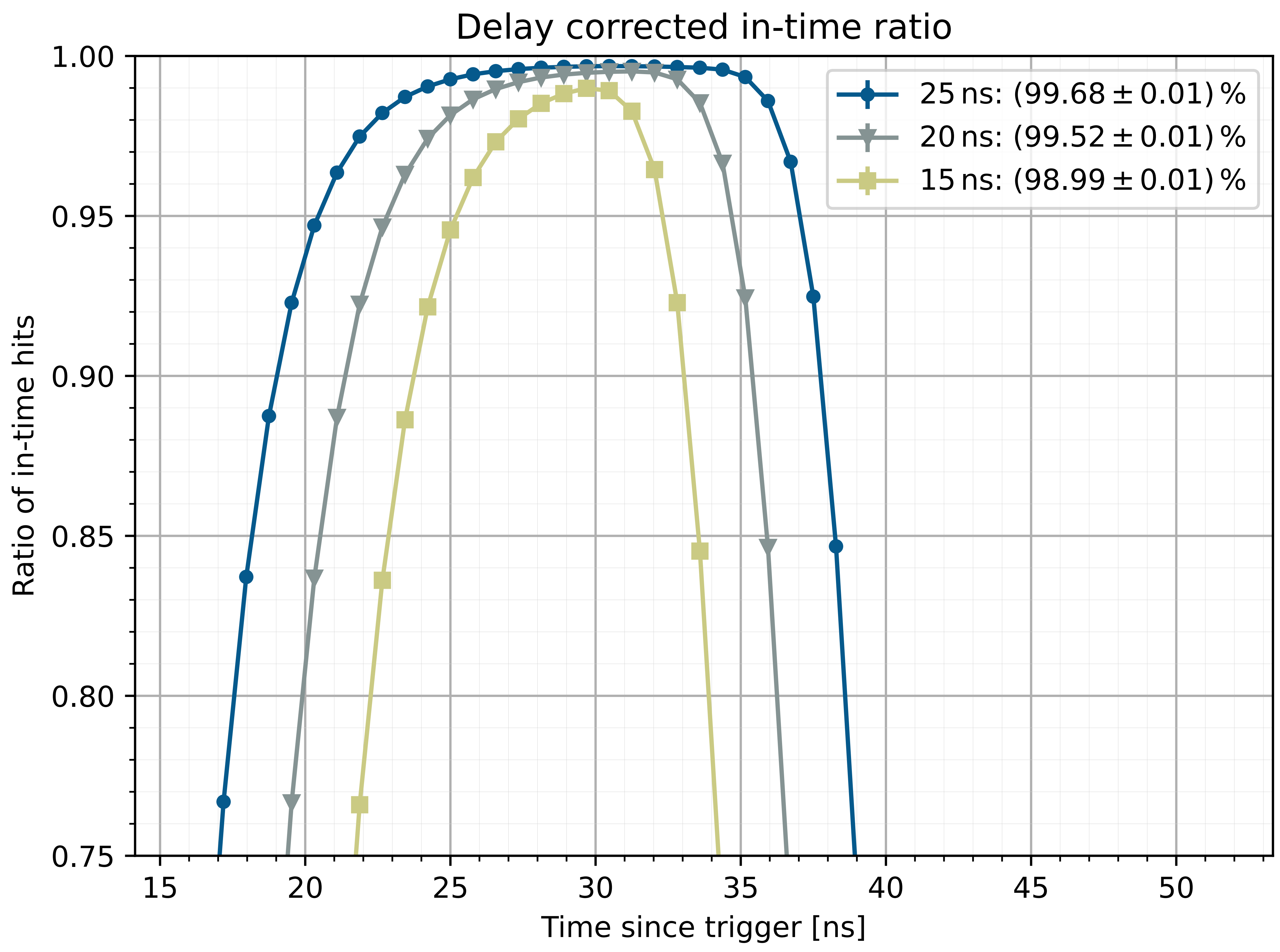
- Beam tests performed at DESY (10/2023)
- Measure time between scintillator hit and HITOR word from in-pixel discriminator
- Delay gradient along column due to signal propagation –> correct by column-wise line fit
- Trigger delay of cluster vs. seed charge (outliers due to mismatch of delay to proper hit)



Time resolution of front-end (measured with analog injection)

TIMING STUDIES

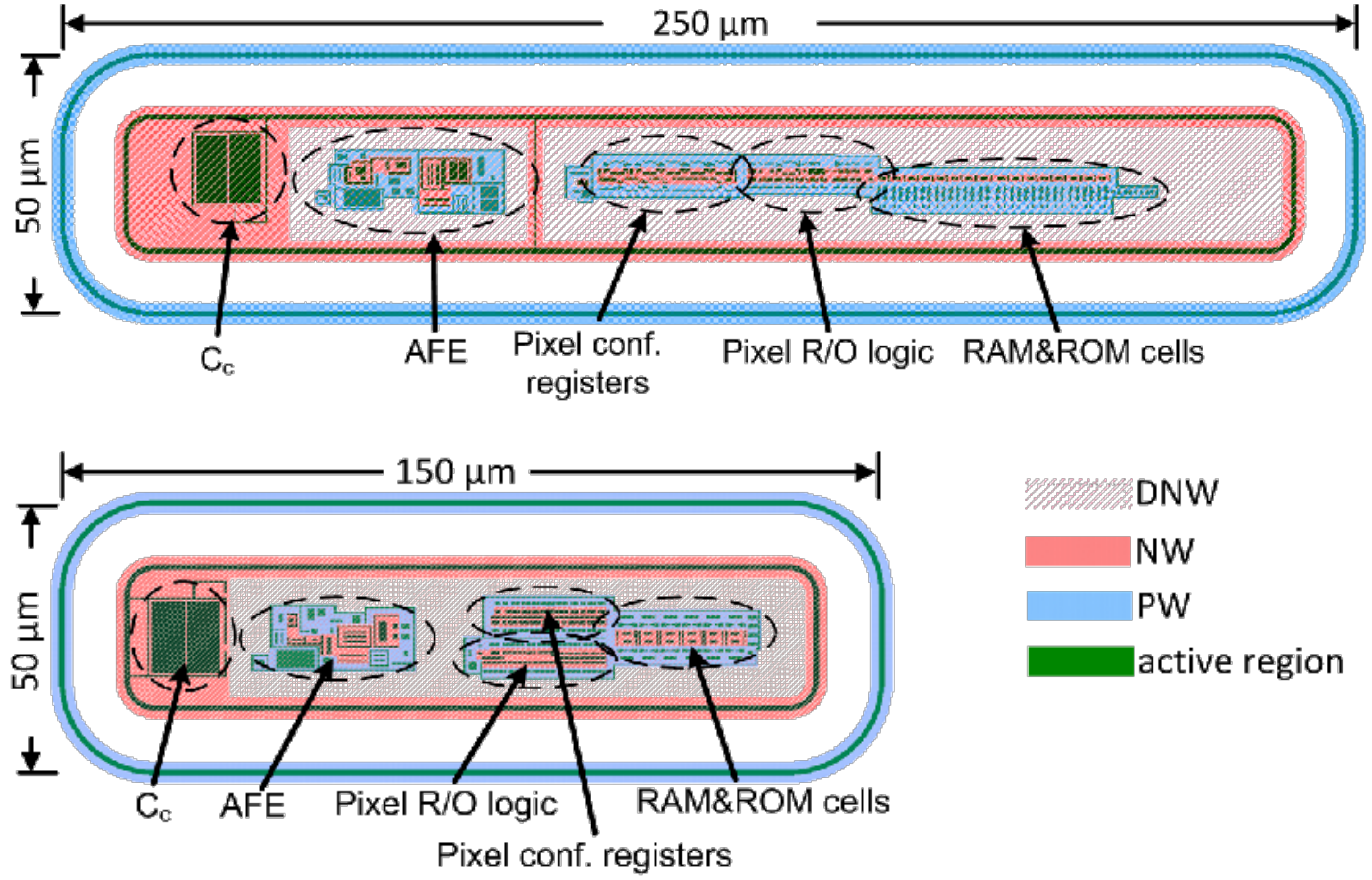
- Measure delay between scintillator and HitOr signal with 640 MHz clock
- Estimate in-time ratio of hits in given time window of trigger distance distribution
- For 30 µm epi chip with **n-gap** modification and **standard front-end**:
  - 99.68 % within 25 ns (ATLAS BX frequency)
  - > 99 % for 20 ns and 15 ns
- Estimate 99.64 % in-time efficiency based on in-time ratio and hit detection efficiency (analysis ongoing)



LF-MONOPIX2 SPECIFICATIONS

- Full scale column length with column-drain R/O
  - **Full in-pixel electronics** while **reducing the pixel pitch by 40%** of predecessor
- **6 bit ToT** information @ 25 ns
- **4 bit in-pixel threshold tuning**
- 6 front-end variations available
  - Differing in CSA, feedback capacitance, tuning
- Successfully thinned down to **100 µm thickness and backside processed**
- Proton irradiated sensors up to 2e15 neq/cm² NIEL damage available
  - Powered off during irradiation, annealed 80min @ 60°C

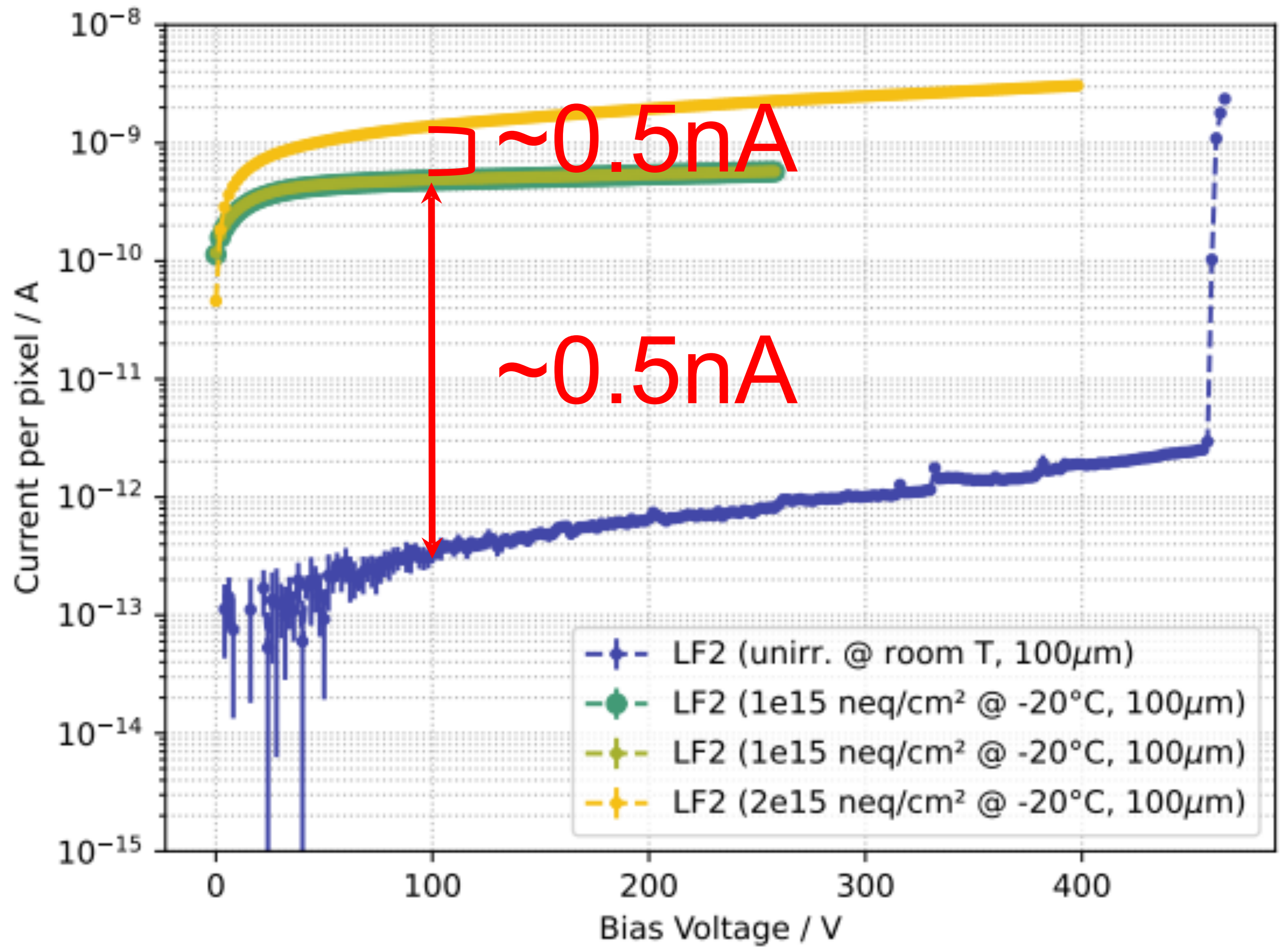
LF-Monopix1 (Mar 2017)

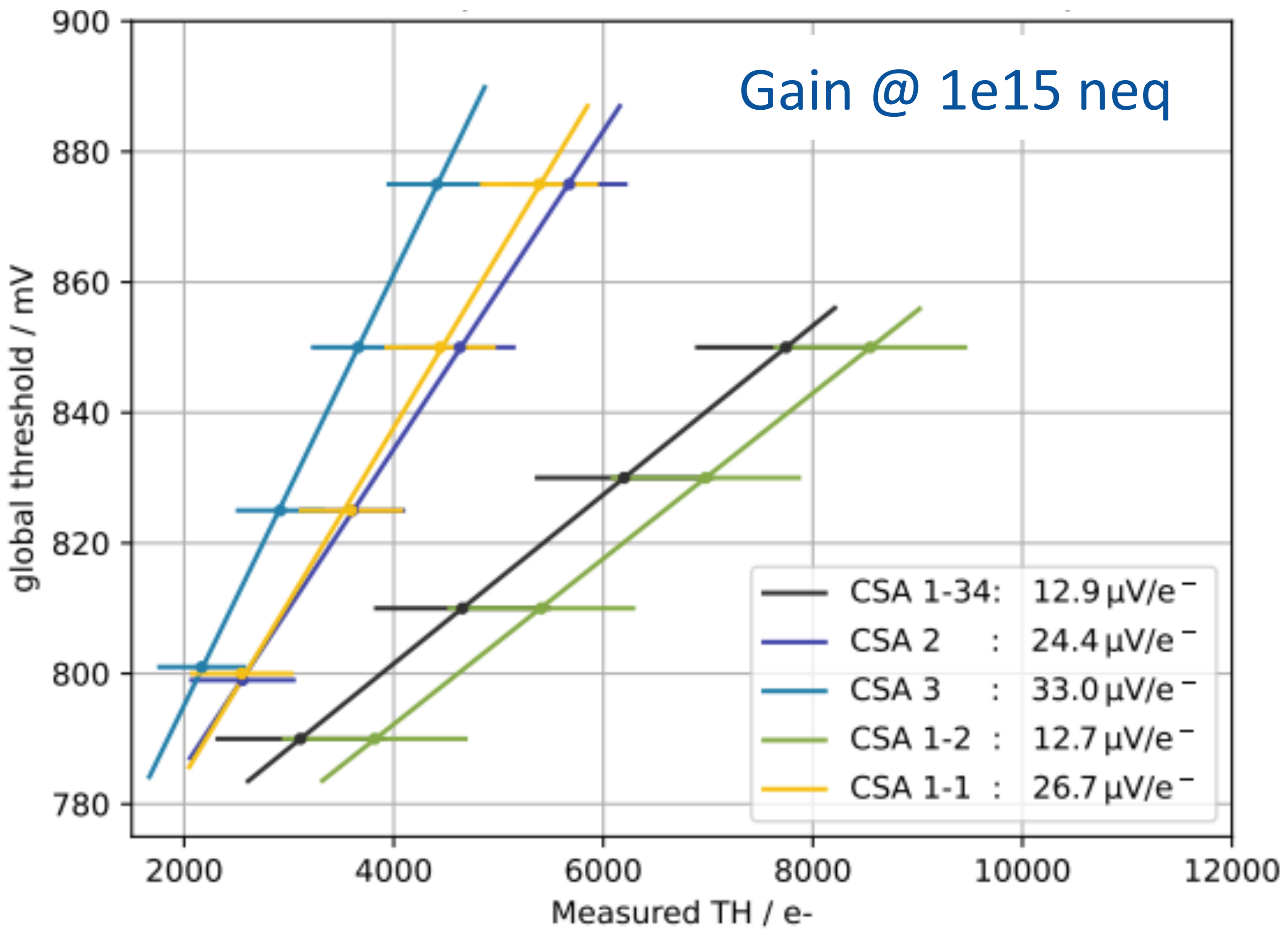


LF-Monopix2 (Feb 2021)

LEAKAGE CURRENT AND GAIN

- Measure **leakage current per pixel** at -20 °C environmental temperature
  - Breakdown at approx. 460 V for unirradiated modules
- **Increase** in leakage current **per pixel 0.5 nA** per 1e15 neq/cm² irradiation step
- Extract **gain** from linear regression of untuned threshold at different global THR settings
  - Smaller feedback capacitance → larger gain (and faster rise time of LE)

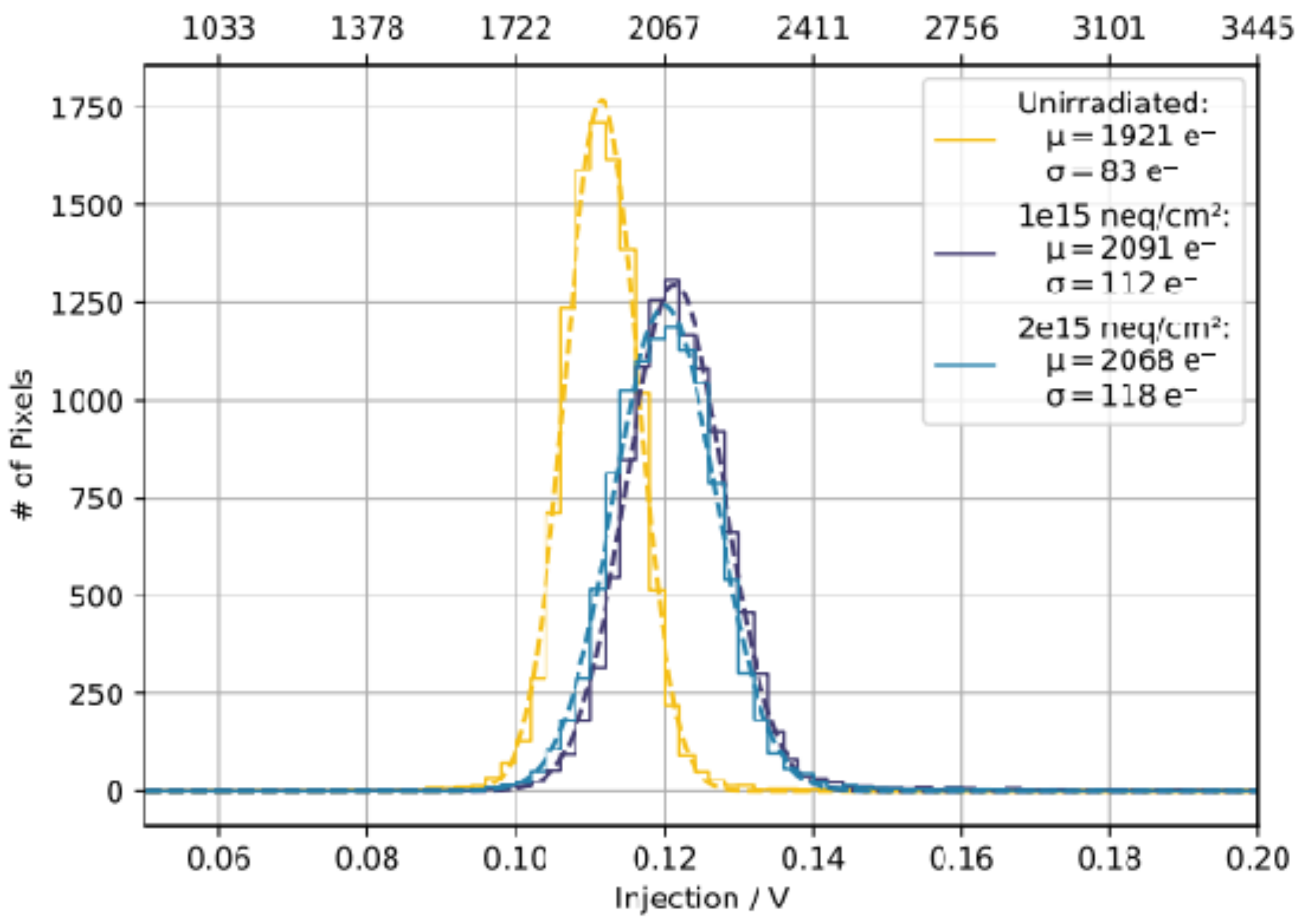




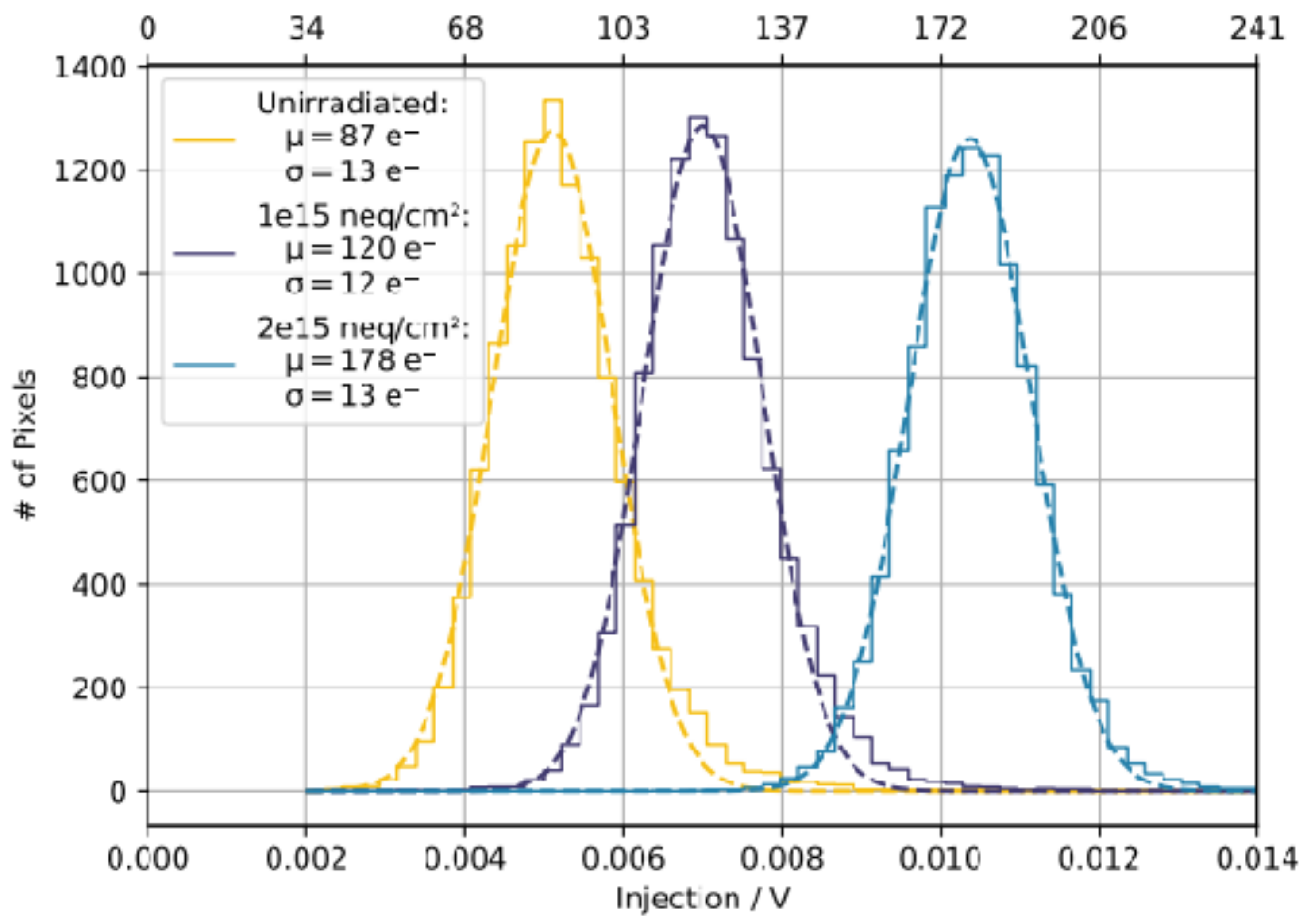
LABORATORY TESTS

- Controlled laboratory environment at -20°C
- Homogeneous threshold across matrix at approx. **2 ke⁻ threshold before and after irradiation**
  - About 40% increase in ENC after each 1e15 neq/cm² fluence step
  - Expected charge MPV of MIP at full depletion 6 ke⁻

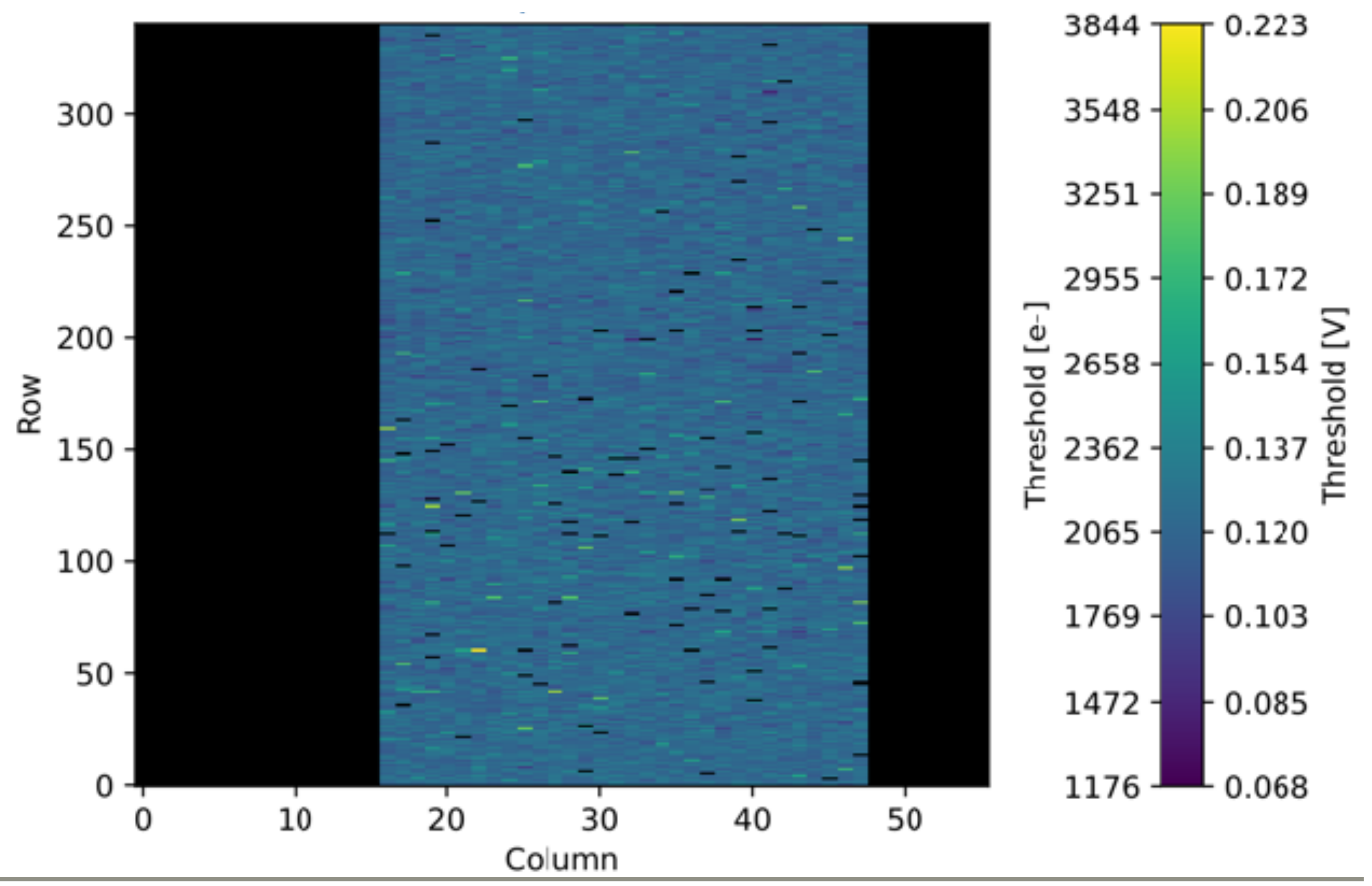
Threshold distribution



ENC distribution



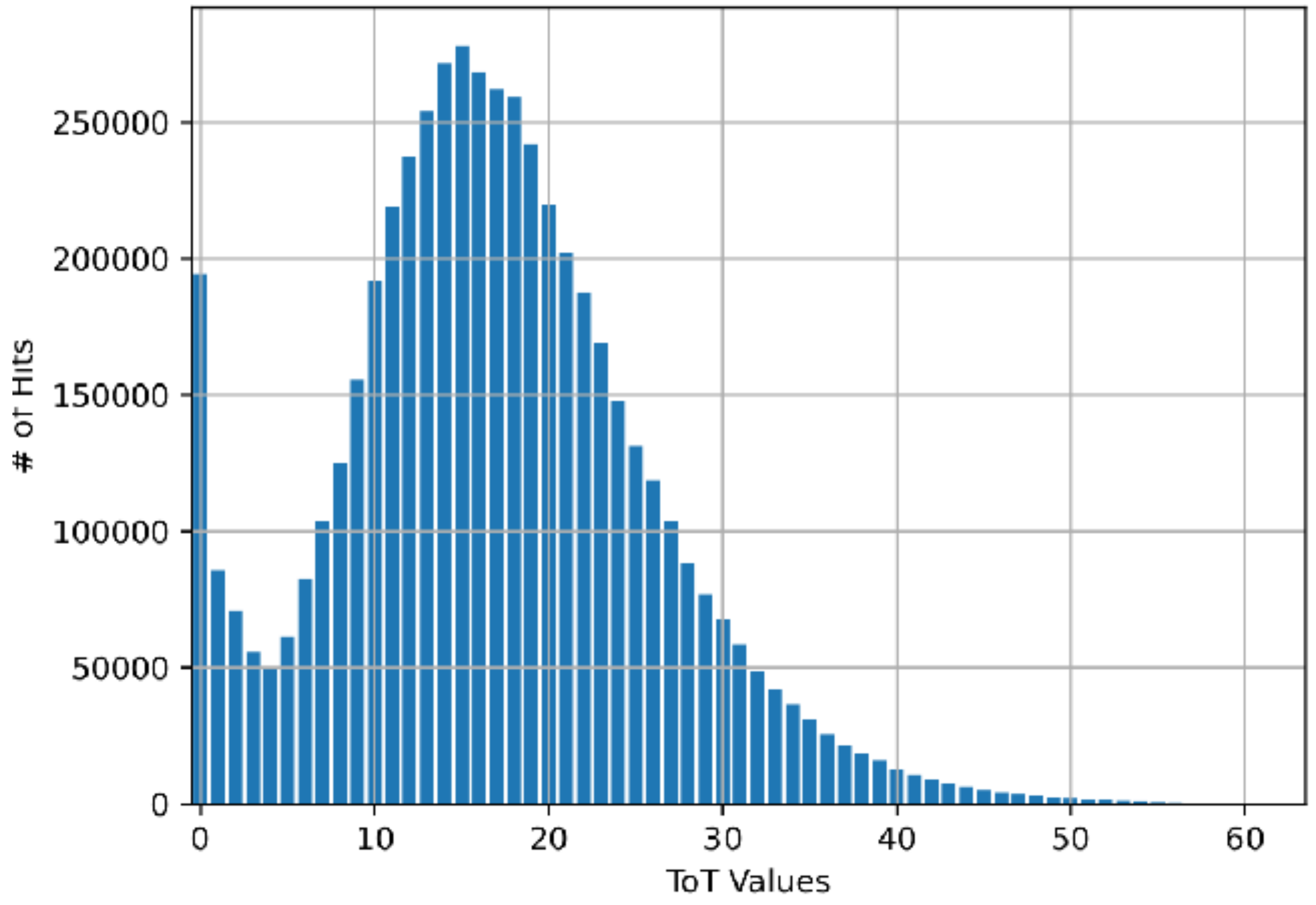
Threshold map



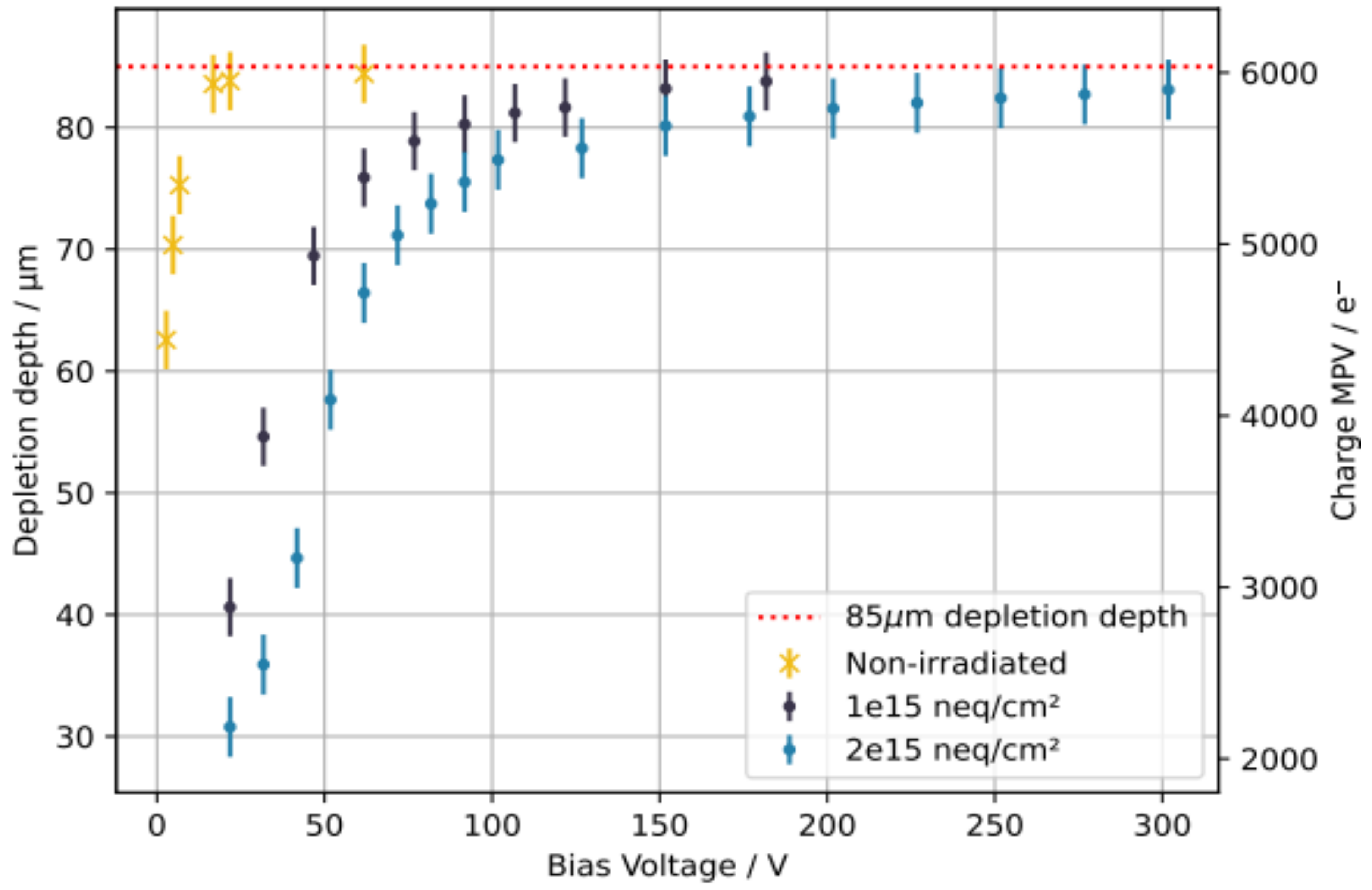
DEPLETION DEPTH OF LF-MONOPIX2

- Get calibrated charge MPV from Landau shaped beam spectrum (**5 GeV electrons at DESY**)
- Necessary voltage for full depletion increases from 15 V before to >100 V after irradiation to 1e15 neq/cm²
  - Large biasing capability enables full depletion even after 2e15 neq/cm² of fluence

ToT beam spectrum



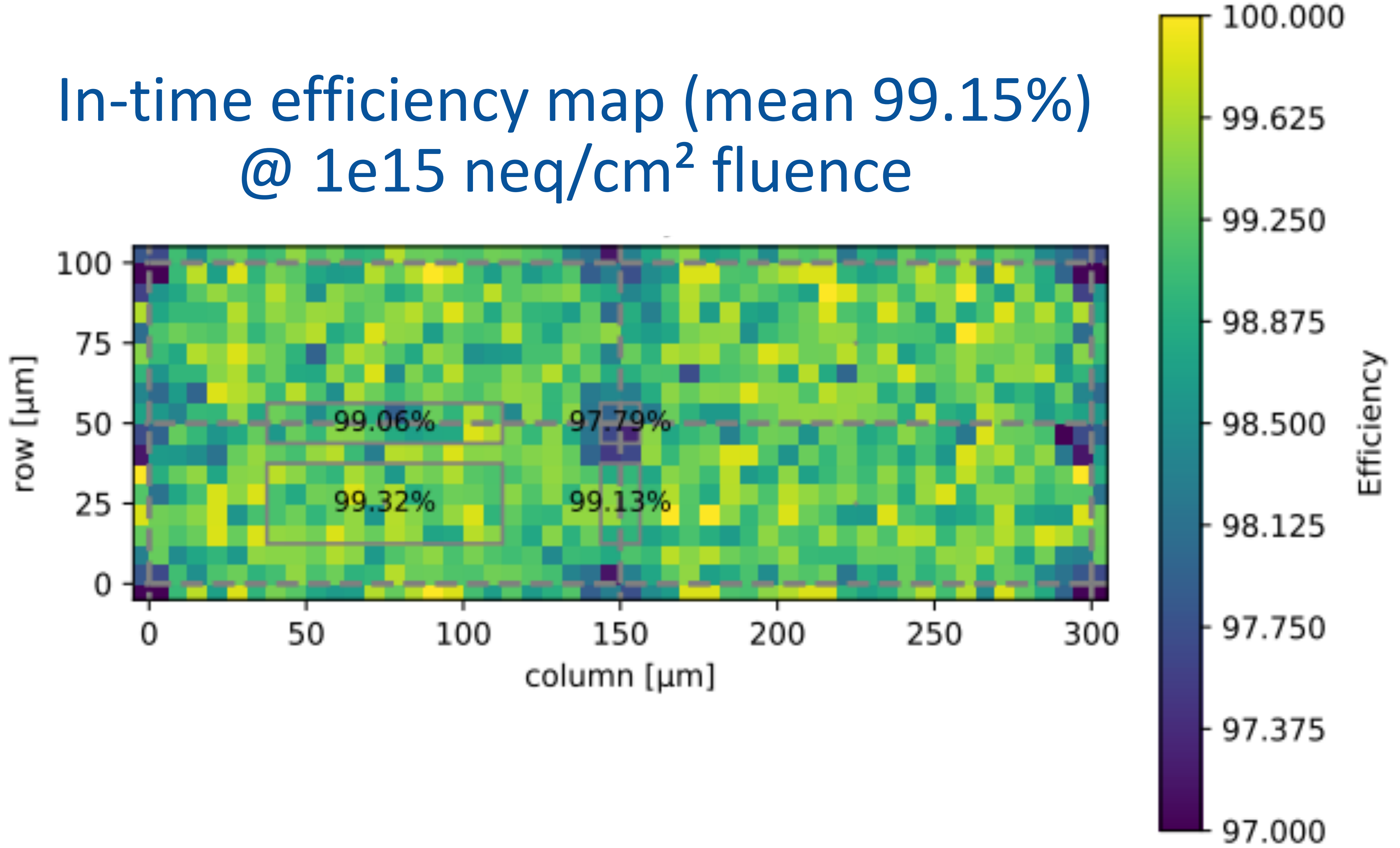
Calibrated charge MPVs



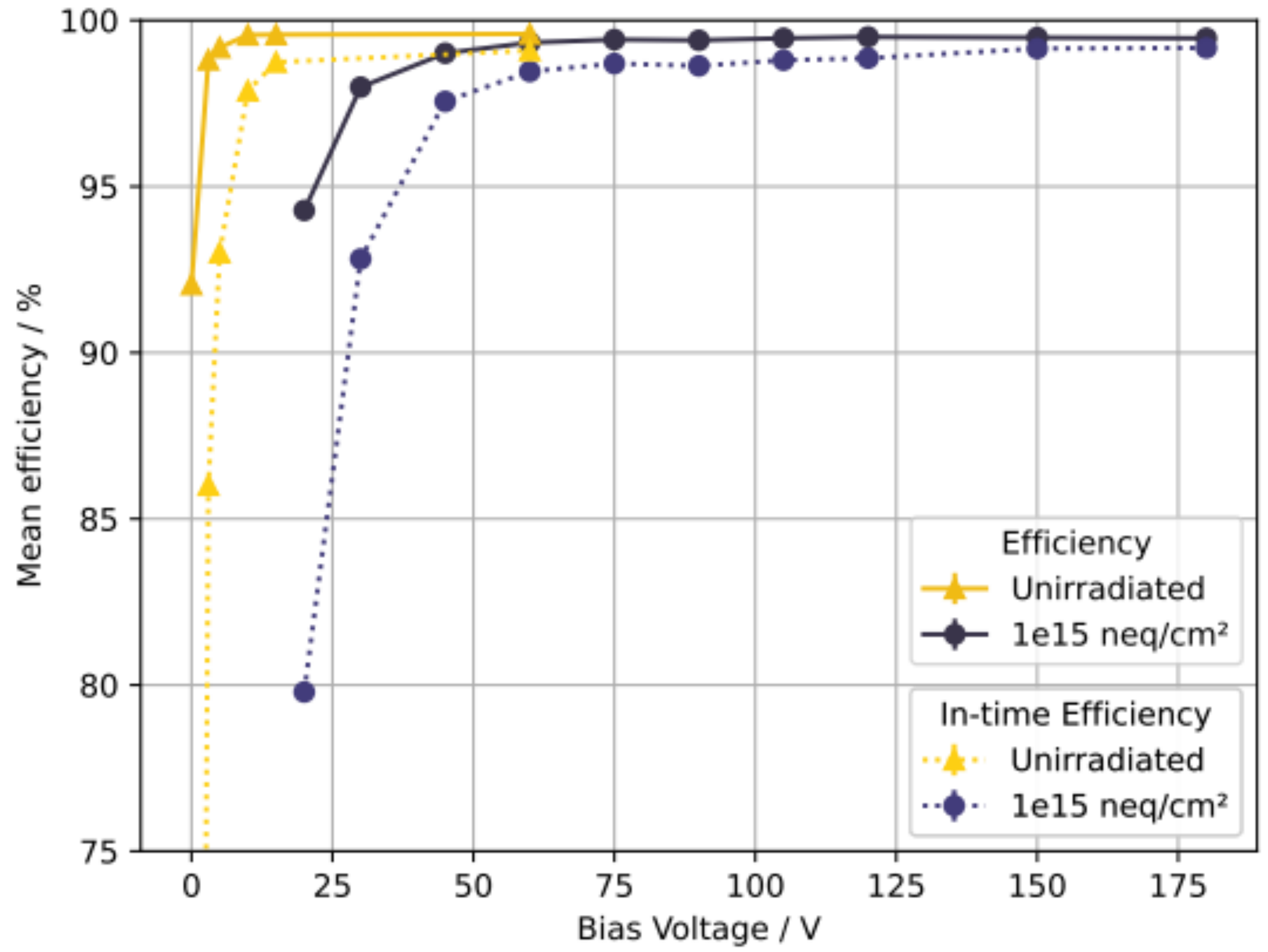
HIT DETECTION EFFICIENCY STUDIES

- Mostly **uniform in-time efficiency (25 ns) across matrix @ 1e15 neq/cm²**
  - Measured at 2 ke⁻ threshold and 150 V bias (fully depleted)
  - Slight drop to 97.79 % in pixel corners
- Verified decrease in efficiency for lower bias voltages → Less collected charge

In-time efficiency map (mean 99.15%) @ 1e15 neq/cm² fluence



Efficiency vs bias voltage

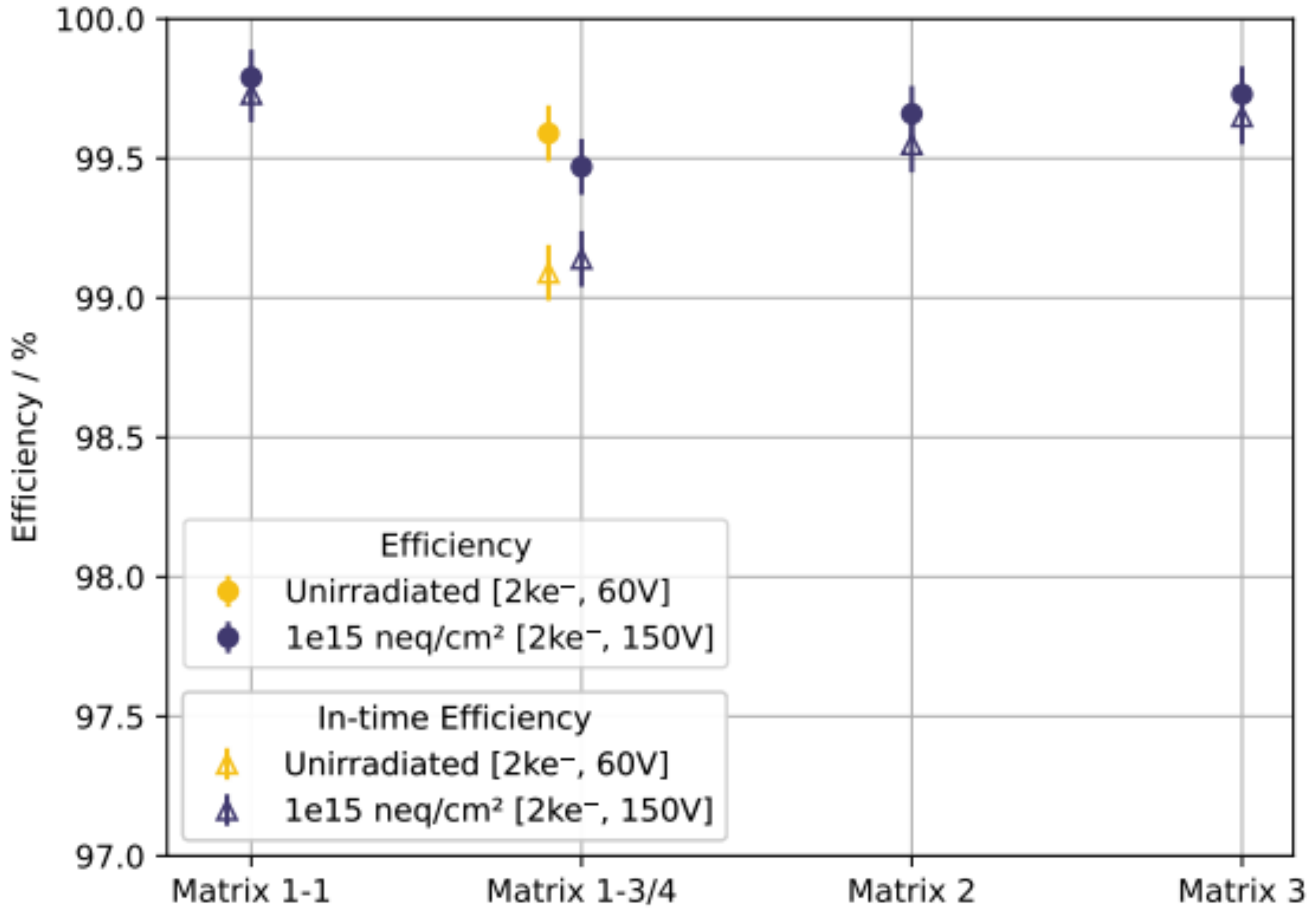


HIT DETECTION EFFICIENCY STUDIES

- **Hit detection and in-time efficiencies > 99%** for all matrices **after irradiation** to 1e15 $\mathbf{n_{eq}\ cm^{-2}}$
  - Measured at **2 ke⁻ threshold** and 150 V bias voltage (**full depletion**)
  - Increase in in-time ratio for larger gain front-end variants
- Result **before irradiation** as reference
  - Similar threshold of ~2 ke⁻
  - 60 V bias voltage (full depletion)

→ No significant efficiency loss after irradiation to 1e15 neq/cm²
Detailed analysis of results after 2e15 neq/cm² ongoing

Efficiency of front-end variants



SUMMARY / OUTLOOK

- Two fully working DMAPS with column-drain readout in 2 cm long columns
- TJ-Monopix2:
  - Hit detection efficiency > 99 % for non-irradiated chips across front-end and substrate variants
  - In-time ratio (within 25 ns) > 99 %
- LF-Monopix2:
  - More than 99% in-time efficiency after irradiation to 1e15 n_{eq} cm^{-2}
  - Promising results for 2e15 n_{eq} cm^{-2} samples, analysis ongoing

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

This project has received funding from the Deutsche Forschungsgemeinschaft DFG (grant WE 976/4-1), the German Federal Ministry of Education and Research BMBF (grant 05H15PDCA9), and the European Union’s Horizon 2020 research and innovation program under grant agreements no. 675587 (Maria Sklodowska-Curie ITN STREAM), 654168 (AIDA-2020), 101004761 (AIDAinnova), and 101057511 (EURO-LABS).

BACKUP

DEPLETED MONOLITHIC ACTIVE PIXEL SENSOR

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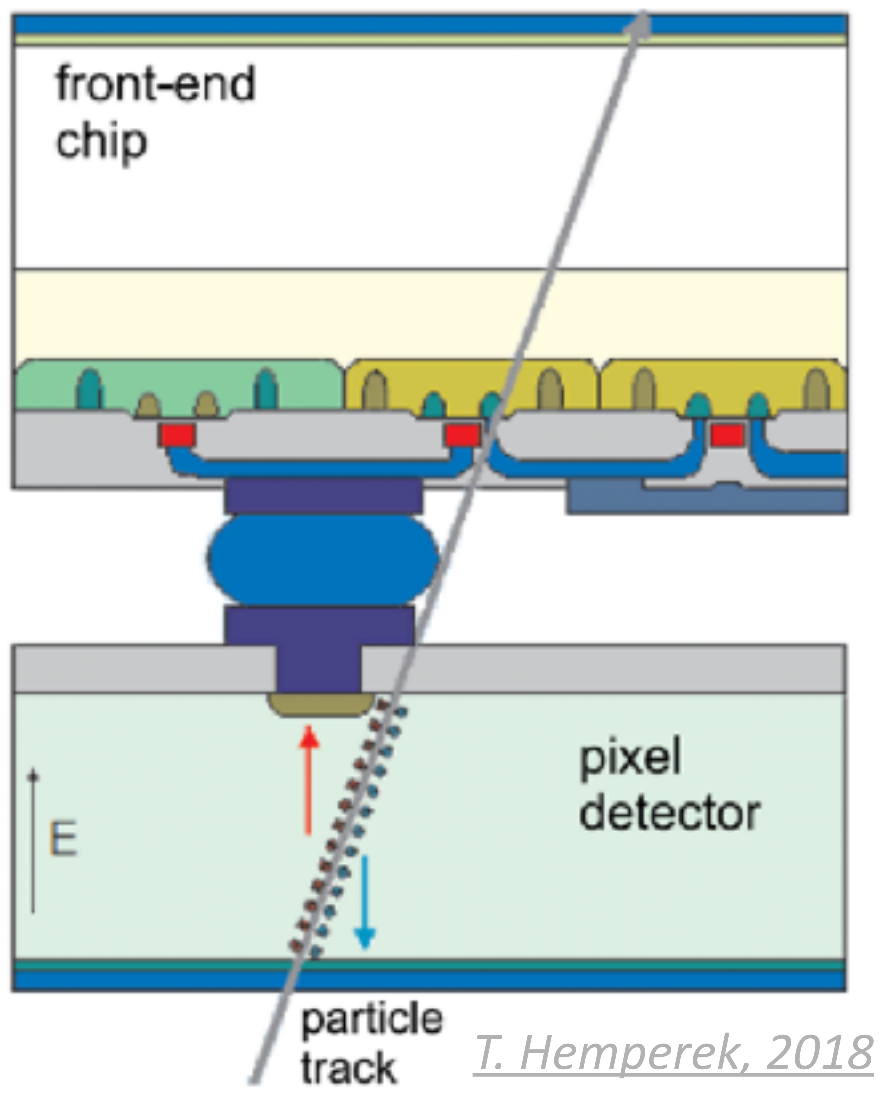
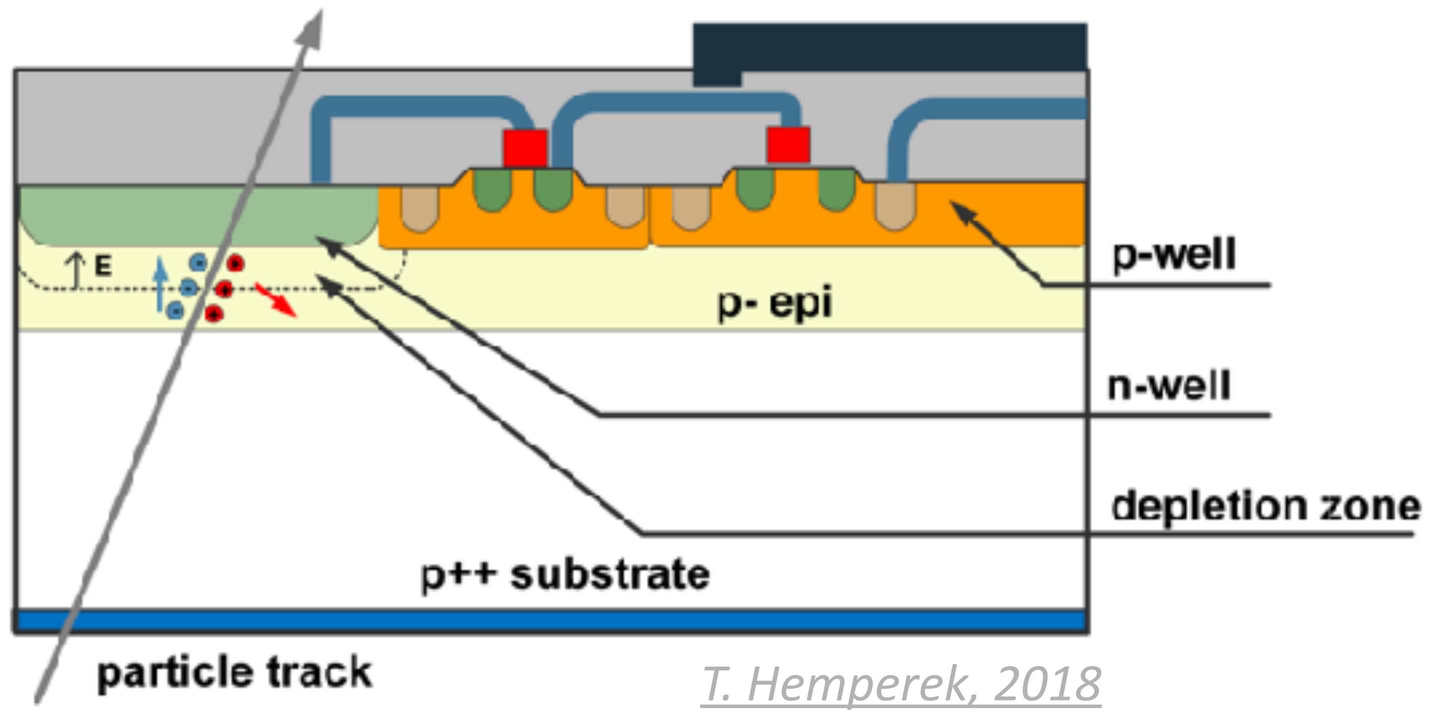
Hybrid detector



✓ Optimized individual parts
✓ High rad. tolerance

✗ Cost and labor intensive bump-bonding

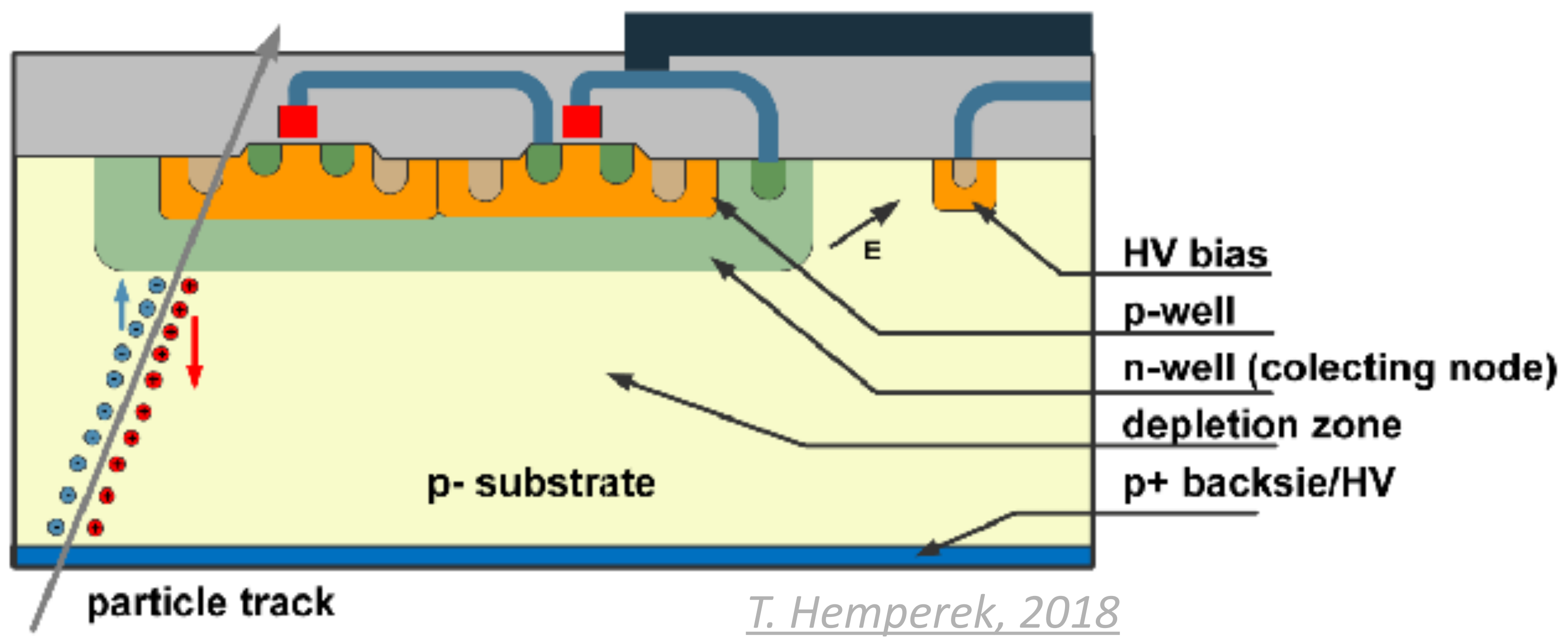
MAPS detector



✓ Reduced material budget
✓ Commercial processes:
- Fast & high volume production
- Lower module cost

✗ Sensor not fully depleted
- Not radiation hard

Depleted MAPS detector

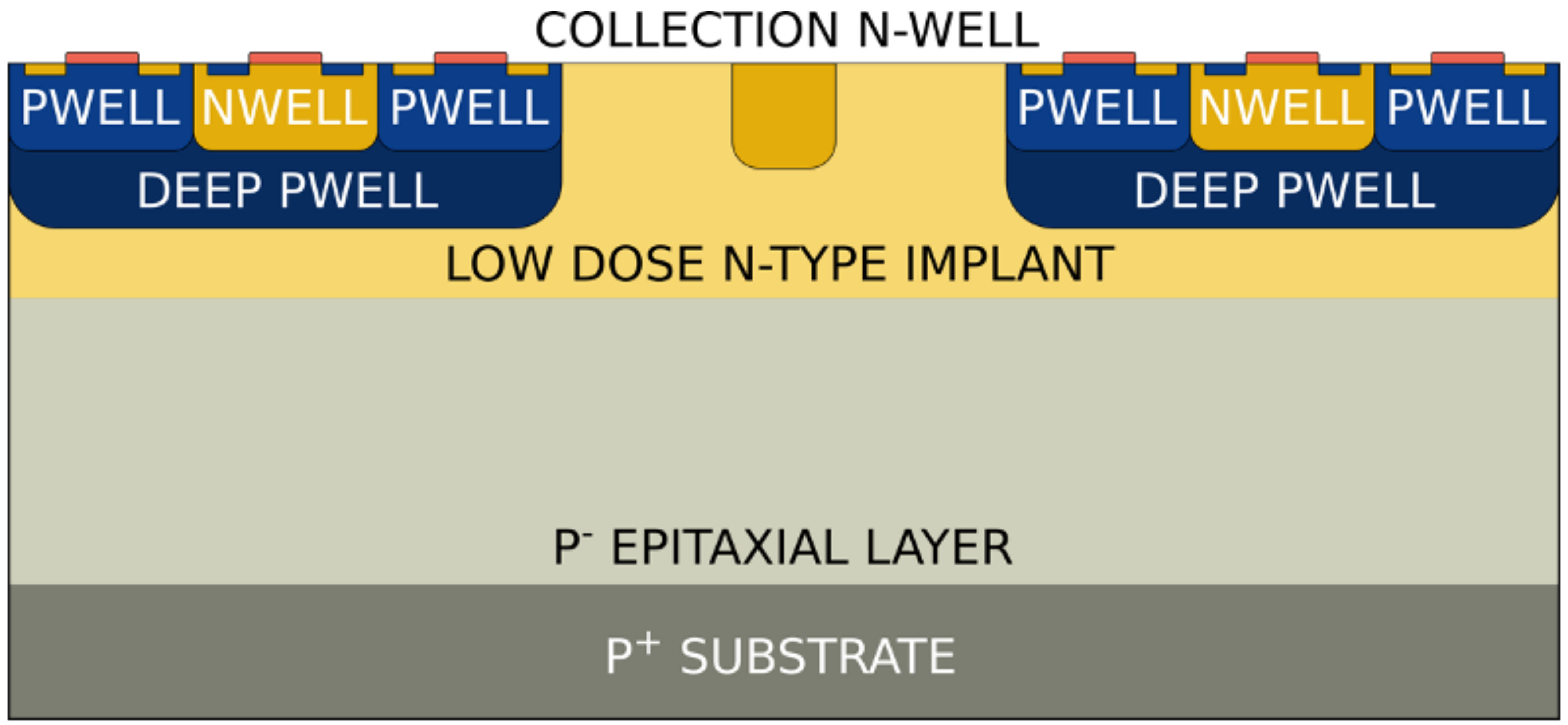


- CMOS processes offer high-resistivity substrate
- Bias voltage capabilities (HV)

✓ Strong drift field
✓ Enhanced charge collection
→ Increased radiation tolerance

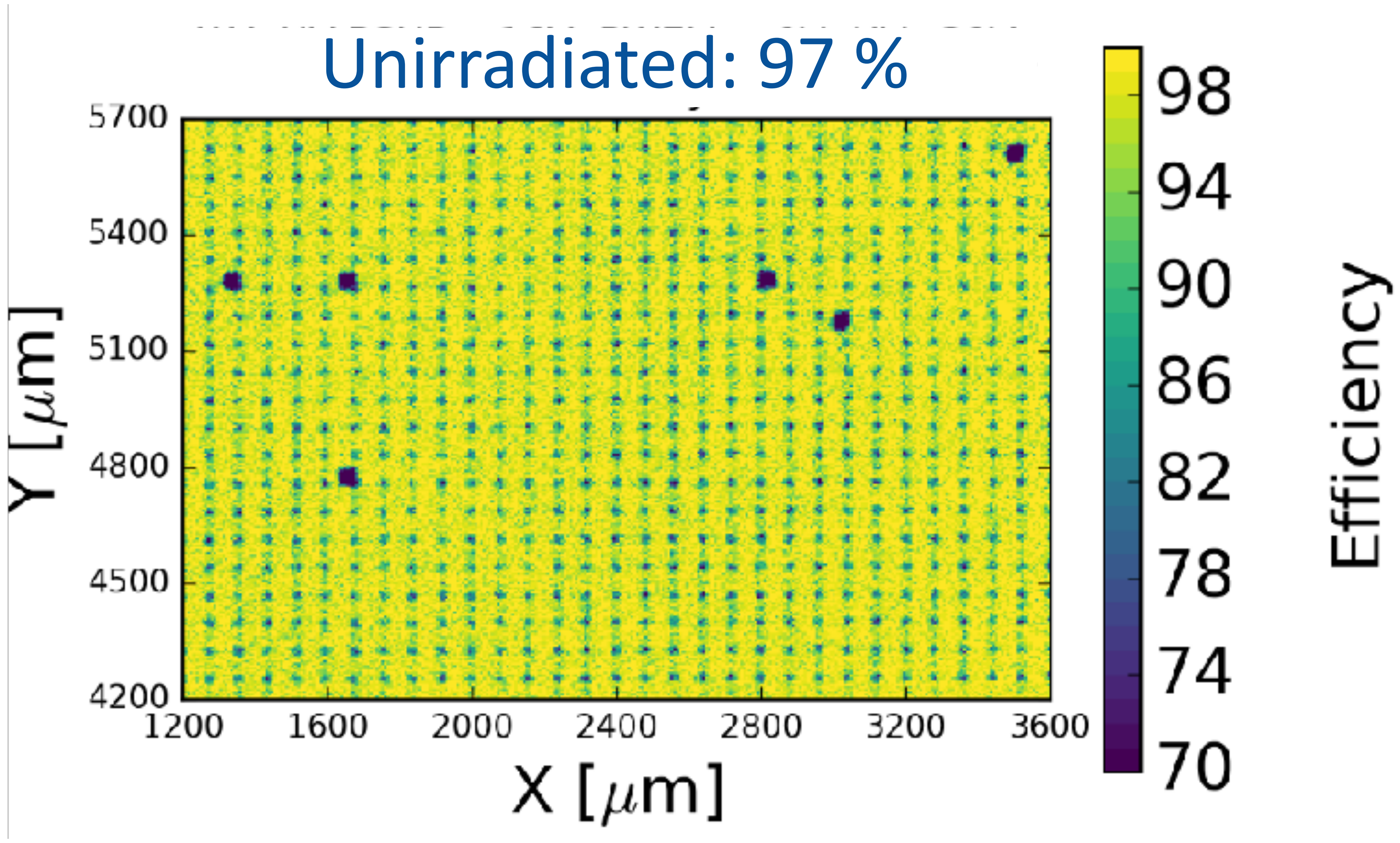
TJ-MONOPIX DESIGN

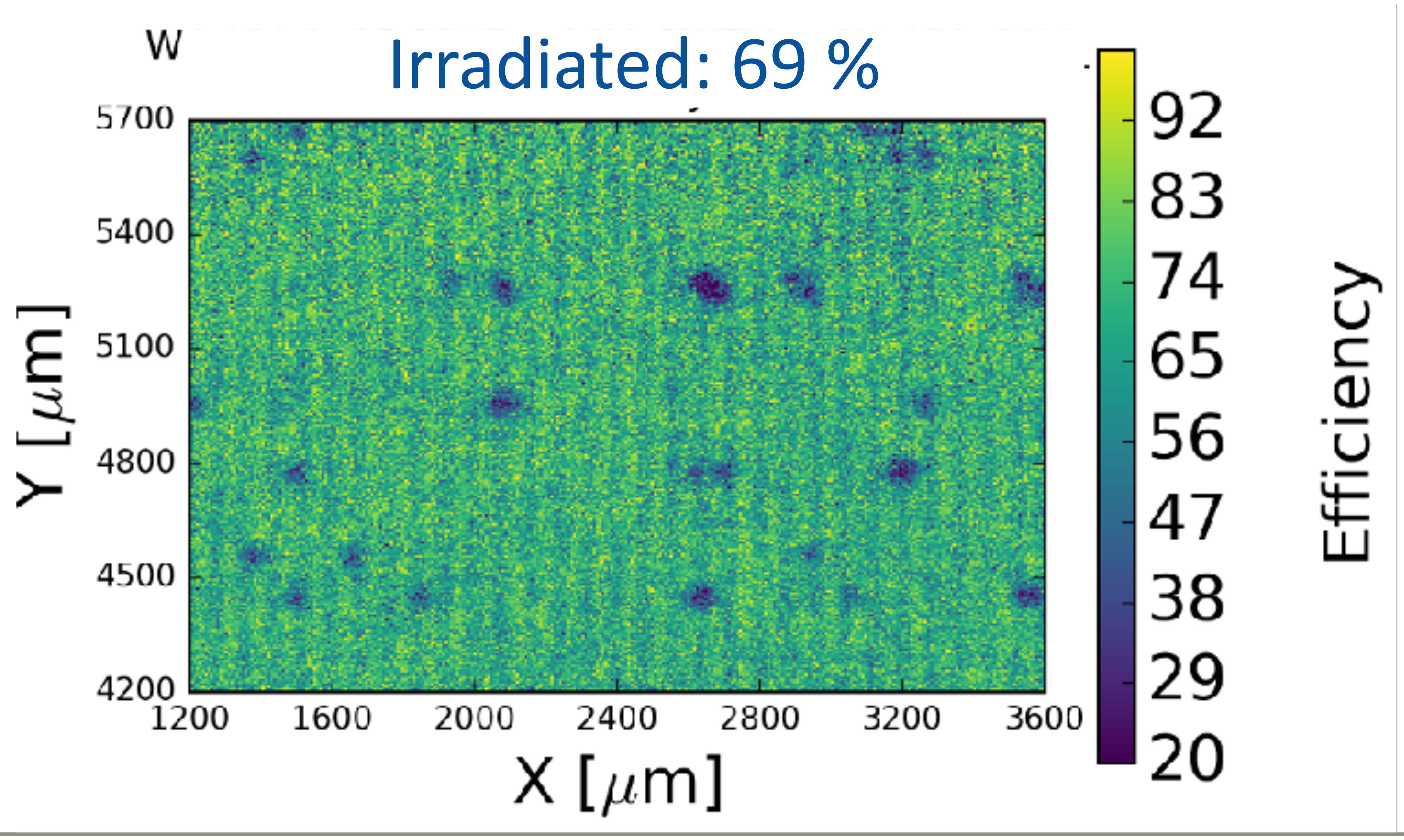
- TJ-Monopix is line of DMAPS designed in a 180 nm Tower CMOS process based on ALPIDE sensor for ALICE ITS upgrade
- Small collection electrode for operations with low power and low noise
- Designed for ATLAS ITk outer layer specs with column-drain readout like in FE-I3 in a 2 cm column
  - Pixel readout capable of dealing with hit rate > 100 MHz / cm^2
  - Goal: 10^{15} 1 MeV n_{eq}/cm^2 NIEL tolerance and 100 MRad TID
- Low dose n-type implant for homogeneous depletion of sensor volume (initial design)
- Radiation hardness not straight-forward in small collection electrode design



RADIATION HARDNESS TJ-MONOPIX1

- Extensive tests performed in 2018 at ELSA beam line (2.5 GeV electrons) in Bonn
- Significant efficiency loss after irradiation to < 70 % (at $10^{15}\,\mathrm{neq\,cm^{-2}}$)
- Charge is lost due to E-field shaping under deep pwell -> need another modification besides low dose n-type





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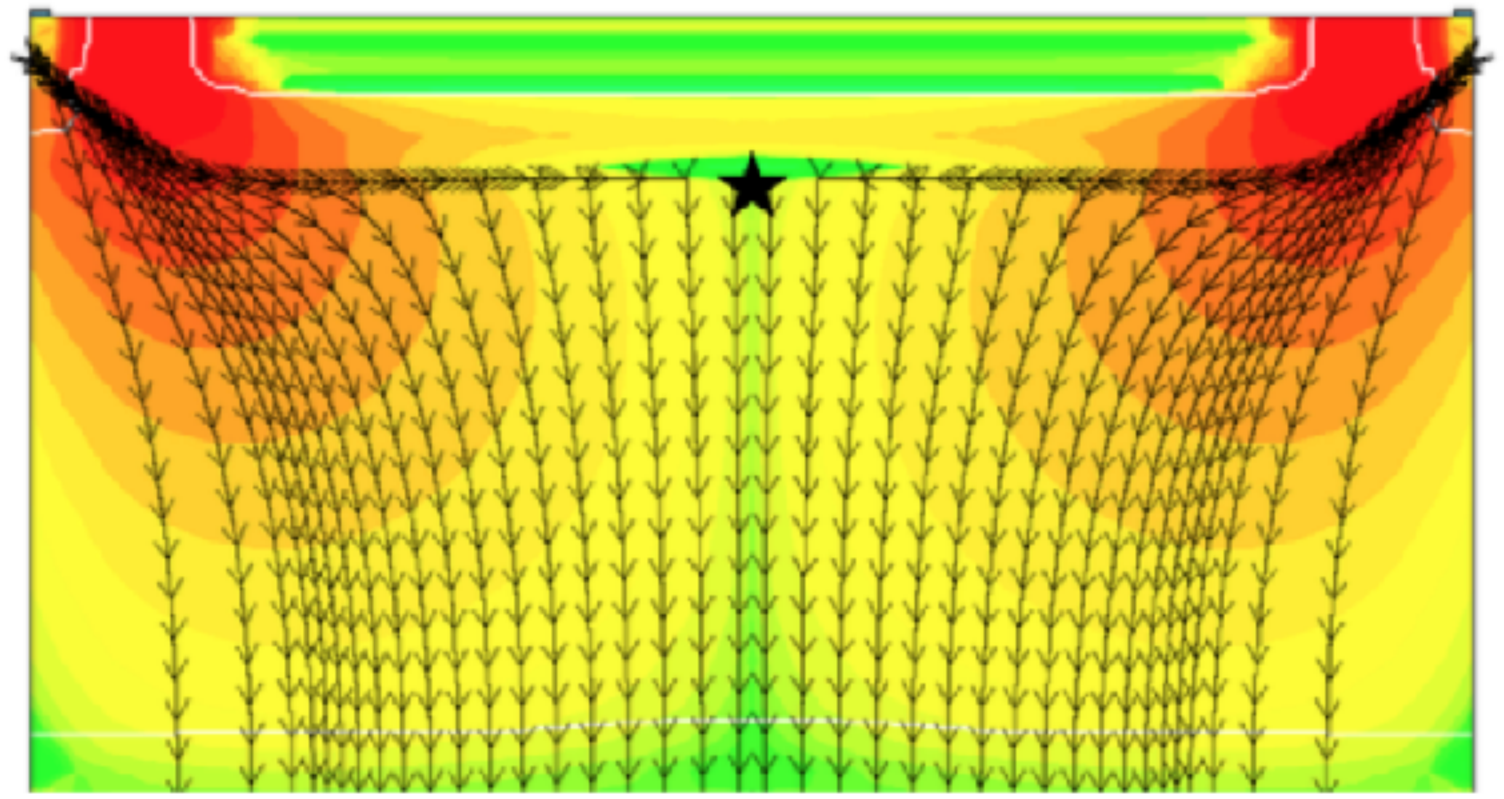
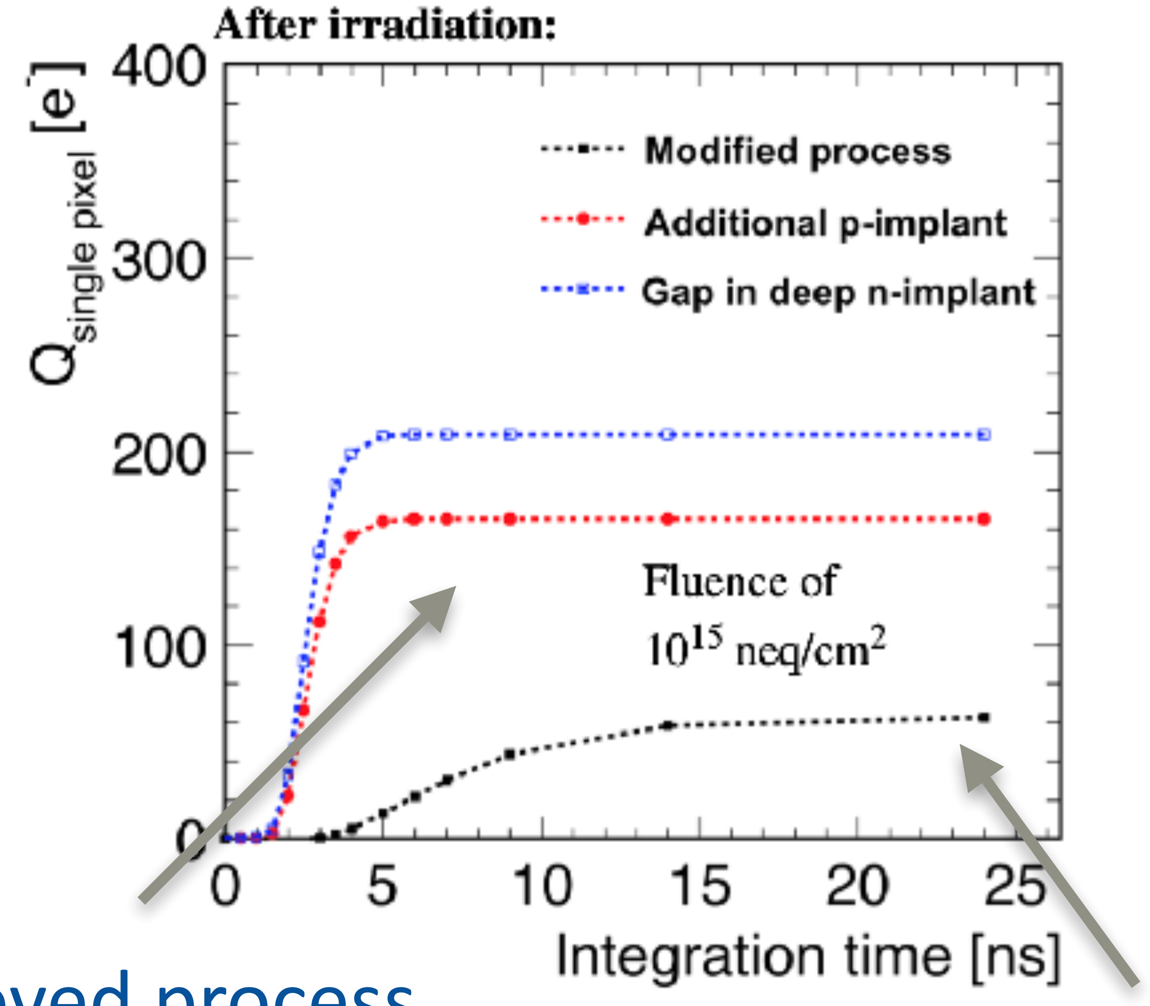
IMPROVED SENSOR DESIGN

- Low electric field below deep p-well in between pixels (minimum indicated by star)
- Gap in n-type implant (or additional p-type well) below readout electronics to shape electrical field towards collection node



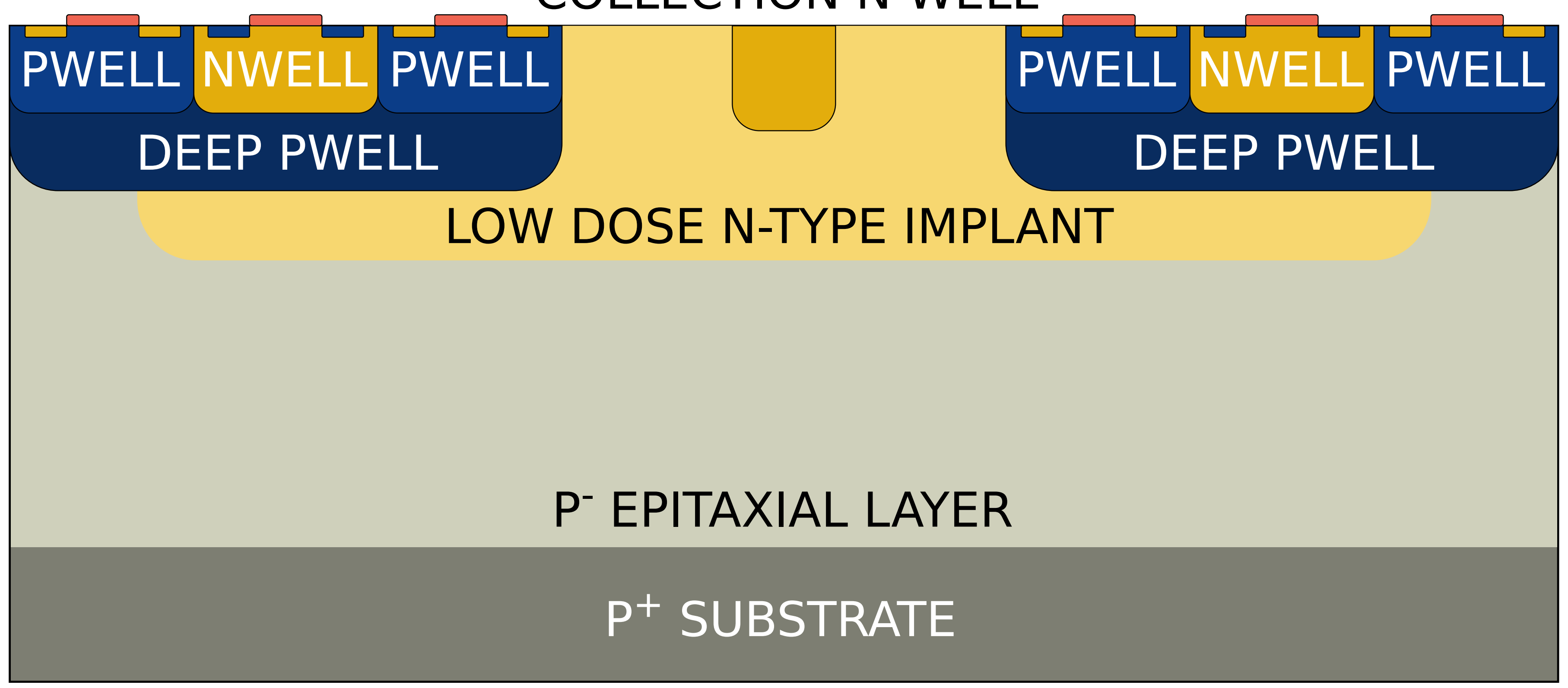


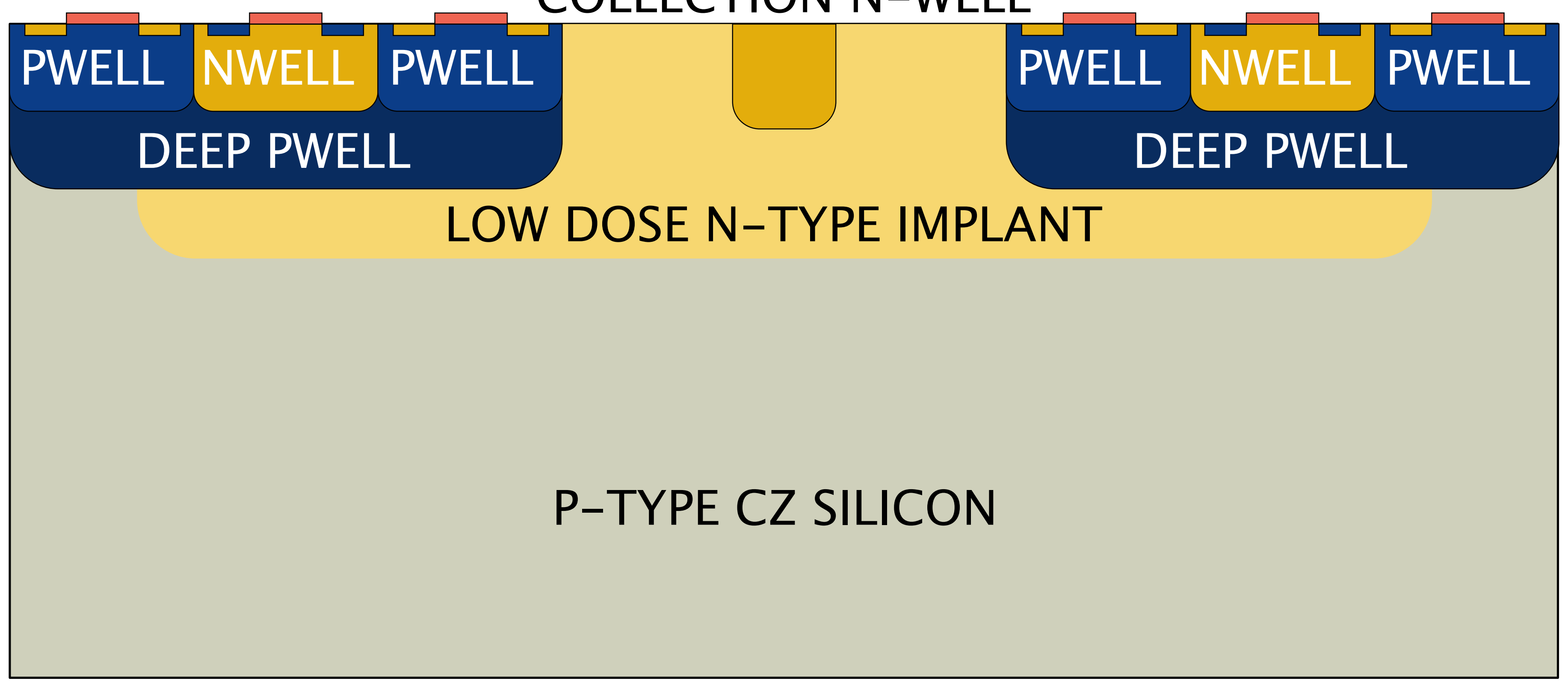
Both: doi.org/10.1088/1748-0221/14/05/C05013

Improved process

Initial process

- Additionally produced on Cz substrate with possibly larger volume

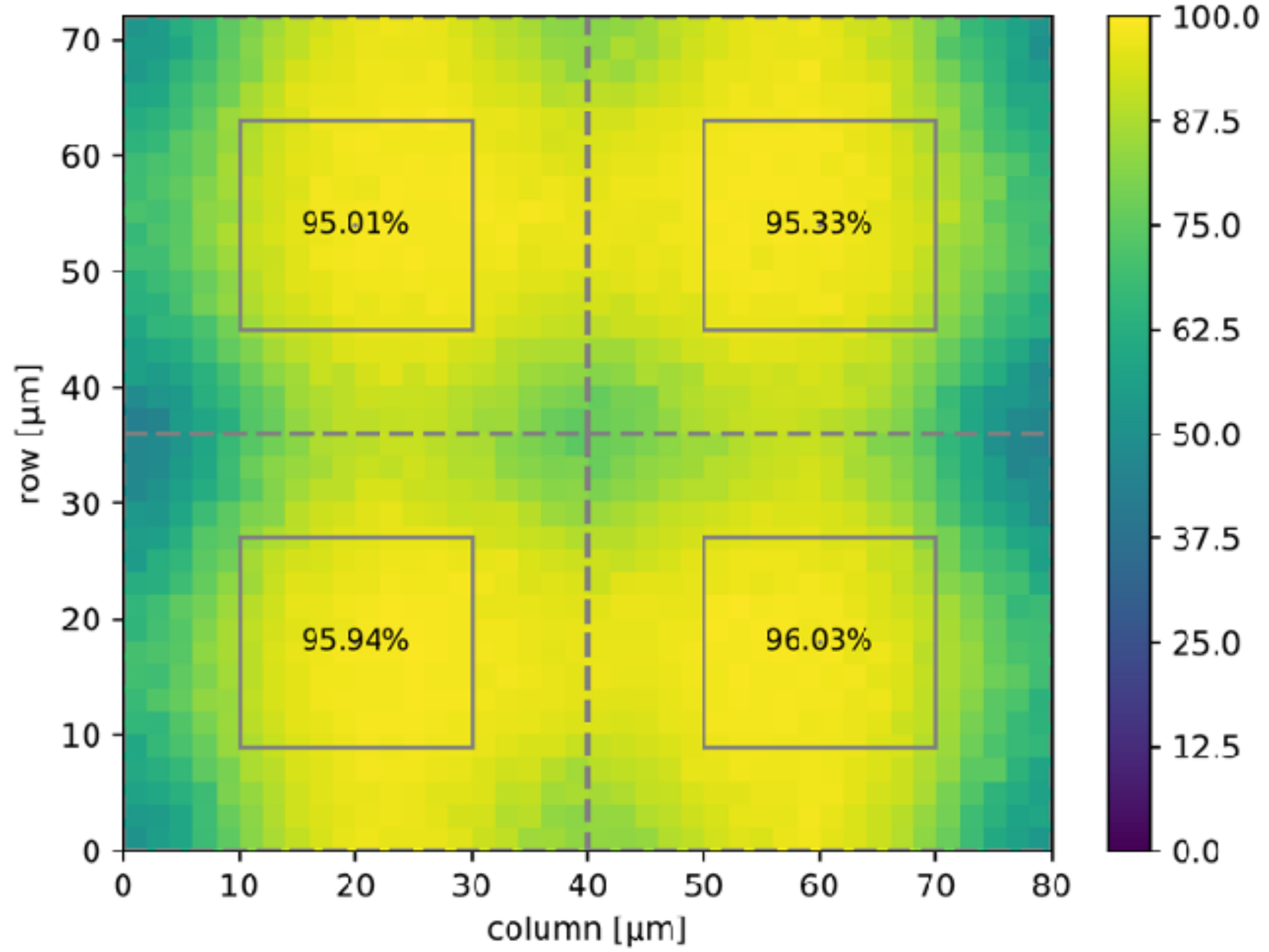




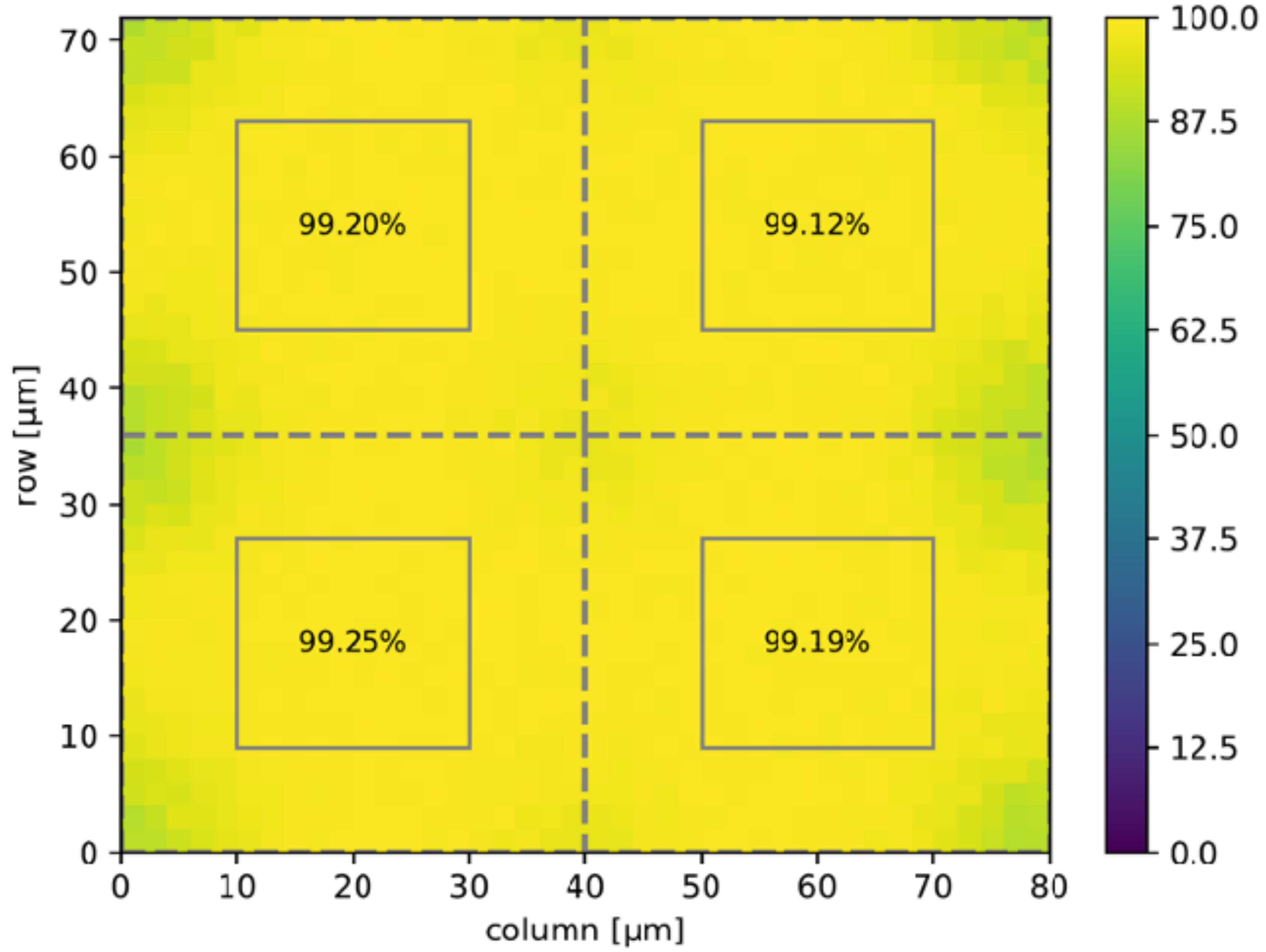
RADIATION HARDNESS NEW DESIGN

- Measured $10^{15}\,\mathrm{neq\,cm^{-2}}$ irradiated chips in 5 GeV electron beam at DESY
- Efficiency improvement in epi chip from 69 % to 87 % due to sensor modifications
- More sensitive volume and more charge in Cz leads to full efficiency after irradiation

30 µm Epi: 87.1 % @ 500 e-

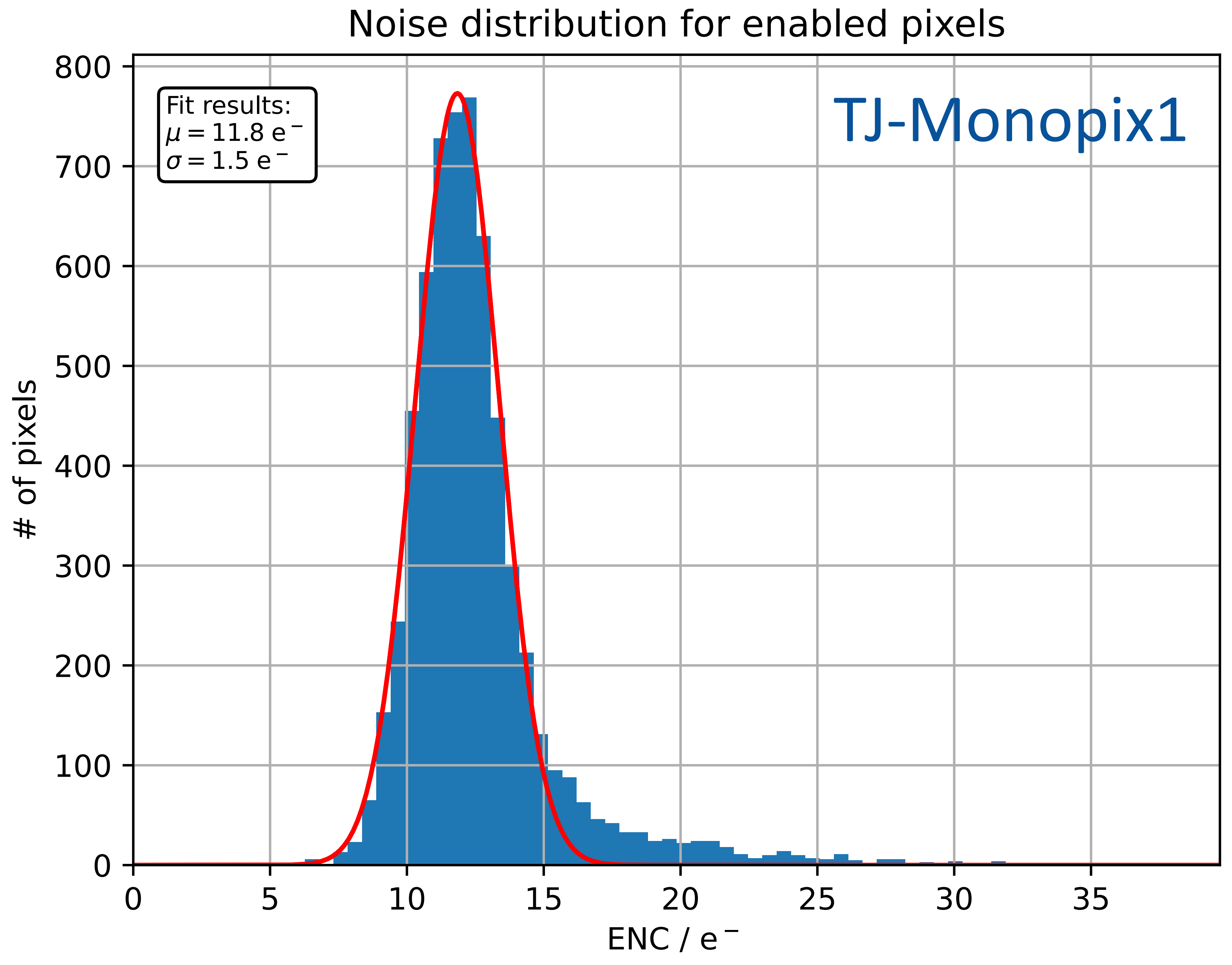


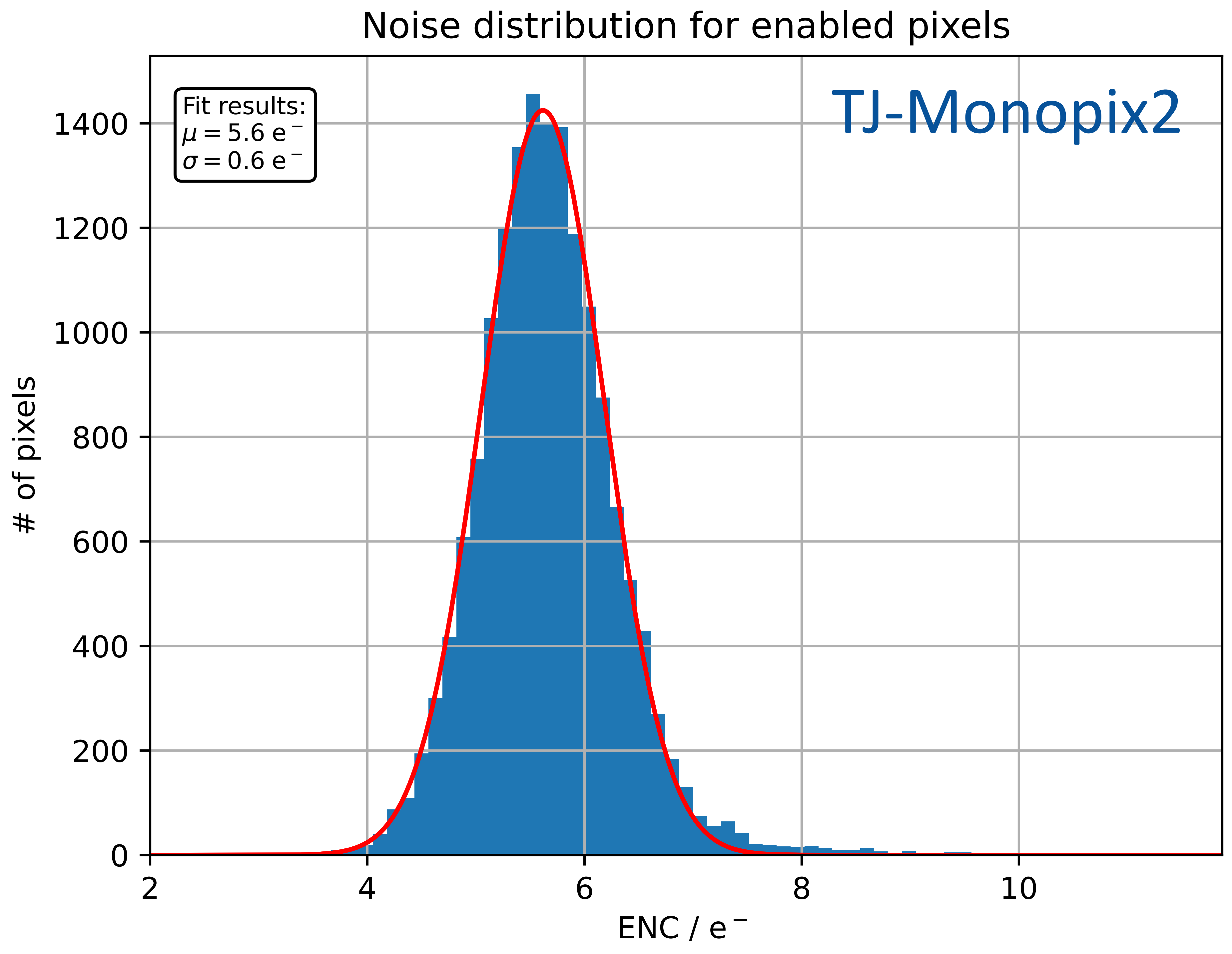
300 µm Cz: 98.6 % @ 490 e-



NOISE IMPROVEMENTS (RTS TAIL)

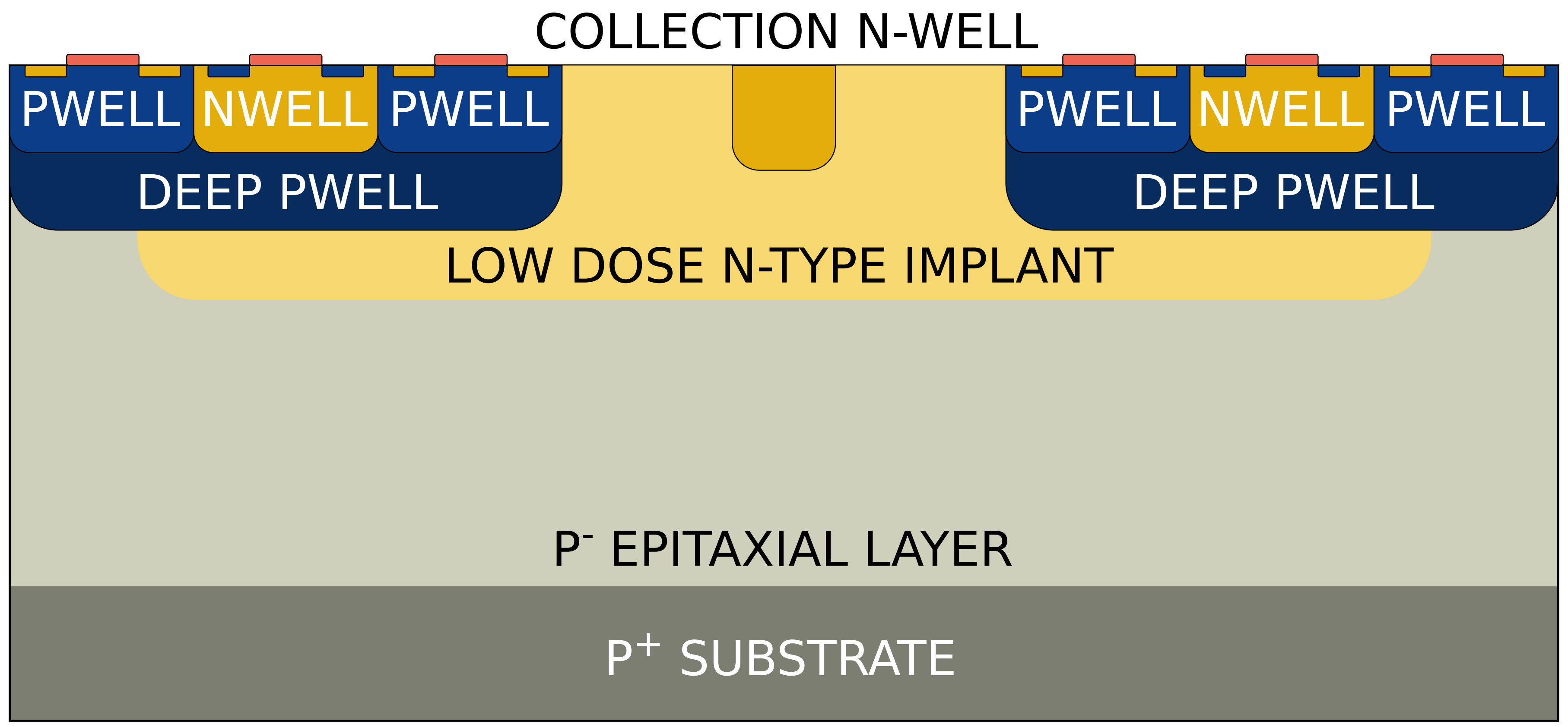
- Threshold in TJ-Monopix1 mostly limited by unexpectedly high noise
- Tail identified as RTS noise
- Enlarged transistors for smaller noise and threshold (tested in miniMALTA before TJ-Monopix2 (CERN))

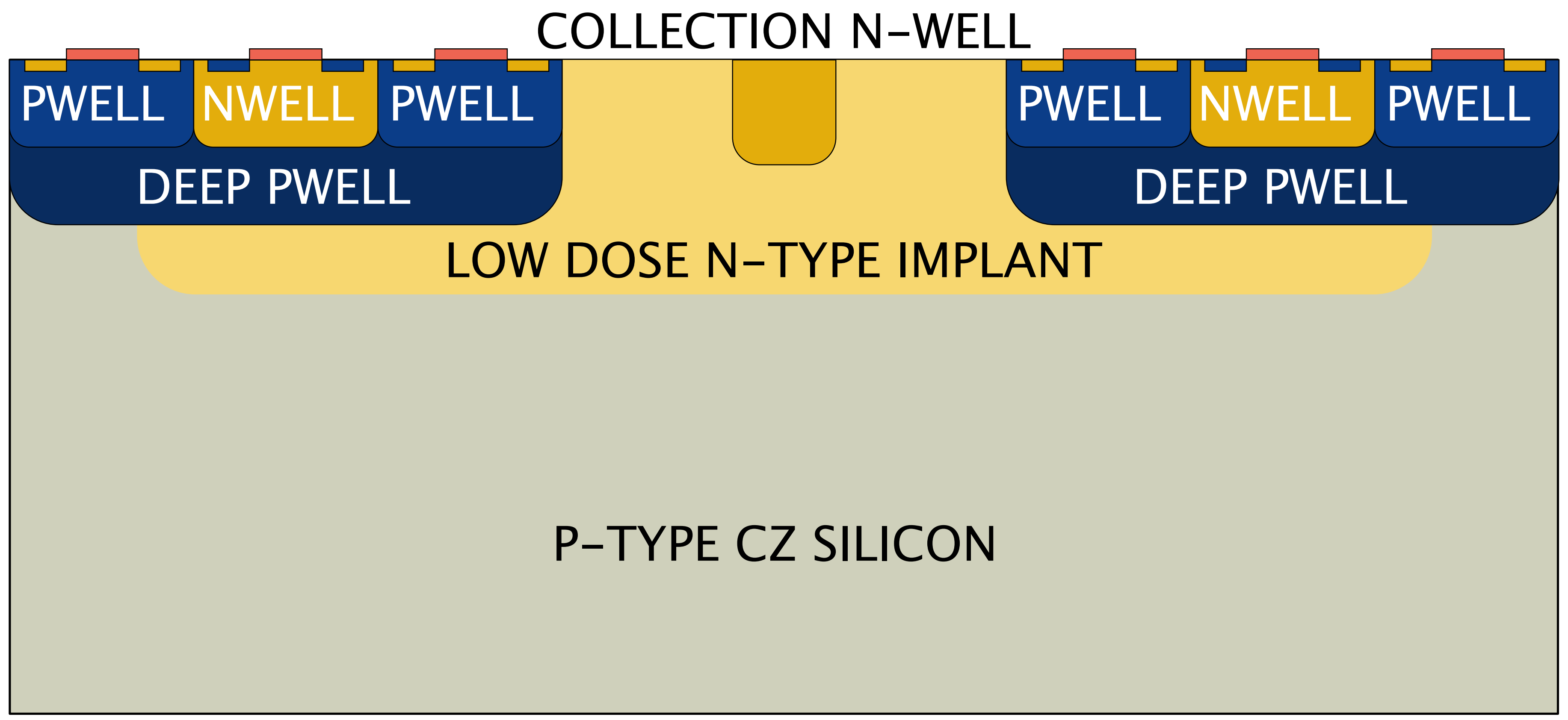




TJ-MONOPIX2 BEAM TESTS

- Beam tests performed at DESY in November 2022 (5 GeV electron beam, Mimosa26 telescope)
- Investigated samples (unirradiated):
  - epitaxial silicon (30 µm thickness) with gap in n-layer
  - Czochralski silicon (100 µm thickness) with gap in n-layer
  - Type of silicon growth (epi vs Cz) not part of investigation, but thickness of sensitive volume
- All samples operating at a threshold of ~200 e^-

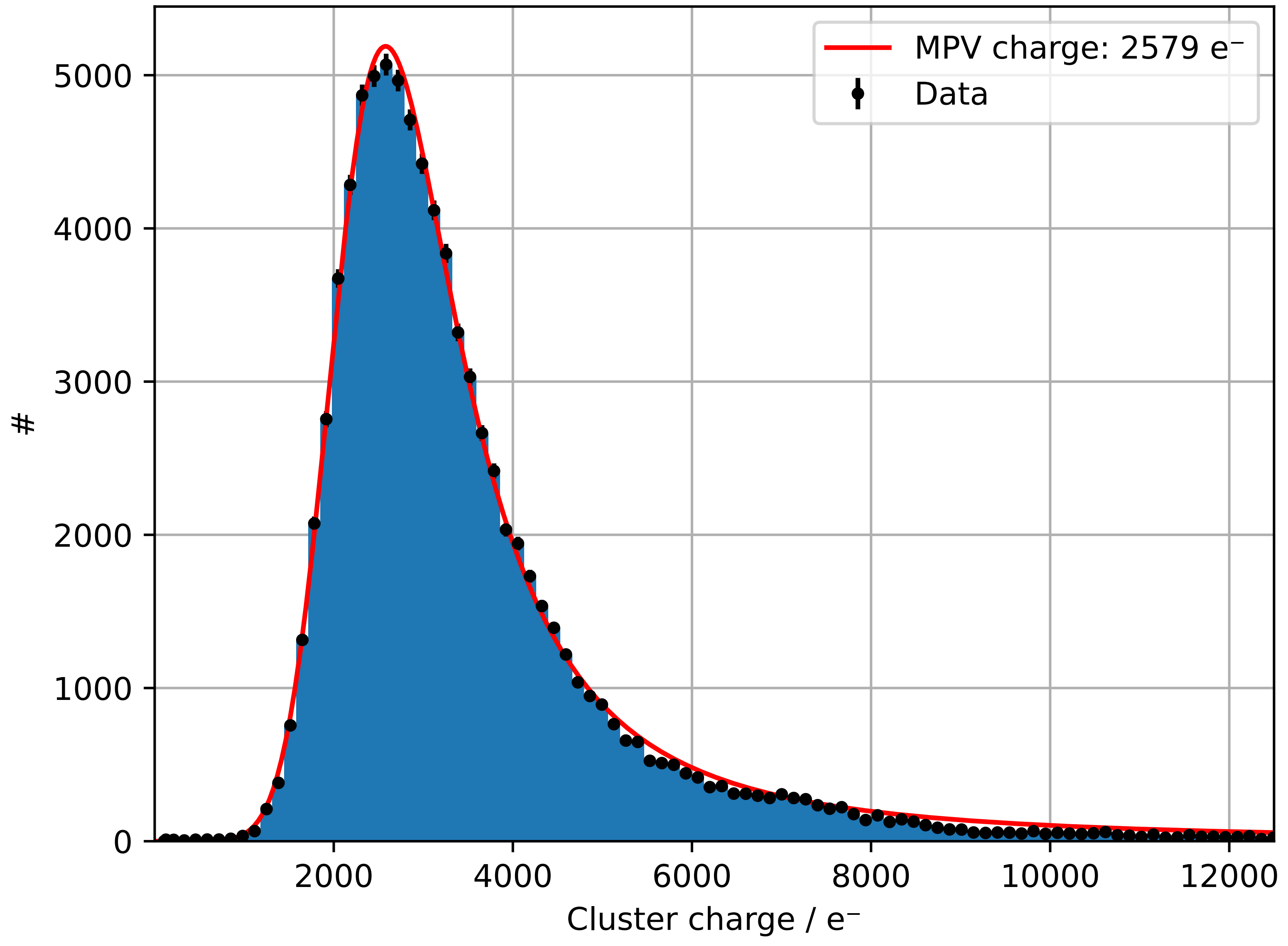




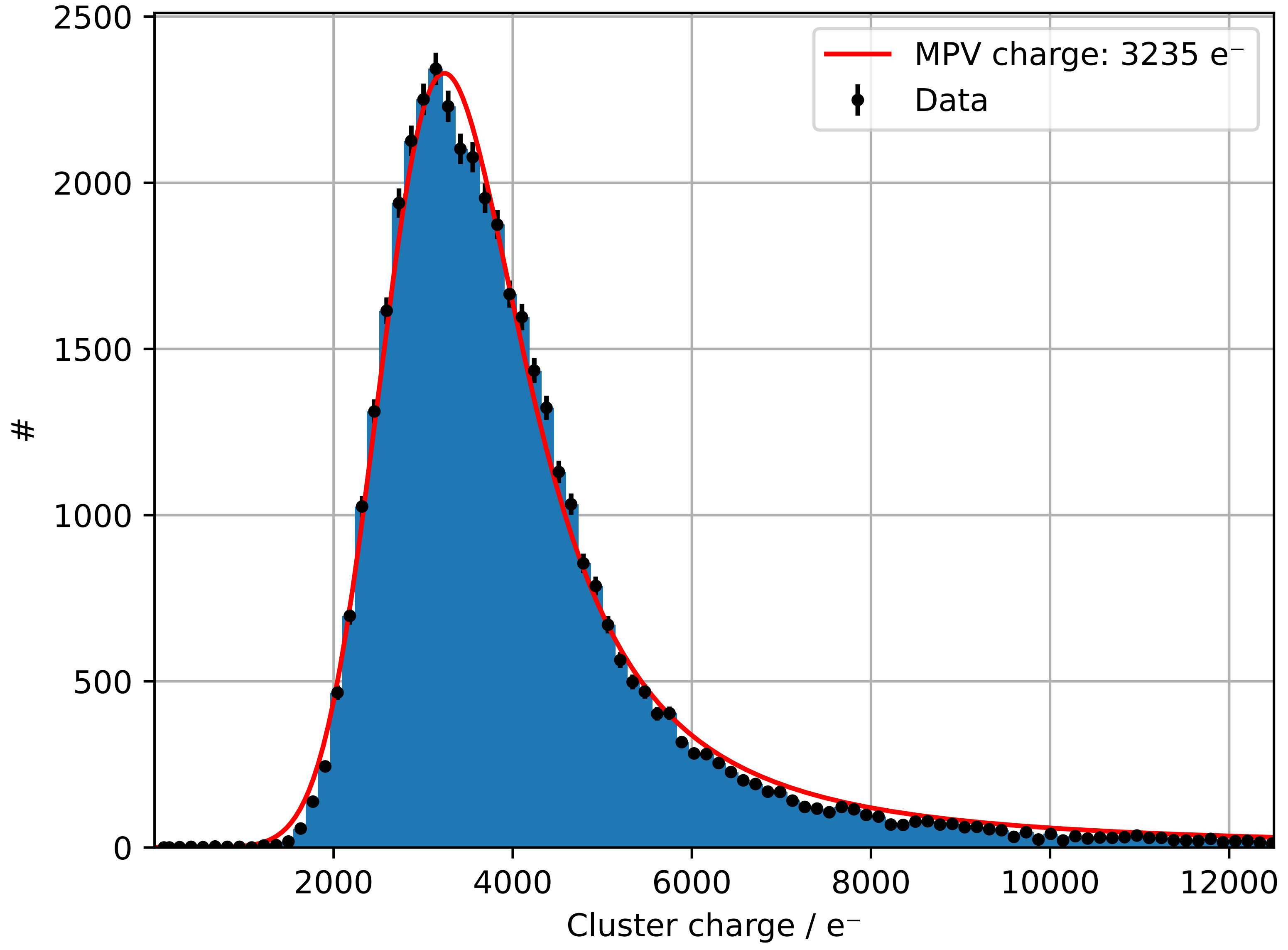
TJ-MONOPIX2 CLUSTER CHARGE

- Cluster charge (MPV) for standard pixel flavor
- Cz sample has higher MPV since depletion is not limited by thickness of epi layer (30 µm)
- Still not fully depleted because of -6 V bias voltage on substrate and p-wells on top of chip

Epi gap in n-layer (30 µm): 2579 e⁻

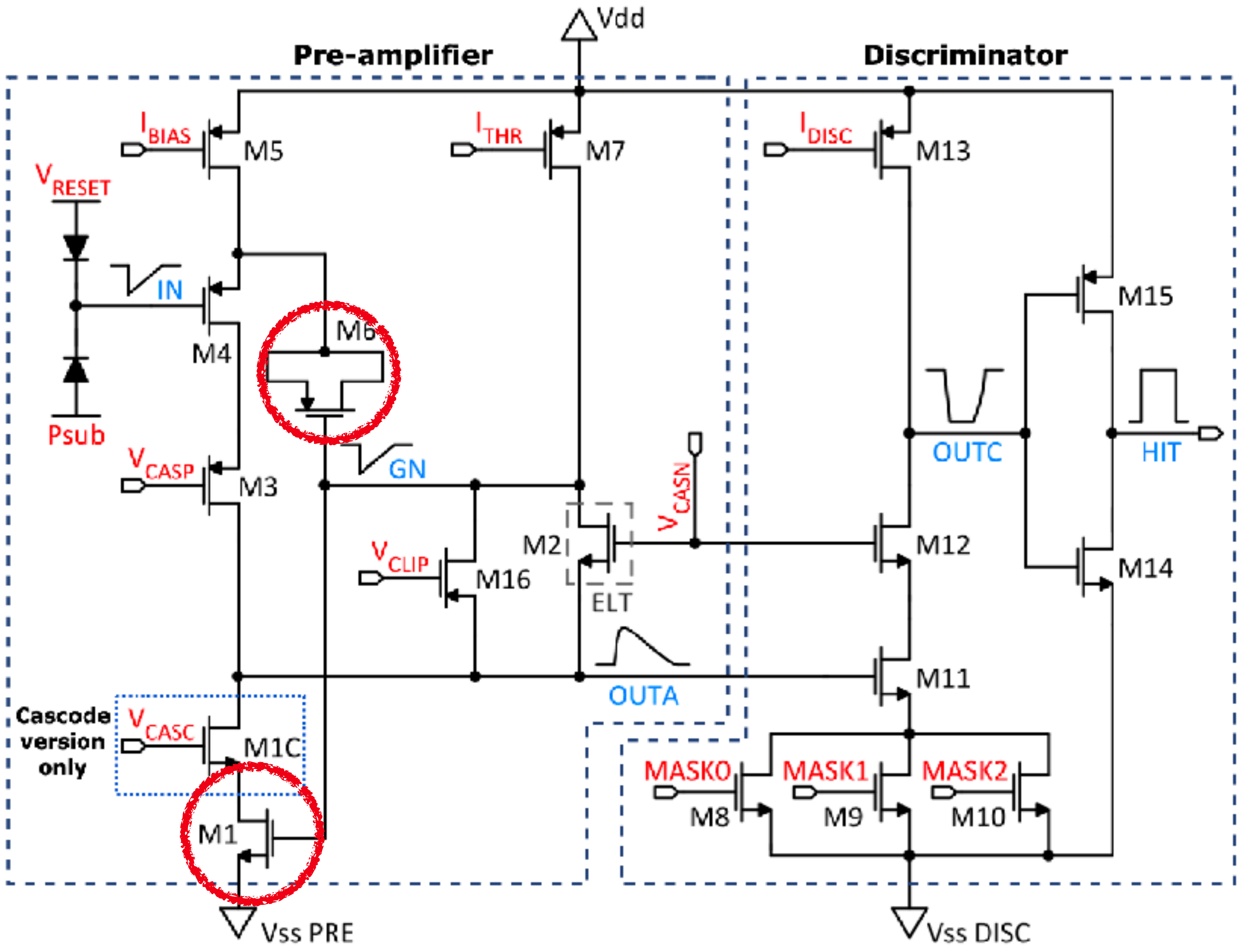


Cz gap in n-layer (100 µm): 3235 e⁻



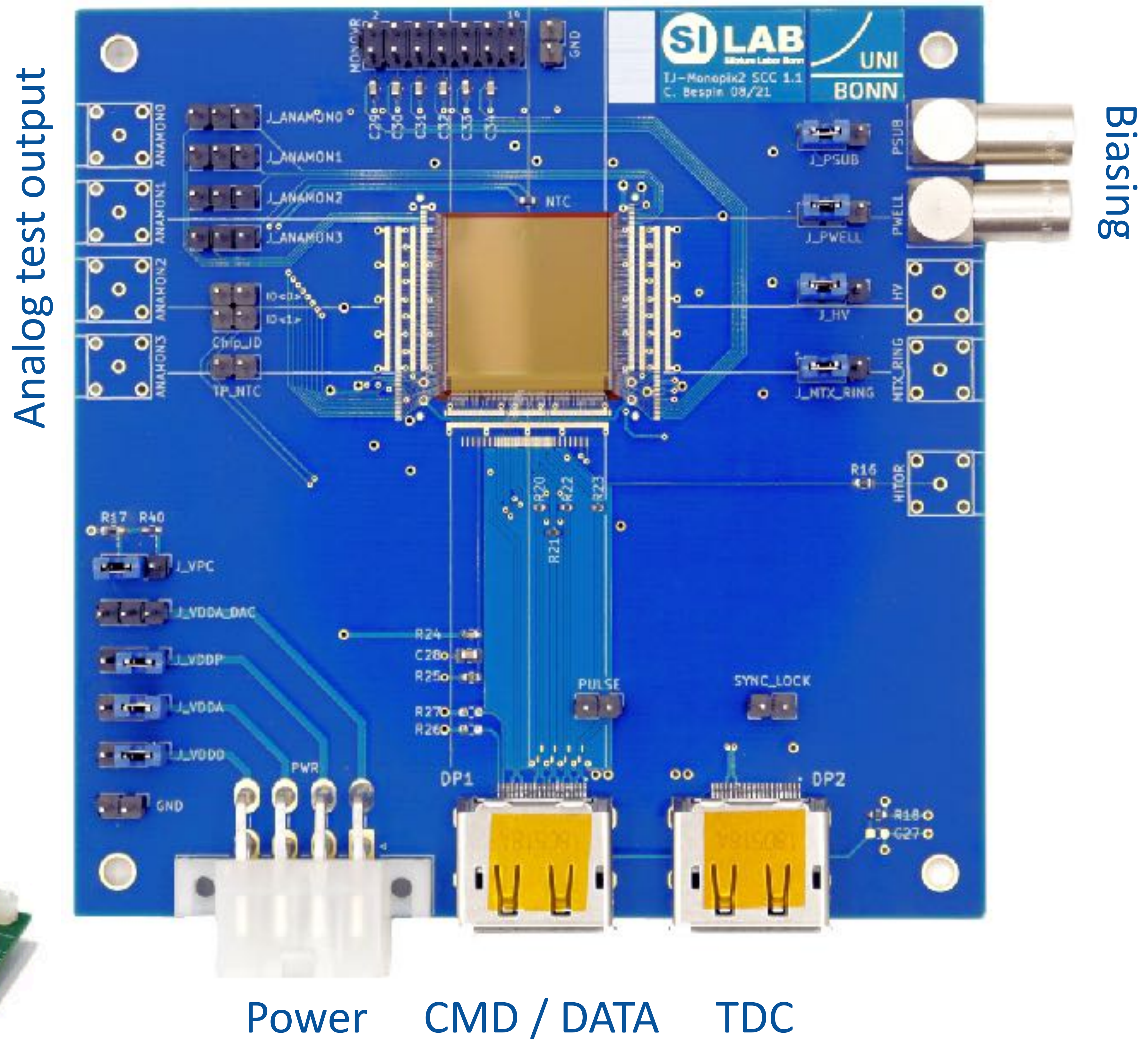
TJ-MONOPIX2 FRONT-END

- Increased size of M1 (and also M6) increases the gain and effectively decreases ENC which in turn allows for lower thresholds
- M6 is coupling capacitor, area increased by factor 7.5 for better coupling to GN node (gain stage input)
- Impedance matching M1 (output) to M2 (input)
- ENC reduced by factor 2 (by simulation)
- Gain at threshold increased by factor 3 (again sim)



TJ-MONOPIX2 DAQ SYSTEM

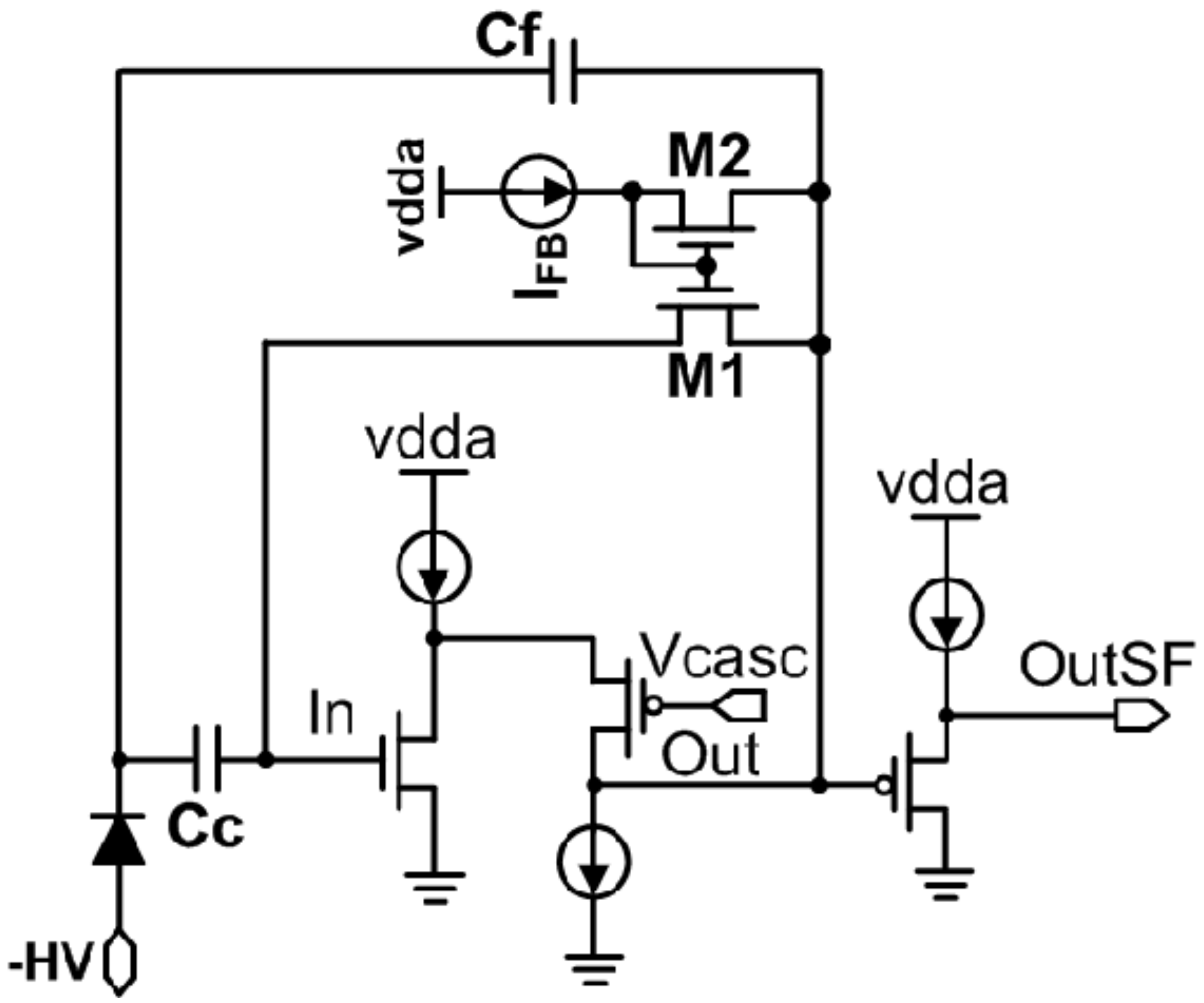
- DAQ System based on RD53A/B readout board bdaq53
- Standalone carrier PCB with power and DisplayPort connector
- Readout board with 1 Gbit/s connection to DAQ computer (10 Gbit/s possible)
- Small and portable setup for irradiations, beam tests etc.



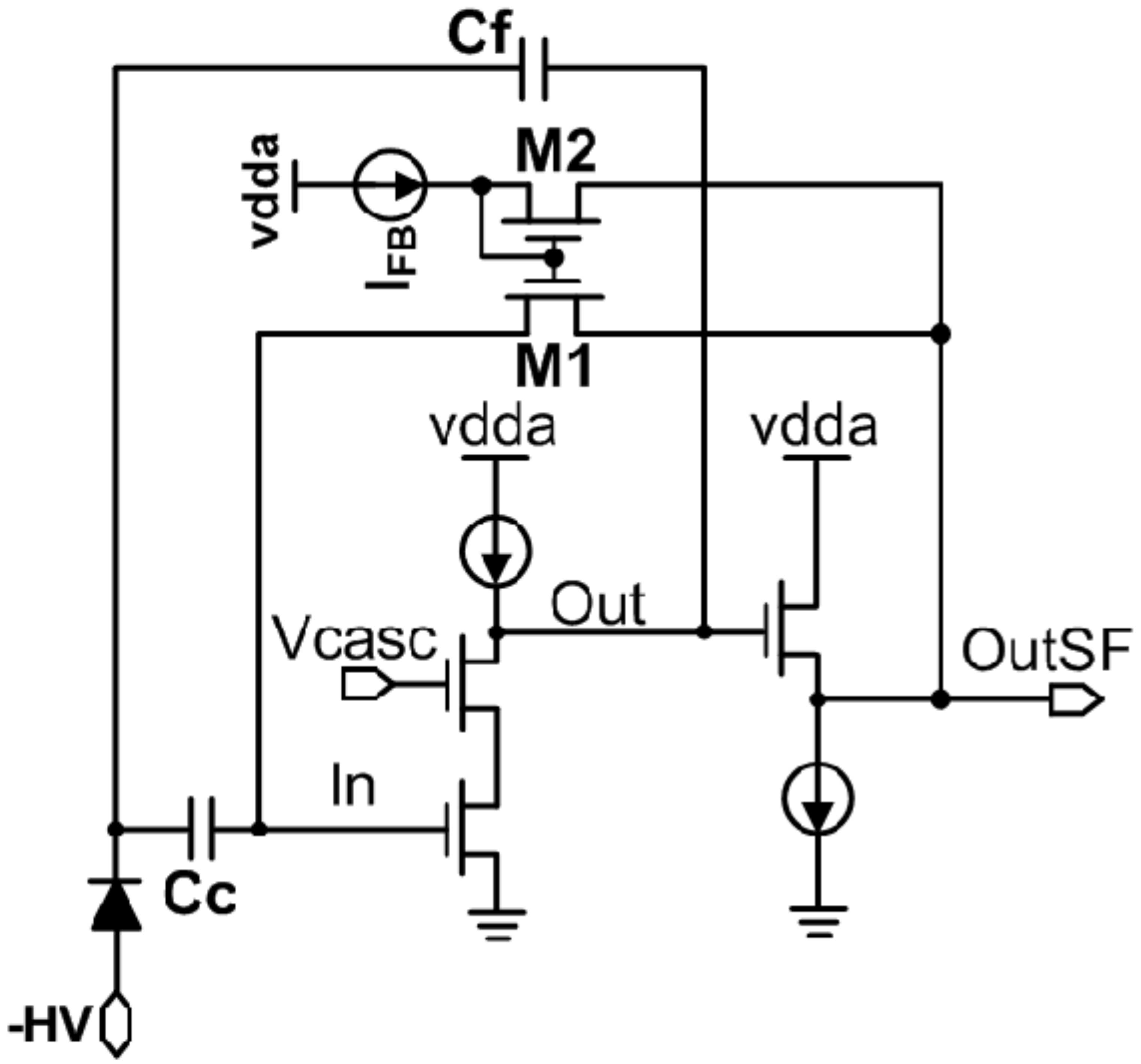
- Chip supports addressing by chip ID (jumper on pin header)
  - Multi-chip readout should be possible with bdaq53

CSA TYPES OF LF-MONOPIX2

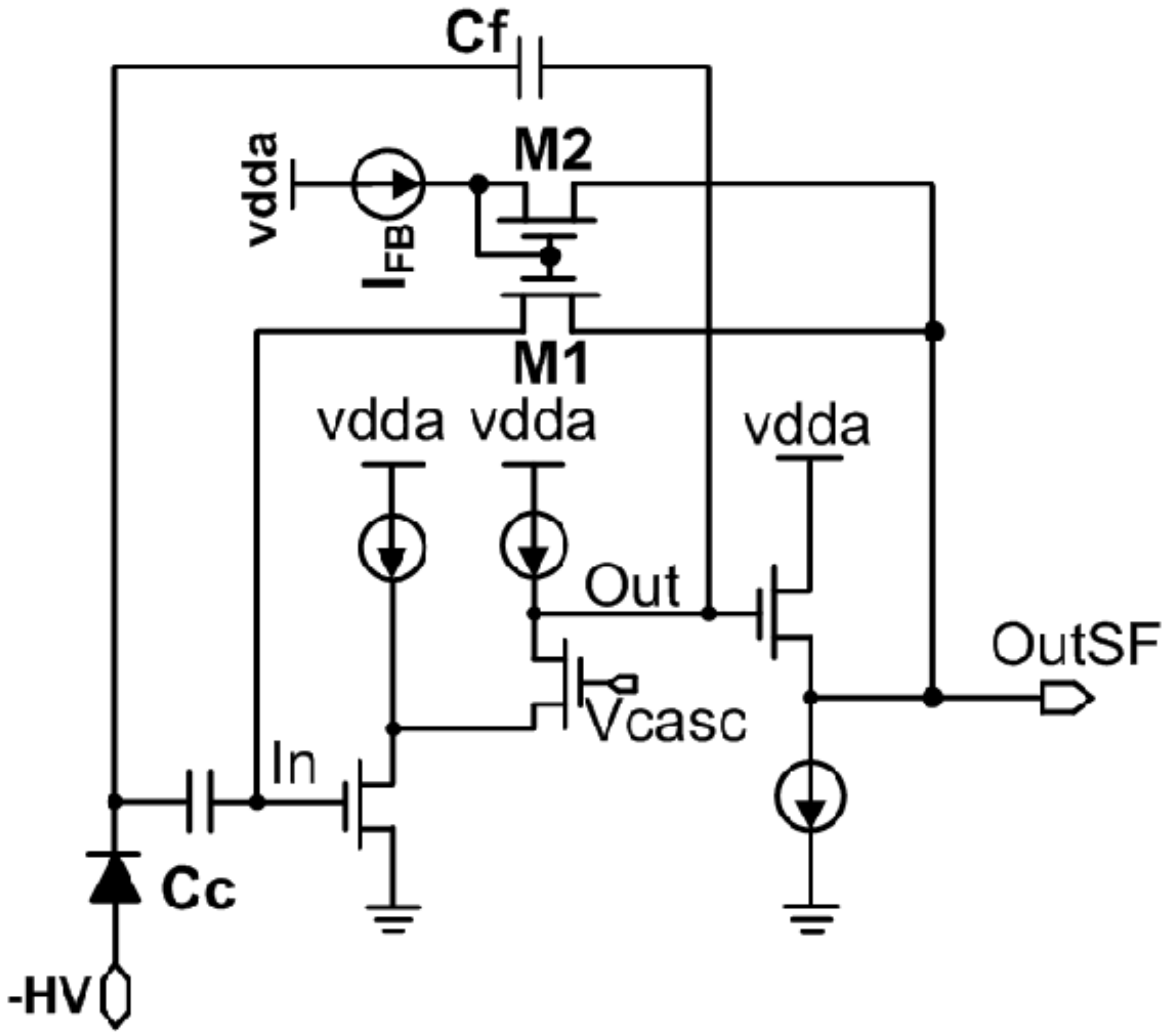
CSA 1
NMOS amplifier from LF-Monopix1



CSA 2
Telescopic cascaded structure

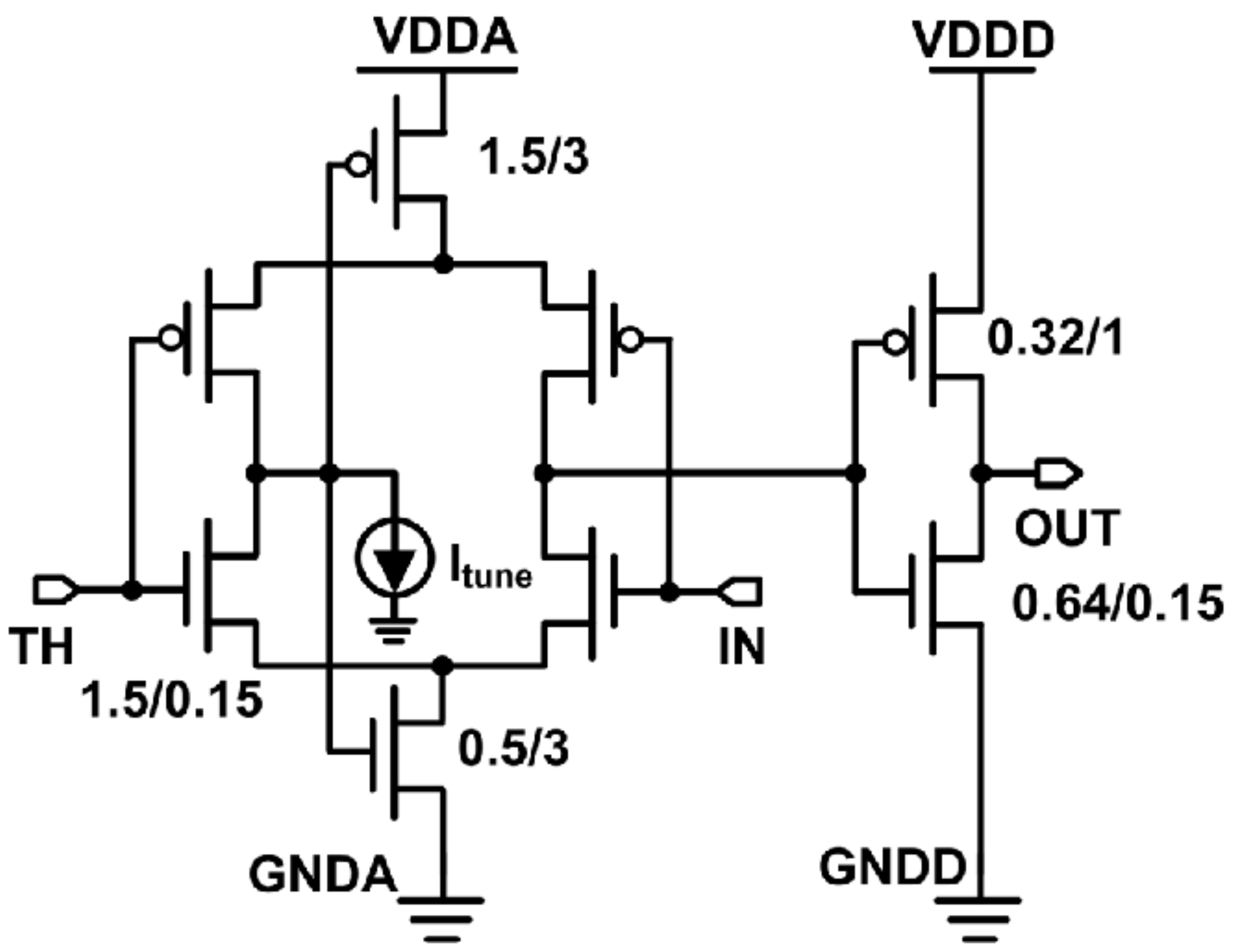


CSA 3
Current into input transistor from two separately adjustable branches

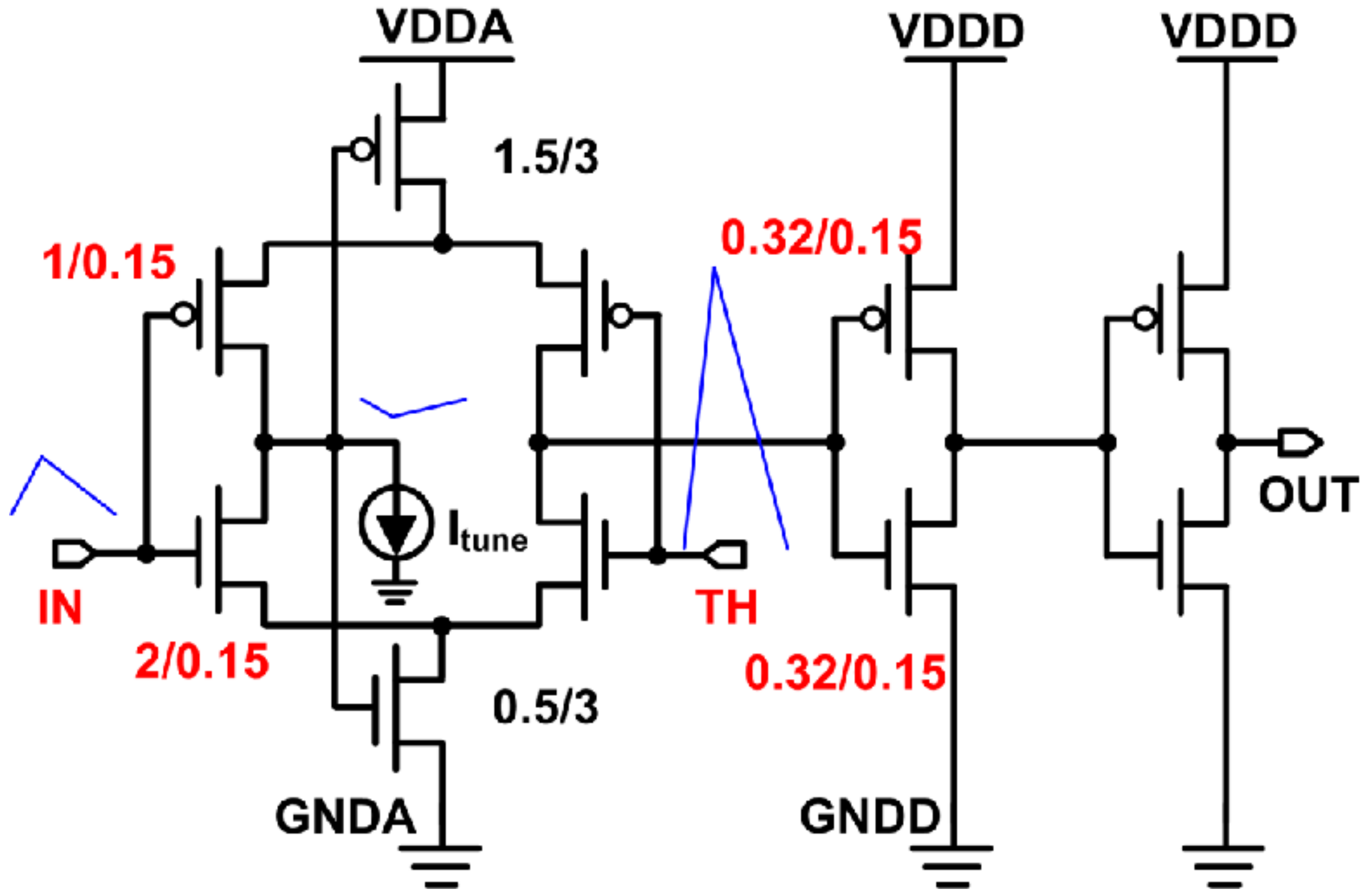


DISCRIMINATOR TYPES OF LF-MONOPIX2

Unidirectional
Self-biased differential amplifier followed by a CMOS inverter

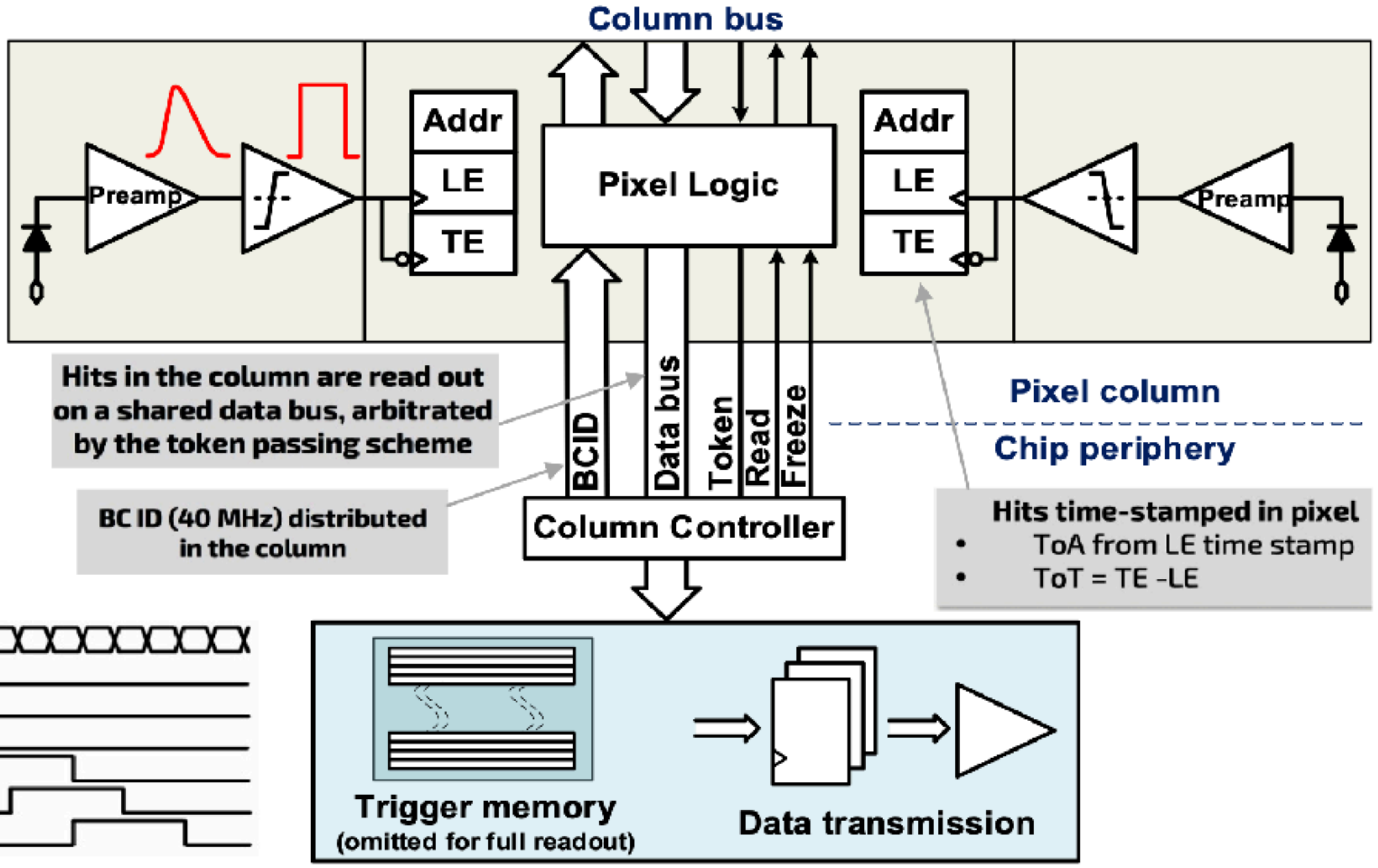


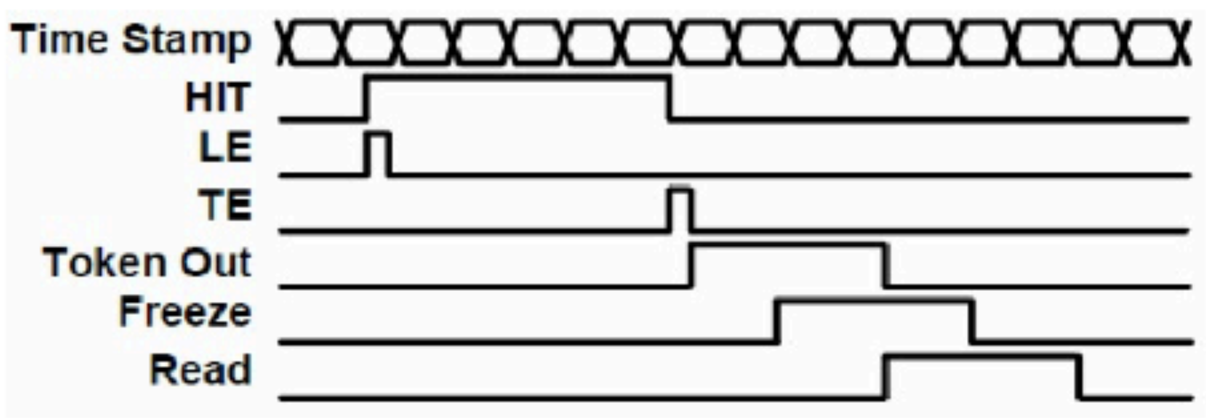
Bidirectional
Optimized transistor dimensions and swapped input ports for faster speed



COLUMN DRAIN READOUT

- Derived from ATLAS FE-I3 readout chip
- Rate capabilities around 100 MHz/cm²
- Token propagation along column
- Readout controller at end of column (READ, FREEZE to pixels)
- Data propagated along column with row address, leading edge and trailing edge
- Periphery merges data from one TOKEN signal into frames that are transmitted 8b10b encoded to readout board





DMAPS DESIGN SPECS

	ALICE LHC	ATLAS HL-LHC		Belle II SuperKEKB
		Outer	Inner	
Time resolution [ns]	20 000	25	25	(100)
Particle rate [kHz / mm^2]	10	1000	10 000	1500
Fluence [neq cm^{-2}]	> 10^{13}	10^{15}	2 x 10^{16}	10^{14}
Ion. Dose [MRad]	0.7	50	> 1000	100

Design specification for rad-hard DMAPS

DMAPS potential candidate