UNIVERSITÄT BONN

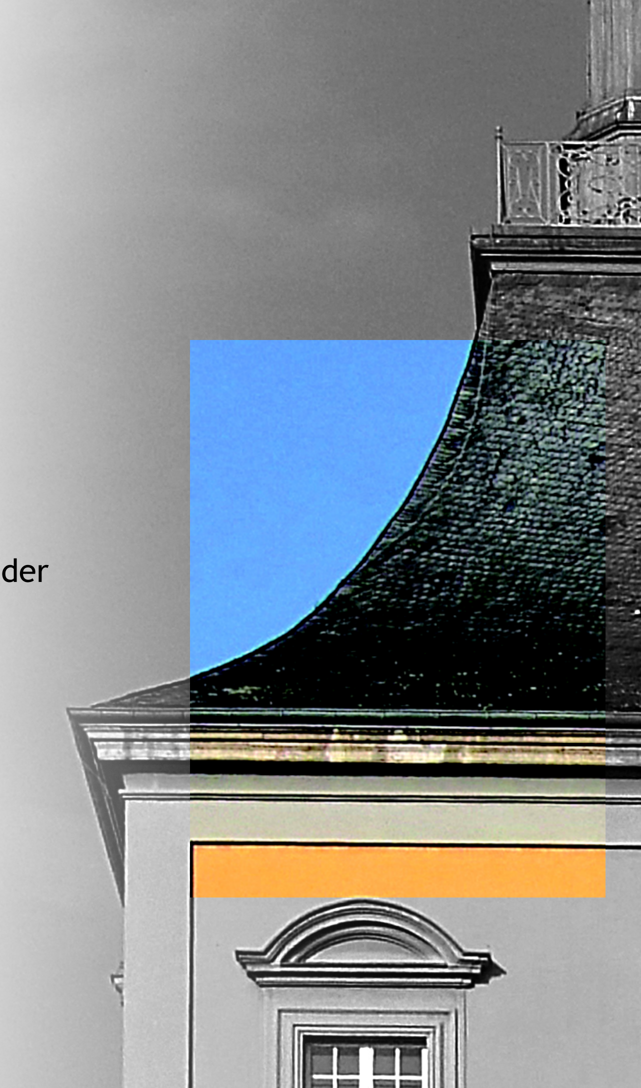
SENSOR DESIGN, GUARD RING, BREAKDOWN:

BREAKDOWN PERFORMANCE OF GUARD RING DESIGNS FOR PIXEL DETECTORS IN 150 NM CMOS TECHNOLOGY

Sinuo Zhang*, Ivan Caicedo, Tomasz Hemperek, Toko Hirono, and Jochen Dingfelder

SENSOR DESIGN OF RD50-MPW4 FOR IMPROVING THE BREAKDOWN VOLTAGE

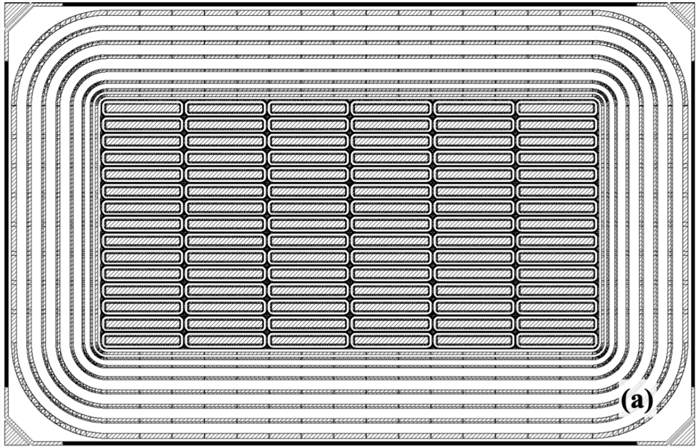
Sinuo Zhang*



PART 1

OVERVIEW

- 6 Passive-CMOS test structures fabricated in 2016:
  breakdown voltage ↔ guard ring structure
- Measurements: IV-characteristics, effect of junction breakdown
- 2D TCAD simulations: IV-curves, potential and electric-field distributions
- Preprint on Arxiv: https://arxiv.org/abs/2310.15717



Breakdown Performance of Guard Ring Designs for Pixel Detectors in 150 nm CMOS Technology

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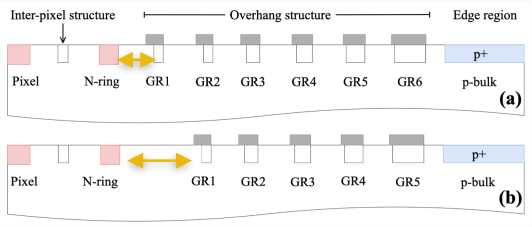
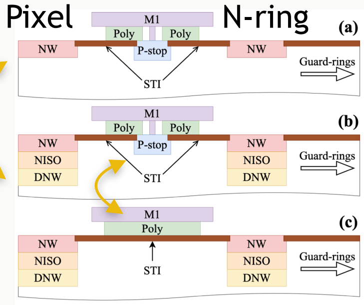
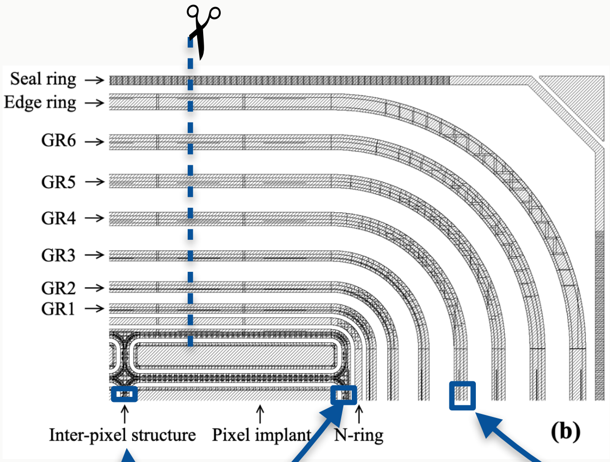
FEATURES OF THE TEST STRUCTURES

- Compare design features
  - 6 test structures (label:“A”to“E”) differs in:

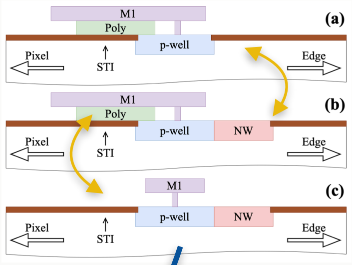


- The number of guard rings (the N-ring to GR1 gap)





- Inter-pixel structure (p-stop or field-plate)
- Use of deep n-well at the pixel and n-ring



For all GR:

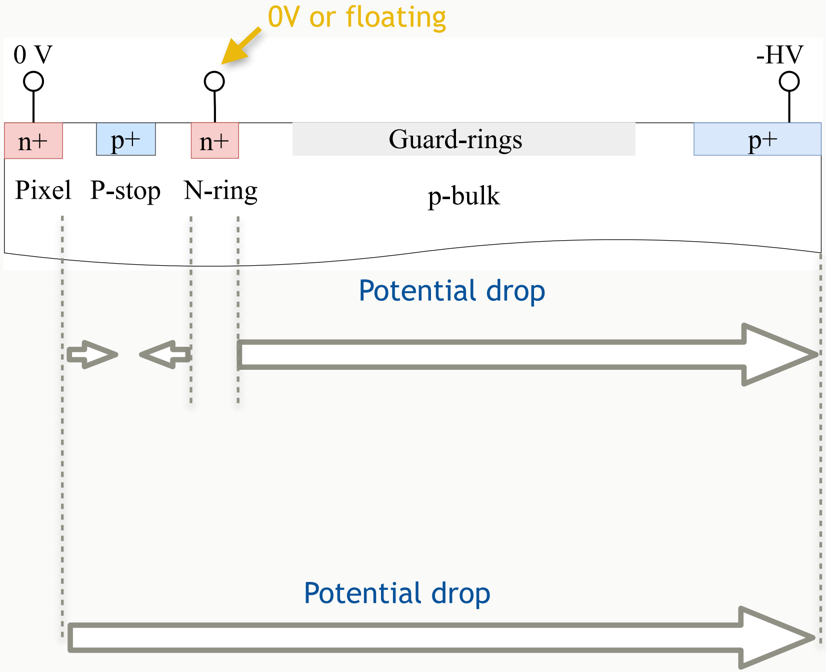
- Implantation type (p or n+p)
- Overhang structure

CHARACTERISATION (1)

- Structures A, B, C, D, F:
  - Floating p-stop

- Grounded n-ring (“default”):
  - Bias voltage across guard rings
  - —> **compare guard ring designs**

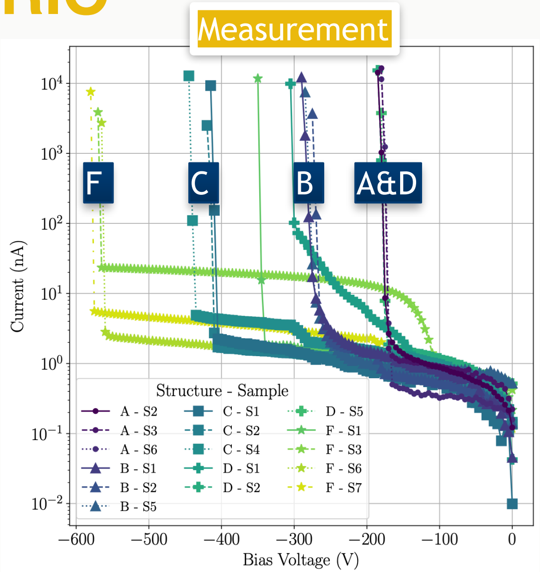
- Floating n-ring:
  - P-stop and n-ring act as GR —> a part of the potential drop (0 to -HV)
  - additional effect of the **deep n-well at the n-ring**

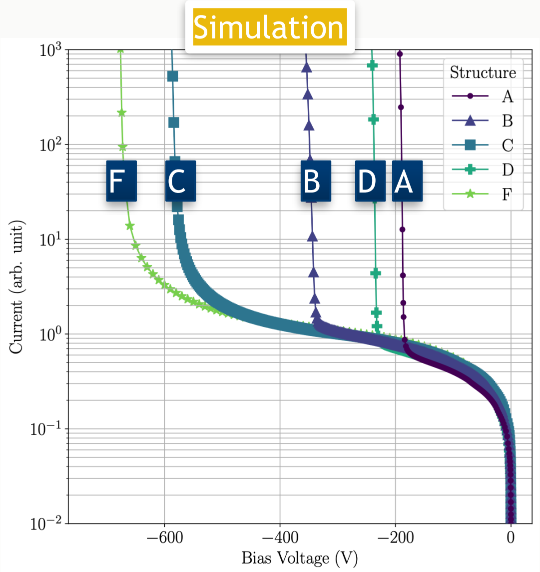


RESULTS FOR GROUNDED N-RING SCENARIO

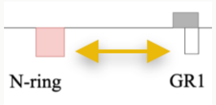
- Measured relations:
  F>C>B>D~A
- Simulation reproduced the relations between test structures
  - Except for A&D

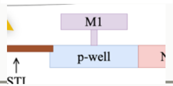
- **Beneficial design features** according to the control group





Control Group	Compared Parameter	Condition for higher breakdown voltage
A & D	Deep implants in the active region	None (–)
B & C	size of GR1 gap	Larger spacing between n-ring and GR1 (C)
B & D	N-implant at the guard rings	With n-implant at the guard rings (B)
C & F	polysilicon overhang	Without polysilicon overhang structure (F)

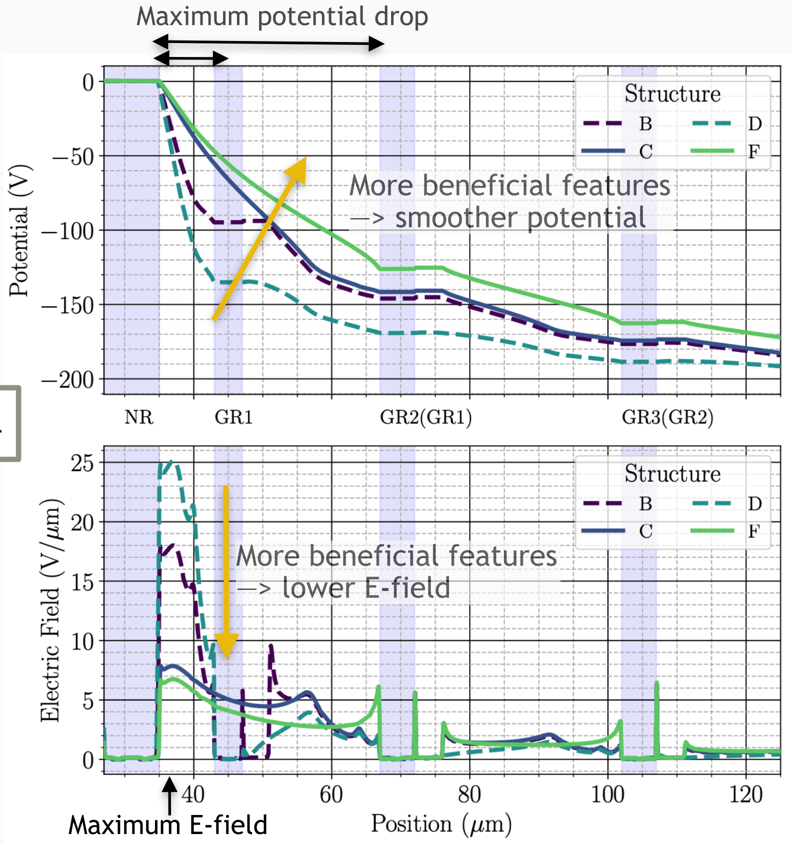




SIMULATION: POTENTIAL AND ELECTRIC FIELD DISTRIBUTION

- Higher E-field —> easier avalanche breakdown
  —> identify and compare the maximum E-field
- Highest potential drop between n-ring & GR1
  - —> Max. E-field at the n-ring reflects the breakdown performance
- Beneficial features smoothen the potential distribution
  - —> reduce the max. E-field
- Structure F:
  - Most beneficial features
  - Highest breakdown voltage
  - —> implemented in DMAPS prototype LF-Monopix2

Pixel

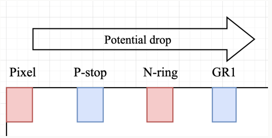


More beneficial features
—> smoother potential

More beneficial features
—> lower E-field

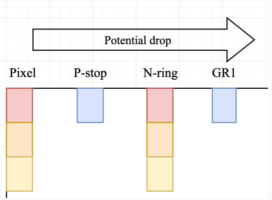
Edge
at -HV

FLOATING N-RING SCENARIO: EFFECT OF DEEP N-WELL



Structure A

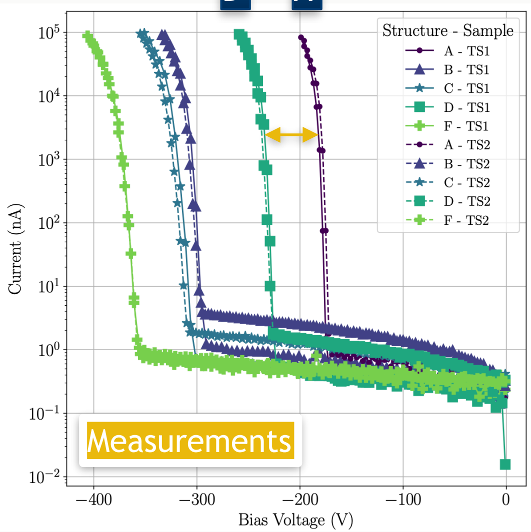
vs.



Structure D

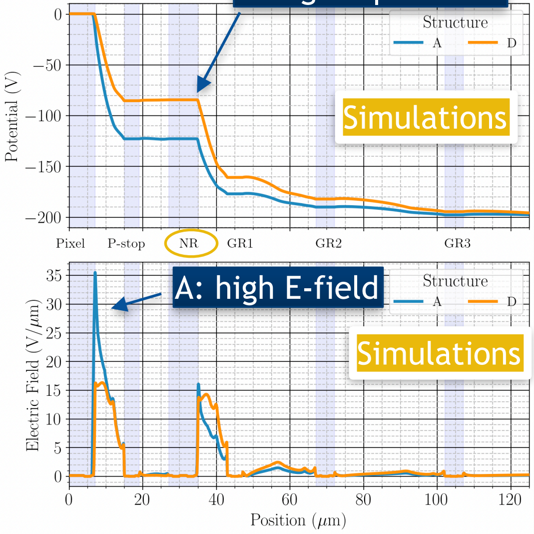
- Breakdown voltage: D > A (both simulations and measurements)
- Max. E-field in A is higher, due to the large potential difference
  —> smaller breakdown voltage
- Floating deep n-well
  —> higher potential than standard n-well
  —> smoother potential distribution
  —> test structures for RD50-MPW3 submission

D A



Measurements

D: deep n-well, higher potential



Simulations

A: high E-field

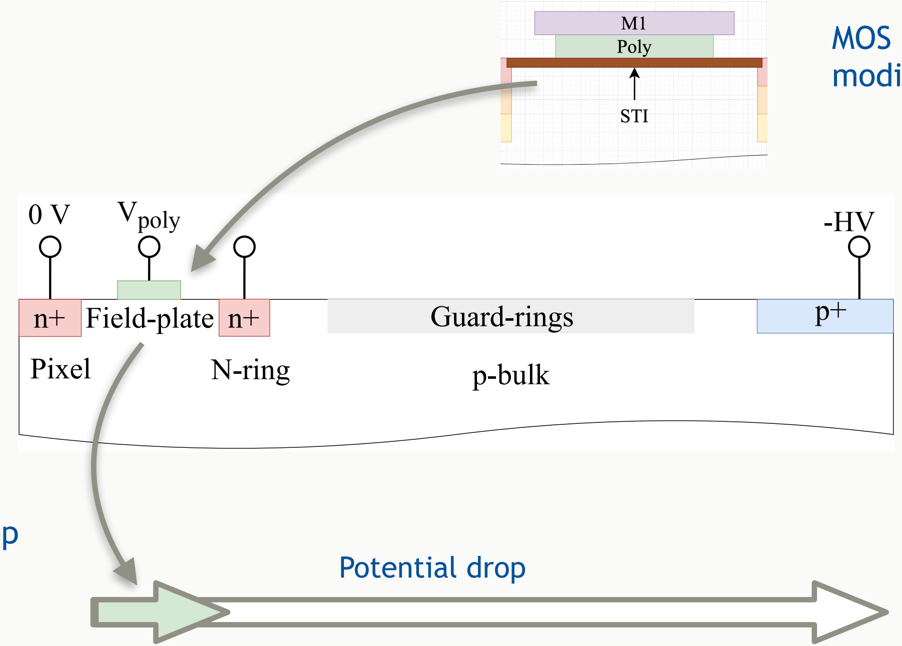
Simulations

CHARACTERISATION (2)

Structure E

- Additional voltage at the field-plate V_{poly}

MOS structure:
modifies the local potential

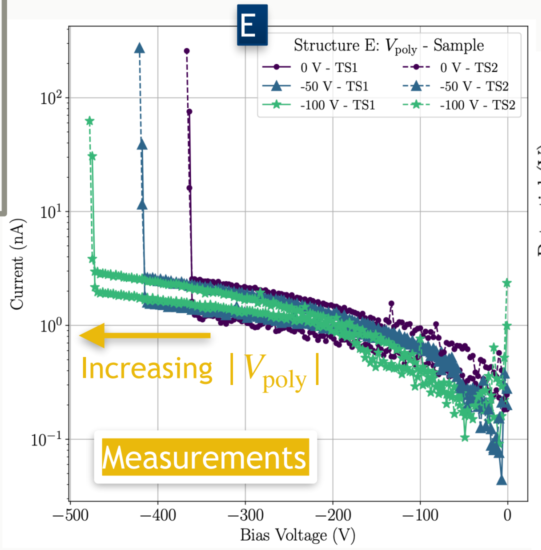


- Focus on floating n-ring:
  —> Field-plate becomes
  a part of the potential drop

—> Influences the breakdown?

FLOATING N-RING SCENARIO: VOLTAGE (V_{poly}) AT THE FIELD-PLATE

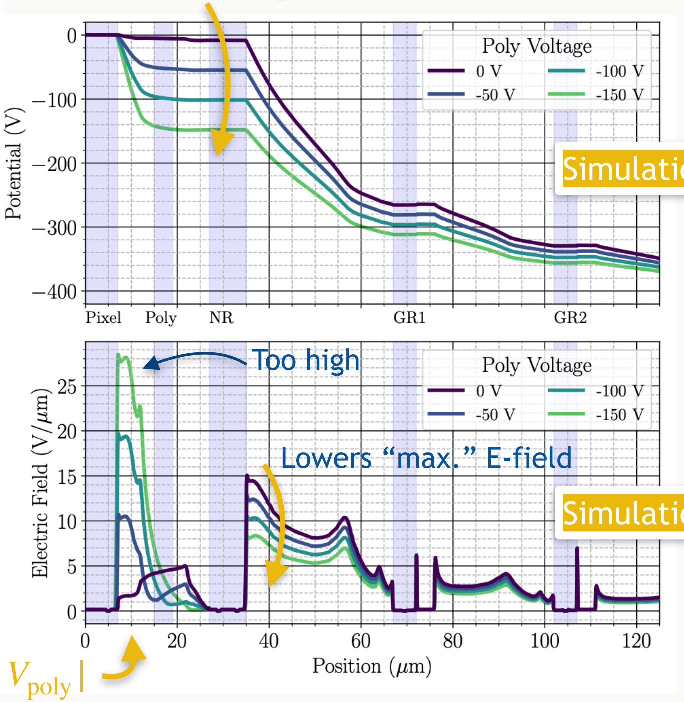
- Structure E (measurements and simulations):
  - $V_{\mathrm{poly}} = 0\,\mathrm{V}, -50\,\mathrm{V}, -100\,\mathrm{V}$ at the the field-plate
    —> increase of breakdown voltage
  - $V_{\mathrm{poly}} = -150\,\mathrm{V}$
    —> early breakdown



Increasing $|V_{\mathrm{poly}}|$

Measurements

Increasing $|V_{\mathrm{poly}}|$



Simulations

Too high

Lowers “max.” E-field

Simulations

Fixed by $|V_{\mathrm{poly}}|$

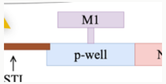
- Potential at the floating n-ring is lowered with ramping bias, and pinned to V_{poly}
- Important E-field peak at
  - Pixel: ↗ with ↗ $|V_{\mathrm{poly}}|$, then **saturates**
  - N-ring: ↘ with ↗ $|V_{\mathrm{poly}}|$, **but ↗ with ↗** $|V_{\mathrm{bias}}|$
    —>“max.” E-field (the candidate)
    —> reduced by $|V_{\mathrm{poly}}|$ leads to higher breakdown voltage
- Large $|V_{\mathrm{poly}}|$ causes too high E-field at the pixel implant —> early breakdown

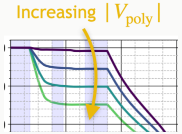
SUMMARY AND CONCLUSION

- The relation between the breakdown performance and the guard ring design for unirradiated case was studied based on 6 passive-CMOS test structures through measurements and simulations

GR design → Optimise → Pot. & E-field distribution → Increase → Breakdown voltage

- Beneficial design features:
  - Large gap between the n-ring and the nearest floating guard ring
  - Use n+p implant. Enhanced by deep n-well
- Overhang:
  - Creates higher electric field —> smaller breakdown voltage
- Field-plate:
  - Applying voltage controls the distributions —> increase the breakdown voltage
    —> test structures with "full poly-rings" have been fabricated

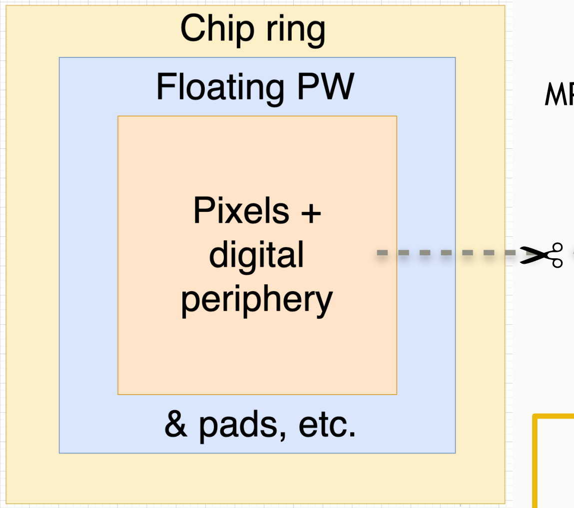




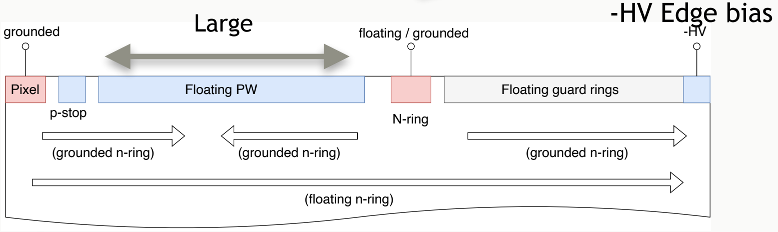
PART 2

BREAKDOWN PERFORMANCE OF THE MPW3

“Floor plan” of MPW3



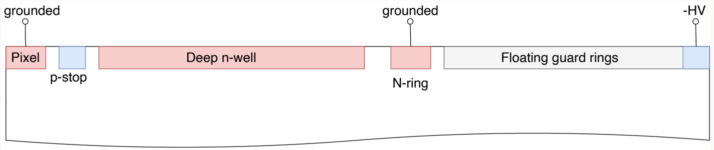
MPW3

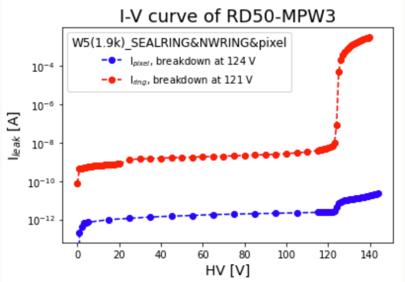


Measurements

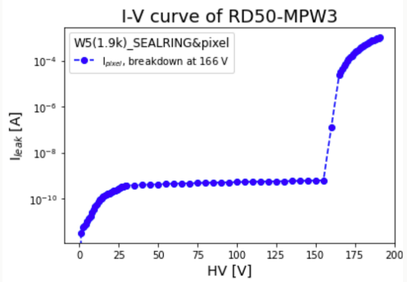
- New chip ring (previous RD50 workshop)
- DNW substitutes PW (this presentation)
- —> higher BDV

MPW4





Grounded n-ring (1)
BDV ~ **120** V



Floating n-ring (2)
BDV ~**150** V

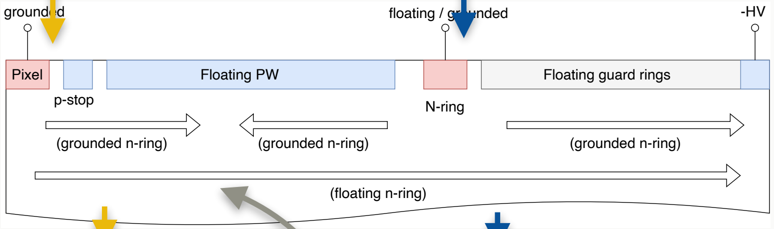
By Chenfan Zhang

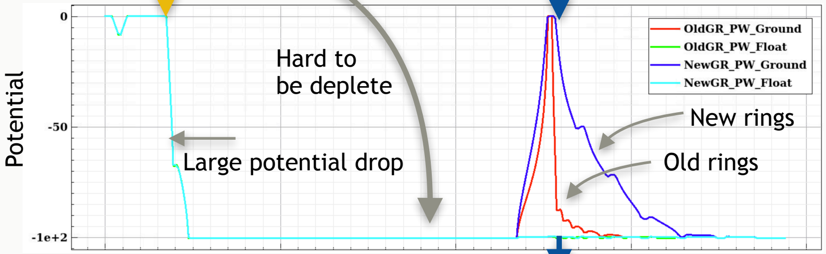
INFLUENCE FROM THE FLOATING PW

- Keep the PW
- old & new guard ring designs, floating & grounded n-ring
- High E-field
    - at the n-ring: for **grounded n-ring**
      —> old chip ring (RD50-MPW3) limits the breakdown
      —> new chip ring in MPW4 solves it
    - at the pixel: in **all cases**
      region under PW hard to be depleted
      —> PW at bias potential, large potential drop
      —> PW determines the similar BDV for all other cases
      (independent of chip ring design)

High field in all cases

High field **when grounded**
Reduced by new GR



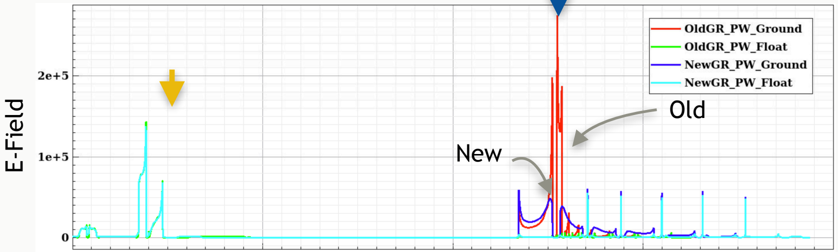


Hard to
be deplete

Large potential drop

New rings

Old rings

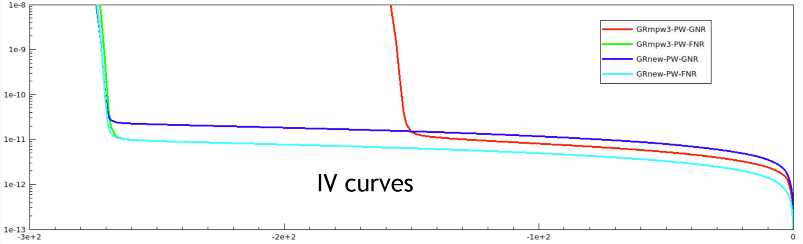


Old

New

Other cases

MPW3 old GR +
grounded n-ring



IV curves

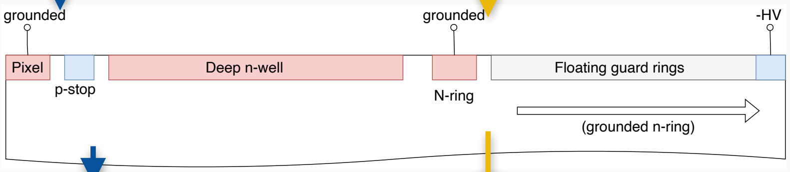
SUBSTITUTE THE PW WITH DEEP N-WELL

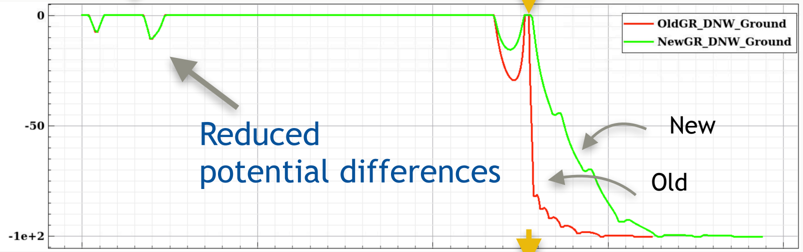
- Use DNW (grounded), grounded n-ring, compare old & new guard ring

- Grounded n-ring & DNW
  - —> regulate the potential between the matrix and the guard rings
  - —> full depletion, and small voltage difference
  - —> guard ring design determines the breakdown

PW: max. field

DNW: max. field

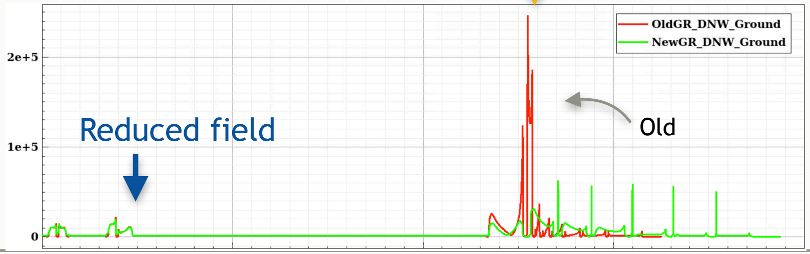




Reduced potential differences

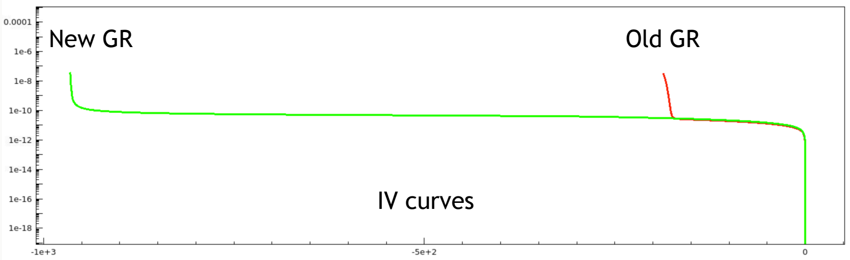
New

Old



Reduced field

Old



IV curves

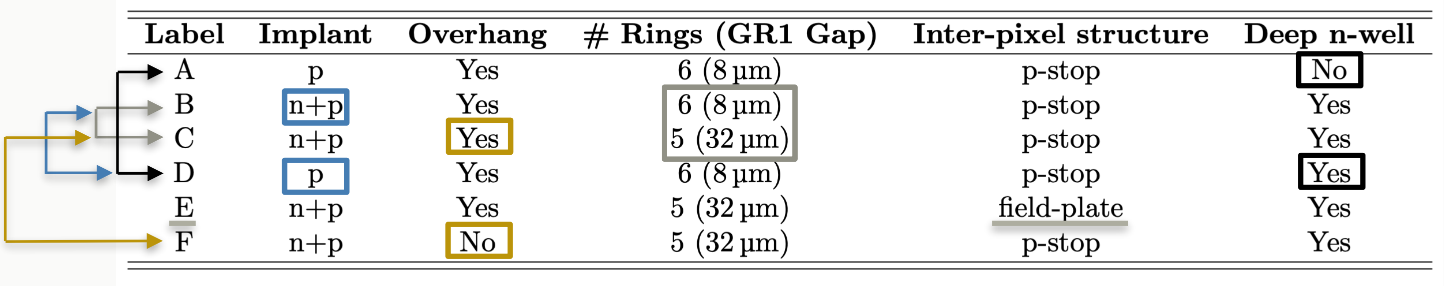
SUMMARY AND CONCLUSION

- Simulation of the breakdown performance of MPW3 and modified structures

- The guard rings and the large floating PW outside the pixel matrix limit the breakdown performance

- Improvements:
  - **New guard ring design:**
    —> smoother potential distribution close to the chip's edge
  - **Grounded DNW** substitute the floating PW:
    —> regulate the potential between the pixel matrix and the guard rings
    —> improve the depletion and reduce the high electric field
- Goal: increase breakdown voltage —> enables larger depletion width

DESIGN FEATURES AND CONTROL GROUPS



Label	Implant	Overhang	# Rings (GR1 Gap)	Inter-pixel structure	Deep n-well
A	p	Yes	6 (8 µm)	p-stop	No
B	n+p	Yes	6 (8 µm)	p-stop	Yes
C	n+p	Yes	5 (32 µm)	p-stop	Yes
D	p	Yes	6 (8 µm)	p-stop	Yes
E	n+p	Yes	5 (32 µm)	field-plate	Yes
F	n+p	No	5 (32 µm)	p-stop	Yes

- 4 control groups
  - A&D: deep n-well
  - B&C: number of rings (the gap size)
  - B&D: n+p implant
  - C&F: overhang

- E: different voltages at the field-plate