RD50 CMOS

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On behalf of many people... (see slides)
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RD50-MPWx chip series
The institutes
The people

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Apologies if I have missed your name... in that case let me know and I will add it

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William Holmkvist
Max Pijacki

Thomas Koffas
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Thomas Koffas

Apologies if I have missed your name... in that case let me know and I will add it
RD50-MPW1 (common project 2017-07)

- **Main goals**
  - To gain expertise, test the process (LFoundry 150 nm HV-CMOS) and test novel designs
  - Process regarded attractive because of HV, nested wells, access to HR wafers in MPW submissions and affordable cost

- **Chip contents**
  - Tests structures for e-TCT and $C_{DET}$ measurements
  - Matrix of depleted CMOS pixels with 16-bit counters
    - 26 x 52 pixels
    - 75 µm x 75 µm pixel area
  - Matrix of depleted CMOS pixels with FE-I3 style readout
    - 40 x 78 pixels
    - 50 µm x 50 µm pixel area
  - Analog and digital readout embedded in the sensing area
  - One LVDS link per matrix
  - Fabricated on 500 Ω·cm and 1.9k Ω·cm wafers
 RD50-MPW1 – Current-to-voltage characteristics

- I-V of central pixel (50 μm x 50 μm)
- Measurement done using a probe station with sensor in complete darkness
- $V_{BD}$~55-60 V as expected from design, but $I_{LEAK}$ was too high
- Despite high $I_{LEAK}$, the chip worked
- The issue was extensively studied: TCAD simulations + support from the foundry (we learned a lot)
RD50-MPW1 – eTCT measurements

- **Test structure**
  - 3 x 3 pixel matrix without readout electronics
  - Central pixel to read out, outer pixels connected together

- **Irradiation**
  - Samples irradiated at TRIGA reactor in Ljubljana (1E13 to 2E5 \(n_{eq}/cm^2\))

- Depletion depth changes with irradiation + acceptor removal effects seen

![Graph showing depletion depth changes with bias voltage and irradiation levels.](image)
DAQ – Caribou (common projects 2021-01, 2023-04)

- **Xilinx Zynq-7000 SoC board**
  - ZC706 (ZC702 possible too)
  - Dual-core ARM Cortex-A9
  - Artix 7 FPGA
  - 2 FMC connectors, GbE, 1 GB DDR3 SDRAM, 128 Mb SPI flash memory, SD card, USB, etc.

- **Control and Readout (CaR) board**
  - Development of Brookhaven National Laboratory
  - Provides common services like power supplies, voltage outputs, ADCs, I2C bus, TLU input, etc.

- **Custom chip board**
  - Provides chip specific features
  - To be developed for each new device
RD50-MPW1

- First prototype was not great...
  - It had bugs

- Circumstances around its R&D...
  - The technology process was new to us and we had to understand it
    - We did it the hard way
  - We developed all the IP from zero
    - This was a lot of work
  - RD50-MPW1 was a version zero chip
    - Yet ambitious chip
      - It implements advanced electronics (analog + digital readout) in a very small pixel cell (50 μm x 50 μm pixel), plus it has a digital interface
  - Small team
ONE STEP AT A TIME..
Towards RD50-MPW2 – Goal to minimise $I_{\text{LEAK}}$

- The issue – what we learned from several discussions with the foundry (*)
  - Structures involving conductive material are added to the design files to prepare them for fabrication (in the pixels, peripheral readout electronics, I/O pads, etc.)
  - These structures contribute quite significantly to the high $I_{\text{LEAK}}$

- The solution – suggested by the foundry
  - Minimise the presence of these structures as much as possible
  - Wherever not possible, place these structures inside a PWELL
The importance of TCAD simulations

Electron current density simulation
Towards RD50-MPW2 – Goal to minimise $I_{\text{LEAK}}$

**The issue**
- Some pixels can be quite close to the edge of the chip
- Defects in silicon lattice due to dicing can become significant
- Leakage current increases when pixel depletion region is near the defect region

**The solution**
- N-type guard ring as safeguard to “collect” leakage current
- P-type guard rings to reduce “chip lateral” depletion
The importance of TCAD simulations

1) Without defects (ideal case)
2) With defects and no guard rings
3) With defects, and n- and p-type rings
4) With defects, and n- and p-type (with deep p) rings
RD50-MPW2 (common project 2019-01)

- **Main goals**
  - To implement solutions to minimise high leakage current observed in RD50-MPW1
  - To test these solutions in a small matrix

- **Chip contents**
  - Tests structures with depleted CMOS pixels
  - Matrix of depleted CMOS pixels
    - 8 x 8 pixels (two pixel flavours)
    - 60 µm x 60 µm pixel area
    - Analog readout embedded in the sensing area
    - Matrix outputs are pixel amplifier and comparator (one pixel at a time), no digital readout
  - SEU tolerant memory array
  - Bandgap reference voltage
  - Test structures with SPADs and depleted CMOS pixels
  - Fabricated on standard, 100 Ω·cm, 1.9k Ω·cm and 3k Ω·cm wafers
RD50-MPW2 – Current-to-voltage characteristics

RD50-MPW2 $\rho = 1100 \ \Omega \text{cm}$

$\rightarrow V_{BD} \uparrow \uparrow$
(PN spacing $\uparrow$)

RD50-MPW1

I\_LEAK $\downarrow \downarrow$

RD50-MPW2
RD50-MPW2 – Crisis

- **Fabrication delay**
  - Chip submitted in early 2019
  - Chip delivered in early 2020
  - Many months delay due to foundry refurbishment

- **Covid**
  - Many RD50-MPW2 measurements produced during lockdowns
  - People had test stands in their living rooms

Sam’s home lab

Klemens + Patrick + Christian at MedAustron in Dec 2020
RD50-MPW2 – Pixel matrix

Bias block
Configuration registers

Continuous reset pixels

Switched reset pixels

Digital readout

Analog readout

2 pixel flavours focused on improving the readout speed
Pixel flavours – Continuous reset

Injection circuit

Amplifier + feedback loop for reset

Trimmable comparator

Source follower output

Comparator output

INJECTION

INJECTION

FB_CONT

-\V

+V

C_FB

CFB

CSA

AMPOUT

SF

SFOUT

HPOUT

trim-DAC

BL

R_BL

CHP

+ Comparator

BL+V_TH

- Comparator

COMPOUT
Pixel flavours – Switched reset

Injection circuit

- Amplifier + feedback loop for reset
- Additional, small current for faster return to baseline

Source follower output

Trimmed comparator

Comparator output
RD50-MPW2 – Lab measurements: matrix electronics

- Many measurements of active pixel matrix
  - In-pixel calibration circuit (S-curves)
  - Pixel gain and noise
  - Trimming DACs
  - Response to radioactive sources
  - At several HV, before and after irradiation

S-curves for all pixels with threshold variation

Trim DAC value 15

Trim DAC values adjusted
RD50-MPW2 – Lab measurements: timing

- **Main goal**
  - To study time-walk dependence on pixel position

- **Method and results**
  - Using edge-TCT setup
  - Measuring in-pixel comparator output
  - Evaluate average charge collection or ToT (L) and timing or ToA (R)

Evaluated volume: 50 µm x 80 µm (W x H), starting 20 µm below the surface
### RD50-MPW2 – Lab measurements: timing

- **Goal**
  - To study matrix and in-pixel time resolution

- **Method**
  - Using edge-TCT setup (back measurements)
  - Measuring rising time of in-pixel comparator output and comparing it against laser pulse

\[
\begin{align*}
\text{σ}_{\text{switched}} &= 211 \pm 45 \text{ ps} \\
\text{σ}_{\text{continuous}} &= 227 \pm 27 \text{ ps} \\

\text{σ}_{\text{switched}} &= 250 \pm 42 \text{ ps} \\
\text{σ}_{\text{continuous}} &= 267 \pm 56 \text{ ps}
\end{align*}
\]

Switched reset pixels have slightly better time resolution.

Better time resolution under collection well.
RD50-MPW2 – Lab measurements: timing

- **Goal**
  - Timing measurements with 90Sr source

- **Method**
  - Reference signal from 1 mm x 1 mm LGAD detector behind the CMOS chip
  - Trigger: sample + LGAD
  - LGAD jitter of ~30 ps negligible in comparison with jitter of CMOS pixel
  - Low rate: ~1 event/min with 18 MBq source
RD50-MPW2 – Used with TPA laser

- **Goal**
  - To study pixel matrix and setup equipment

- **Method**
  - High precision xy probing of in-pixel structure
  - Detailed map of the electric field
RD50-MPW2 – Test beams with protons

- **Main goals**
  - To integrate RD50-MPW2 into test beam data acquisition system and evaluate the chip with a particle beam

- **Methods**
  - Switched reset pixel
    - ToT in simulations ~30 ns (for all energies)
  - Standalone firmware (counter in FPGA)
  - Double sided silicon strip detectors as trigger
  - Triggered by coincidence with AIDA-TLU

Measurements (800 MeV protons) → in good agreement with simulations
RD50-MPW2 – Test beam with ions

- At RBI in Zagreb (ion microbeam facility)
  - To see SEU events
  - To measure pixel CCE
KEEP CALM AND LET'S MOVE ON
Test rings

64 X 64 pixel matrix

Digital periphery
RD50-MPW3 (common project 2021-04)

- **Main goals**
  - To extend the number of pixels in the active matrix to perform advanced measurements (e.g. test beams)
  - On-chip in-pixel column drain digital readout electronics (FE-I3 style)
  - On-chip digital periphery for effective pixel configuration and fast data transmission

- **Chip contents**
  - Matrix of depleted CMOS pixels with FE-I3 style readout
    - 64 x 64 pixels
    - 62 \(\mu\)m x 62 \(\mu\)m pixel area
    - Analog and digital readout embedded in the sensing area
    - Double column scheme to alleviate routing congestion and minimise crosstalk
    - Digital periphery with I2C, Wishbone bus and one LVDS link
  - Tests structures (top band with chip rings, e-TCT, DLTS)
  - Fabricated on standard, 1.9k \(\Omega\cdot\)cm and 3k \(\Omega\cdot\)cm wafers
Pixel layout

Double column scheme to alleviate routing congestion and minimise crosstalk
Towards RD50-MPW3 – The hidden things

- **Cadence Design Share Agreement**
  - Agreement between Cadence and organisations who wish to share Cadence produced design files between them (managed by Europractice)
  - It took us one year to understand how it works
  - The agreement uses a bi-directional all-connected topology
    - n institutes $\rightarrow$ n*(n-1) Design Share Agreements
    - 7 design institutes in RD50-MPW3 $\rightarrow$ 42 agreements!
  - The agreement model changed after RD50-MPW3

- **Cliosoft SOS repository**
  - Software integrated within Cadence for sharing design files between remote organisations
  - We use it for analogue design files and all layout views
  - We set up a SOS server, to which all the remote organisations connect

- **GitLab repository**
  - We use it for digital design files and all layout views
  - And also for DAQ firmware and software
RD50-MPW3 – Test beams

- **Main goals**
  - To integrate RD50-MPW3 into reference system while enabling synchronisation between the chip and AIDA2020 TLU
  - To evaluate the chip with a particle beam
  - To form an effective RD50 CMOS test beam crew

- **Methods and results**
  - CERN SPS (120 GeV electrons and pions)
  - Mimosa-26 planes controlled by EUDAQ2
  - Autumn 2022
  - High threshold voltage due to high noise especially for those pixels that are near the digital periphery (and synchronisation problem in the DAQ)
  - Average chip efficiency ~60%
RD50-MPW3 – Test beams

- **Main goals**
  - To evaluate the chip (with an improved DAQ) with a particle beam
  - To evaluate irradiated samples (1E14 n_{eq}/cm^2)

- **Methods and results**
  - DESY (4.2 GeV electrons)
  - Adenium telescope
  - Summer 2023
  - High noise half matrix was ignored
  - Synchronisation issue was solved
  - Average chip efficiency \sim 98.3% (before irradiation)
  - (other test beams at MedAustron)
RD50-MPW3 – Test beam team

CERN, autumn 2022

DESY, summer 2023
The importance of post-layout simulations

- Simulated analogue output signals of pixels from different locations
  - **Left** The pixel matrix and readout periphery share the same digital power and ground
  - **Right** The digital power and ground of the pixel matrix and periphery are separated
RD50-MPW4 (common project 2023-02)

- **Main goals**
  - To further improve the current-to-voltage-characteristics
    - Much higher $V_{BD}$ (and much higher radiation tolerance)
    - New chip ring frame (test structure in RD50-MPW3)
    - Chip substrate biasing with topside edge contacts or backside contacts
  - To achieve low-noise by separating the digital in-pixel and digital peripheral power and ground domains
  - To reduce the size of the digital periphery
  - To fix small design bugs

- **Chip contents**
  - Matrix of depleted CMOS pixels with FE-I3 style readout
  - Tests structures (e-TCT, DLTS)
  - Fabricated on standard and 3k $\Omega\cdot$cm wafers
  - Backside biasing is possible

*To be delivered very soon... stay tuned!*
FULL-SIZE SUBMISSION FOR ATLAS ITK

- Frontside process: Reticule stitching for large sensors
- Wafers received backside processing
- 150 um thick Float-Zone wafers instead of Czechralski wafers

Not only pixel sensors, also strip sensors: Talk by Jan Cedric Honig

Work done with: A. Macchiolo, D. Münstermann, M. Backhaus

28.11.2023 – Last (43rd) RD50 Workshop @ CERN

IV-CURVES: FULL-SIZE ATLAS ITK SENSORS

- Had issue with backside processing leading to increase of current when depletion zone touches the backside

Solved by increasing the implant-dose of backside implant:
- Keeps depletion zone away from damaged silicon at backside
- $V_{dep} \sim 30\,\text{V} (<100\,\text{V}, \text{for } 150\,\text{um})$
- $I_{leak} < 0.75\,\mu\text{A/cm}^2 \times 80\,\text{V} (V_{dep} + 50\,\text{V})$
- $V_{break} \sim 200-180\,\text{V} (>V_{dep} + 70\,\text{V})$
- Sensors fulfill specifications

- Measurements on irradiated samples will be performed soon

Example IV-curve

0.75 \mu A/cm^2

0 25 50 75 100 125 150 175 200
Voltage / V

0 10^{-8} 10^{-7} 10^{-6} 10^{-5} 10^{-4}
Current / mA

LATEST MONOPIX PROTOTYPES

TJ-Monopix2:
- 180 nm TowerSemi CMOS technology
- Small collection electrode
- 2x2 cm² matrix with 33x33 μm² pixel pitch
- Substrate resistivity > 1 kΩcm

Same fast column drain readout architecture (FE-I3 like)

LF-Monopix2:
- 150 nm LFoundry CMOS technology
- Large collection electrode
- 2x1 cm² matrix with 50x150 μm² pixel pitch
- Substrate resistivity > 2 kΩcm

28.11.2023 – 43rd RD50 Workshop
Summary

- 4 monolithic CMOS pixel chip prototypes + 1 DAQ (Caribou, and new Caribou)
- 17 institutes worldwide and approx. 50 people
- Fruitful relationship with the manufacturer, and we have contributed to develop the design kit
- New Cadence Design Share Agreement model
- One test beam at CERN, one at DESY, and several at medical facilities
- 34 RD50-MPWx presentations in RD50 Workshops, plus many other presentations at conferences
- 12 peer-reviewed publications (+2 under review, + others in preparation)
- Countless meetings and emails
- Several PhD and undergraduate students: Ana Catalán, Jernej Debevc, Daniel Domenech, Fabian Förster, Klemens Flöckner, Matt Franks, Lukas Haider, William Holmkvist, Bernhard Pilsl, Sam Powell, Lingxin Meng, Thijs Niemeijer, Douwe Nobels, Patrick Sieberer, Christina Tsolanta, Chenfan Zhang
- Collaborative RD50 spirit… some groups have contributed with design, others with DAQ, others with measurements, others with skills and knowledge or access to specialised instrumentation, some groups with several things... everybody has always been welcome... together we have reached where we are today... thanks everyone 😊
Yes, we did it!

Yes, I did it!

I will do it
I can do it
I’ll try to do it
How do I do it?
I want to do it
I can’t do it
I won’t do it

Which step have you reached today?
Back up slides
## RD50-MPWx chip series – Overview

<table>
<thead>
<tr>
<th>Parameter</th>
<th>RD50-MPW1</th>
<th>RD50-MPW2</th>
<th>RD50-MPW3</th>
<th>RD50-MPW4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device size [mm x mm]</td>
<td>5 x 5(1)</td>
<td>3.2 x 2.1</td>
<td>5.1 x 6.6</td>
<td>5.4 x 6.3</td>
</tr>
<tr>
<td>Pixel matrix size</td>
<td>40 x 78</td>
<td>8 x 8</td>
<td>64 x 64</td>
<td>64 x 64</td>
</tr>
<tr>
<td>Pixel size [µm x µm]</td>
<td>50 x 50</td>
<td>60 x 60</td>
<td>62 x 62</td>
<td>62 x 62</td>
</tr>
<tr>
<td>P-n spacing [µm]</td>
<td>3</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>In-pixel electronics</td>
<td>Analogue Digital</td>
<td>Analogue</td>
<td>Analogue Digital</td>
<td>Analogue Digital</td>
</tr>
<tr>
<td>Output data</td>
<td>Pixel address</td>
<td>Binary</td>
<td>Pixel address</td>
<td>Pixel address</td>
</tr>
<tr>
<td></td>
<td>Time-stamp</td>
<td></td>
<td>Time-stamp</td>
<td></td>
</tr>
<tr>
<td>Digital periphery</td>
<td>78 EOCs</td>
<td>8 EOCs</td>
<td>32 EOCs, with 32-events</td>
<td>32 EOCs, with 16-events</td>
</tr>
<tr>
<td></td>
<td>2 LVDs lines</td>
<td></td>
<td>24-bit FIFOs</td>
<td>24-bit FIFOs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>128-events 32-bit TX FIFOs</td>
<td>64-events 32-bit TX FIFOs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>I2C</td>
<td>I2C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Wishbone bus</td>
<td>Wishbone bus</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 LVDs line</td>
<td>1 LVDs line</td>
</tr>
</tbody>
</table>

(1) Half of the chip has a pixel matrix for applications beyond physics.
## RD50-MPWx chip series – Overview

<table>
<thead>
<tr>
<th>Parameter</th>
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<th>RD50-MPW3</th>
<th>RD50-MPW4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Chip guard ring frame</strong></td>
<td>None</td>
<td>1 n-ring</td>
<td>1 n-ring</td>
<td>1 n-ring</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6 p-rings</td>
<td>6 p-rings</td>
<td>5 n-/p-rings</td>
</tr>
<tr>
<td><strong>Substrate biasing</strong></td>
<td>Through p-stop contacts</td>
<td>Through p-stop contacts</td>
<td>Through p-stop contacts</td>
<td>Through chip edge or backside</td>
</tr>
<tr>
<td><strong>Substrate resistivity</strong></td>
<td>0.5 – 1.1</td>
<td>Standard</td>
<td>Standard</td>
<td>Standard</td>
</tr>
<tr>
<td>[kΩ·cm]</td>
<td>1.9</td>
<td>0.2 – 0.5</td>
<td>1.9</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3</td>
</tr>
<tr>
<td><strong>Device thickness [µm]</strong></td>
<td>280</td>
<td>280</td>
<td>280</td>
<td>280</td>
</tr>
<tr>
<td><strong>V_{BD} [V]</strong></td>
<td>56</td>
<td>120</td>
<td>120</td>
<td>500(^{(2)})</td>
</tr>
<tr>
<td><strong>I_{LEAK} [µA/pixel]</strong></td>
<td>1</td>
<td>1E-4</td>
<td>1E-6</td>
<td>1E-6(^{(2)})</td>
</tr>
<tr>
<td><strong>Depletion depth [µm]</strong></td>
<td>118</td>
<td>110</td>
<td>Not tested</td>
<td>Fully depleted(^{(2)})</td>
</tr>
<tr>
<td><strong>ENC [mV]</strong></td>
<td>50</td>
<td>2</td>
<td>&lt; 140, &gt; 50</td>
<td>&gt; 50(^{(2)})</td>
</tr>
<tr>
<td><strong>Efficiency [%]</strong></td>
<td>Not tested</td>
<td>Not tested</td>
<td>&gt; 98</td>
<td>&gt; 99(^{(2)})</td>
</tr>
</tbody>
</table>

\(^{(2)}\)Anticipated values for RD50-MPW4
Process and sensor cross-section

- **150 nm HV-CMOS LFoundry**
  - P-substrate/DNWELL sensing junction
  - Pixel readout electronics embedded inside DNWELL
  - CMOS electronics in sensing diode & isolated from DNWELL with PSUB
Pixel electronics

- **Column drain architecture (FE-I3 style)**
- **Electronics to**
  - Mask noisy pixels (MASK)
  - Possibility to pause digitisation of new hits until readout is complete (FREEZE)
  - 8-bit SRAM shift register for serial configuration
    - Pixel-trimming to compensate for threshold voltage variations (4-bits)
    - Flag to mask noisy pixels (1-bit)
    - Signals to enable/disable calibration circuit (1-bit), SFOUT (1-bit), COMPOUT (1-bit)
Digital periphery

- **End-Of-Column (EOC) architecture**
  - FIFO stores hit data (LE TS, TE TS and ADDR)
  - FSM reads double column
  - Token mechanism to determine which EOC is read out

- **Readout**
  - Pixel is read out immediately after hit (if FIFO is not full)
  - CU reads EOCs sequentially
  - Data stored temporarily in TX FIFO
  - Data TX unit with LVDS port @ 640 Mbps

- **Slow control**
  - Based on I2C protocol for external communication using internal Wishbone bus
RD50-MPW3 – I-V measurements

- Measurement using probe station with needles
- $V_{BD} > 120 \text{ V}$ ($V_{BD} > 300 \text{ V}$ in RD50-MPW4)
- $I_{LEAK}$ per pixel in pA range before breakdown
RD50-MPW3 – Lab results

- High noise due to coupling effects (solved in RD50-MPW4)
- Pixel gain measured to be 82.9 μV/e⁻