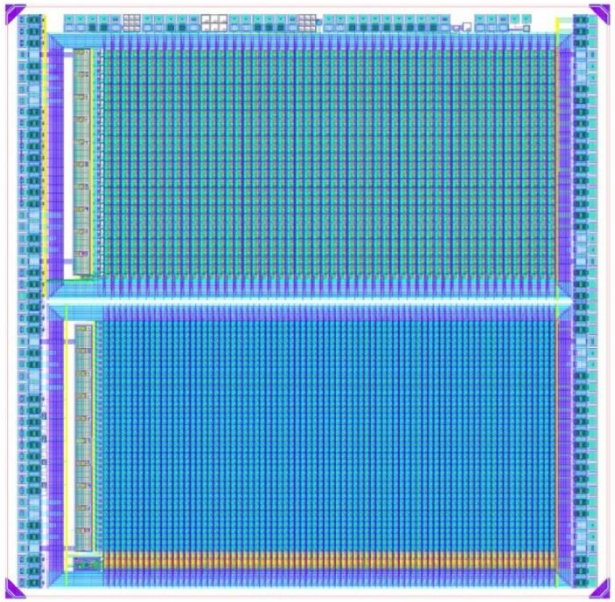
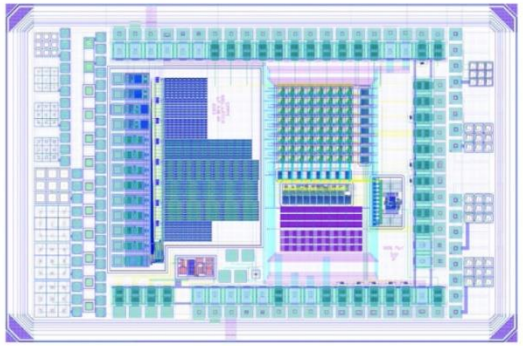
RD50-MPWx chip series

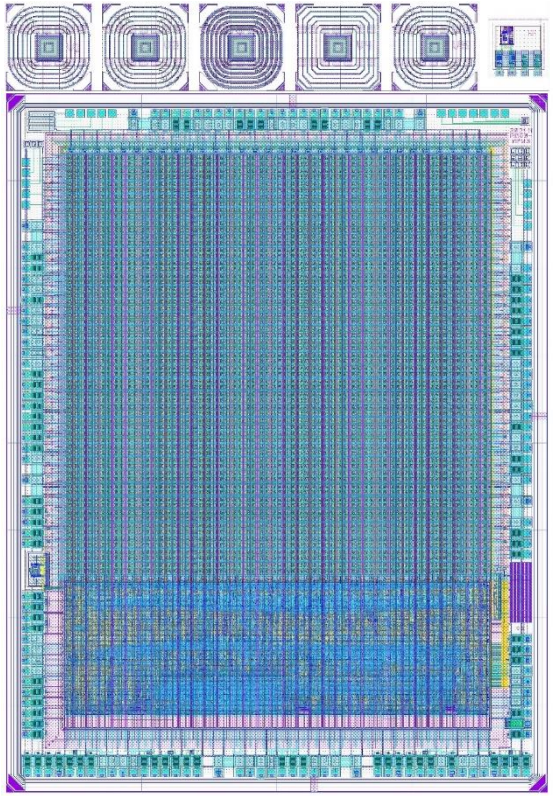
RD50-MPW1



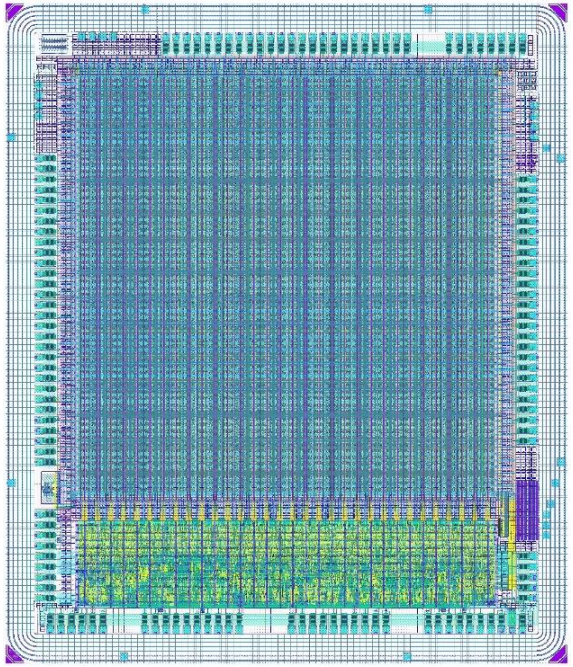
RD50-MPW2



RD50-MPW3



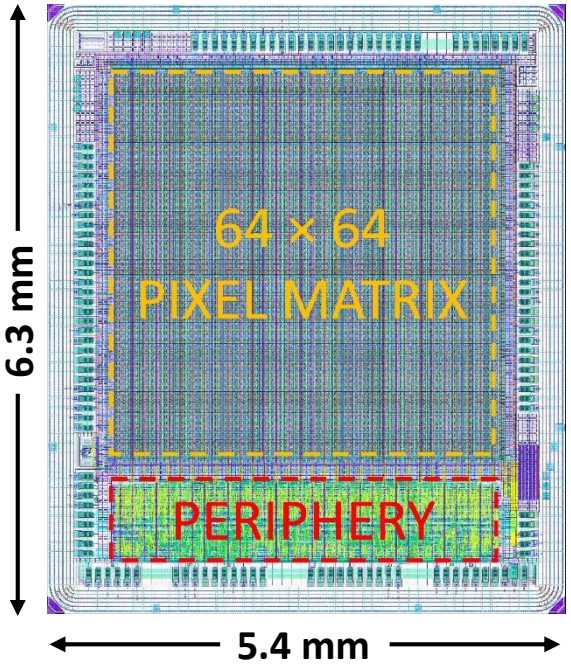
RD50-MPW4

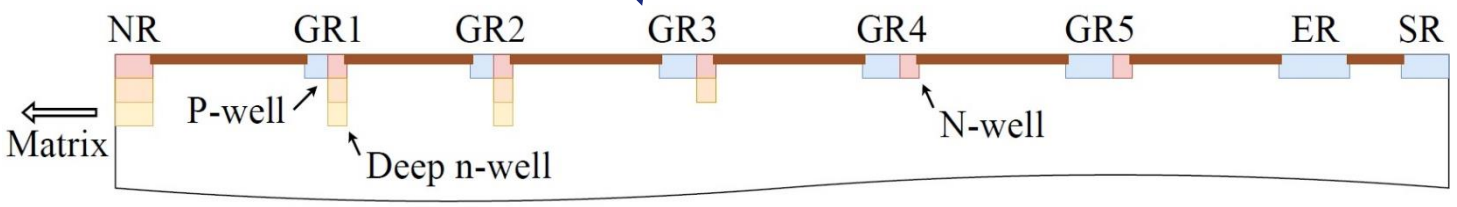


2017 2018 2019 2020 2021 2022 2023 +

RD50-MPW4 (common project 2023-02)

- **Main goals**
  - To further improve the current-to-voltage-characteristics
    - Much higher V_BD (and much higher radiation tolerance)
    - New chip ring frame (test structure in RD50-MPW3)
    - Chip substrate biasing with topside edge contacts or backside contacts
  - To achieve low-noise by separating the digital in-pixel and digital peripheral power and ground domains
  - To reduce the size of the digital periphery
  - To fix small design bugs





- **Chip contents**
  - Matrix of depleted CMOS pixels with FE-I3 style readout
  - Tests structures (e-TCT, DLTS)
  - Fabricated on standard and 3k Ω·cm wafers
  - Backside biasing is possible

To be delivered very soon… stay tuned!

RD50-MPW4 (common project 2023-02)

- We expect to receive topside biased samples before the end of the year…
- and backside biased samples some time in the new year
- The production of the chip carrier board is ongoing, and we think it will be ready to start measuring the chip once this is delivered
- We have requested beam time in spring at DESY
  - If people want to contribute with lab measurements
  - Or join our test beam campaign(s)
  - Please get in touch!