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Gallium Nitride for Radiation Hard Sensors

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Carleton University, Ottawa, ON, Canada
RD50 Workshop
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NRC works through collaboration

- 3,700 scientists, engineers, technicians, client relations experts and other specialists, including 255 SME technology advisors
- Manages 178 buildings in 72 locations across the country
- >$1B annual expenditure, including $271M in contribution funding for SMEs

Last year we worked with

- 4500 SMEs (advice)
- 3500 SMEs (funding)
- 1000 companies (R&D collaborations)
- 152 hospitals
- 72 colleges and universities
- 34 federal departments
- 39 provincial/municipal departments
- 36 countries

Advanced Electronics & Photonics Research Centre

Canadian Photonics & Fabrication Centre (CPFC)

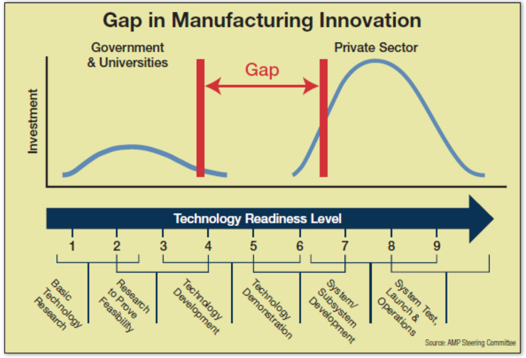
- Pure-play foundry for 3” & 4” wafers
  - 10-100’s of wafers per month (InP & GaAs)
  - Operates 2 multi-wafer MOCVD reactors (3 and 12 wafers)
  - Strong epitaxial growth of bulk and quantum structures

Advanced Technology Facility for R&D

- Newer technologies, proof of concept demonstration including GaN and GaSb processing

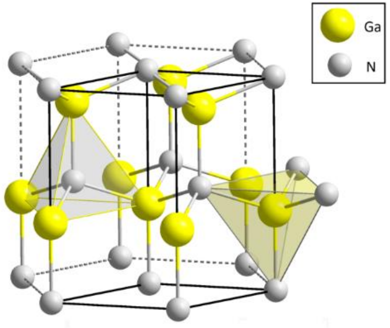
Materials & Devices

- Epitaxy (CBE, MBE), organics, *electronics*, photonics, systems & integration, thin-film optical coatings



Source: AMP Steering Committee

GaN as a Radiation Hard Material for Sensing



Wide (direct) bandgap semiconductor (3.4 eV) with a wurtzite crystalline structure

High atomic bond energy (~9 eV/atom)

High bulk electron mobility (up to 2000 cm^2/Vs)

- Even with high electron conc in 2DEG in GaN/AlN structures

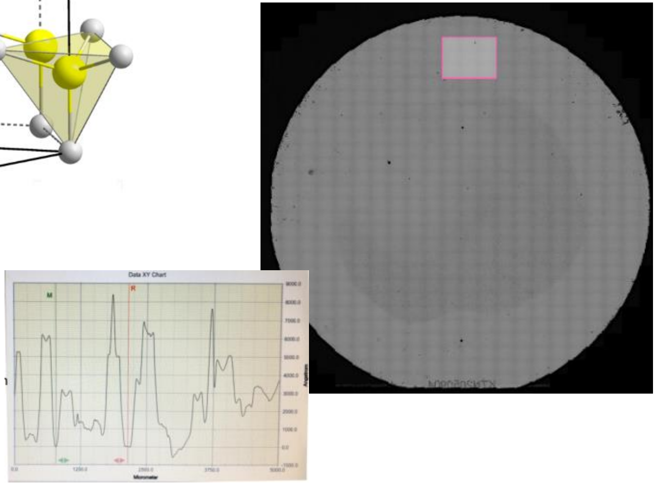
High breakdown voltage (600-1200 V/µm)

High power density and faster switching speed compared to silicon → power electronics

However, less mature technology, typically with high dislocation density >1E6 cm^2

Goal of project to fabricate GaN Schottky devices using 8 µm GaN epi-layer on a n+GaN native substrate

kyma technologies

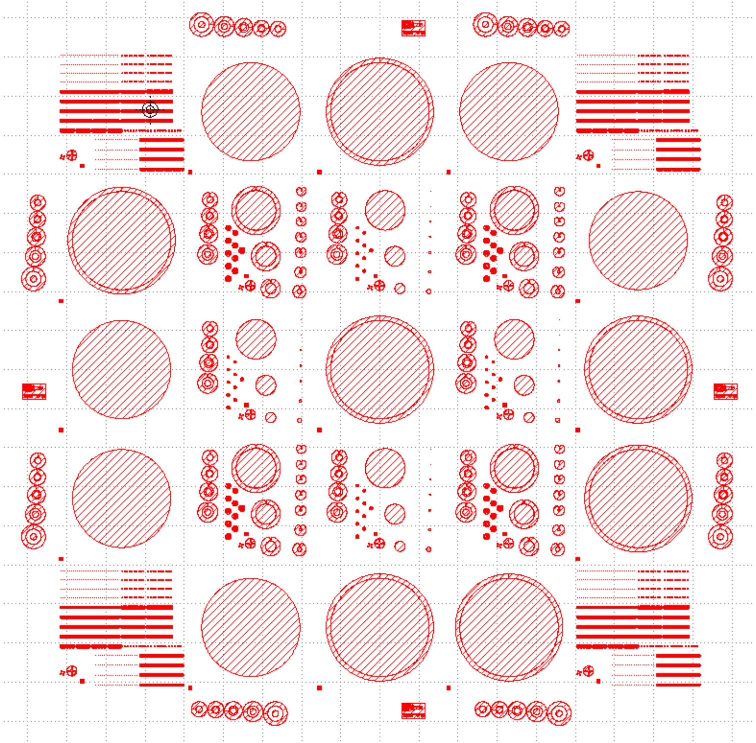


Continuation of previous work presented at RD50 Workshop in June 2022 by J-P Noel

Processing Target Devices

Initial processing plan on 2” Kyma wafer:

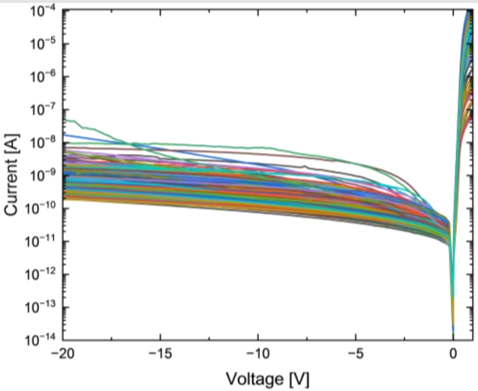
- **Deposit rear-side Ohmic metal with high temperature anneal**
- **Deposit front-side Schottky metal to test rectification behavior**
  - Ni/Au Schottky metal with ~0.8 eV barrier after rapid thermal anneal
  - Variable area devices with & without guard rings to suppress surface leakage
  - Ring devices for charge collection



Basic Electrical Characterization

Summit 1200 Cascade probe station for automated measurements → statistics!

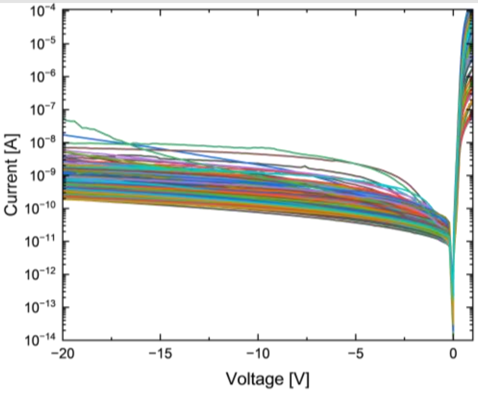
- Agilent 4155C Semiconductor Parameter Analyzer for I-V

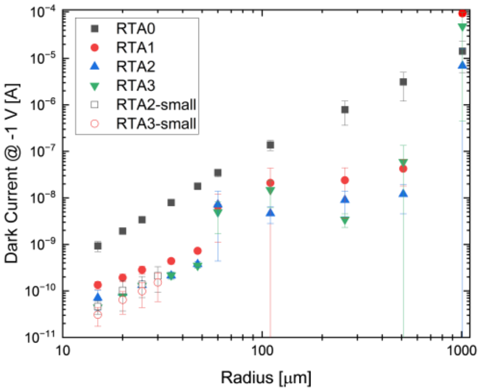


Basic Electrical Characterization

Summit 1200 Cascade probe station for automated measurements → statistics!

- Agilent 4155C Semiconductor Parameter Analyzer for I-V
  - Evaluate impact of rapid thermal anneal on dark current

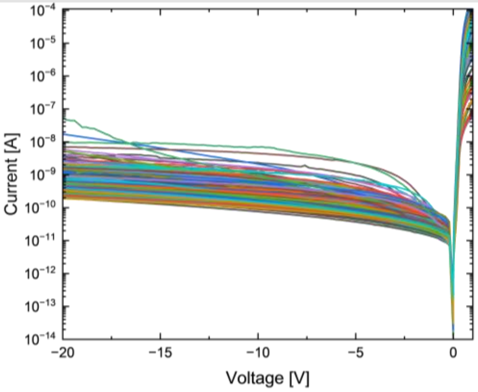


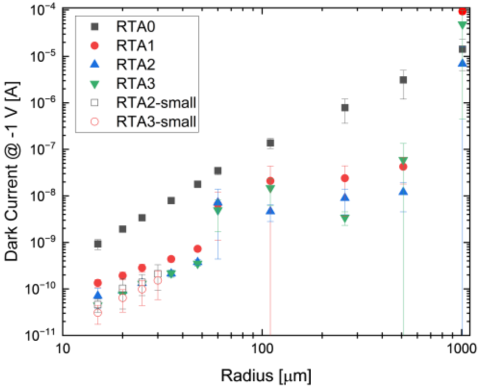


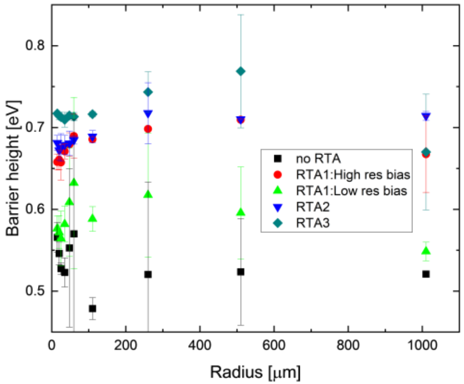
Basic Electrical Characterization

Summit 1200 Cascade probe station for automated measurements → statistics!

- Agilent 4155C Semiconductor Parameter Analyzer for I-V
  - Evaluate impact of rapid thermal anneal on dark current and on Schottky barrier height



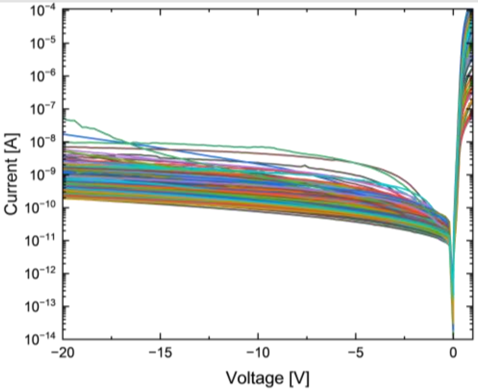


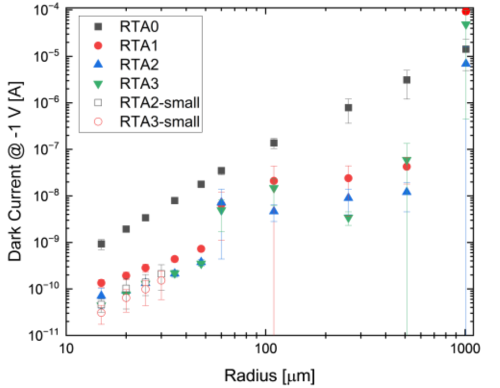


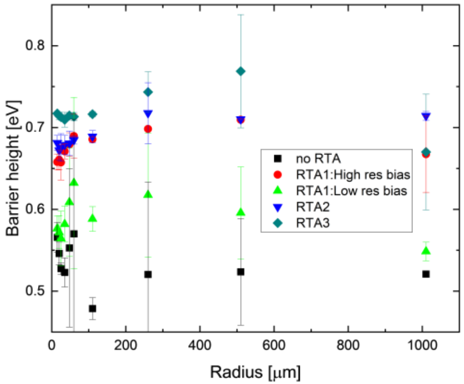
Basic Electrical Characterization

Summit 1200 Cascade probe station for automated measurements → statistics!

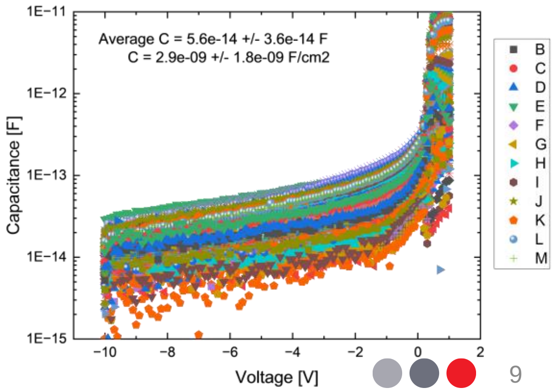
- Agilent 4155C Semiconductor Parameter Analyzer for I-V
  - Evaluate impact of rapid thermal anneal on dark current and on Schottky barrier height
- Agilent 4284A Precision LCR meter for C-V
  - Evaluate carrier concentrations







Filtered D50: removed 12 devices out of 160 for a yield of 92.5.



Impact of RTA on Unguarded Device Leakage

Plotting current density vs perimeter/area reveals bulk and surface contributions for *unguarded* devices

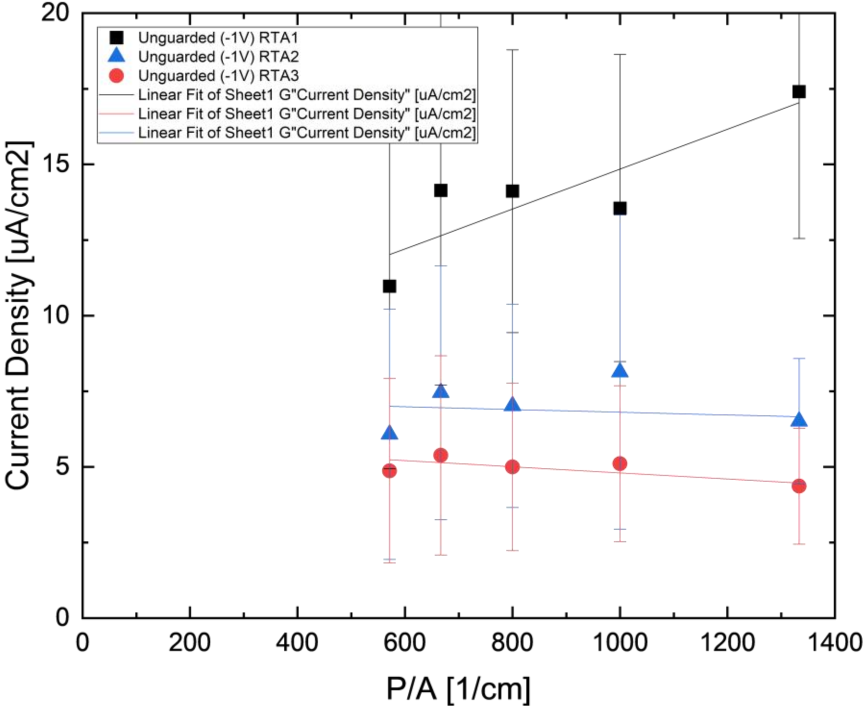
$$J = J_{perim} \times P/A + J_{bulk}$$

Each data point has >100 devices

Shows a clear decrease in perimeter contributions for increasing RTA

- Note that no RTA data are outside range

Bulk contributions are in agreement (within uncertainty)



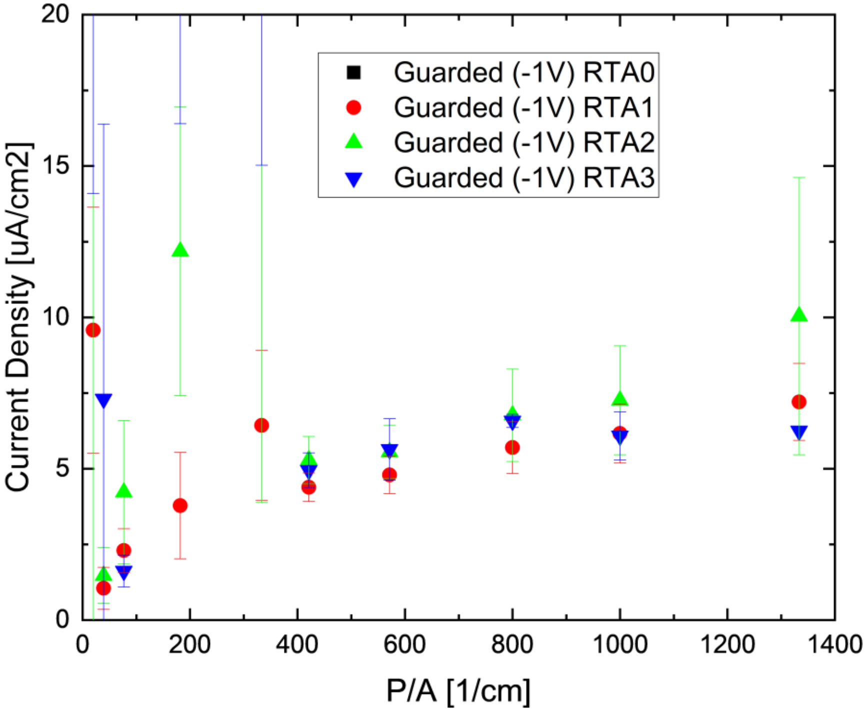
Impact of RTA on Guarded Schottky Devices

Scales are identical to previous plot

Data agrees with unguarded data from previous slide

- But statistics are not sufficient: 4 devices per data point

RTA has minor impact on bulk dark current contributions once surface effects are effectively inhibited by guard ring



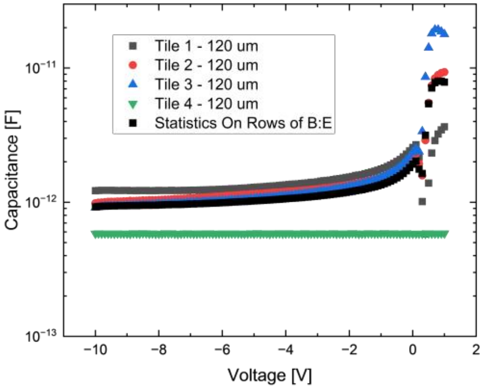
Carrier Concentrations from C-V

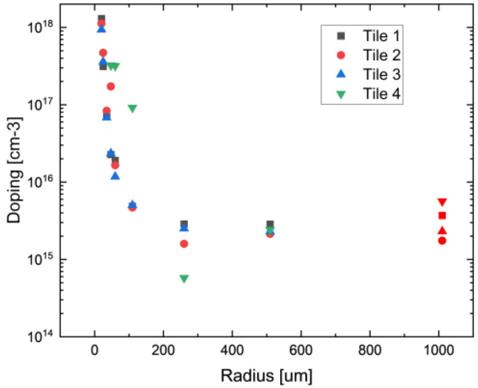
One area of wafer demonstrated no capacitance signal (tile 4)

- Devices showed low forward bias current

$1/C^2$ analysis reveals low carrier concentrations in the low 10^{15} cm^{-3} range, as expected from Kyma

- Small area devices show higher capacitance than expected
  - Fringe effects from large perimeter contributions → need simulations to confirm

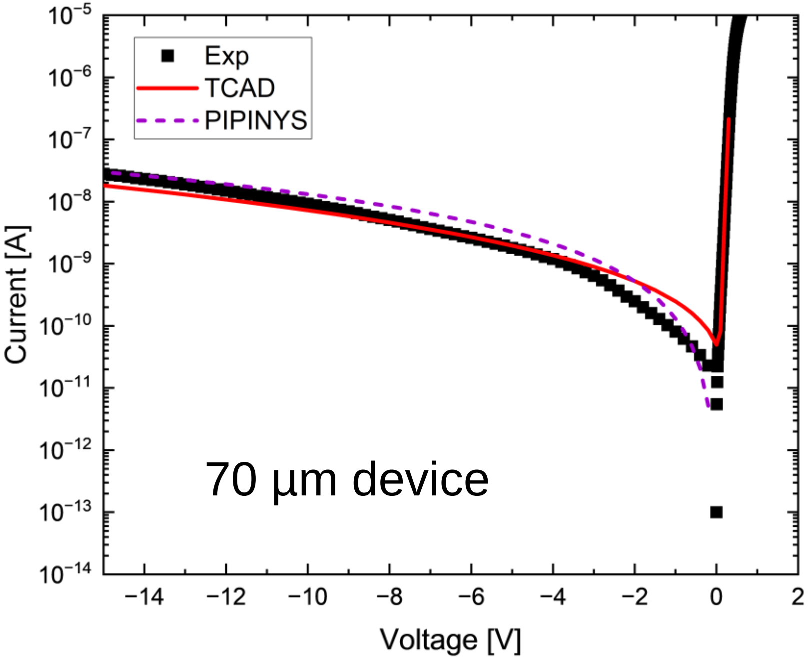




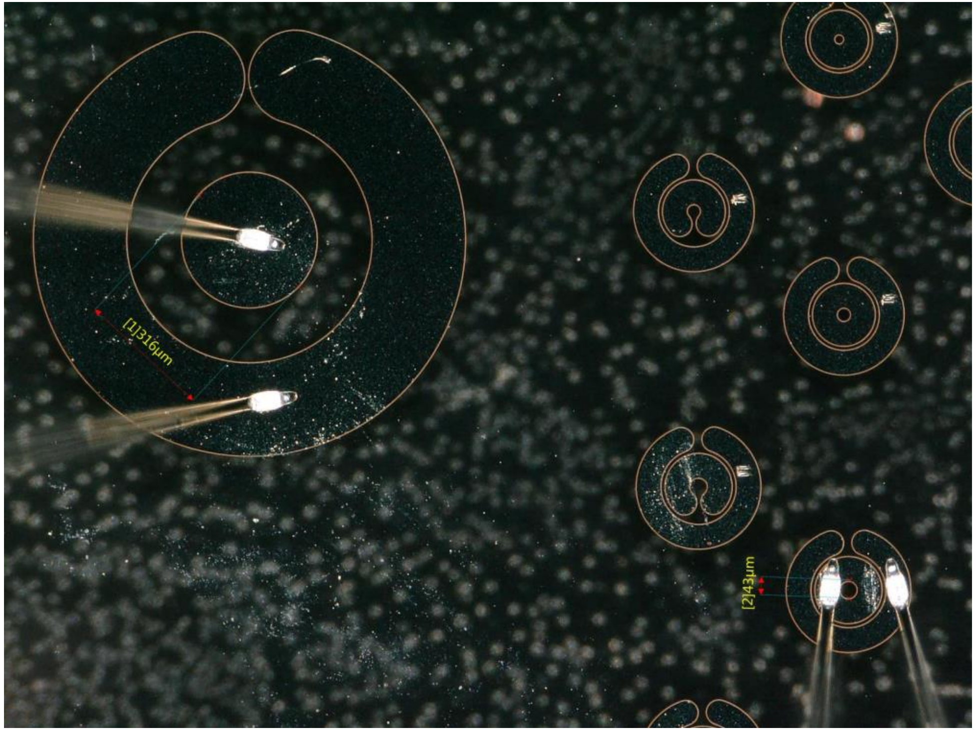
TCAD Model Development

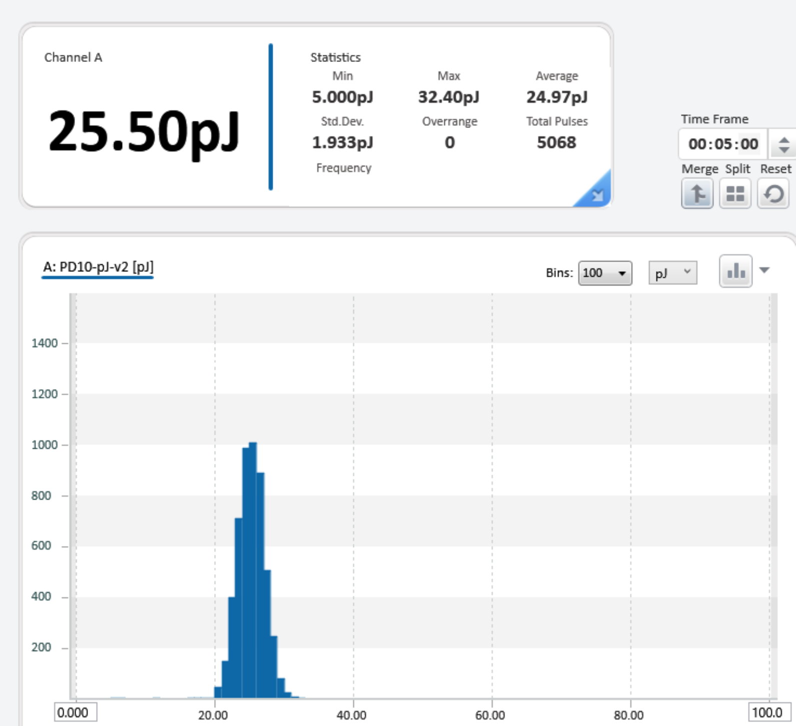
Silvaco Atlas to simulate GaN Schottky

- **PIPINYS model describes a phonon-assisted electron tunneling effect:**
  - Electron emission from local states at metal/semiconductor interface
  - Dependent on Schottky barrier height, trap energy level, trap density, phonon energy and electron-phonon interaction constant
  - Need parameters consistent with area → optimization!



Charge Collection Efficiency using UV Laser





Channel A

25.50pJ

Statistics

Min	Max	Average
5.000pJ	32.40pJ	24.97pJ
Std.Dev.	Overrange	Total Pulses
1.933pJ	0	5068
Frequency		

Time Frame: 00:05:00

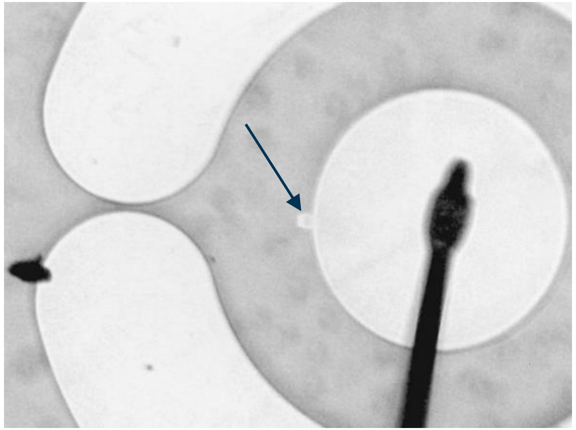
A: PD10-pJ-v2 [pJ]

Bins: 100

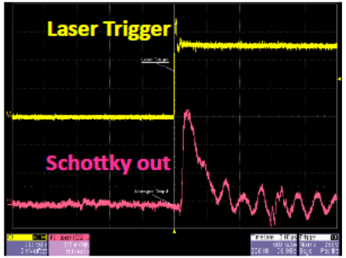
pJ

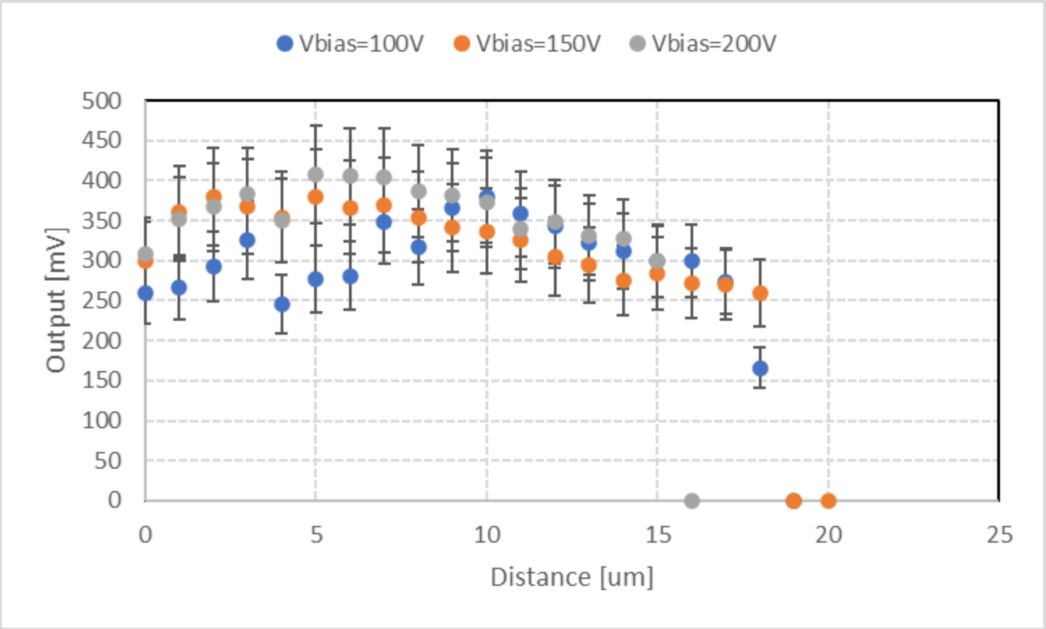
Trilite NewWave Research, λ = 355 nm, $\langle E \rangle$ = 25 pJ, σ_E = 1.9 pJ, beam size 10 x 10 um^2

Photoresponse versus position



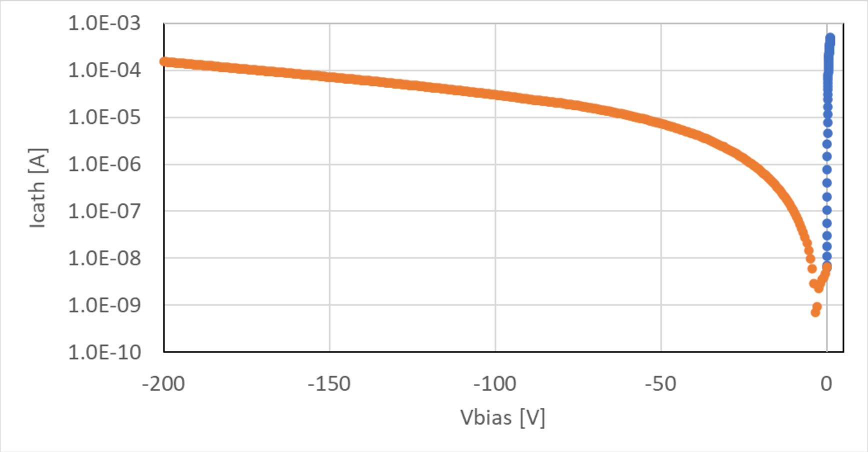
10 um

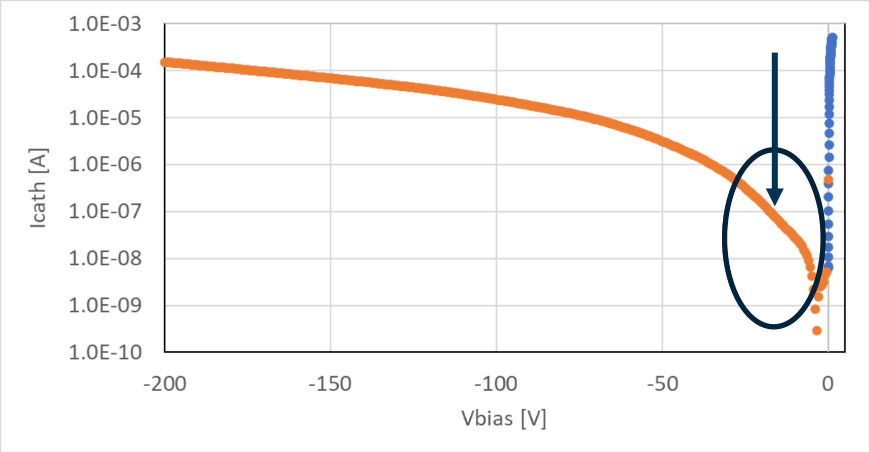




Extracted charge ~100 fC → ~1%

Visible Light Reduces Leakage





IV plot (FWD/REV) with NO LIGHT

IV plot (FWD/REV) with VISIBLE LIGHT

Trap saturation effect? → Deep-level transient spectroscopy

Conclusions & Future Work

Received GaN/GaN wafers from Kyma with poor surface morphology…

- Reasonably low carrier concentration in low 10^{15} cm^{-3}
- Material quality? Needs more study.

Demonstrated Schottky process showing rectification behaviour with sufficient thermal anneal

Performed preliminary UV responsivity measurements

- Requires further investigation for lower noise measurements, higher intensity
- Perform DLTS measurements coupled to TCAD

Future work involves testing NTT and Kyma wafers with further processing

THANK YOU

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Extracting Schottky Barrier Height and Ideality

Fit forward bias for V>3kT/q

Prior to series resistance roll-off

Ideality factor is also extracted as a function of bias