4th 28nm Mixed-Signal Design Workshop

Report of Contributions

https://indico.cern.ch/e/1336561

Contribution ID: **1** Type: **not specified**

Welcome

Monday 11 December 2023 09:00 (20 minutes)

Presenter: CARATELLI, Alessandro (CERN, EPFL)

Session Classification: Overview of the 28nm technology

Contribution ID: **2** Type: **not specified**

Technology Overview and designer's guidelines

Monday 11 December 2023 09:20 (50 minutes)

Presenter: BANDI, Franco Nahuel (CERN)

Session Classification: Overview of the 28nm technology

Contribution ID: **4** Type: **not specified**

Overview of the 28nm common design platform

Monday 11 December 2023 10:10 (30 minutes)

Presenter: ANDORNO, Marco (CERN)

Session Classification: Overview of the 28nm technology

Contribution ID: **5** Type: **not specified**

Total Ionizing Dose response of the 28nm technlogy

Monday 11 December 2023 10:55 (1h 5m)

Presenter: BORGHELLO, Giulio (CERN)

Session Classification: Overview of the 28nm technology

Contribution ID: **6** Type: **not specified**

Single event effects hardening in digital design

Wednesday 13 December 2023 11:00 (1 hour)

Presenter: CARATELLI, Alessandro (CERN, EPFL)

Session Classification: Digital design

Contribution ID: **16** Type: **not specified**

Lab session

Presenter: CARRIERE, Philippe (Cadence)

Session Classification: Analog design

Contribution ID: **17** Type: **not specified**

Digital flow introduction

Wednesday 13 December 2023 10:15 (45 minutes)

Main steps of the flow, tools, Flowkit

Presenter: DEKHIL, Erwan (Cadence)

Session Classification: Digital design

Contribution ID: **18** Type: **not specified**

Block-level implementation

Thursday 14 December 2023 09:00 (1h 15m)

Synthesis, floorplan

Presenter: DEKHIL, Erwan (Cadence)

Session Classification: Digital design

Contribution ID: **19** Type: **not specified**

Block-level implementation

Thursday 14 December 2023 10:30 (1h 30m)

Placement, clock tree synthesis, routing

Presenter: DEKHIL, Erwan (Cadence)

Session Classification: Digital design

Contribution ID: **20** Type: **not specified**

Lab session (Block-level implementation)

Thursday 14 December 2023 13:30 (1h 15m)

Author: DEKHIL, Erwan (Cadence)

Presenters: CARATELLI, Alessandro (CERN, EPFL); DEKHIL, Erwan (Cadence); ANDORNO, Marco (CERN)

Session Classification: Digital design

Contribution ID: **21** Type: **not specified**

Lab session (Block-level implementation)

Thursday 14 December 2023 15:00 (2h 30m)

Author: DEKHIL, Erwan (Cadence)

Presenters: CARATELLI, Alessandro (CERN, EPFL); DEKHIL, Erwan (Cadence); ANDORNO, Marco (CERN)

Session Classification: Digital design

Contribution ID: **22** Type: **not specified**

Hierarchical implementation

Friday 15 December 2023 09:00 (1h 15m)

Top level analysis with use of block model, assemble design

Presenter: DEKHIL, Erwan (Cadence)

Session Classification: Digital design

Contribution ID: **23** Type: **not specified**

Signoff

Friday 15 December 2023 13:30 (1h 30m)

Timing analysis, power analysis, DRC, LVS

Presenter: DEKHIL, Erwan (Cadence)

Session Classification: Digital design

Contribution ID: **24** Type: **not specified**

Lab session

Author: GENNERET, Bertrand (cadence design systems)

Presenters: CARATELLI, Alessandro (CERN, EPFL); GENNERET, Bertrand (cadence design systems); ANDORNO, Marco (CERN)

Session Classification: Digital design

Contribution ID: **25** Type: **not specified**

Lab session (Signoff)

Friday 15 December 2023 15:15 (2h 15m)

Author: DEKHIL, Erwan (Cadence)

Presenters: CARATELLI, Alessandro (CERN, EPFL); DEKHIL, Erwan (Cadence); ANDORNO, Marco (CERN)

Session Classification: Digital design

Contribution ID: **26** Type: **not specified**

Lab session (Analog simulation)

Monday 11 December 2023 13:50 (1h 25m)

Presenter: DORNELAS, Helga (Cadence)

Session Classification: Analog design

Contribution ID: **27** Type: **not specified**

Lab session (Mixed-signal simulation)

Tuesday 12 December 2023 09:00 (1h 30m)

Presenter: DORNELAS, Helga (Cadence)

Session Classification: Mixed-signal design

Contribution ID: **28** Type: **not specified**

Lab session (Mixed-signal simulation)

Monday 11 December 2023 16:00 (1h 30m)

Presenter: DORNELAS, Helga (Cadence)

Session Classification: Mixed-signal design

Contribution ID: **29** Type: **not specified**

Analog Backend VXL Best Practices

Tuesday 12 December 2023 10:45 (15 minutes)

Presenter: CARRIERE, Philippe (CERN)

Session Classification: Analog design

Contribution ID: **30** Type: **not specified**

Lab session (Analog backend)

Tuesday 12 December 2023 13:30 (1h 15m)

Presenter: CARRIERE, Philippe (Cadence)

Session Classification: Analog design

Contribution ID: **31** Type: **not specified**

DRC/LVS with PVS

Tuesday 12 December 2023 15:50 (20 minutes)

Presenter: CARRIERE, Philippe (Cadence)

Session Classification: Analog design

Contribution ID: **32** Type: **not specified**

Analog simulation with Explorer and Assembler

Monday 11 December 2023 13:30 (20 minutes)

Presenter: DORNELAS, Helga (Cadence)

Session Classification: Analog design

Contribution ID: **33** Type: **not specified**

Mixed-signal simulation with Xcelium and Virtuoso

Monday 11 December 2023 15:30 (30 minutes)

Presenter: DORNELAS, Helga (Cadence)

Session Classification: Mixed-signal design

Contribution ID: **34** Type: **not specified**

Lab session (Analog backend)

Tuesday 12 December 2023 11:00 (1 hour)

Presenter: CARRIERE, Philippe (CERN)

Session Classification: Analog design

Contribution ID: **35** Type: **not specified**

Lab session (DRC/LVS with PVS)

Tuesday 12 December 2023 16:10 (1h 20m)

Presenter: CARRIERE, Philippe (CERN)

Session Classification: Analog design

Contribution ID: **36** Type: **not specified**

IP block integration (Liberty file and Abstract)

Wednesday 13 December 2023 09:00 (15 minutes)

Presenter: ANDORNO, Marco (CERN)

Session Classification: Mixed-signal design

Contribution ID: **37** Type: **not specified**

Lab session (Liberty file)

Wednesday 13 December 2023 09:15 (45 minutes)

Presenters: CARATELLI, Alessandro (CERN, EPFL); ANDORNO, Marco (CERN)

Session Classification: Mixed-signal design

Contribution ID: **38** Type: **not specified**

Timing constraints and synthesis

Wednesday 13 December 2023 13:00 (1h 45m)

Presenter: DEKHIL, Erwan (Cadence)

Session Classification: Digital design

Contribution ID: **39** Type: **not specified**

Lab session (TMR)

Wednesday 13 December 2023 15:00 (30 minutes)

Presenters: CARATELLI, Alessandro (CERN, EPFL); ANDORNO, Marco (CERN)

Session Classification: Digital design

Contribution ID: **40** Type: **not specified**

Lab session (Synthesis and LEC)

Wednesday 13 December 2023 15:30 (2 hours)

Author: DEKHIL, Erwan (Cadence)

Presenters: CARATELLI, Alessandro (CERN, EPFL); DEKHIL, Erwan (Cadence); ANDORNO, Marco (CERN)

Session Classification: Digital design

Contribution ID: **41** Type: **not specified**

Lab session (Hierarchical implementation)

Friday 15 December 2023 10:30 (1h 30m)

Author: DEKHIL, Erwan (Cadence)

Presenters: CARATELLI, Alessandro (CERN, EPFL); DEKHIL, Erwan (Cadence); ANDORNO, Marco (CERN)

Session Classification: Digital design

Contribution ID: **42** Type: **not specified**

Abstract generation

Tuesday 12 December 2023 15:00 (20 minutes)

Presenter: CARRIERE, Philippe (CERN)

Session Classification: Mixed-signal design

Contribution ID: **43** Type: **not specified**

Lab session (Abstract)

Tuesday 12 December 2023 15:20 (30 minutes)

Presenter: CARRIERE, Philippe (CERN)

Session Classification: Mixed-signal design