

ISOTDAQ

International School of Trigger
and Data Acquisition



Towards pico-seconds Time Digitization in FPGAs













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Introduction: why the timing precision matters!



2008 Beijing Olympics, 100m results (men)

Rank	Team	Participant	Results
G	 JAM	 Usain Bolt	09.690
S	 TTO	 Richard Thompson	09.890
B	 USA	 Walter Dix	09.910
4	 AHO	 Churandy Martina	09.930
5	 JAM	 Asafa Powell	09.950
6	 JAM	 Michael Frater	09.970

World records (by now), 100m: 9.58 (men); 10.49 (women) ~ 10 m/s

Milliseconds!

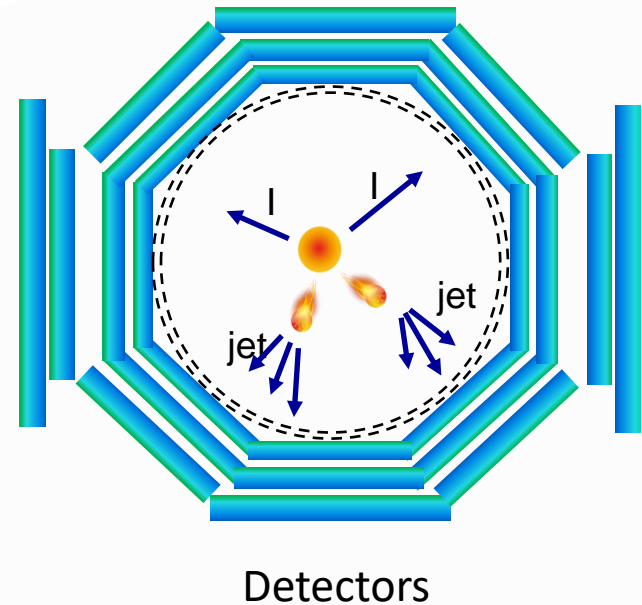
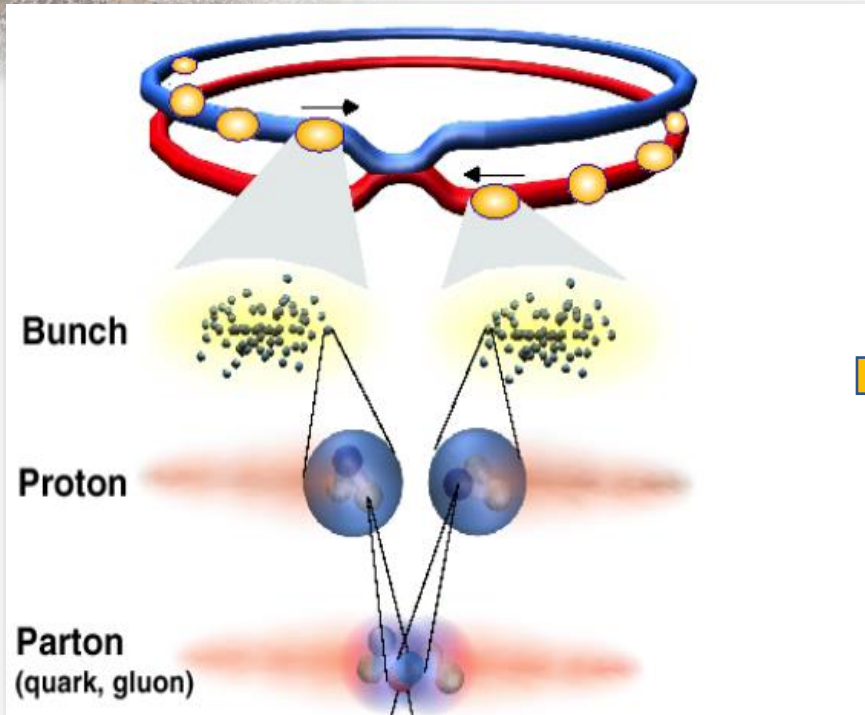
● Introduction: why the timing precision matters!



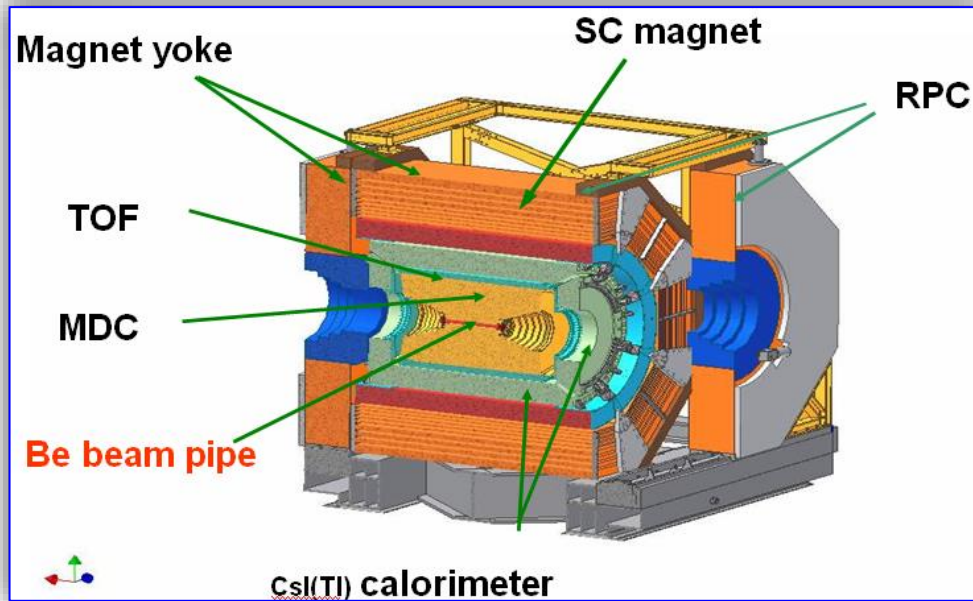
Particles travelling at a speed
Approximating the speed of light!

$$\sim 3 \times 10^8 \text{ m/s}$$

- 1 ms (10^{-3}) \rightarrow \sim 300 km
- 1 ns (10^{-9}) \rightarrow 0.3 m (30 cm)
- 10 ps (10^{-11}) \rightarrow 0.003 m (3mm)



Introduction: why the timing precision matters!



$$\begin{aligned} \Delta t &= \frac{L}{v_1} - \frac{L}{v_2} = \frac{L}{c} \left(\frac{1}{\beta_1} - \frac{1}{\beta_2} \right) \\ &= \frac{L}{c} \frac{(m_2^2 - m_1^2)}{(P/c)^2} \left(\frac{\beta_1 \beta_2}{\beta_1 + \beta_2} \right) \\ &\leq \frac{L}{c} \frac{(m_2^2 - m_1^2)}{2(P/c)^2} \end{aligned}$$

BES III (Beijing Spectrometer III) , separate K/ π with 2σ at 1GeV/c \rightarrow 100 ps timing precision for the TOF (time of Flight)

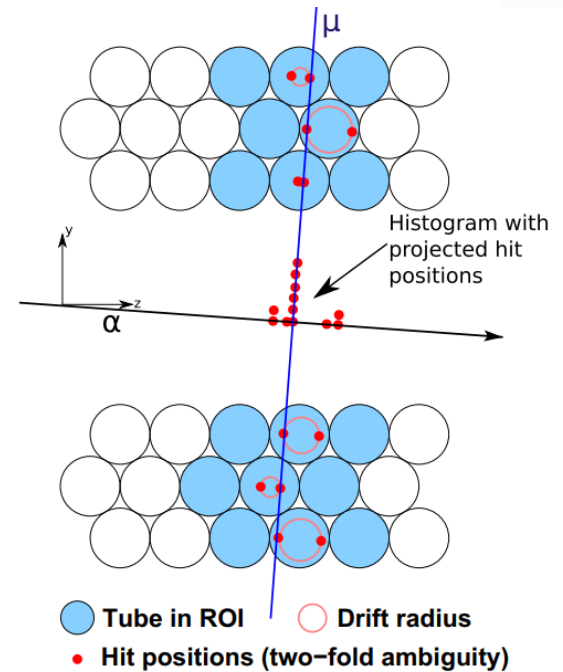
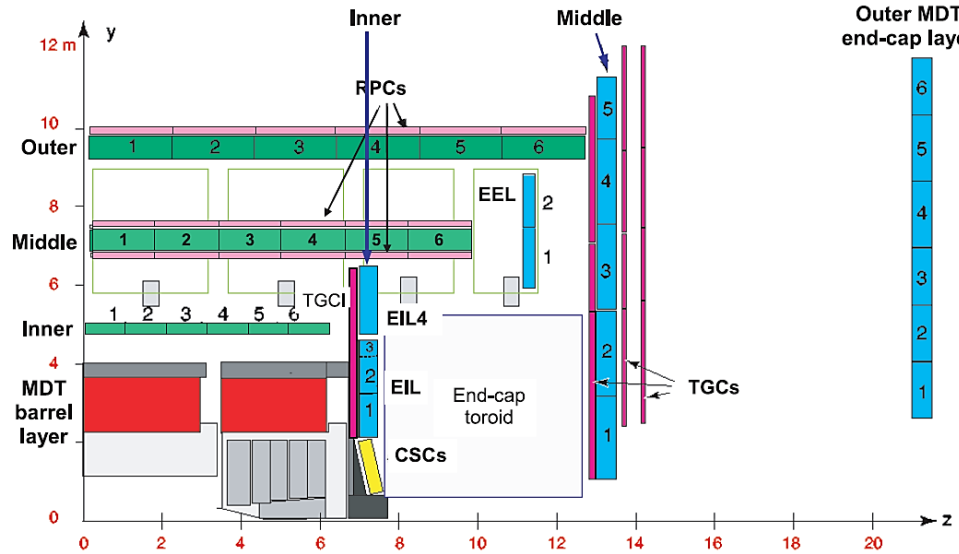
$$\sigma^2 = \sigma_{\text{detector}}^2 + \sigma_{\text{bunch}}^2 + \sigma_Z^2 + \sigma_{\text{elec.}}^2 + \sigma_{\text{time-walk}}^2$$

$$\sigma_{\text{detector}} \sim 80 \text{ ps}, \quad \sigma_Z \sim 10 \text{ ps}, \quad \sigma_{\text{bunch}} \sim 35 \text{ ps}, \quad \sigma_{\text{time-walk}} \sim 10 \text{ ps}$$

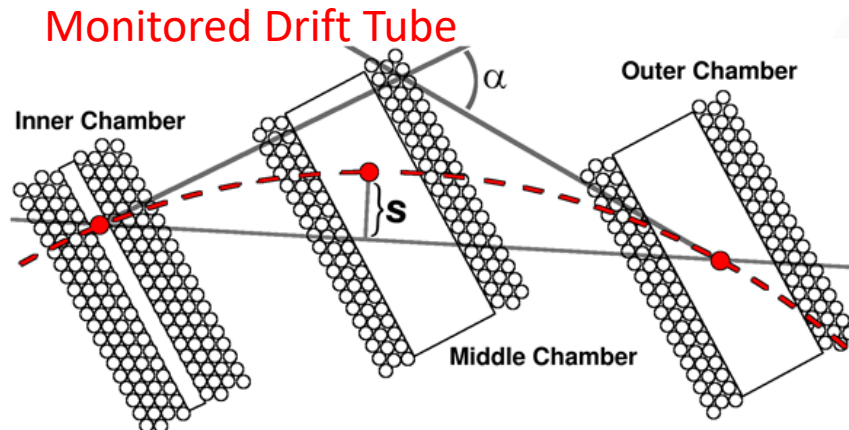
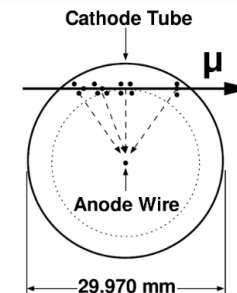
$$\sigma_{\text{elec.}} < 25 \text{ ps}$$

Introduction: why the timing precision matters!

Measuring muon momentum through its bending trajectories



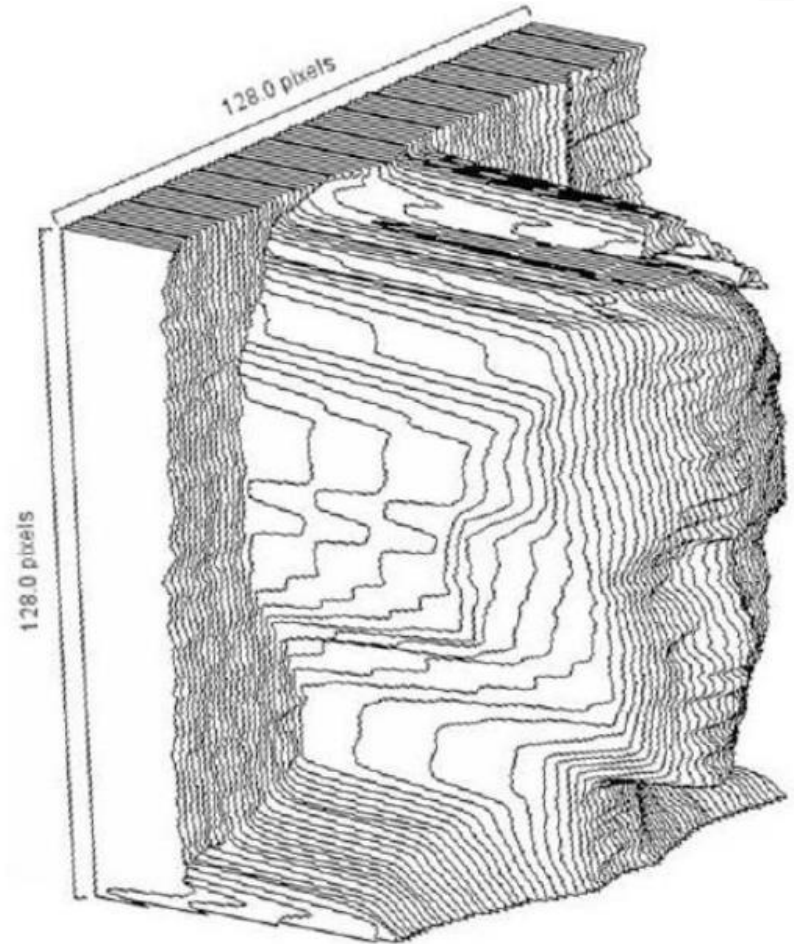
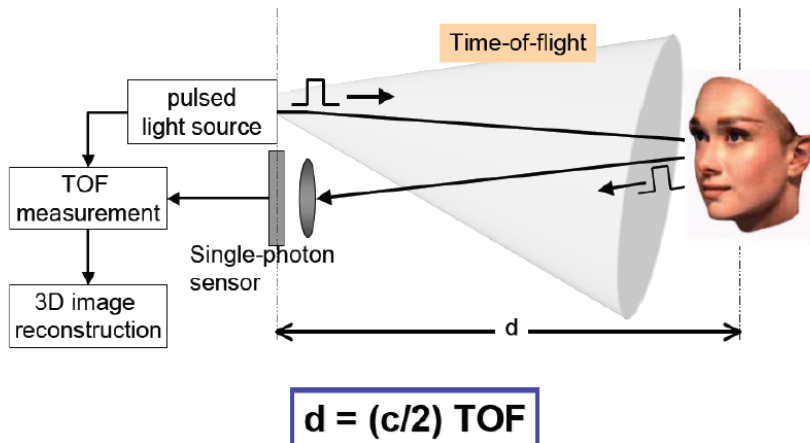
Trajectory reconstruction



- Magnet field bends the trajectory of the muons
- Momentum is measured through “inner-middle-outer” layers

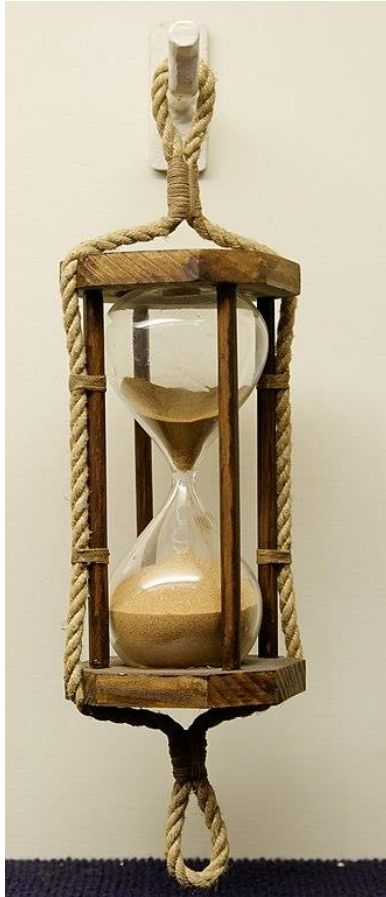
Introduction: why the timing precision matters!

3D imaging



Introduction: Examples of timing techniques

See "Introduction to FPGAs" by Hannes Sakulin



A marine sandglass
(seconds-minutes)



A stop watch
(milliseconds)



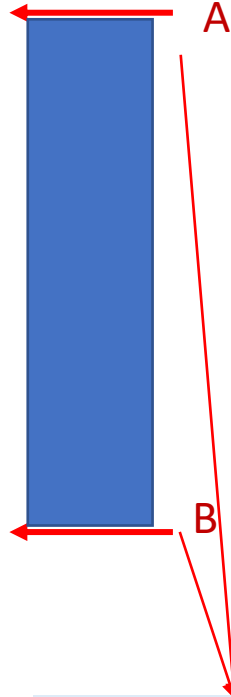
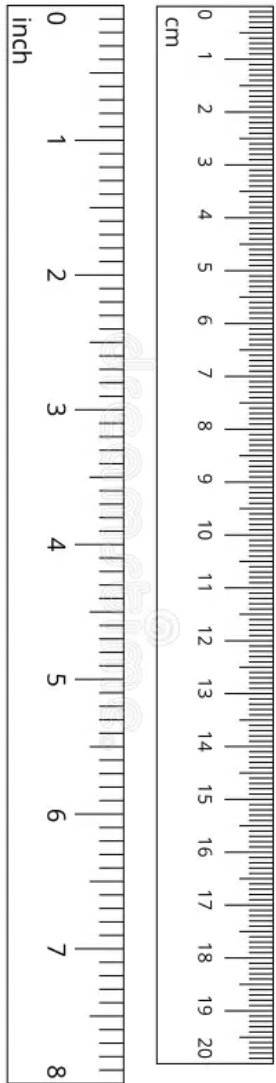
Scaled by $1/10^9$



A XXXXX?
(picoseconds)

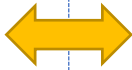
Introduction: Essentials of timing techniques

Measuring the length of a rectangle

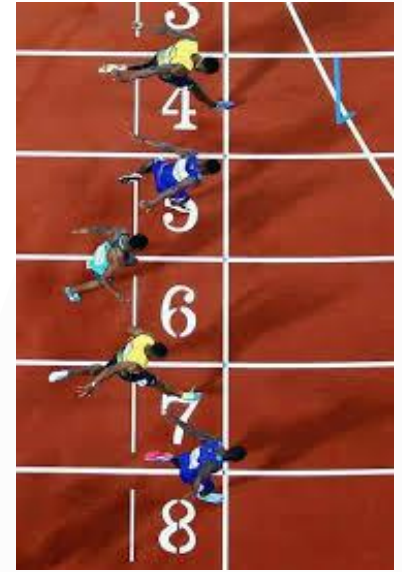


Measure by millimeters

Count at Finer Intervals



Starting line



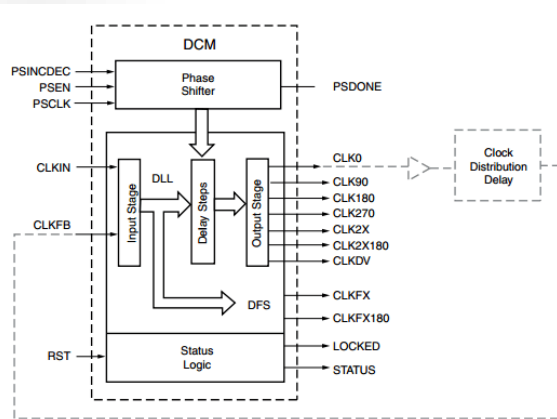
Finishing line



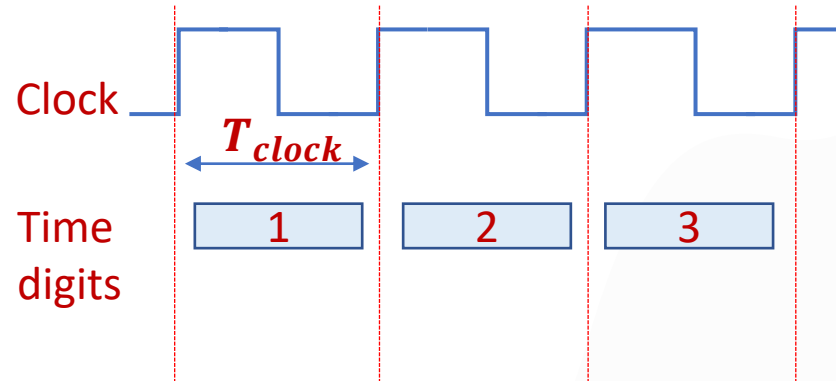
Count by milliseconds

So, let's start counting, in an FPGA!

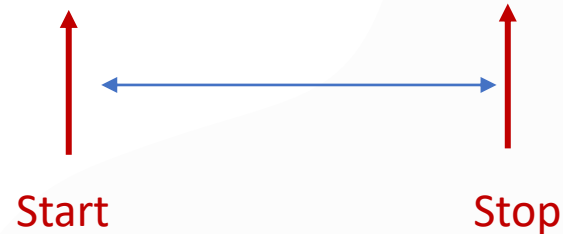
Time Digitization in FPGAs: Counter



Clock Manager

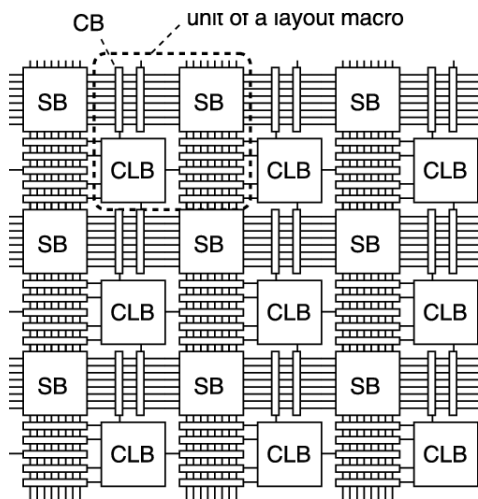


Clock
Time digits



Start

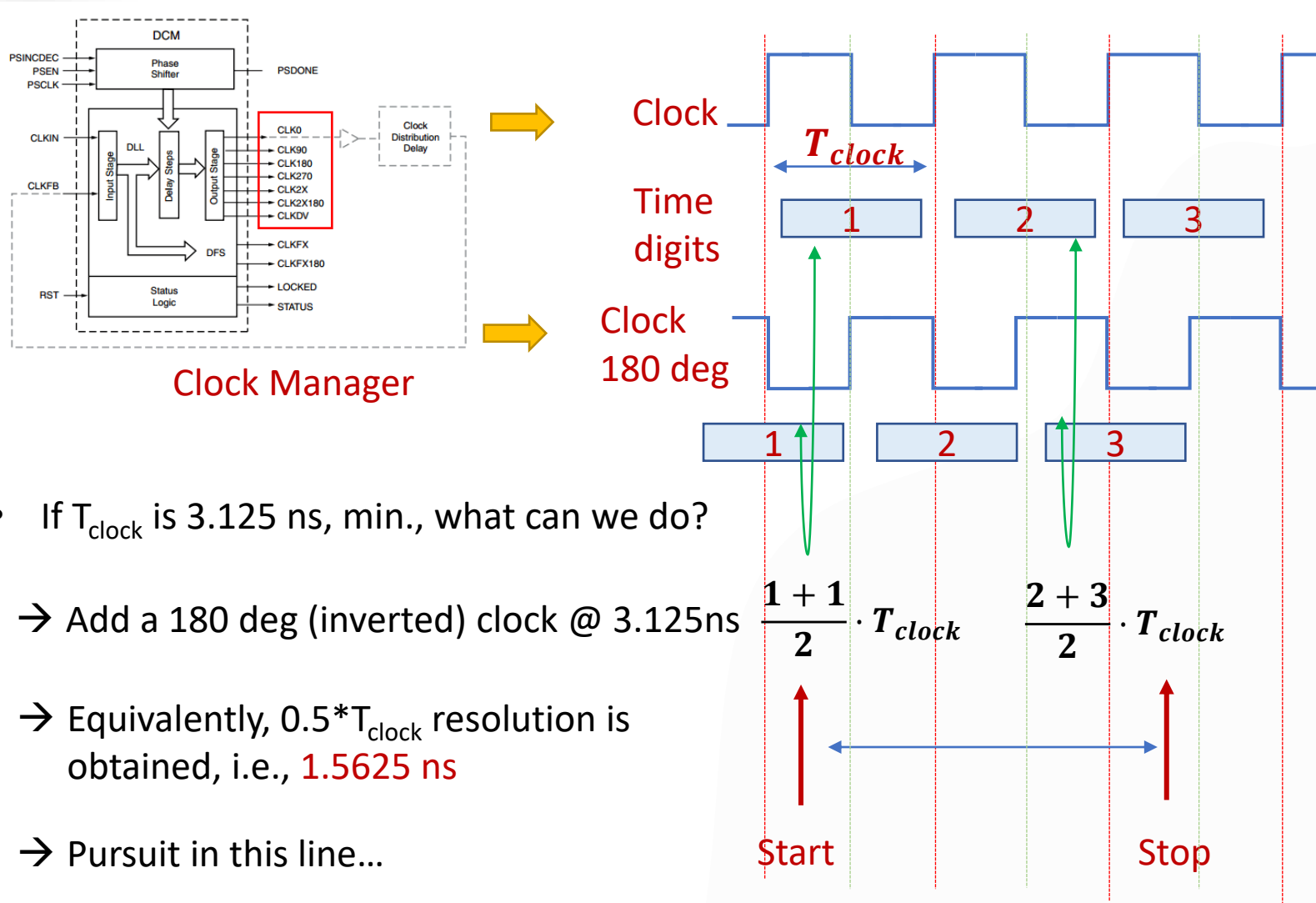
Stop



Logic blocks

- Timing resolution corresponds to T_{clock}
- min. period of Clock is limited in FPGAs typ. in nano-seconds ranges min.
- If T_{clock} is 3.125 ns (320MHz), min., what can we do?

Time Digitization in FPGAs : dual Counter



- If T_{clock} is 3.125 ns, min., what can we do?

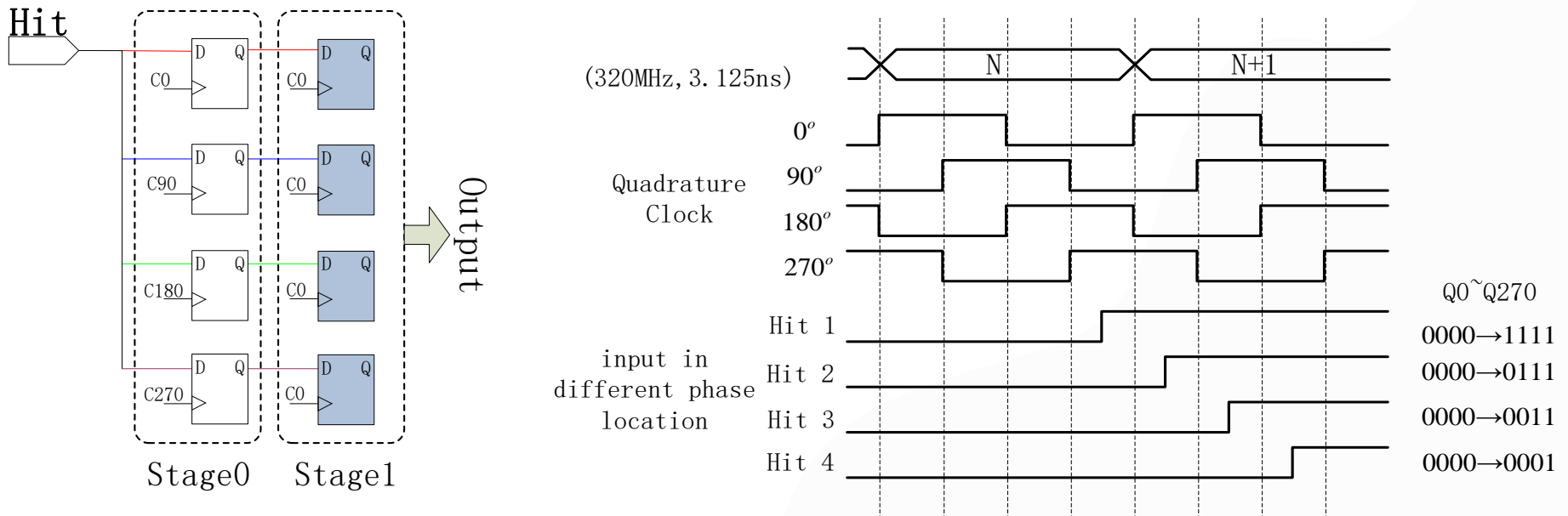
→ Add a 180 deg (inverted) clock @ 3.125ns

→ Equivalently, $0.5 \cdot T_{clock}$ resolution is obtained, i.e., **1.5625 ns**

→ Pursuit in this line...

Time Digitization in FPGAs : phase interpolation

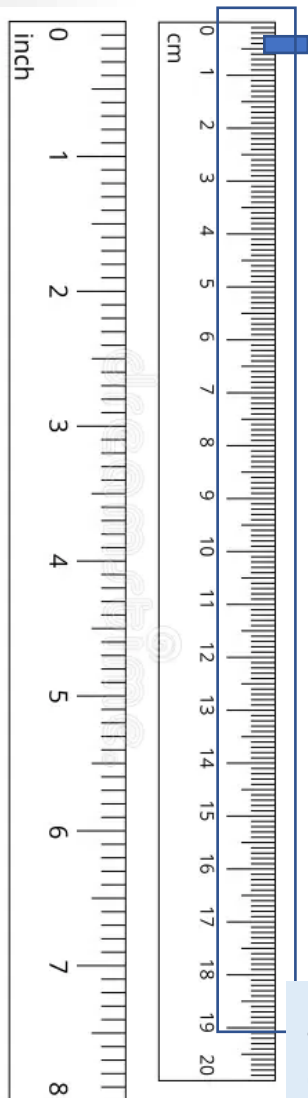
- Four phases of 320 MHz, (0, 90, 180, 270), equivalently ~780 ps resolution



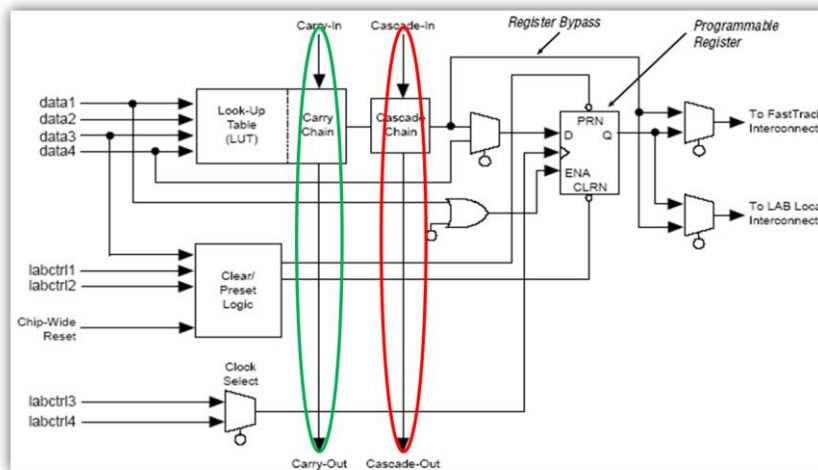
- Limited by number of finer clock phases (generated from clock managers)
→ plus, difficulty in keeping alignment of clock edges (cons)
- Pros: simple, and easy to implement with macro blocks
- Achieved resolution: ~ **100s pico-seconds**

Progress by now: ~ hundreds ps

Pico-seconds ?

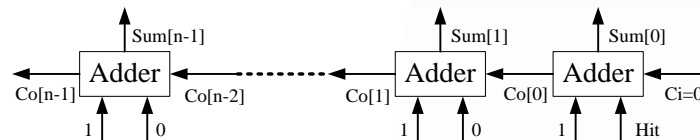


1: identify finer time intervals
(e.g., if a “component”/unit/cell with ~ 50 ps delay is found, and there are many of them to be added together uniformly)



Pioneered by Jinyuan Wu @ Fermilab
Cascade chain (2003)
<https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=1352025>

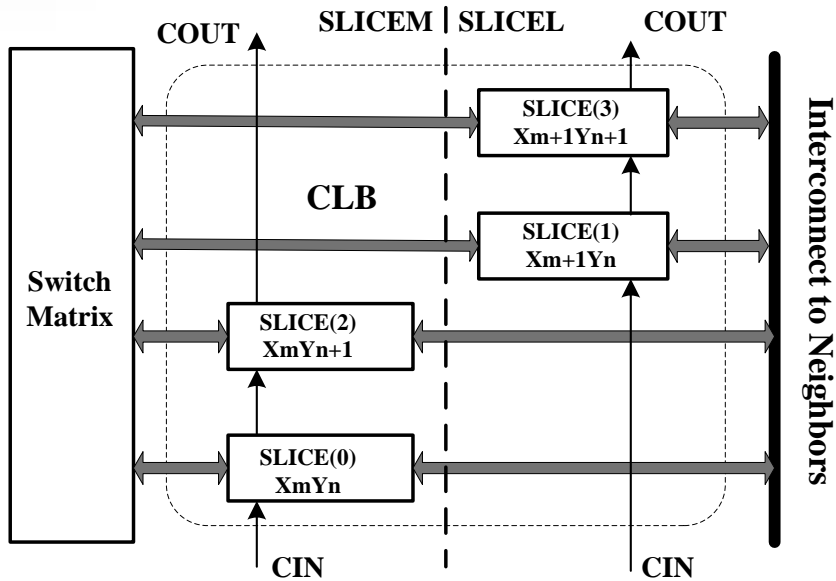
Inspired by Wu's idea,
A carry-chain version was invented @ USTC
<https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=1610982>



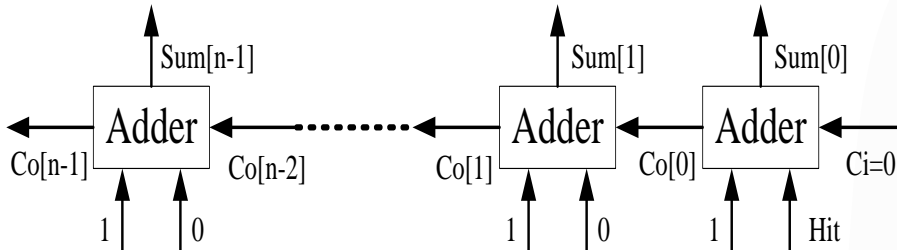
Nowadays, the delay of typical carry-chain cell is around **10s picoseconds**

2: add up to a “working” range
(e.g., add as many components up to 3.125 ns, the “counter” clock period)

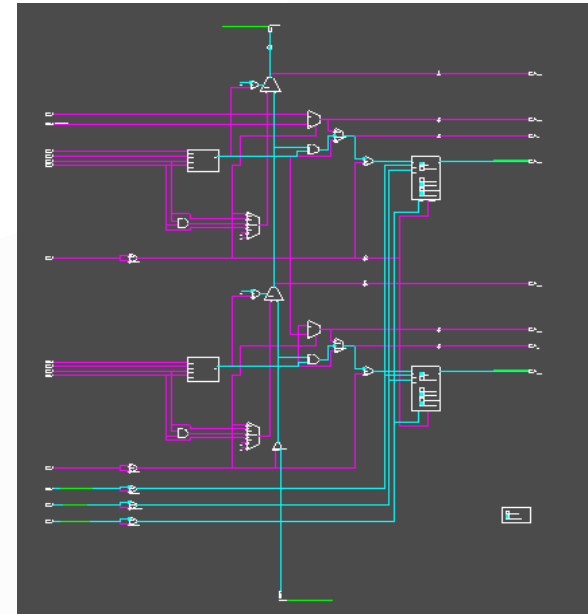
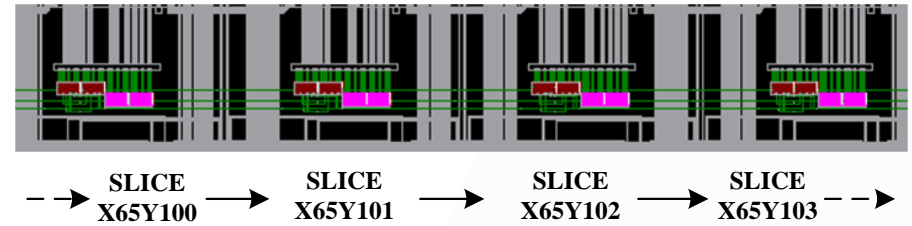
With Carry-chain as the "Delay"



a) Carry-in in a Slice



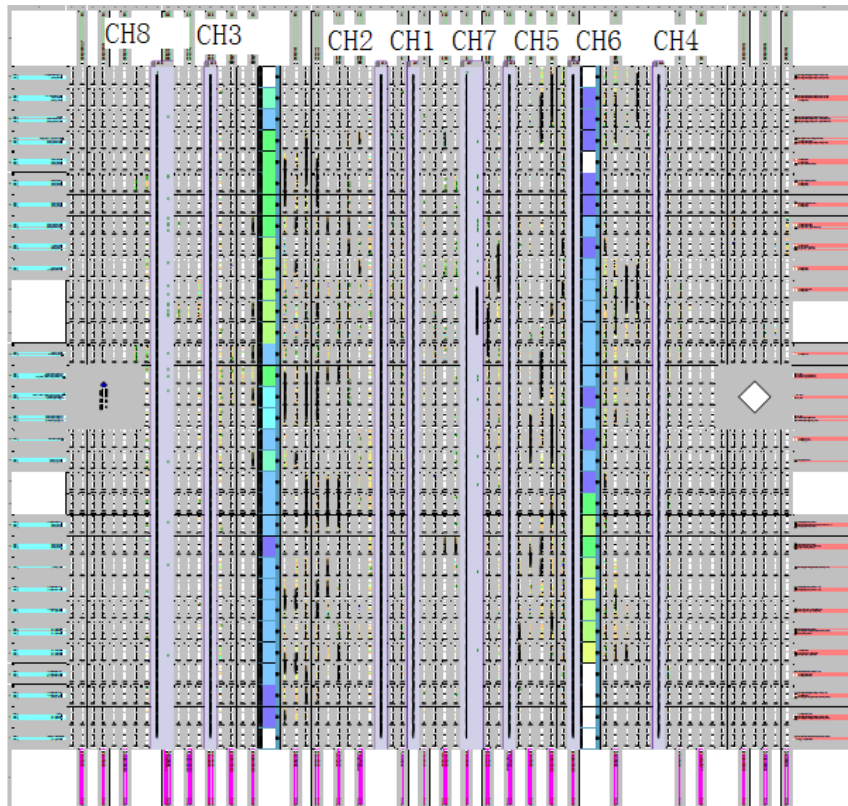
c) Carry chain of a multi-bit adder



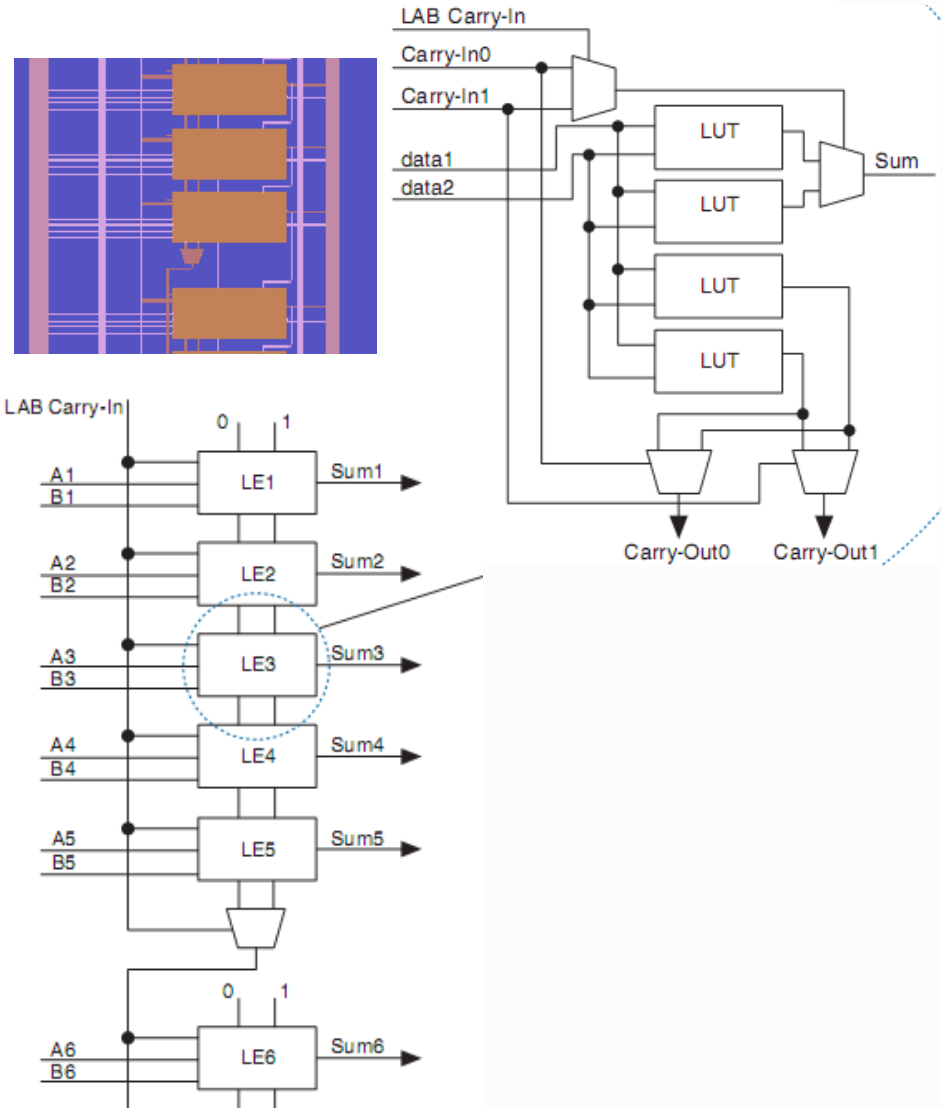
b) Rout in a SLICE

Forming a chain of "Delay"

In Altera (Intel) FPGAs

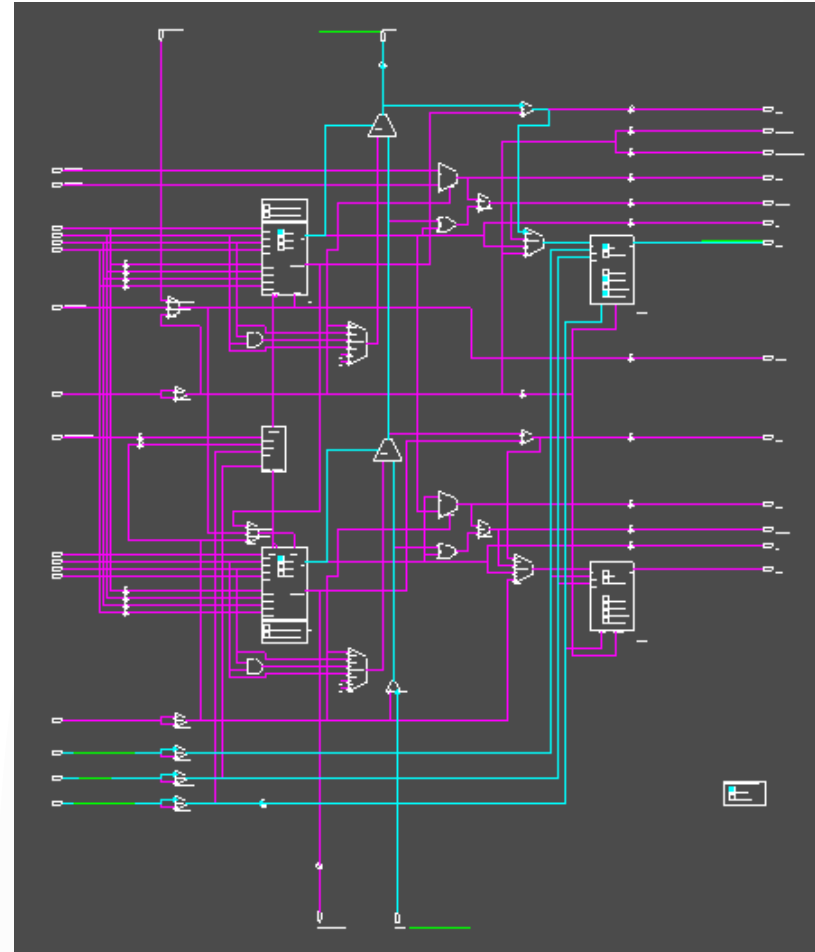
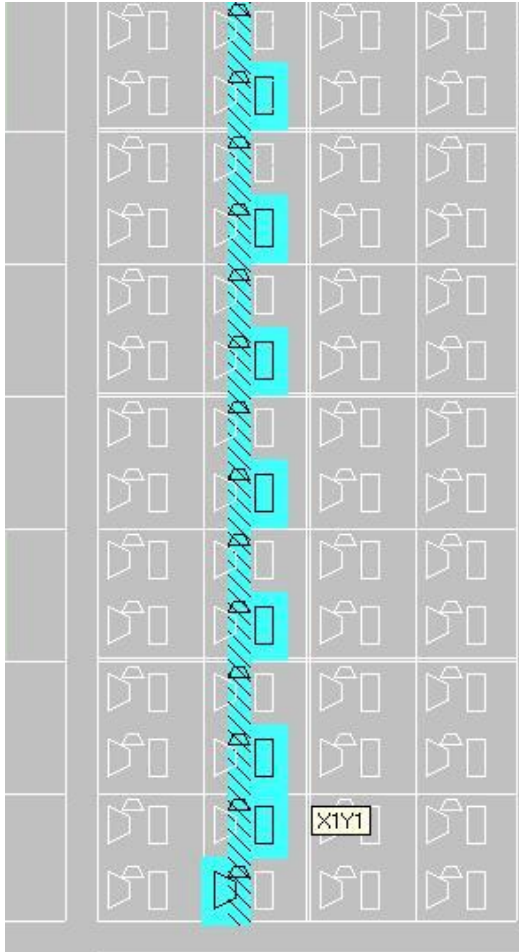


CYCLONE



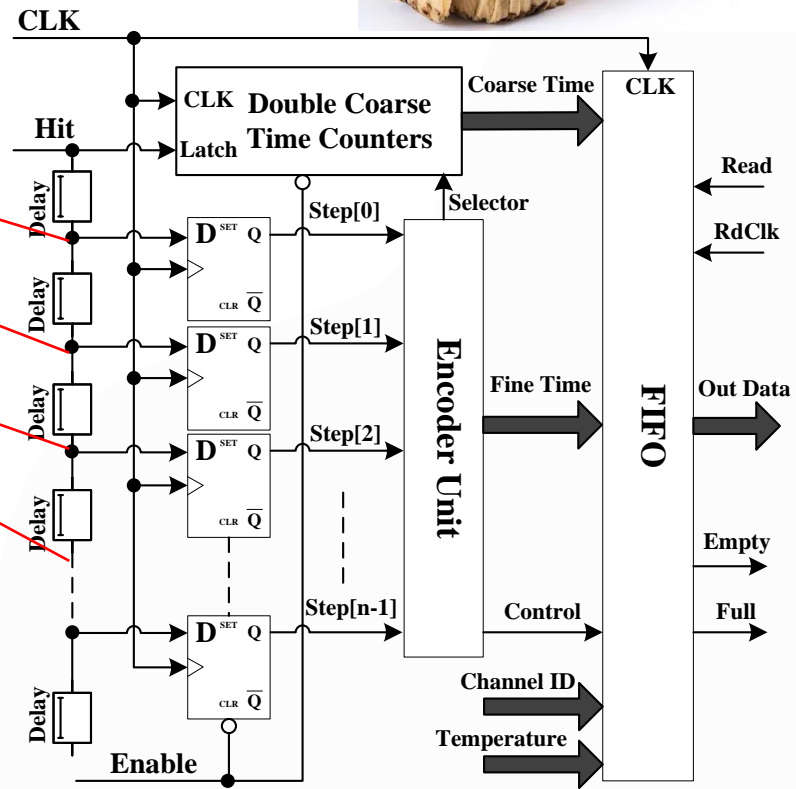
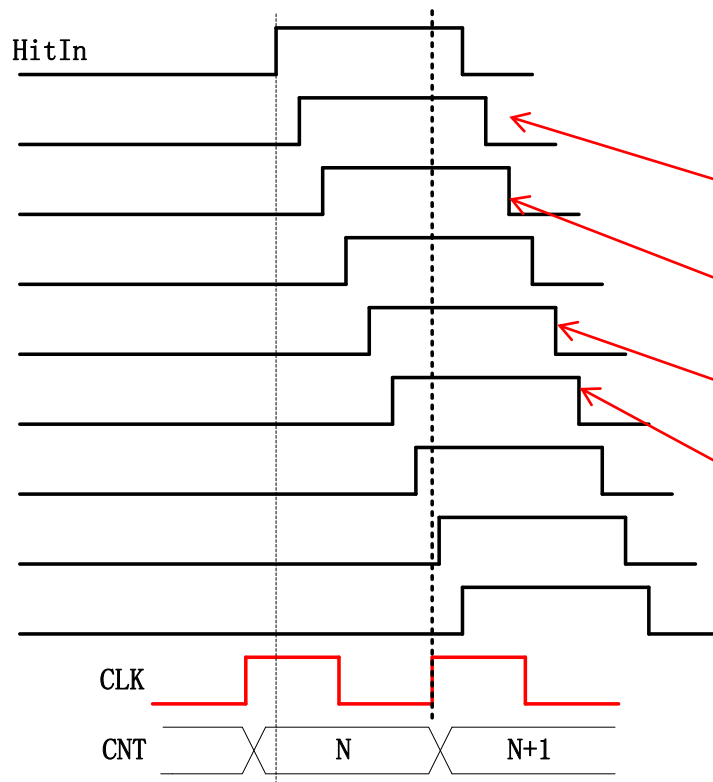
Forming a chain of "Delay"

In Xilinx (AMD) FPGAs

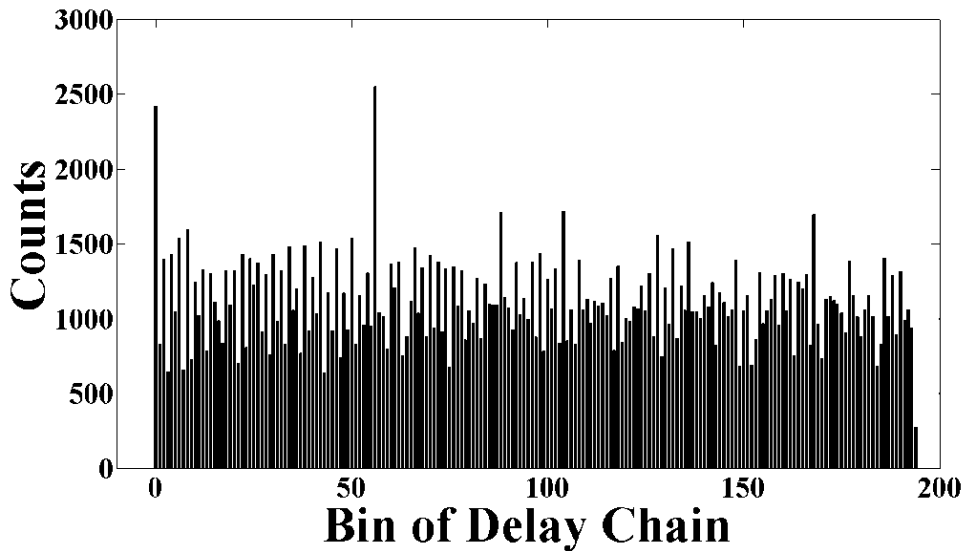


Principle: tapped-delay-line approach

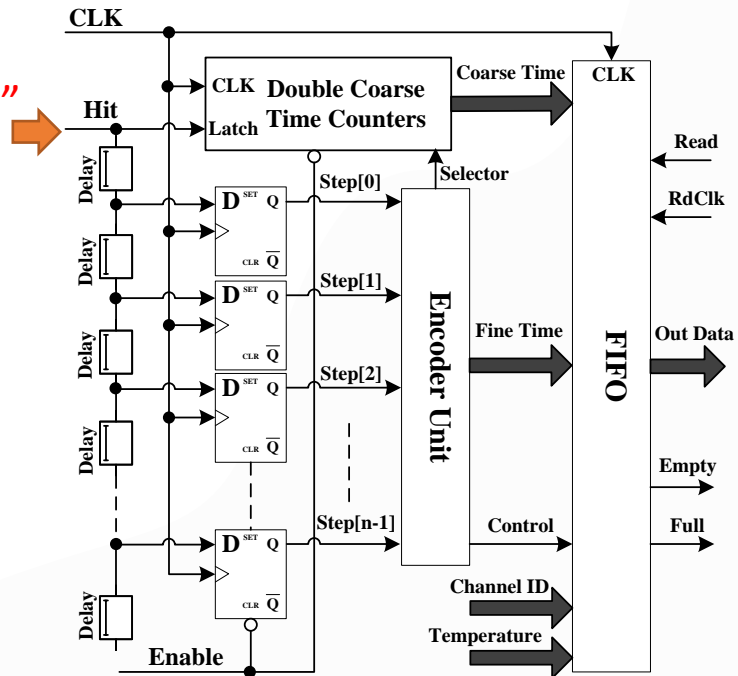
- Divide a clock period into finer slices (DELAY)
→ Forming a tapped-delay line (TDL)



Determine delay time of "Delay"



"Random" Signals**



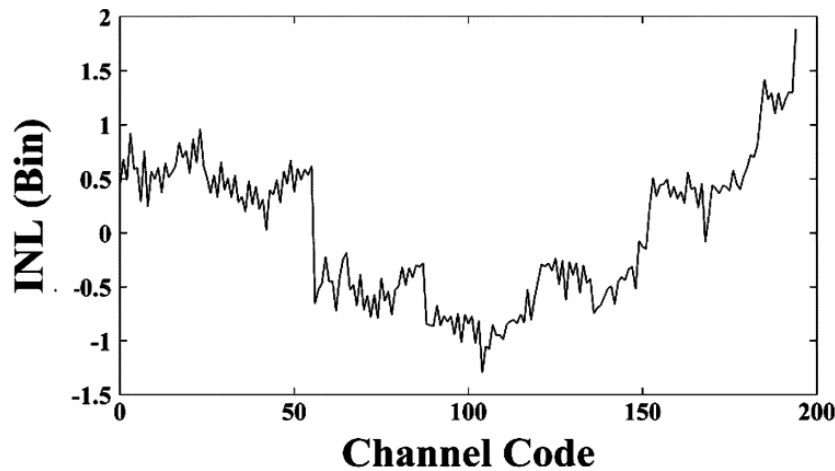
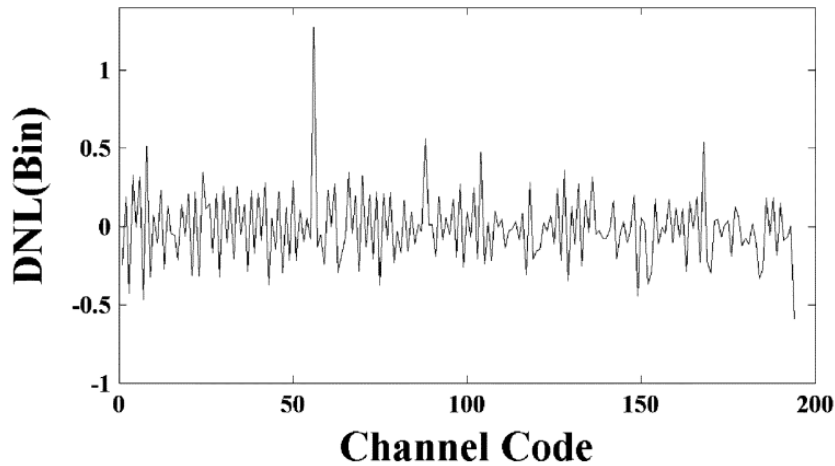
$$n = N + \frac{C_N}{C_{mean}}$$

Average Bin size: T_{clk}/n

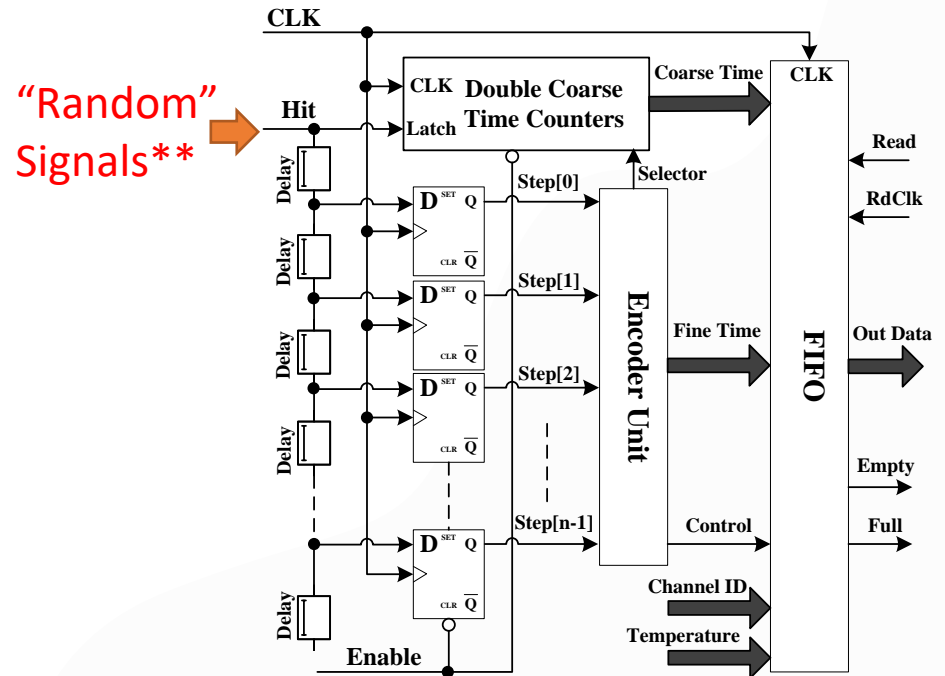
Or, since bin width is proportional to its counts, calculate the bin width for each bin

Determine delay time of "Delay"

$$DNL(i) = Bin_i - \overline{Bin}$$



$$INL(p) = \sum_{i=0}^{i=p} DNL(p)$$



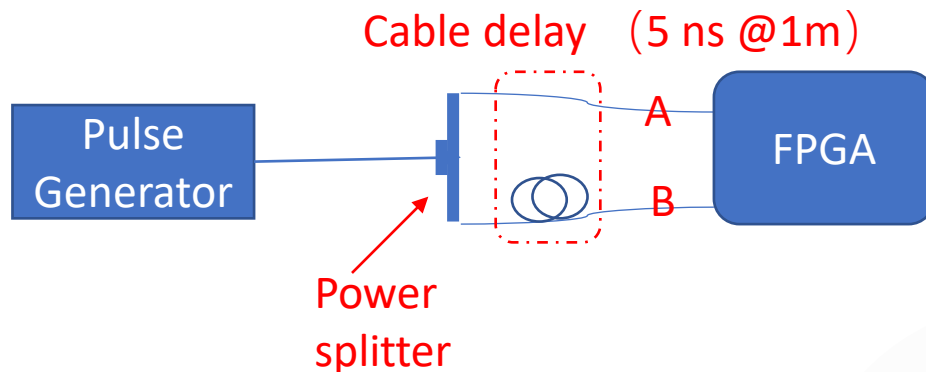
$$n = N + \frac{C_N}{C_{mean}}$$

Average Bin size: T_{clk}/n

Or, since bin width is proportional to its counts, calculate the bin width for each bin

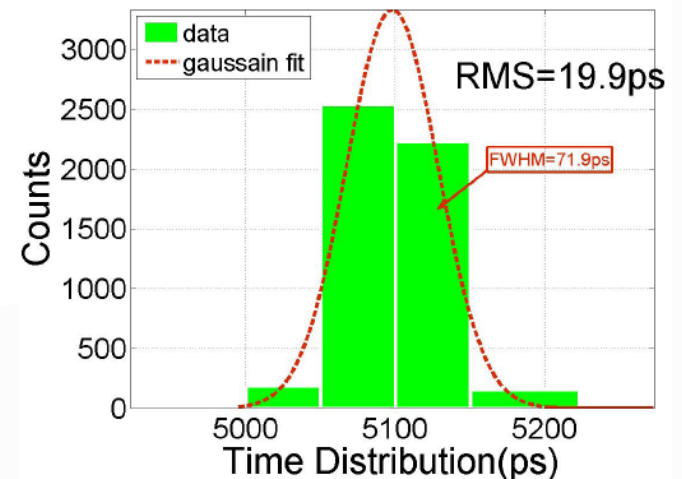
Timing Performance Evaluation

- Generation of a stable time interval, pico-seconds stability
 - High resolution signal generator (e.g., AWG)
 - Delay line approach



- Power splitter splits input pulse into two branches
- Each branch share similar time uncertainty, thus could be reduced by measuring their relative difference
- A/B are two “identical” channels in FPGA (TDC) → timing uncertainty for a single channel: $1/\sqrt{2}$

Cabel Delay Test: Mean=5097.9ps

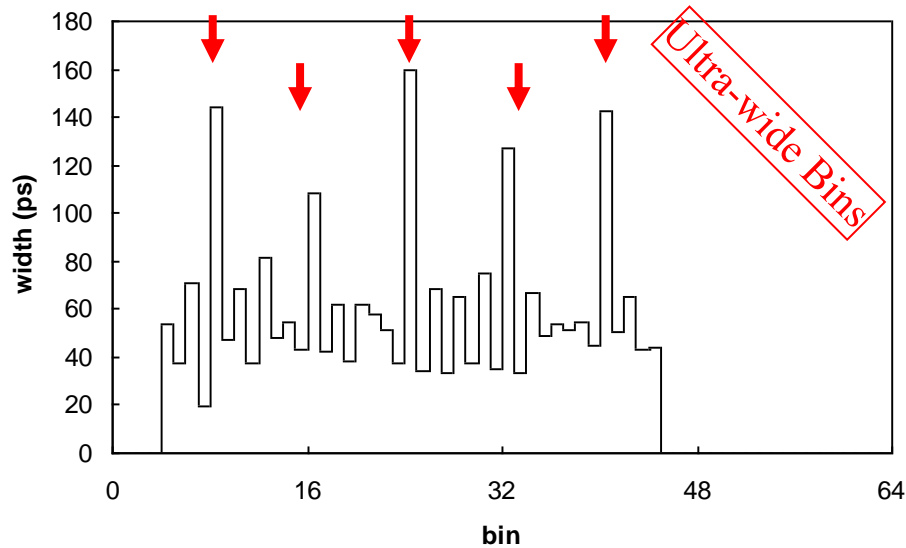
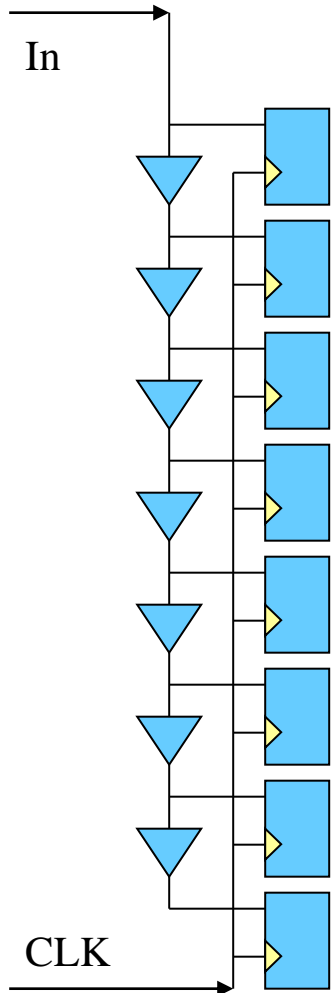


- Bin size (average)
- Nonlinearity (DNL/INL)
- Timing uncertainty (RMS)
- ...

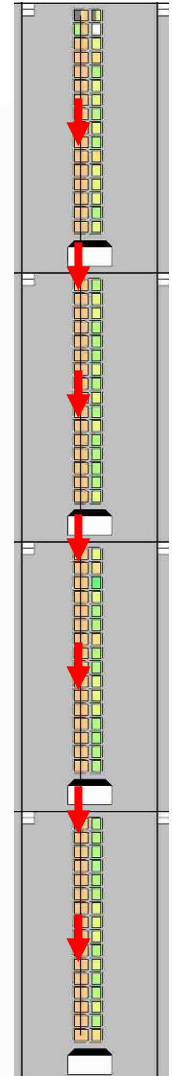
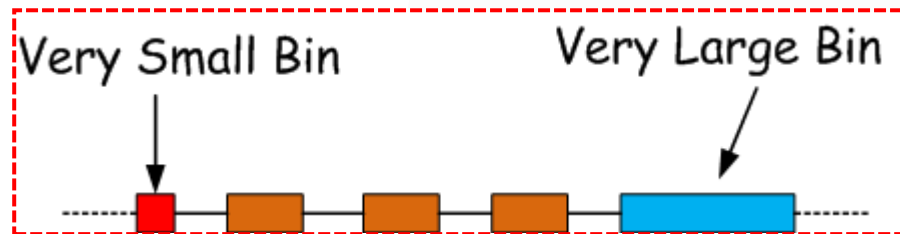
Progress by now: ~ 20 ps

The WaveUnion Approach

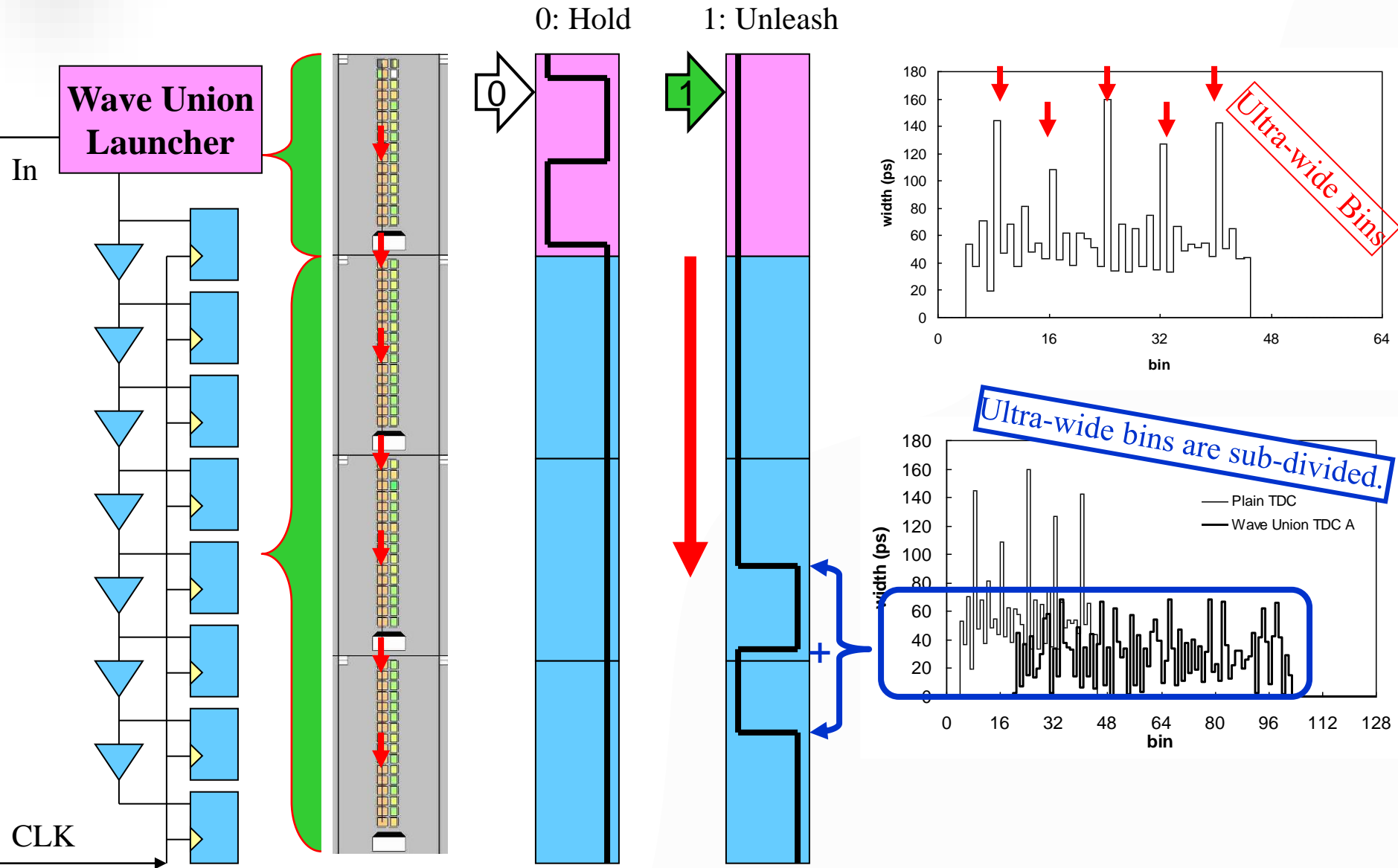
- Boosting the TDL-TDC approach beyond its cell delay



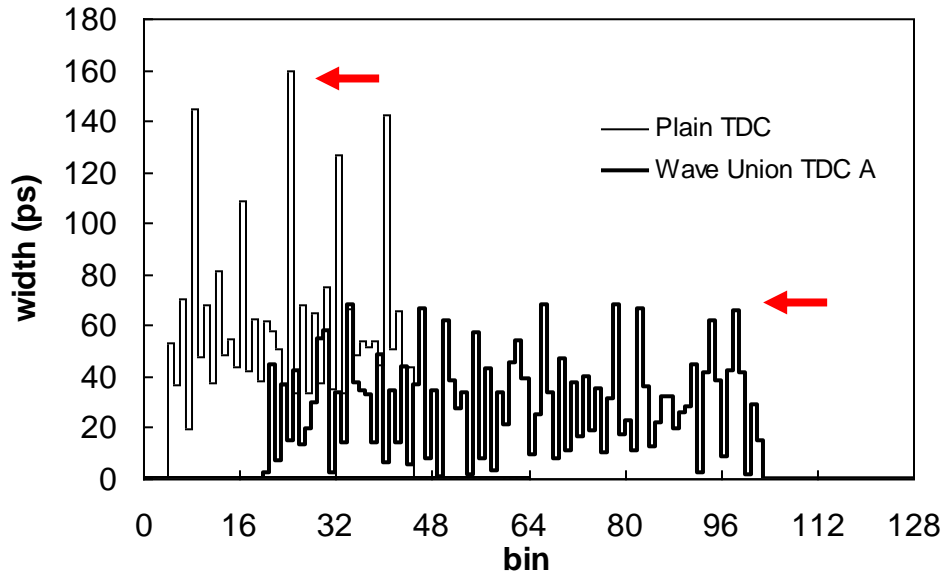
Ultra-Large Bin in the Carry-chain



WaveUnion A (Jinyuan Wu @Fermilab)



WaveUnion A (Jinyuan Wu @Fermilab)



Device: EP2C8T144C6

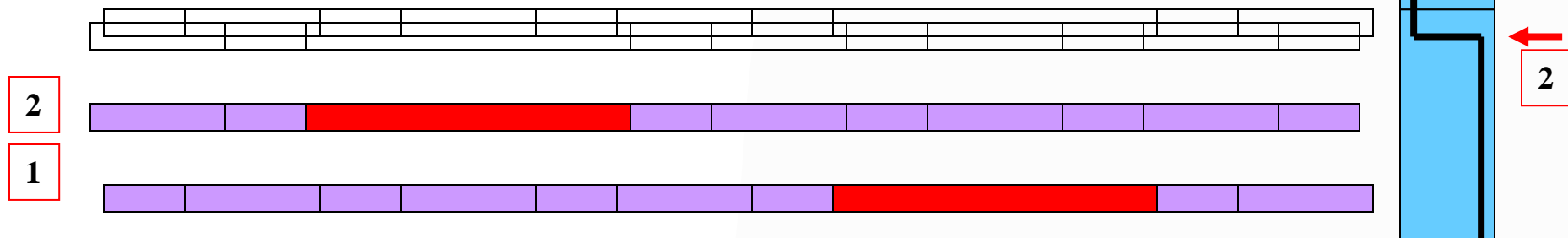
■ Plain TDC:

- Max. bin width: 160 ps.
- Average bin width: 60 ps.

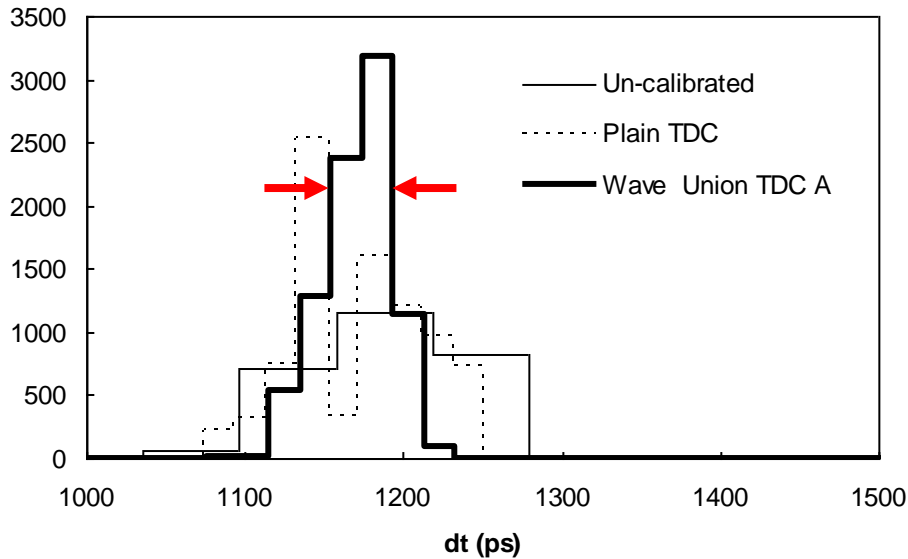
■ Wave Union TDC A:

- Max. bin width: 65 ps.
- Average bin width: 30 ps.

1: Unleash



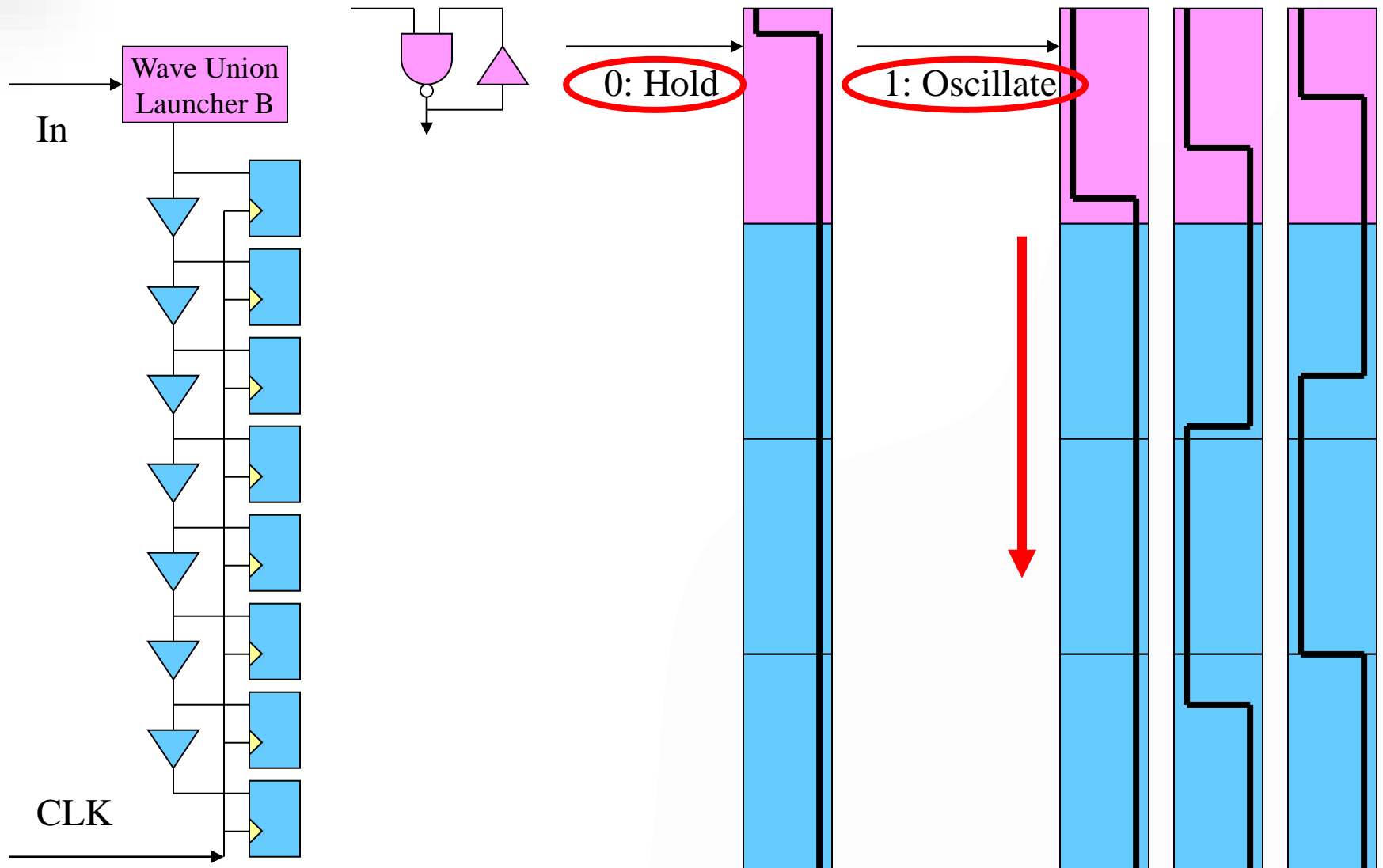
WaveUnion A (Jinyuan Wu @Fermilab)



- Plain TDC:
 - delta t RMS width: 40 ps
 - 25 ps single hit

- Wave Union TDC A:
 - deltat RMS width: 25 ps
 - 17 ps single hit

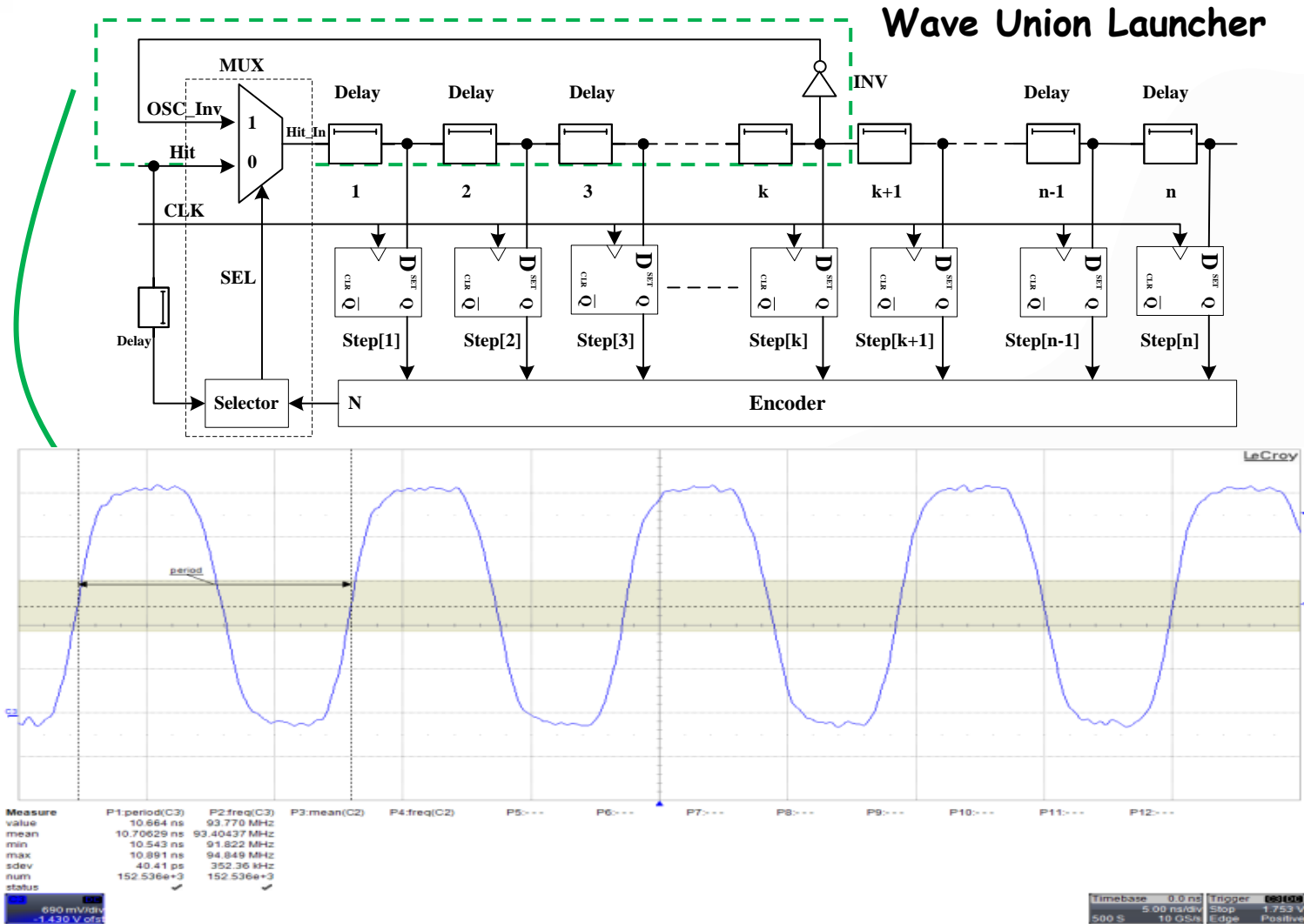
WaveUnion B (Jinyuan Wu @Fermilab)



Does more oscillation cycles always mean better performance?

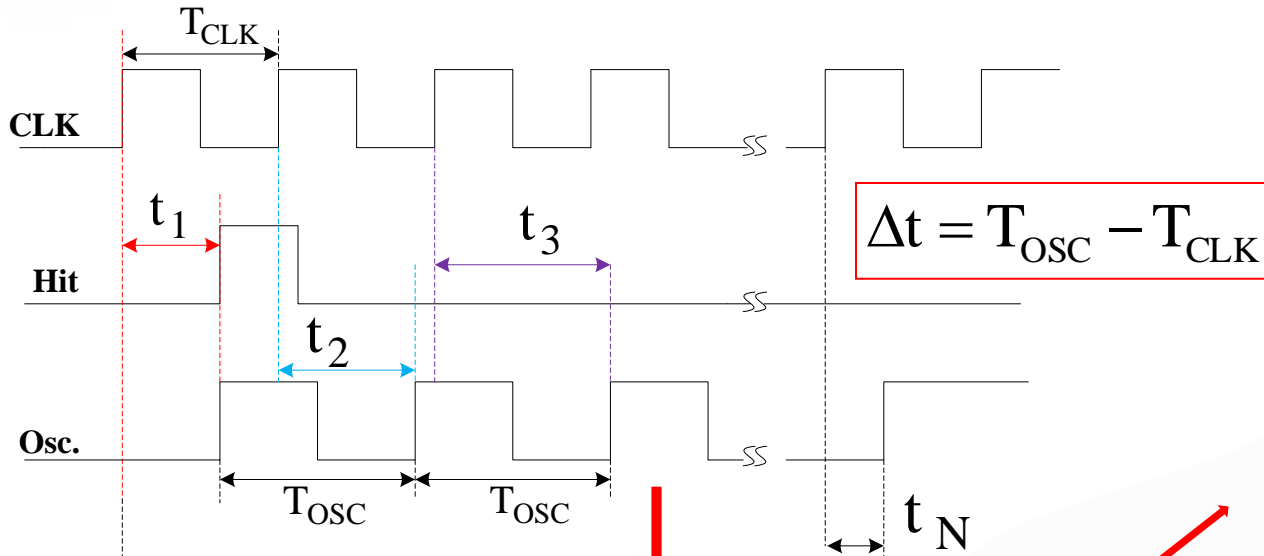
WaveUnion B (USTC)

Principle of the 10-ps FPGA TDC

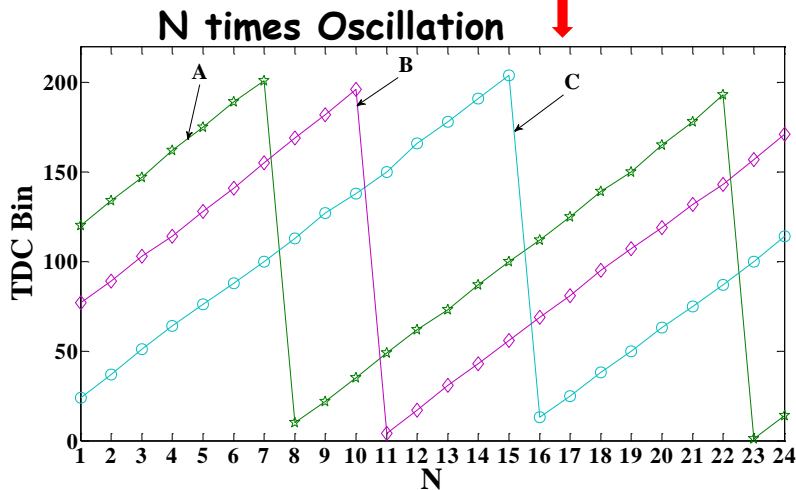


WaveUnion B (USTC)

Signal Processing of the Raw TDC time



$$\begin{cases} t_{01} = t_1 \\ t_{02} = t_2 - \Delta t \\ t_{03} = t_3 - 2\Delta t \\ \dots \\ t_{0k} = t_k - (k-1)\Delta t \\ \dots \\ t_{0N} = t_N - (N-1)\Delta t \end{cases}$$



$$t_0 = \frac{1}{N} \times \sum_{i=1}^N t_{0i}$$

WaveUnion B (USTC)

Signal Processing of the multi-averaging TDC

➤ RMS timing precision (σ_{delay}) vs. N

- Non-uniformed distribution of the carry chain delay (σ_{cell})
- Random uncertainty of the oscillation period (σ_{osc})
- Other contributors, e.g. the steady of the clock (σ_{other})

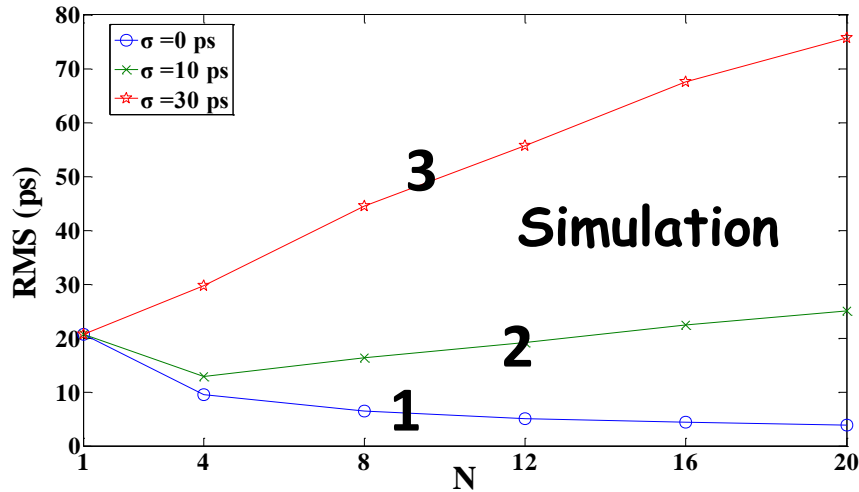
$$\sigma_{\text{delay}} = \sqrt{\frac{N-1}{4} \times \sigma_{\text{osc}}^2 + \frac{1}{N} \times \sigma_{\text{cell}}^2 + \sigma_{\text{other}}^2}$$

Three possible cases:

- Case 1: $\sigma_{\text{osc}} \ll \sigma_{\text{cell}}$ $\sigma_{\text{delay}} \approx \frac{1}{\sqrt{N}} \times \sigma_{\text{cell}}$
- Case 2: $\sigma_{\text{osc}} \approx \sigma_{\text{cell}}$ The best timing @ $N = \left[2 \times \frac{\sigma_{\text{cell}}}{\sigma_{\text{osc}}} \right]$
- Case 3: $\sigma_{\text{osc}} \gg \sigma_{\text{cell}}$ $\sigma_{\text{delay}} \approx \frac{\sqrt{N-1}}{2} \times \sigma_{\text{osc}}$

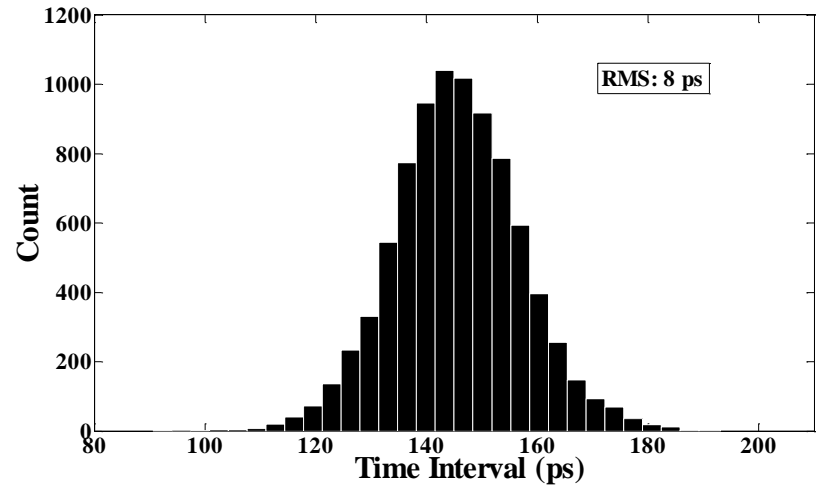
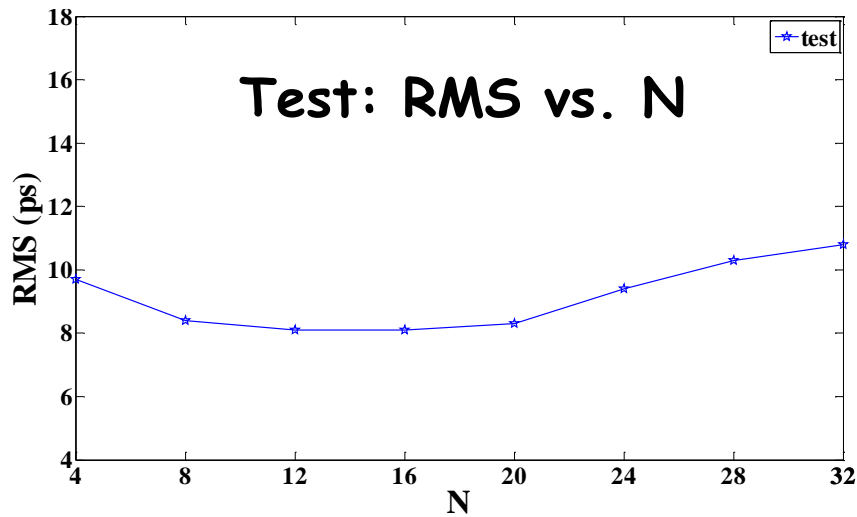
WaveUnion B (USTC)

Simulation and Test



- Case 1: $\sigma_{osc} \ll \sigma_{cell}$
- Case 2: $\sigma_{osc} \approx \sigma_{cell}$
- Case 3: $\sigma_{osc} \gg \sigma_{cell}$

Actual implementation falls in to Case 2



Progress by now: ~ 10 ps

WaveUnion B (USTC)

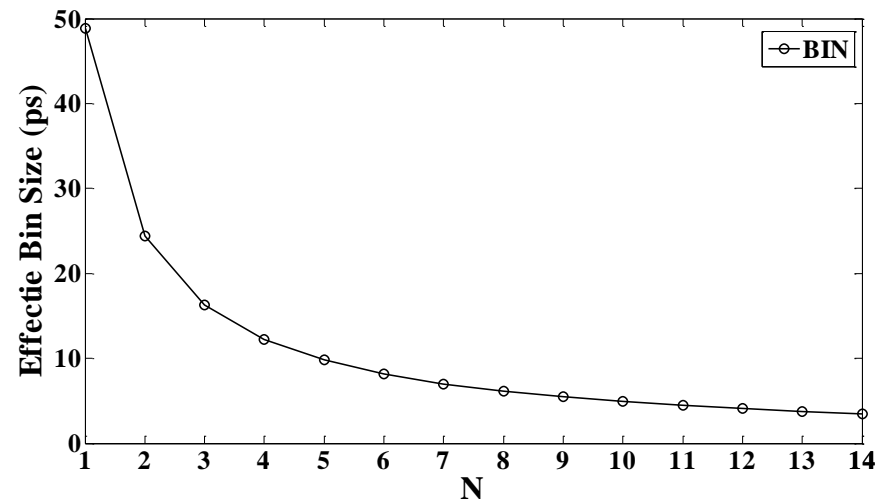
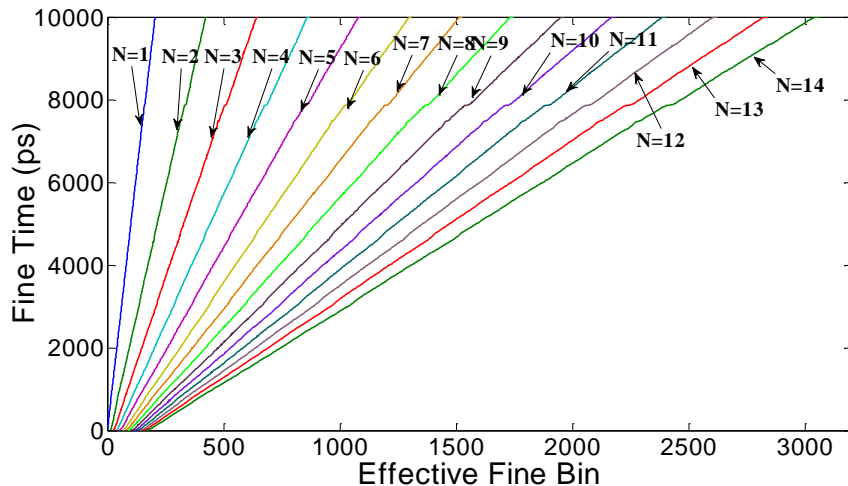
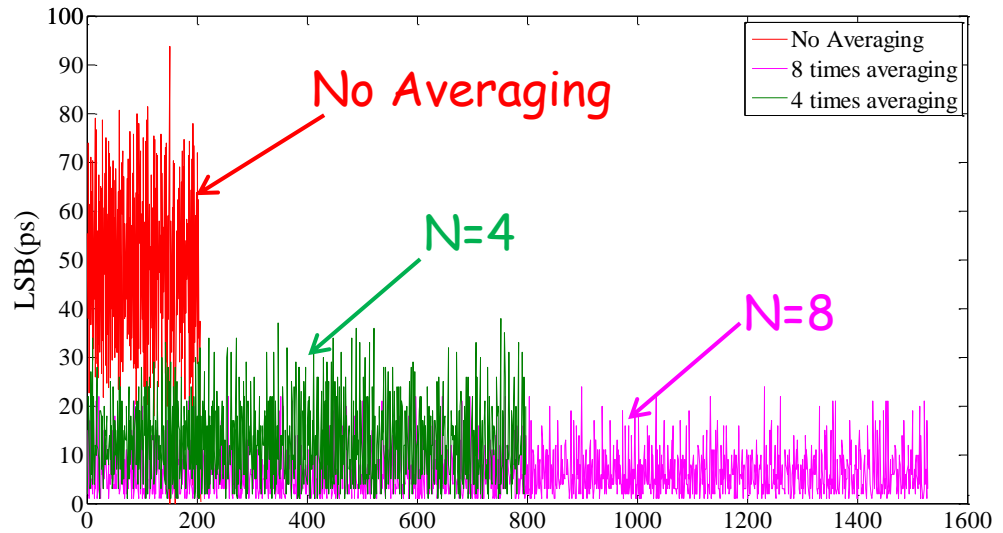
Simulation and Test

Bin size vs. N

Effective Bin size:

$$C_{\text{eff}} = \sum_{i=1}^N C_i$$

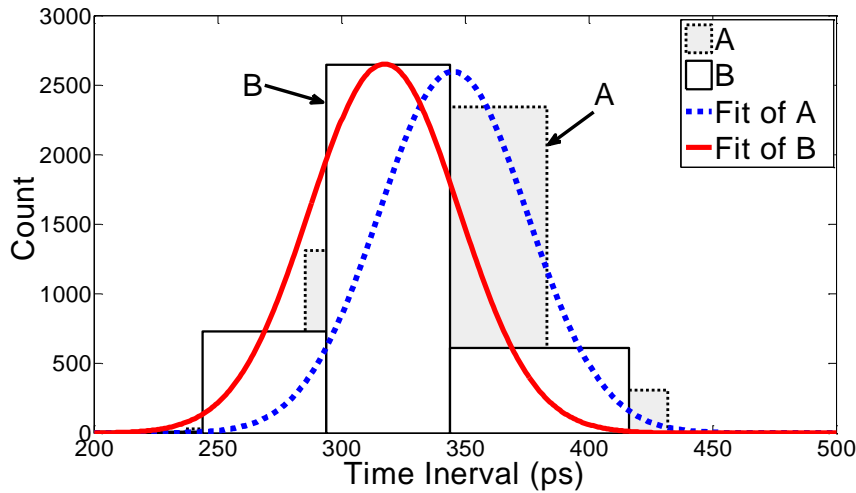
Scales as $1/N$



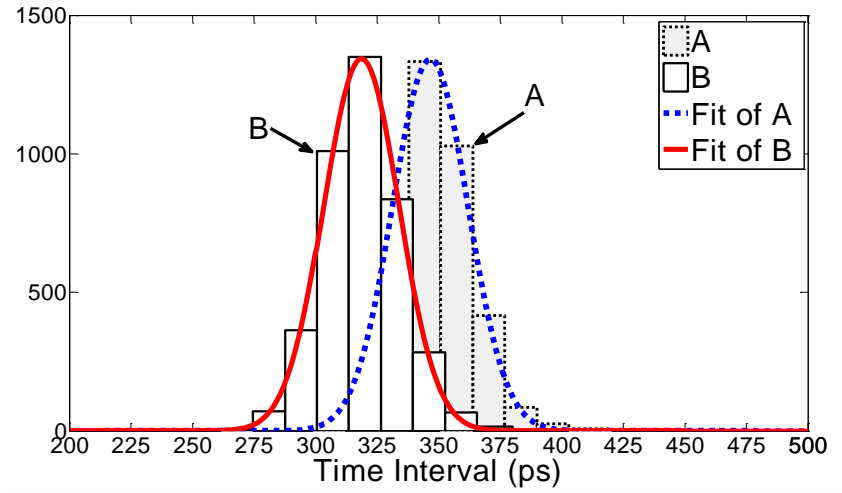
WaveUnion B (USTC)

➤ Pros and Cons

✓ Larger N results in smaller bin size, lower timing precision



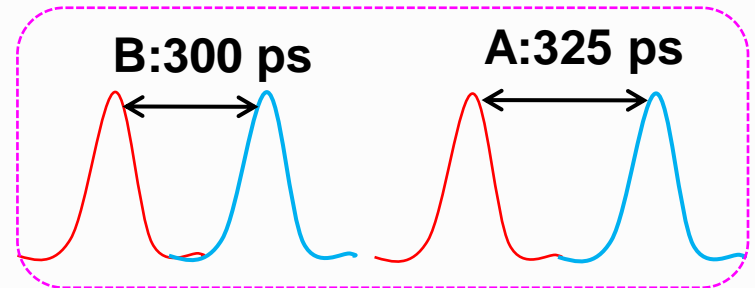
No Averaging



N=4

× Larger N results in larger dead time

$$\sim (N+1) * T_{CLK}, \quad \text{☹}$$



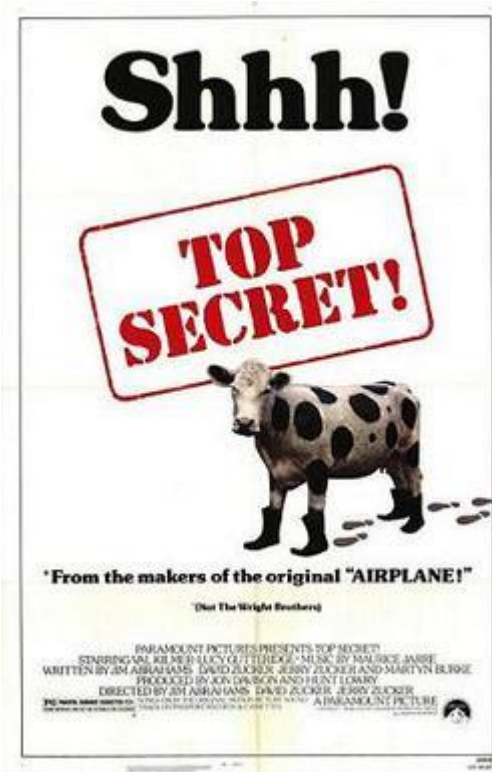
Trade-off should be made between TDC timing performance and N

● Outlook

- sub-10 ps resolution/precision time digitization already achieved in FPGAs (**15 years ago**)
→ is it possible to overcome the 1 ps barrier?
- TDL approach is the most popular one in achieving sub-10 ps resolution, but not the only one, the choice of architecture is a trade off among power, resource utilization ...
- Timing resolution/precision is just one single measure of timing performance, among linearity, **power**, resource utilization...
→ Nowadays, FPGAs typically not limited by configuration logic resources, thus more attention on **power efficiency** might be necessary.

Quiz

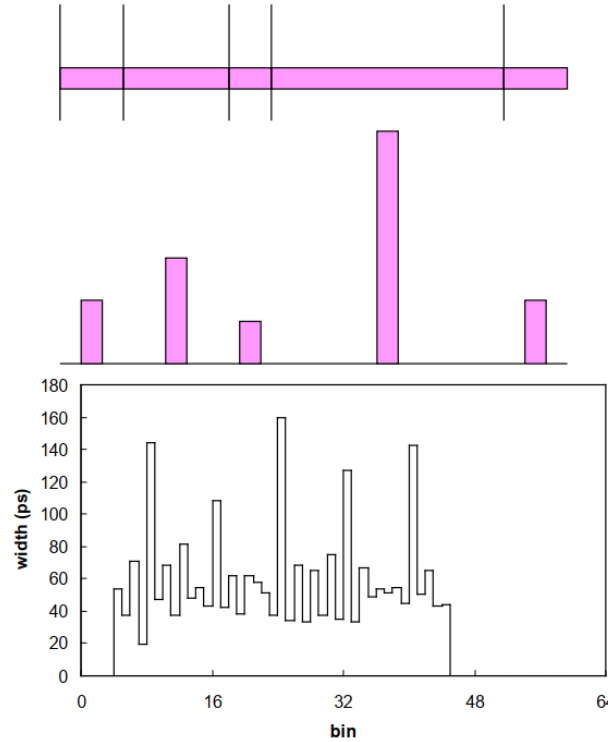
Top secrets before class...



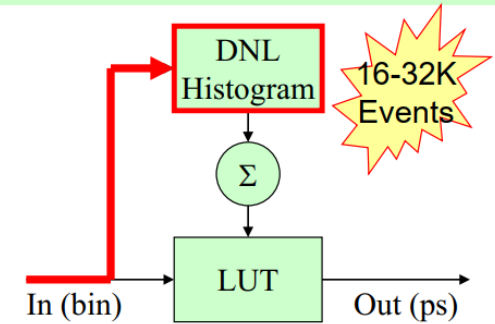


Bin-by-Bin Code Density Calibration

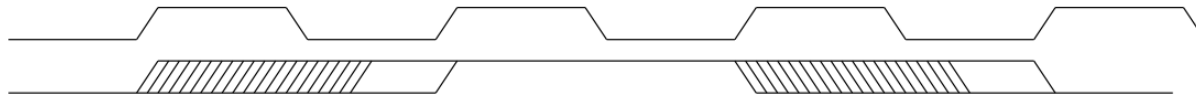
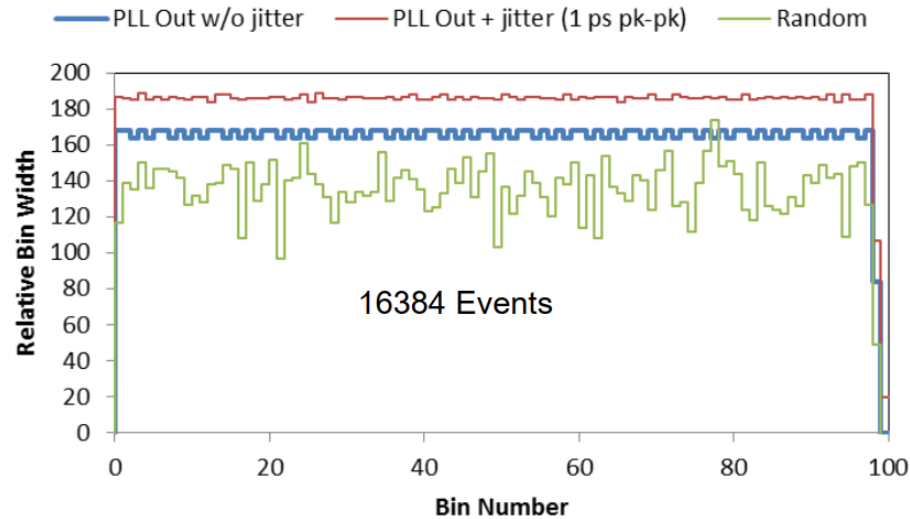
- TDC digitize hits with evenly spread arrival times.
- A histogram is booked.
- Number of counts in each bin is proportional to the width of the bin.



- In the auto calibration process, a bin width histogram (DNL histogram) is first booked.
- More counts are accumulated in wider bins.



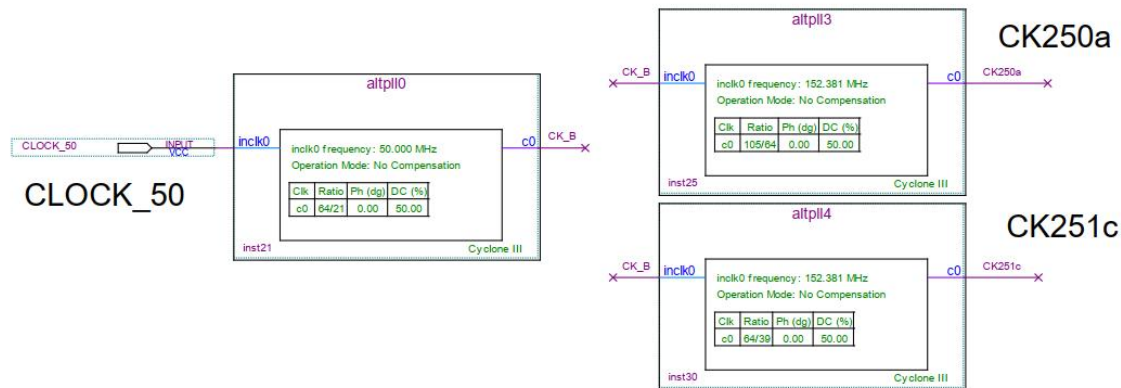
Random != Evenly Spread



- The random hits have statistical fluctuation, and the variation is large with limited calibration events.
- Hits with evenly spread arrival times are more desirable for calibration.



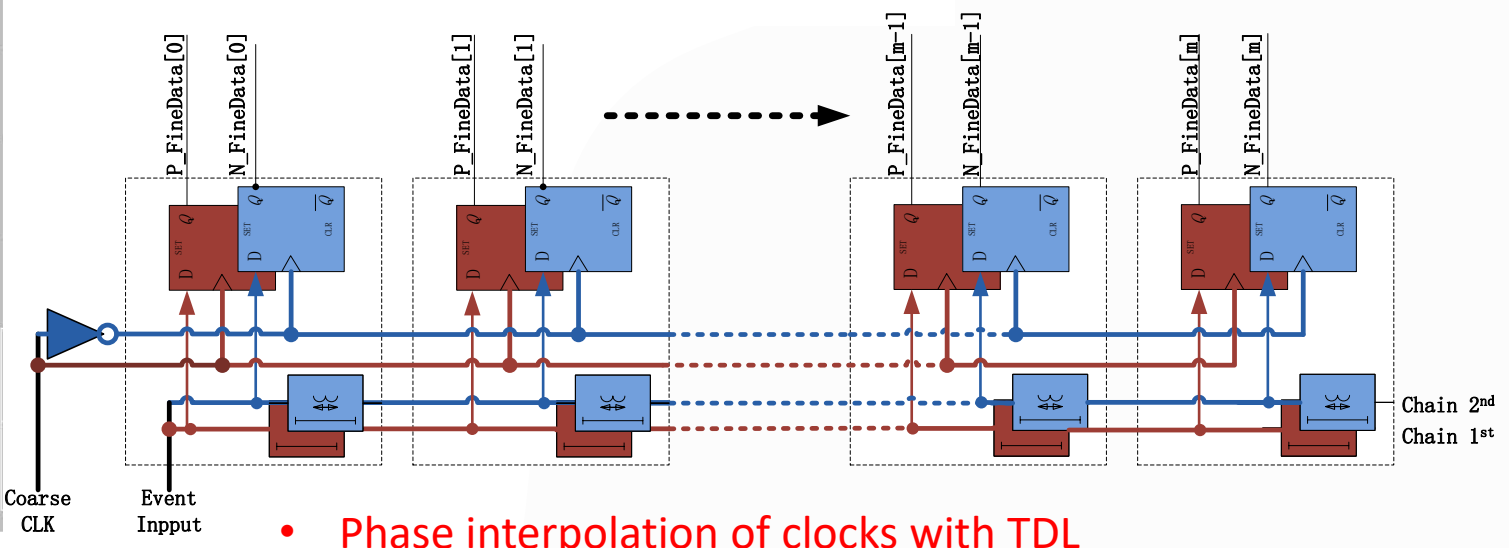
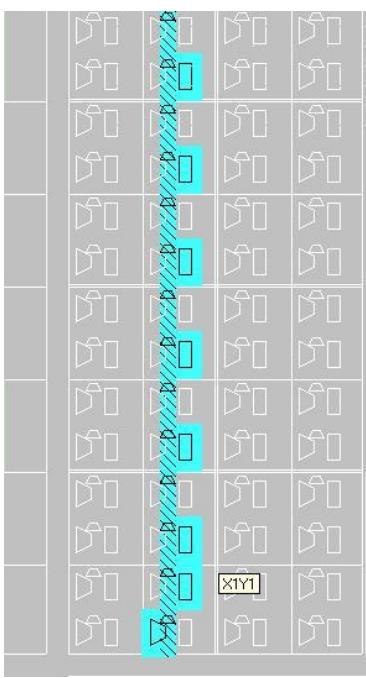
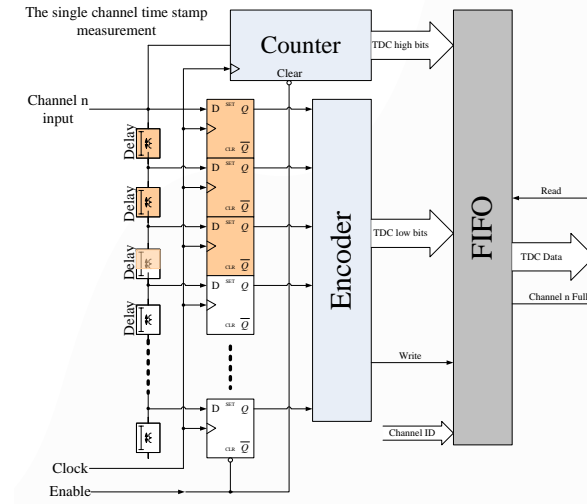
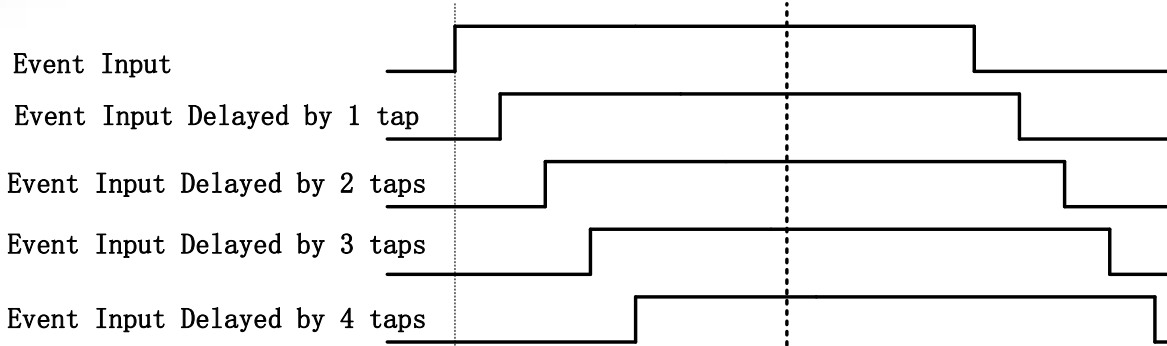
Generating Clocks with Smooth Phase Drift Using Cascaded PLL



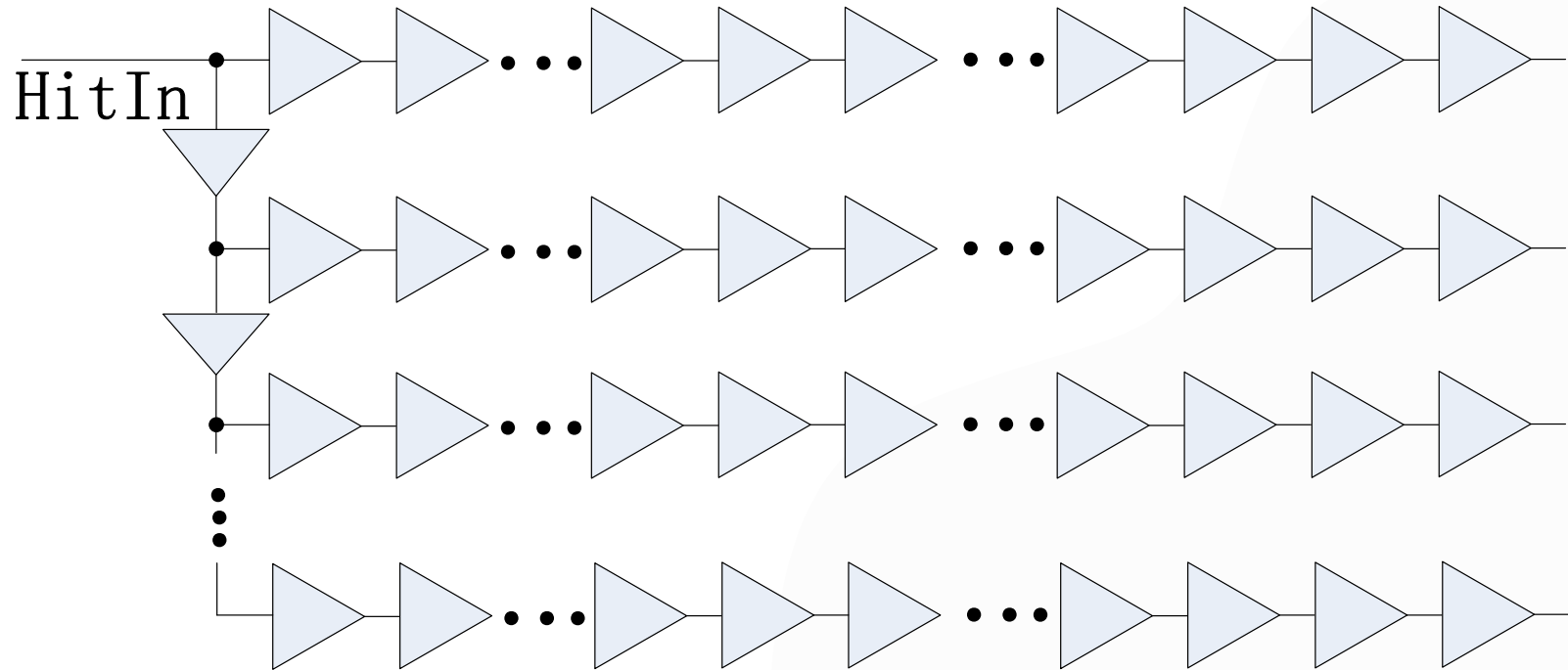
- Two stages of PLL circuits are cascaded together.
 - $f(\text{CK250a}) = 250 \text{ MHz}$
 - $f(\text{CK251c}) = 250.06 \text{ MHz}$
 - $f(\text{CK251c}) = (4096/4095) * f(\text{CK250a})$
 - $T(\text{CK250a}) - T(\text{CK251c}) = 0.97 \text{ ps}$.

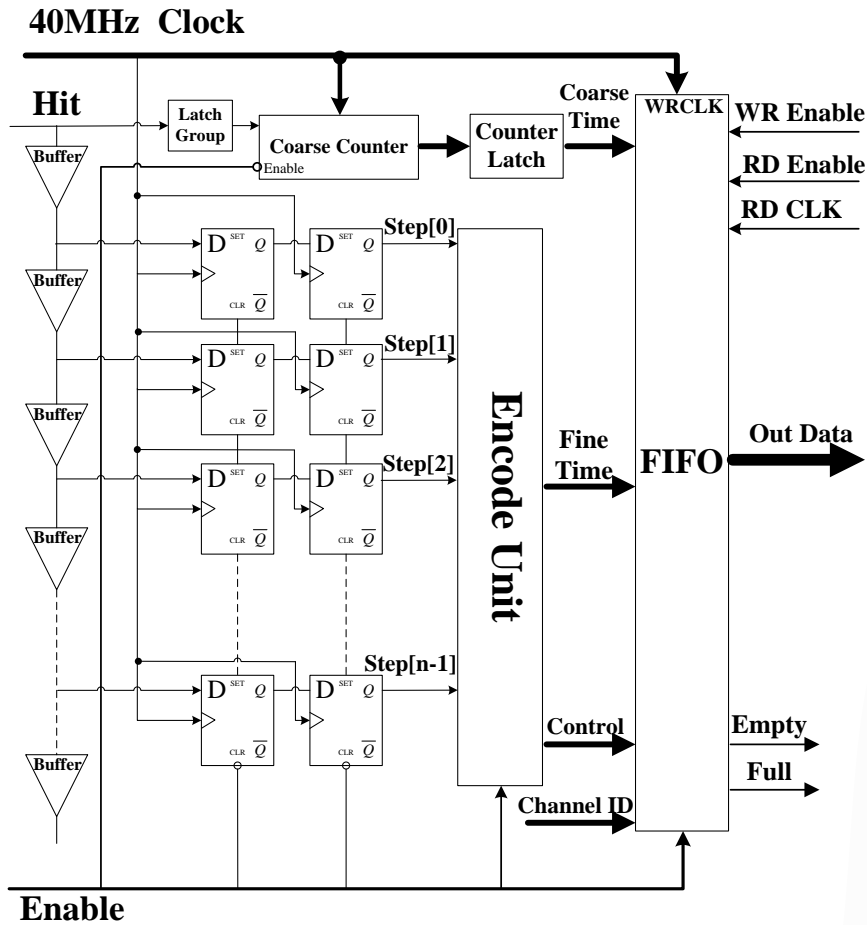
What if TDL is not long enough?

- Typically it means clock period is relatively large!



- Phase interpolation of clocks with TDL





• ACTEL FPGA

- Flash

- IGLOO、PROAISC3(E)

- Anti-fuse

- AXCELERATOR、SX_A、RTAX_SSL

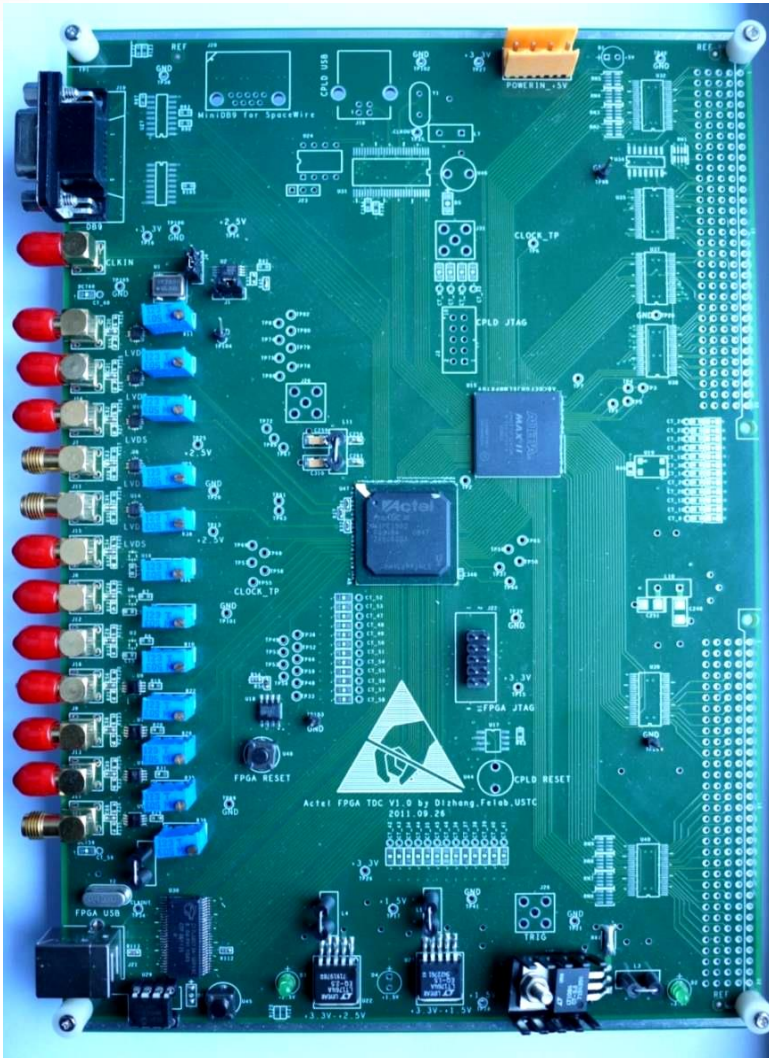
• TDC

- Flash Buffer

- Bin Size~440ps

- Anti-fuse

- Bin Size ~ 80ps



ACTEL FPGA : A3PE1500

DNL of ACTEL-FPGA-TDC ch3

