The upgrade of the ATLAS Trigger and Data Acquisition system for the High Luminosity LHC

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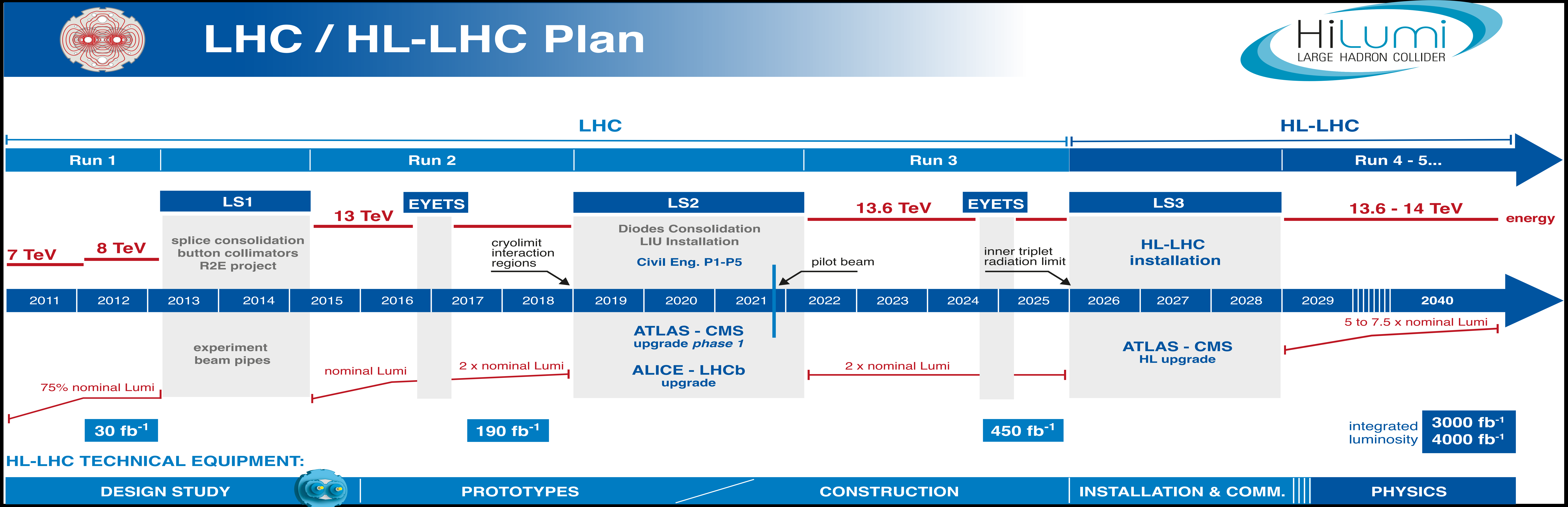
on behalf of the ATLAS Collaboration

LHC and HL-LHC plans

High Luminosity LHC web page

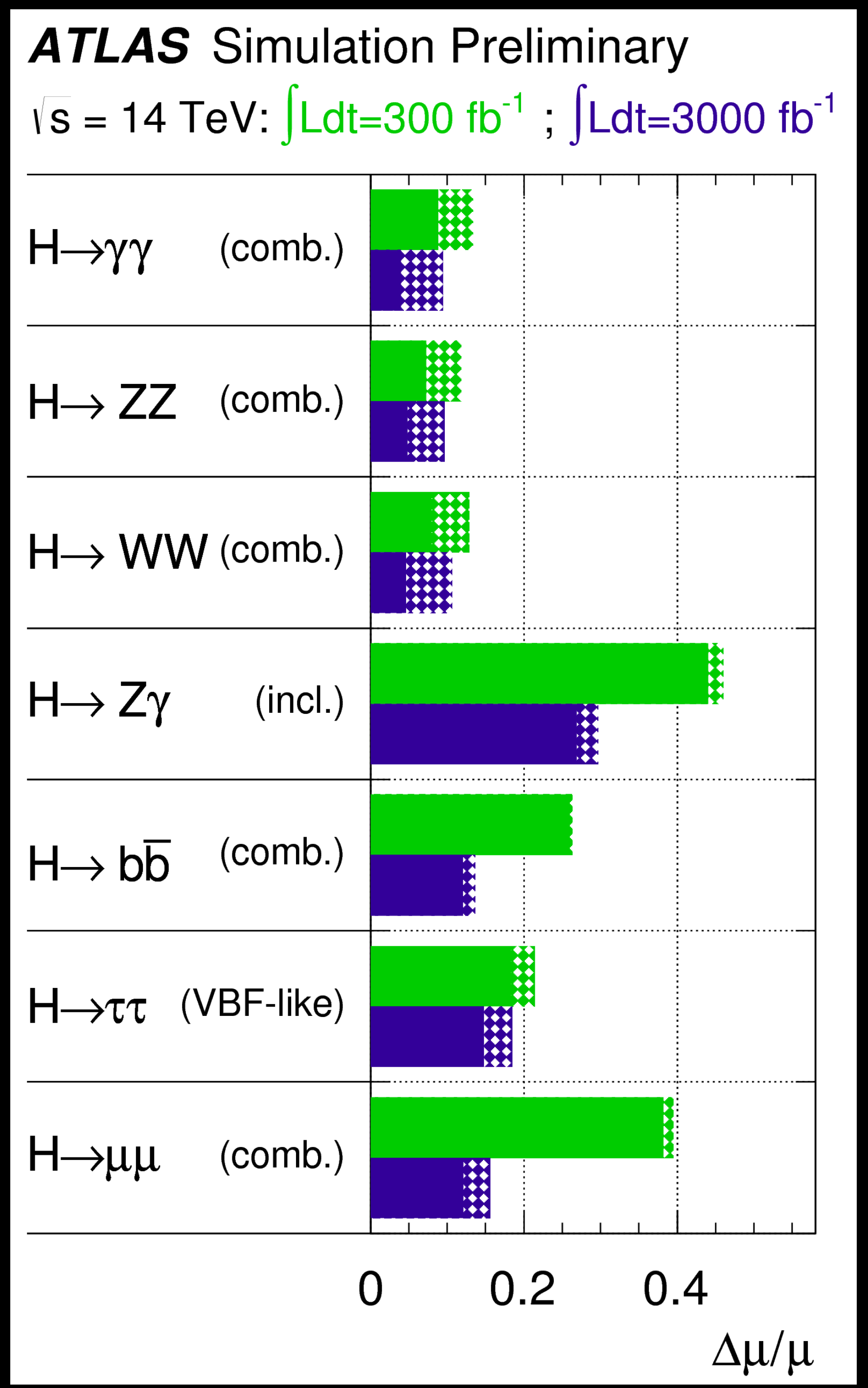


- LHC plan update (February 2022)
- Run3 LHC luminosity: 2×10^{34} $cm^{-2}s^{-1}$ @ 13.6 TeV; integrated luminosity: 450 fb^{-1}
- Run4-Run5 HL-LHC luminosity: up to 7.5×10^{34} $cm^{-2}s^{-1}$ @ 14 TeV; integrated luminosity: 4000 fb^{-1}
- Technological challenge on the experiments coming from such a large dataset, rates and pile-up

ATLAS physics plans for Run4

- Higgs boson and SM processes precision measurements
- SM rare processes measurements (H -> μμ, self-coupling Higgs from double Higgs events, …)
- High density QCD measurements (from heavy-ion and pp collisions)
- Forward physics (from exclusive production processes tagging)
- Beyond SM physics (SUSY, dark matter, long lived particles, …)
- …

ATL-PHYS-PUB-2018-010



ATL-PHYS-PUB-2013-003, 2014-007

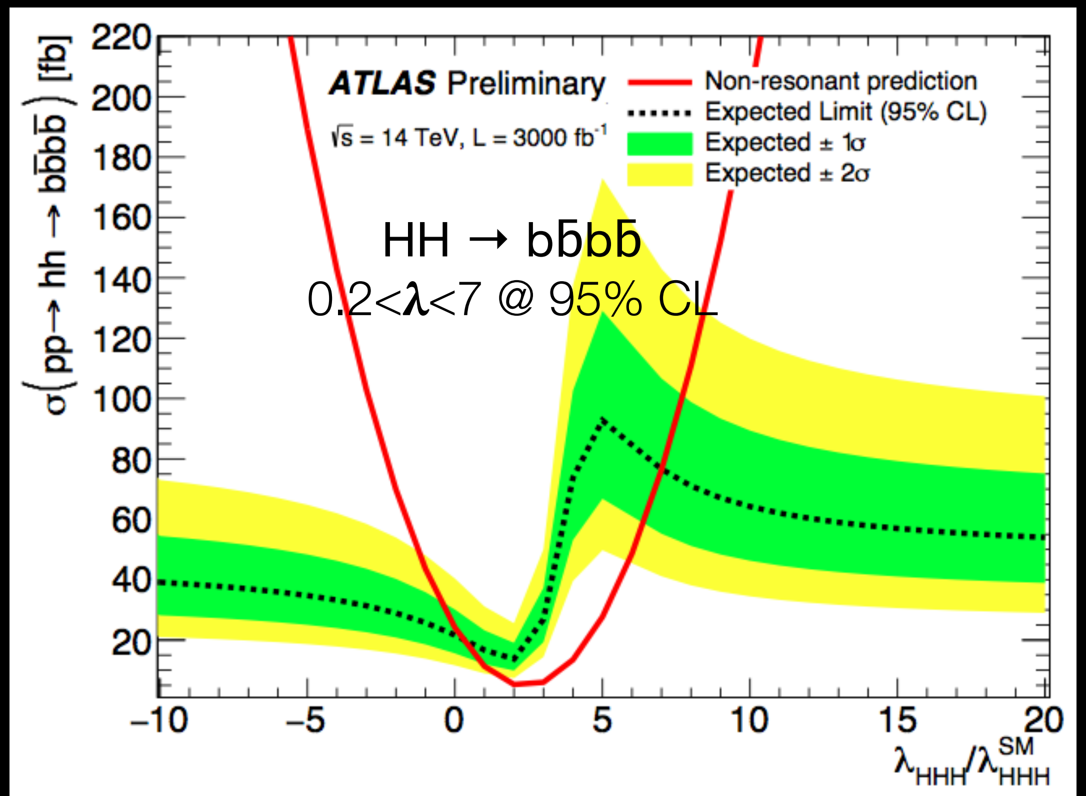
ATLAS Mass reach for Exotic signatures

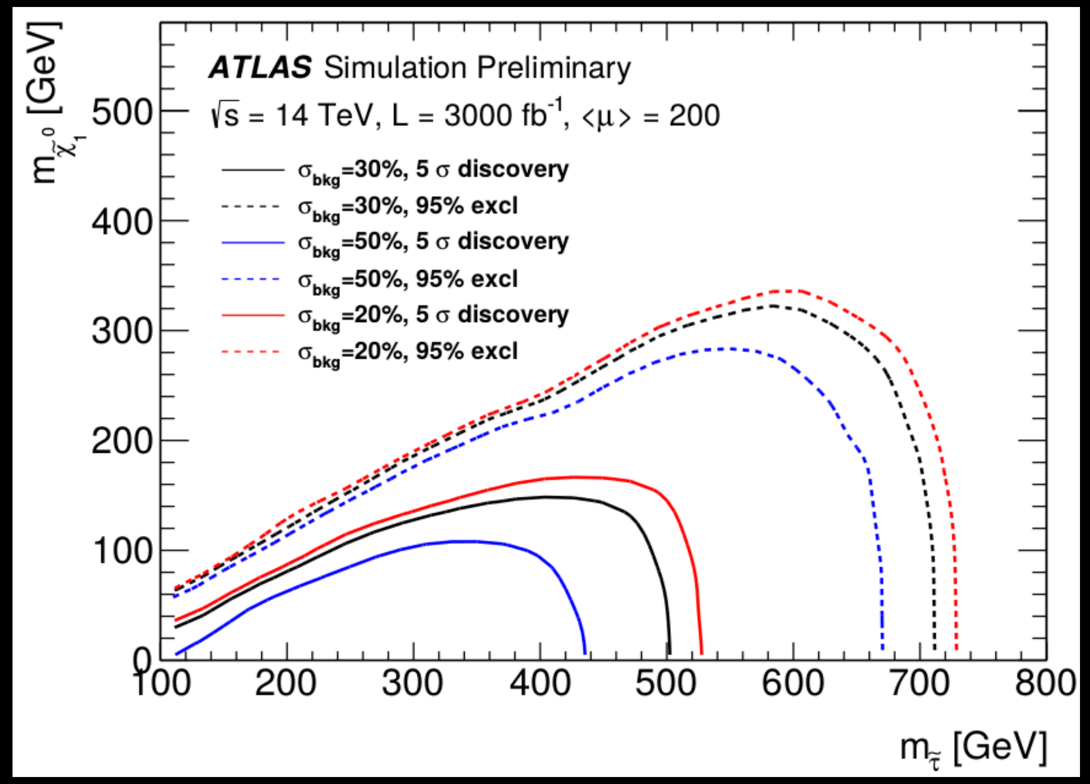
ATLAS @14 TeV	Z' → ee SSM 95% CL limit	g_{KK} → t t RS 95% CL limit	Dark matter M* 5σ discovery
300 fb^{-1}	6.5 TeV	4.3 TeV	2.2 TeV
3000 fb^{-1}	7.8 TeV	6.7 TeV	2.6 TeV

ATL-PHYS-PUB-2014-010 , 2013-011, 2015-032

ATLAS Mass reach for SUSY particles

ATLAS projection	gluino mass	squark mass	stop mass	sbottom mass	χ_1^+ mass WZ mode	χ_1^+ mass WH mode
300 fb^{-1}	2.0 TeV	2.6 TeV	1.0 TeV	1.1 TeV	560 GeV	None
3000 fb^{-1}	2.4 TeV	3.1 TeV	1.2 TeV	1.3 TeV	820 GeV	650 GeV



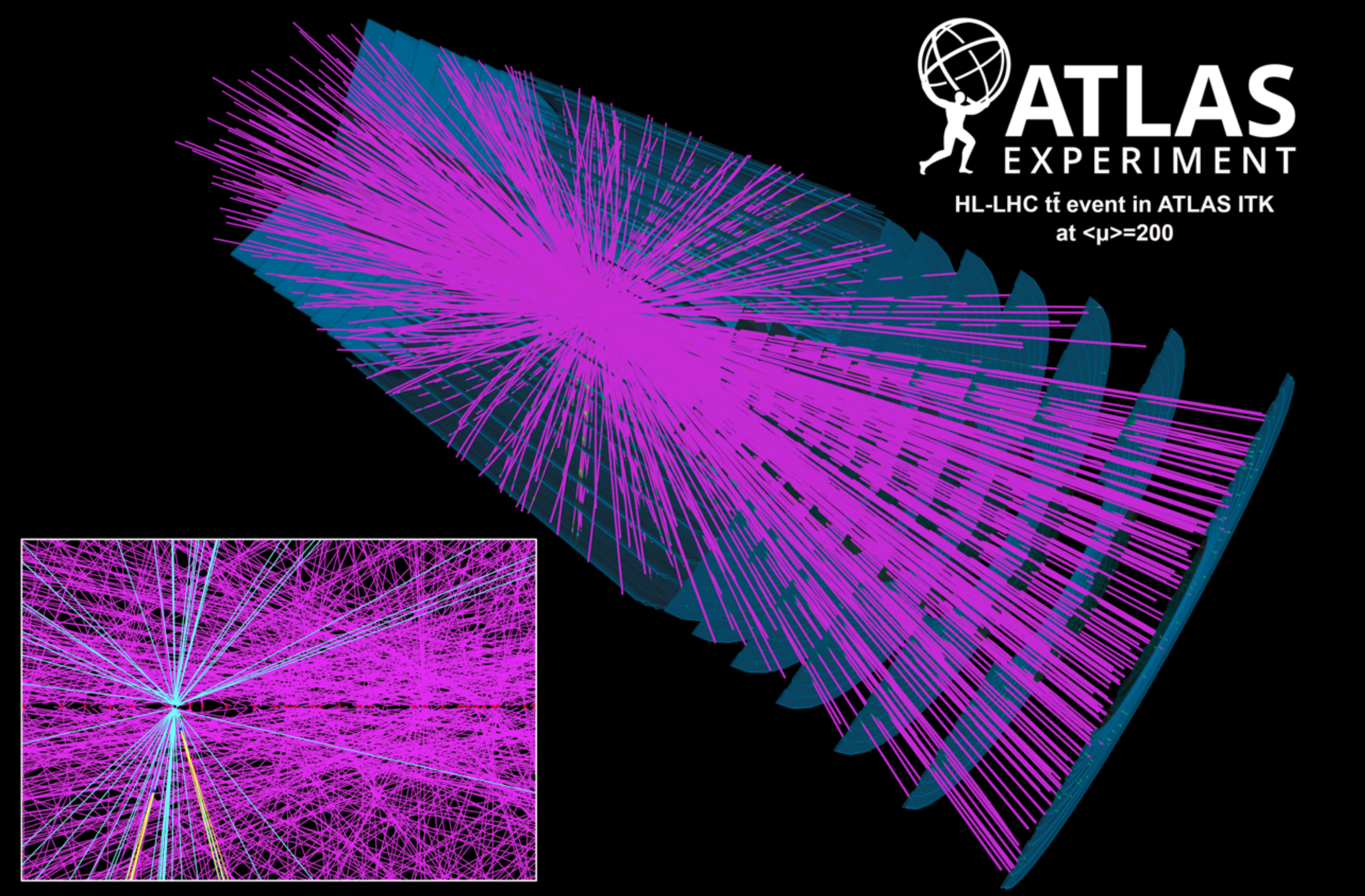


Increasing luminosity impact on ATLAS

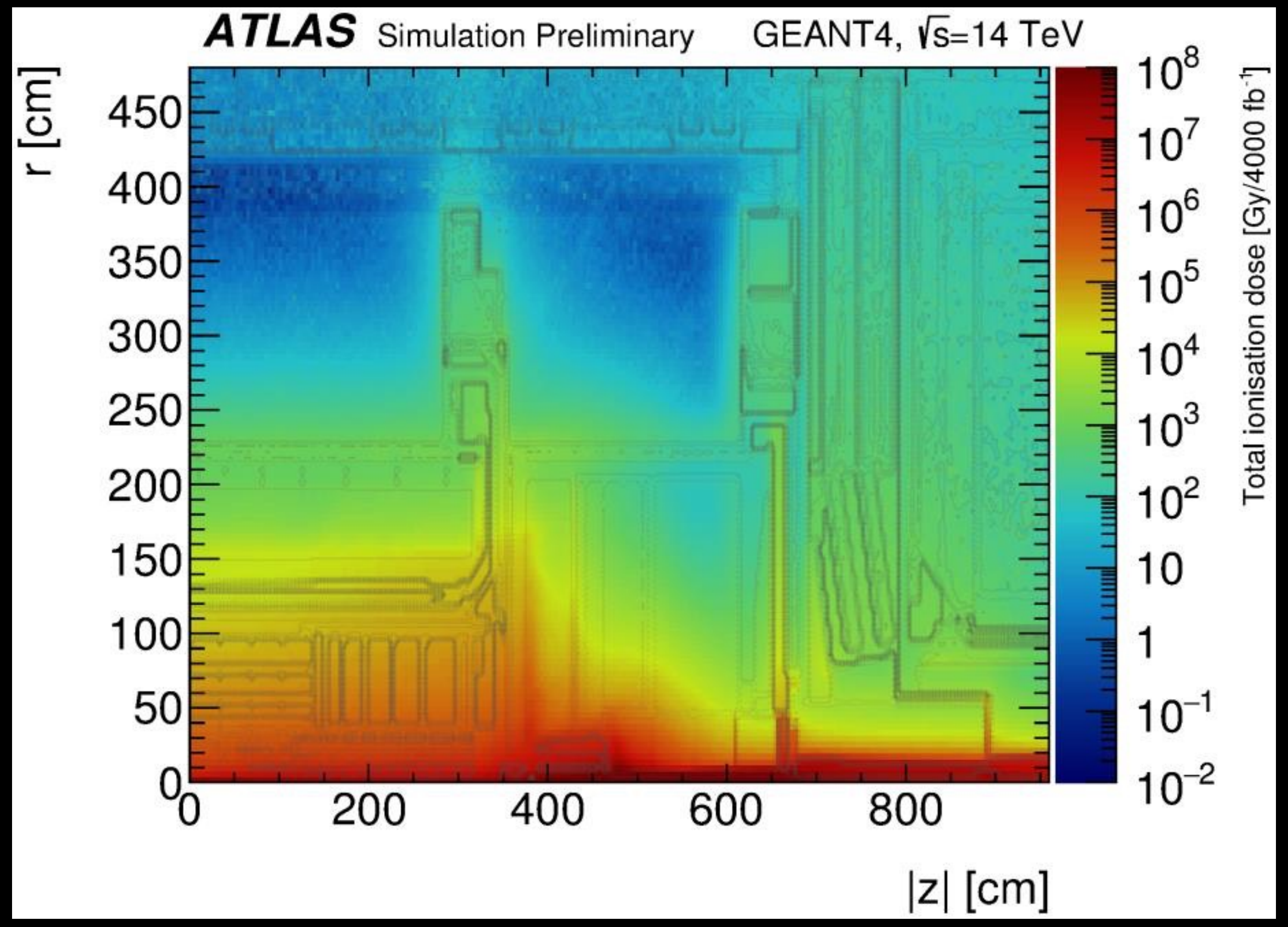
- High luminosity is needed to achieve physics goals
- The experiment has to stand the Run4 foreseen peak luminosity of 7.5 x 10^{34} cm^{-2} s^{-1}
  - high pile-up ~200 collisions/crossing
  - high radiation levels, up to ~10^{16} neq/cm^2, 10 MGy
- Requirements:
  - maintain good physics performances in the challenging environment
  - keep acceptable trigger rate for low p_T threshold
  - mitigate impact of pile-up up to high η

ATLAS pileup for Run4

ATLAS public results

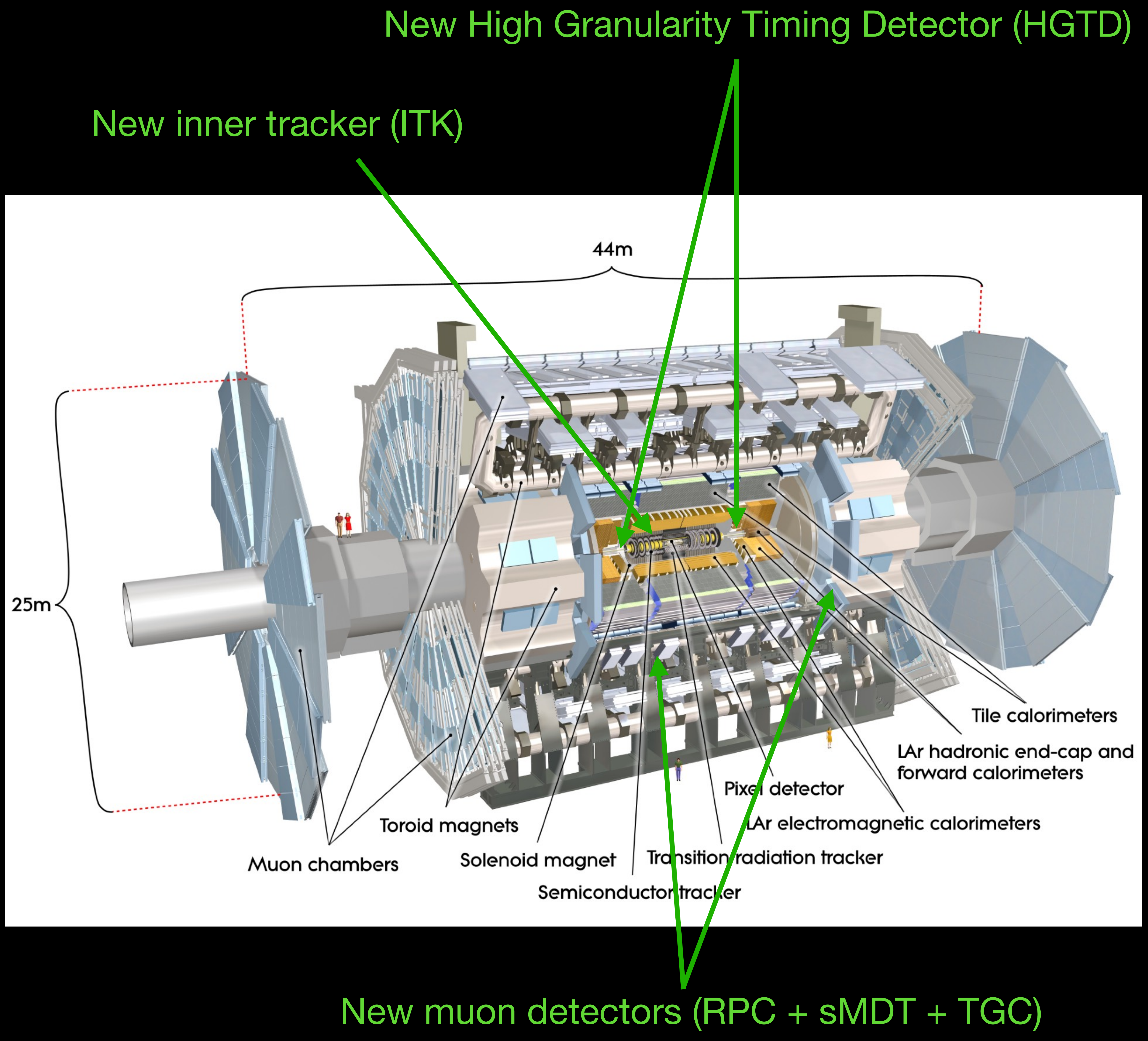


ATLAS TID radiation levels for Run4



ATLAS upgrades for Run4

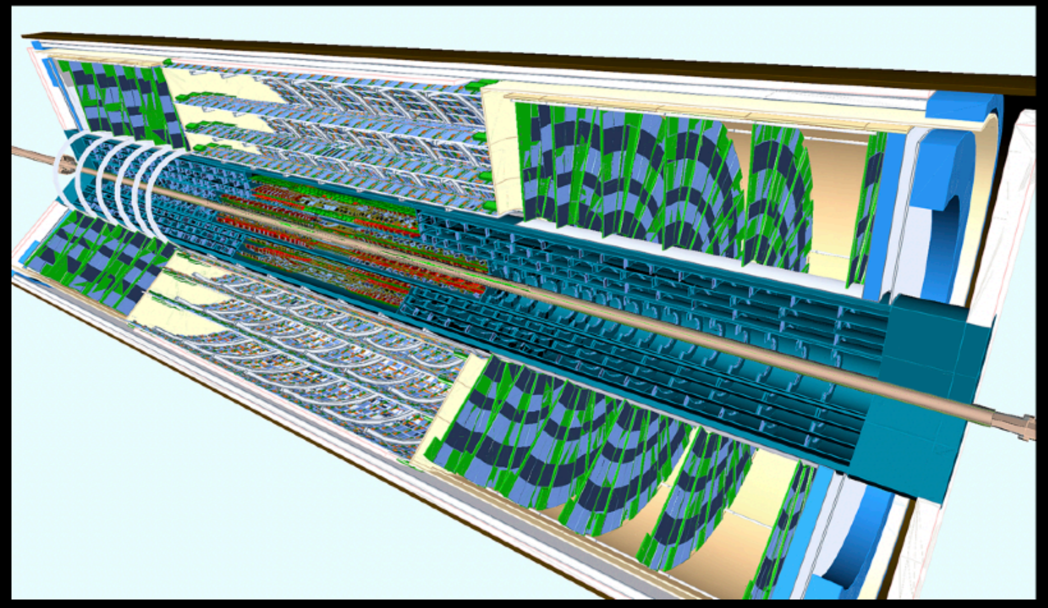
- Detector upgrades:
  - ITk: silicon inner tracker (pixels + strip detector) with η coverage up to 4
  - RPC and sMDT muon detector in the barrel inner region, sTGC in the end-cap inner region
  - High Granularity Timing Detector in the forward region
  - Calorimeters and muon detectors (TGC/RPC/MDT) front-end readout at 40 MHz
  - Upgrades of luminosity and forward detectors
- TDAQ off-detector electronics:
  - Level-0 hardware trigger: calorimeter, muon, global, CTP (FPGA-based boards)
  - Readout: FELIX for all ATLAS detectors
  - Event Filter processor farm and hardware tracking



Front-end replaced for calorimeters and muon detectors

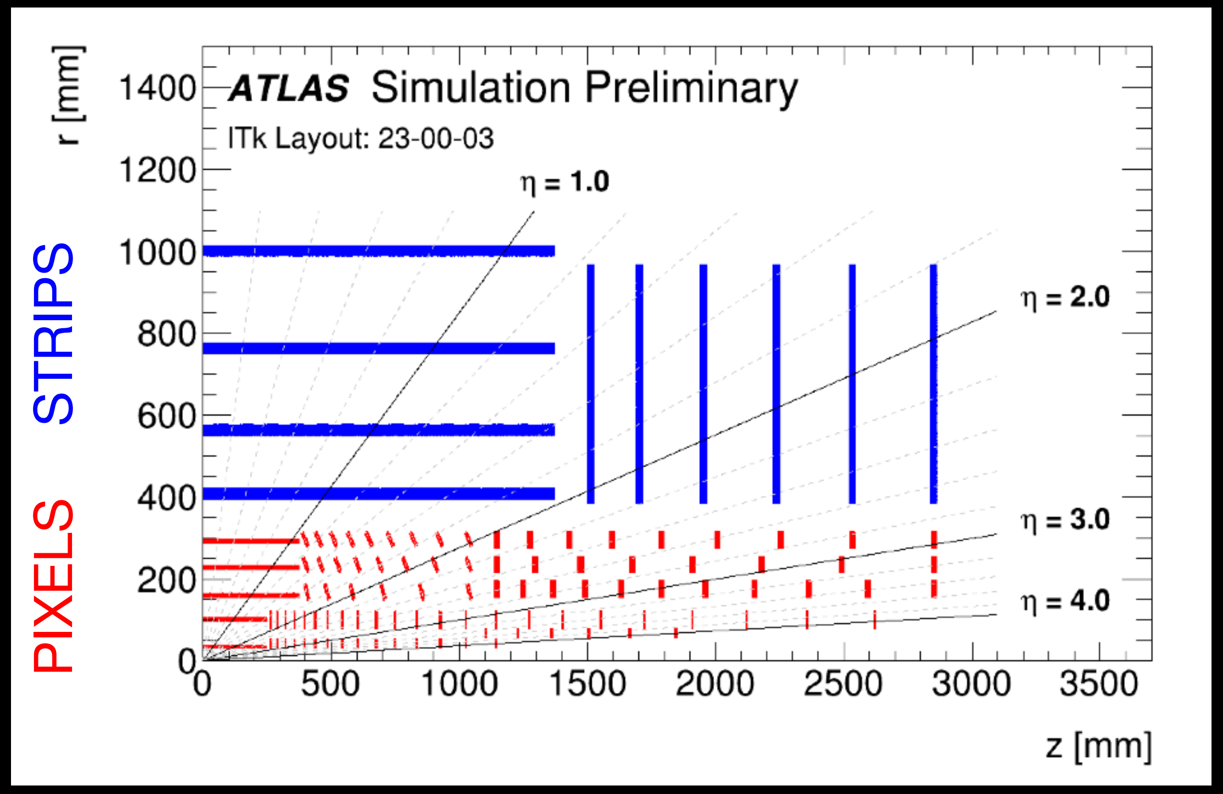
Inner Tracker

- New all-silicon tracking system, extension up to $|\eta| = 4$ ($|\eta| = 2.5$ today)
- Pixel detector at small radius close to the beam line + large area strip tracker surrounding it:
  - Pixels: $|\eta| < 4.0$, 165 m^2, 60M channels, 18k modules (25x100 / 50x50µm^2 pixel size)
  - Strips: $|\eta| < 2.7$, 13 m^2, 5.1G channels, 9.2k modules
- Increased surface and complexity with respect to the present system but reduced quantity of material
- High tracking performances and reconstruction efficiency thanks to the improved granularity, reduced material (multiple scattering) and detector redundancy
- > 99% efficiency for muons with $p_T > 3$ GeV; > 85% efficiency for pions and electrons above 1 GeV, keeping fake rates below 1%
- Rad-hard (10 MGy) pixel and strip front-end readout electronics

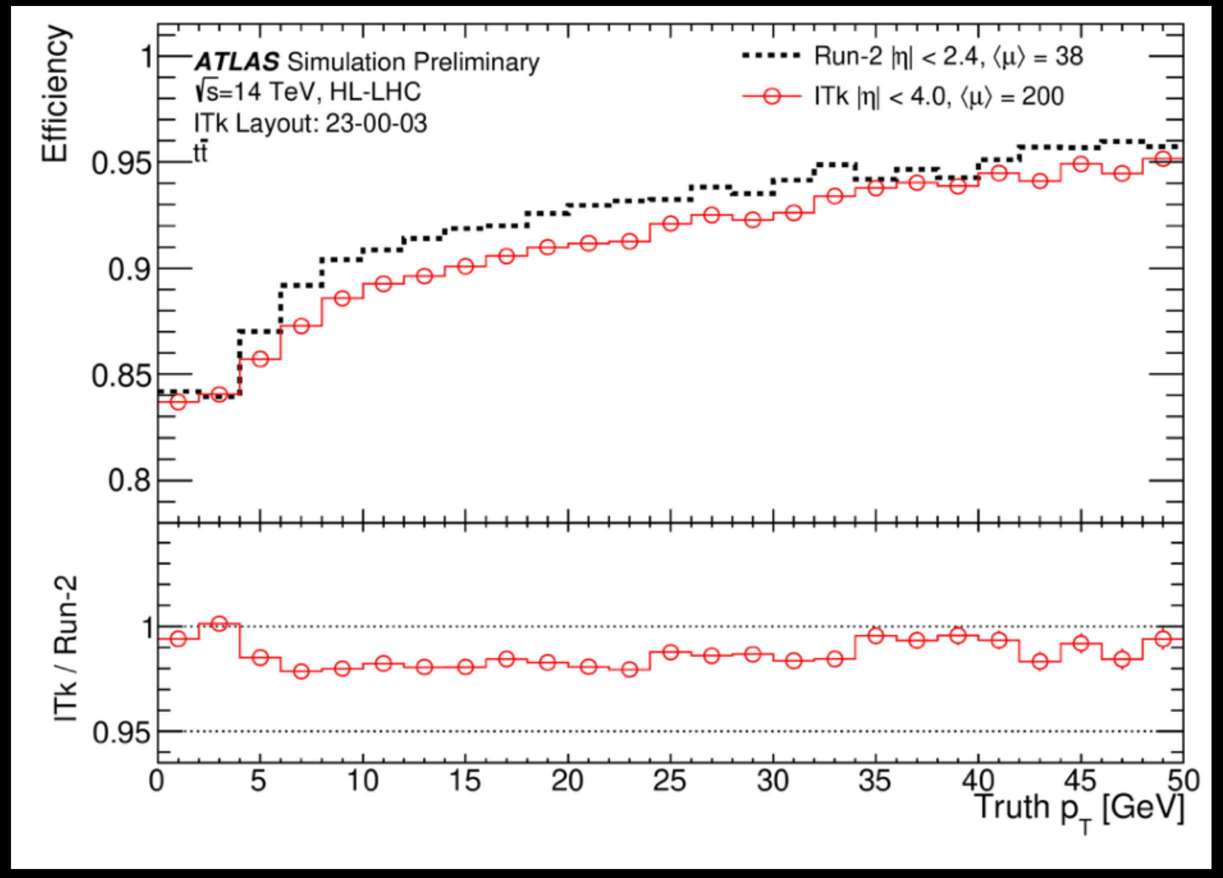


ATLAS-TDR-025-2017

ITK new layout ATL-PHYS-PUB-2021-024

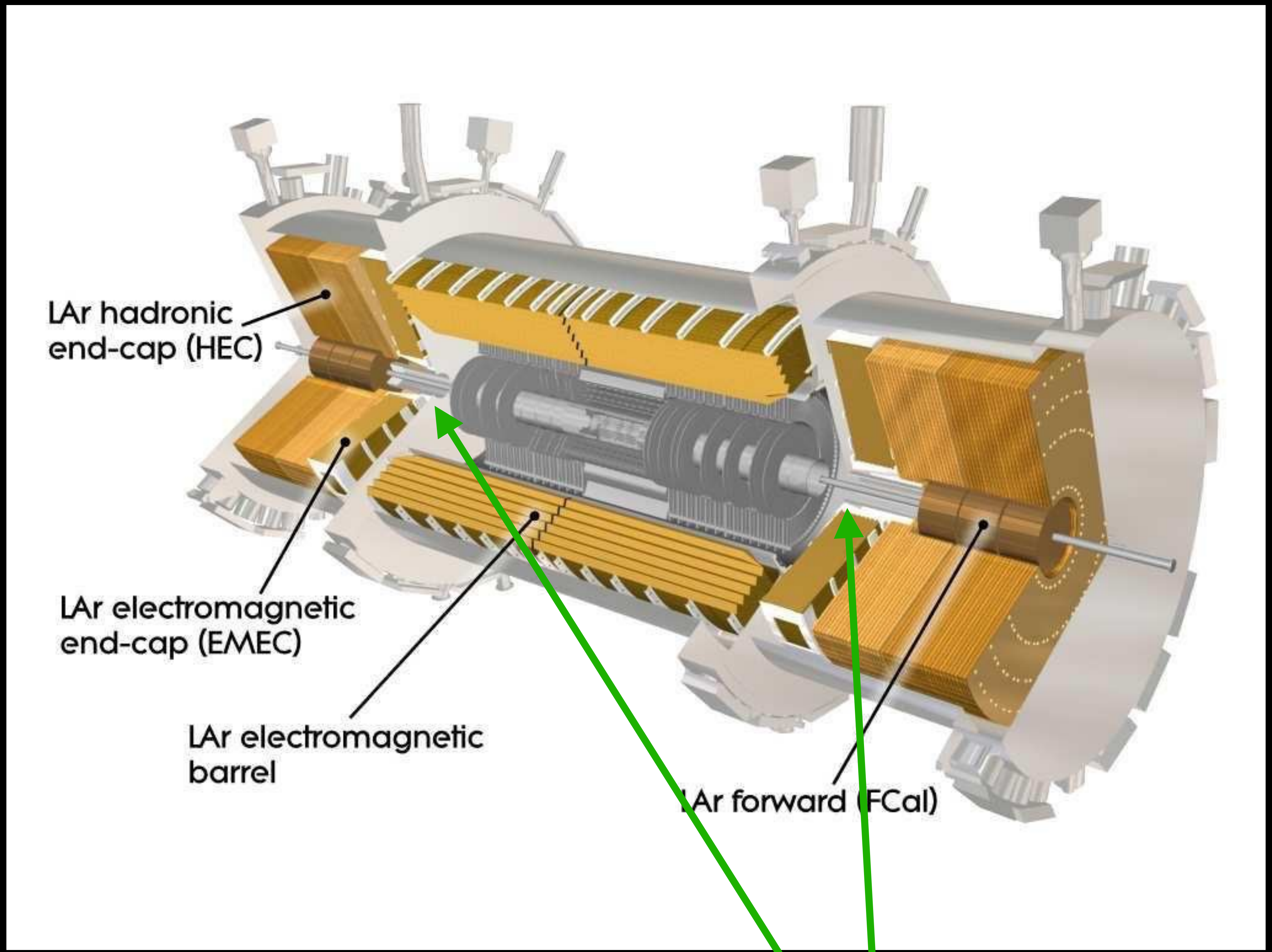


Tracking efficiency for $t\bar{t}$ events with $\langle\mu\rangle$=200 compared with the Run2 detector



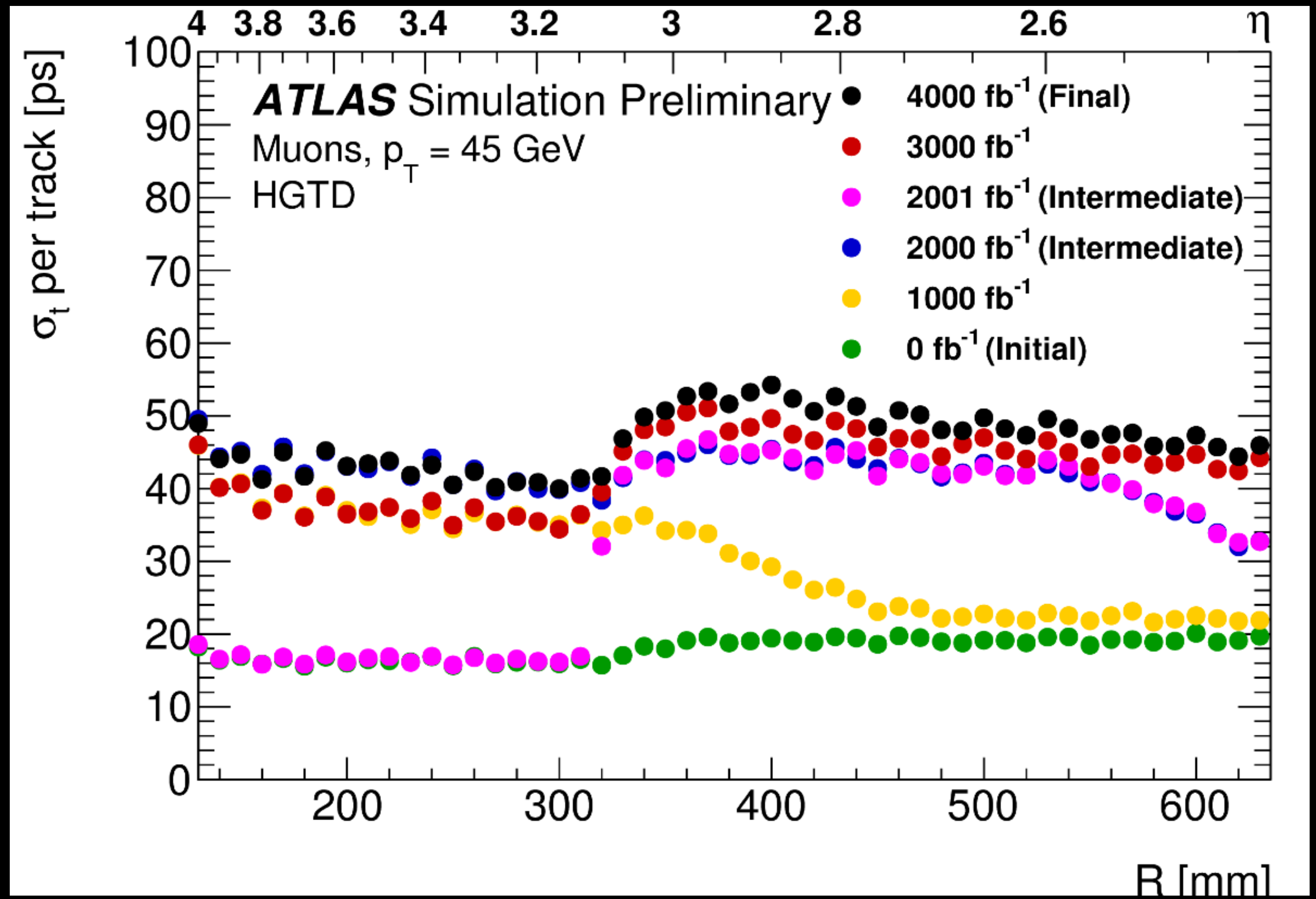
LAr calorimeter and HGTD

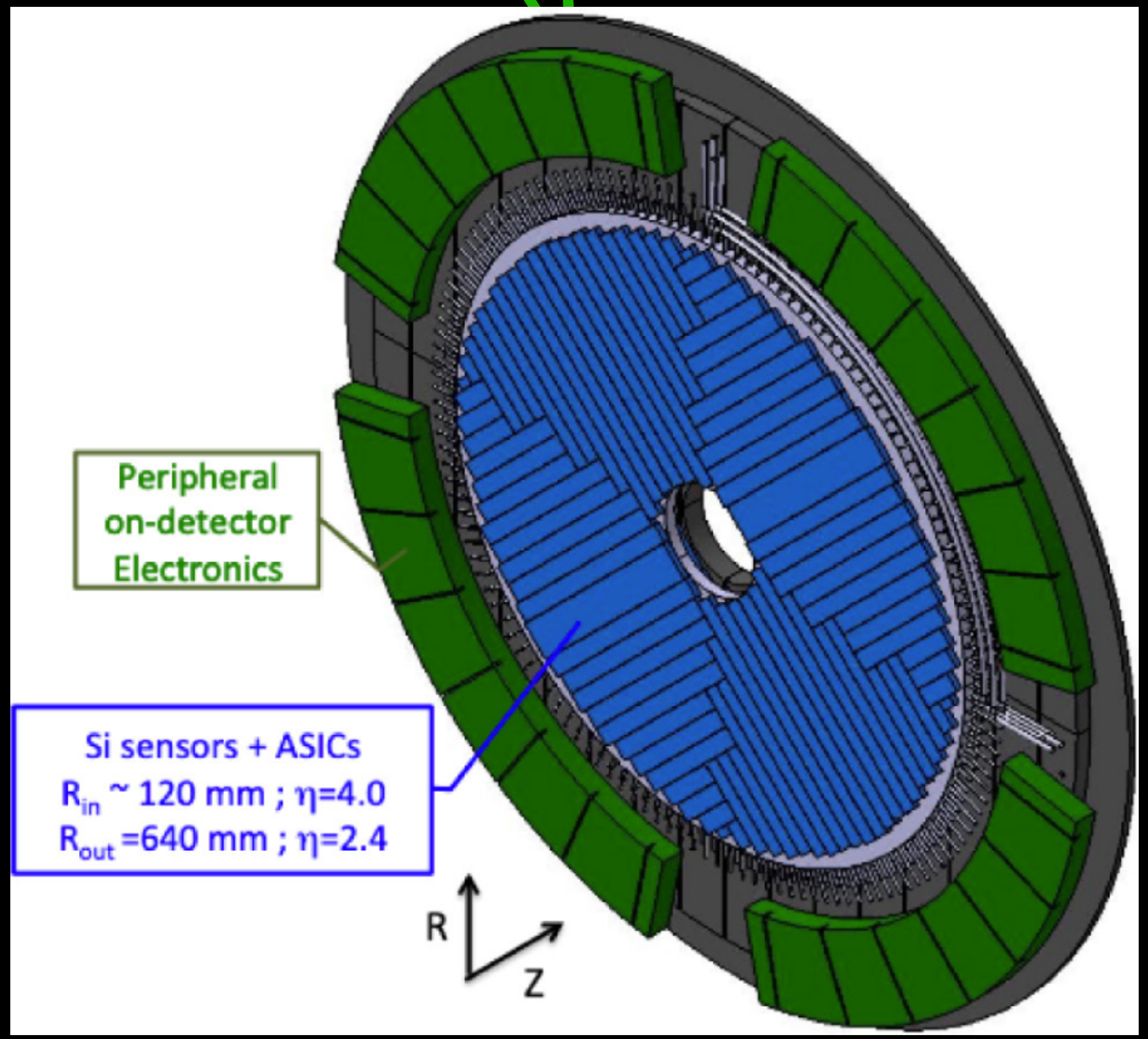
- Liquid Argon Calorimeter:
  - Run3 upgraded boards will continue to be used
  - Replacement of readout electronics (front-end and back-end):
    - Full granularity digital data sent at 40 MHz to back-end
    - Improved algorithms to deal with overlapping events deriving from increased pile-up
    - FPGA based electronics: AI algorithms applied for measuring the energy



- High Granularity Timing Detector:
  - Radiation-hard silicon-sensor detector, two disks per each end-cap, two sensor layers per each disk
  - Four layers of Low Gain Avalanche Detectors technology, 1.3x1.3 mm^2 readout cells, for precise timing and luminosity measurements
  - Timing resolution of ~30 ps for minimum-ionizing particles for precise vertex reconstruction and to disentangle events in high pile-up
  - Enhances ITk in region 2.4 < |η| < 4.0

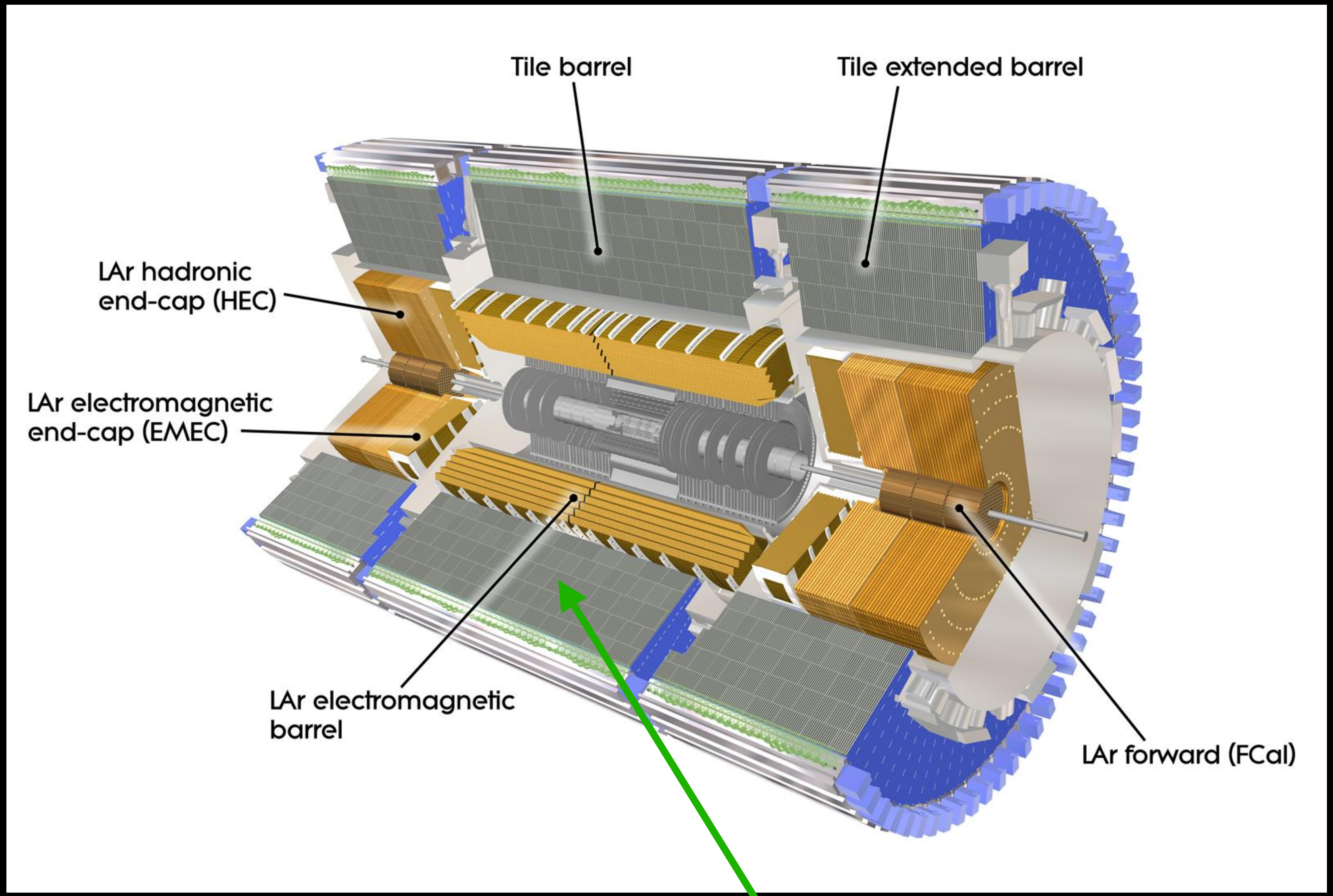
ATLAS public results web page - HGTD



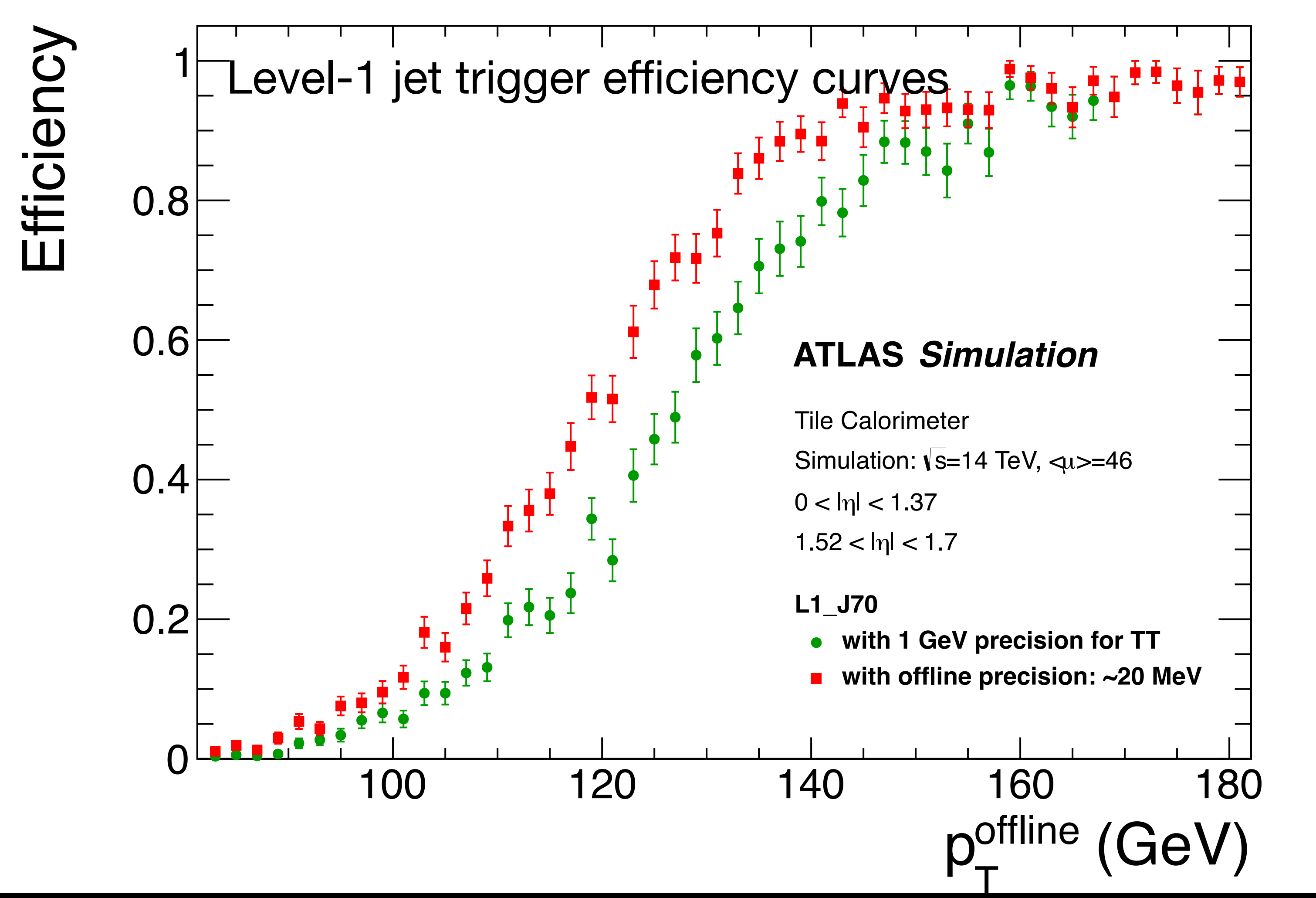


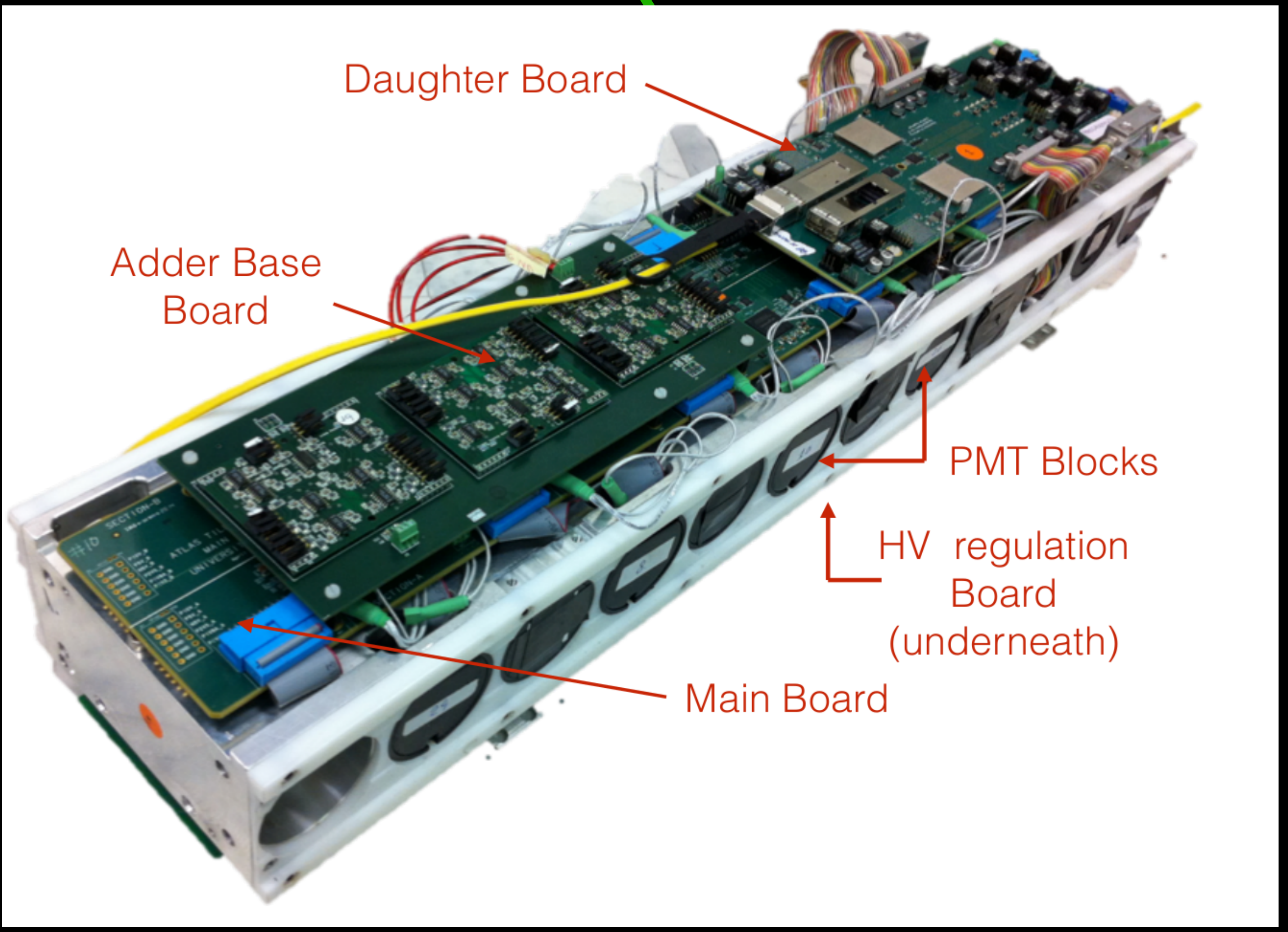
Tile calorimeter

- On-detector and off-detector electronics fully replaced to improve the radiation tolerance and the performances at high pile-up
- Front-end signals from calorimeter cells are digitized and sent directly to the back-end electronics, where the signals are reconstructed, stored, and sent to the Level-0 trigger at 40 MHz
- Better precision of the calorimeter signals used by the trigger system for more complex trigger algorithms



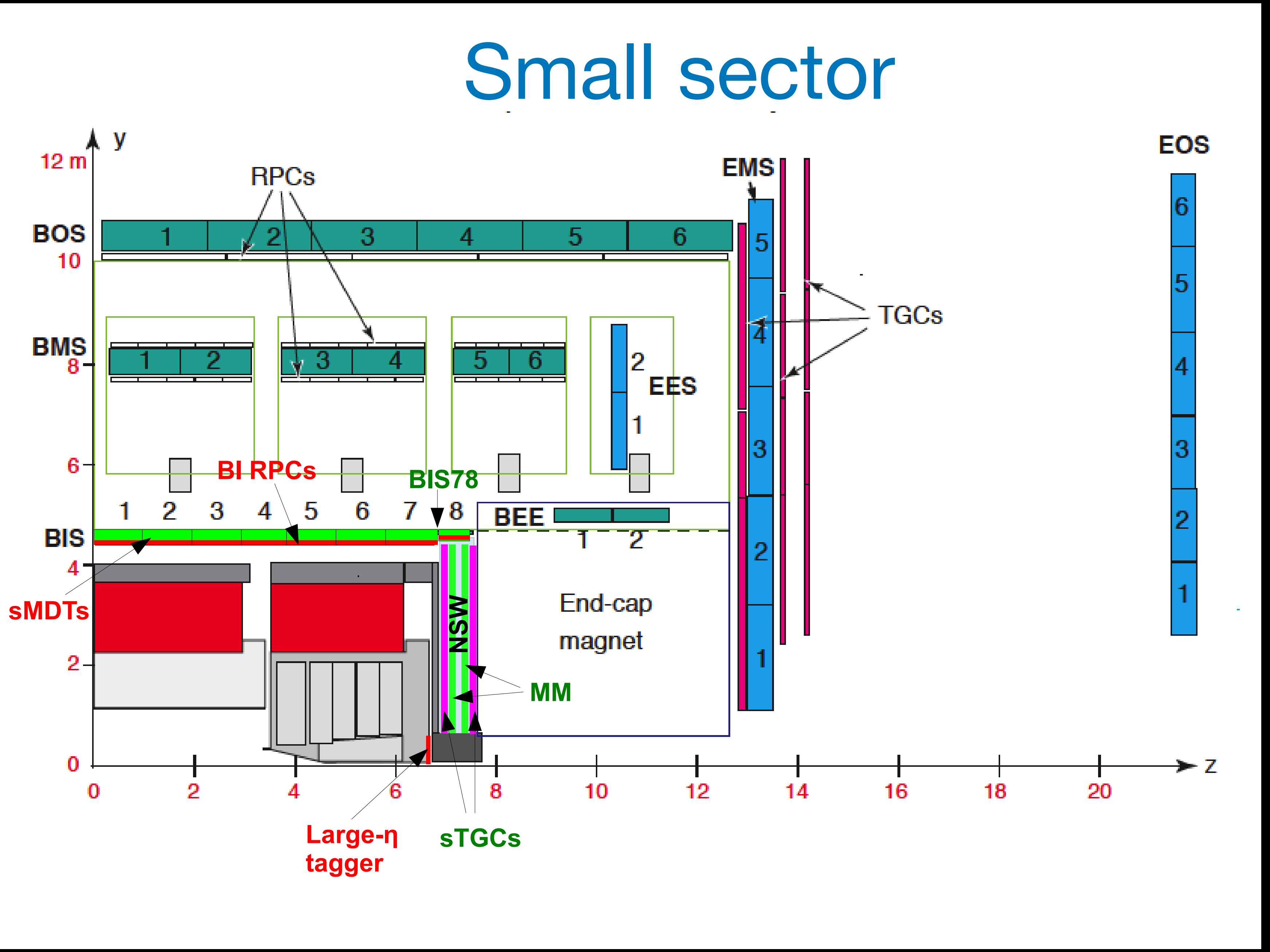
Tile Cal Phase-II TDR plots

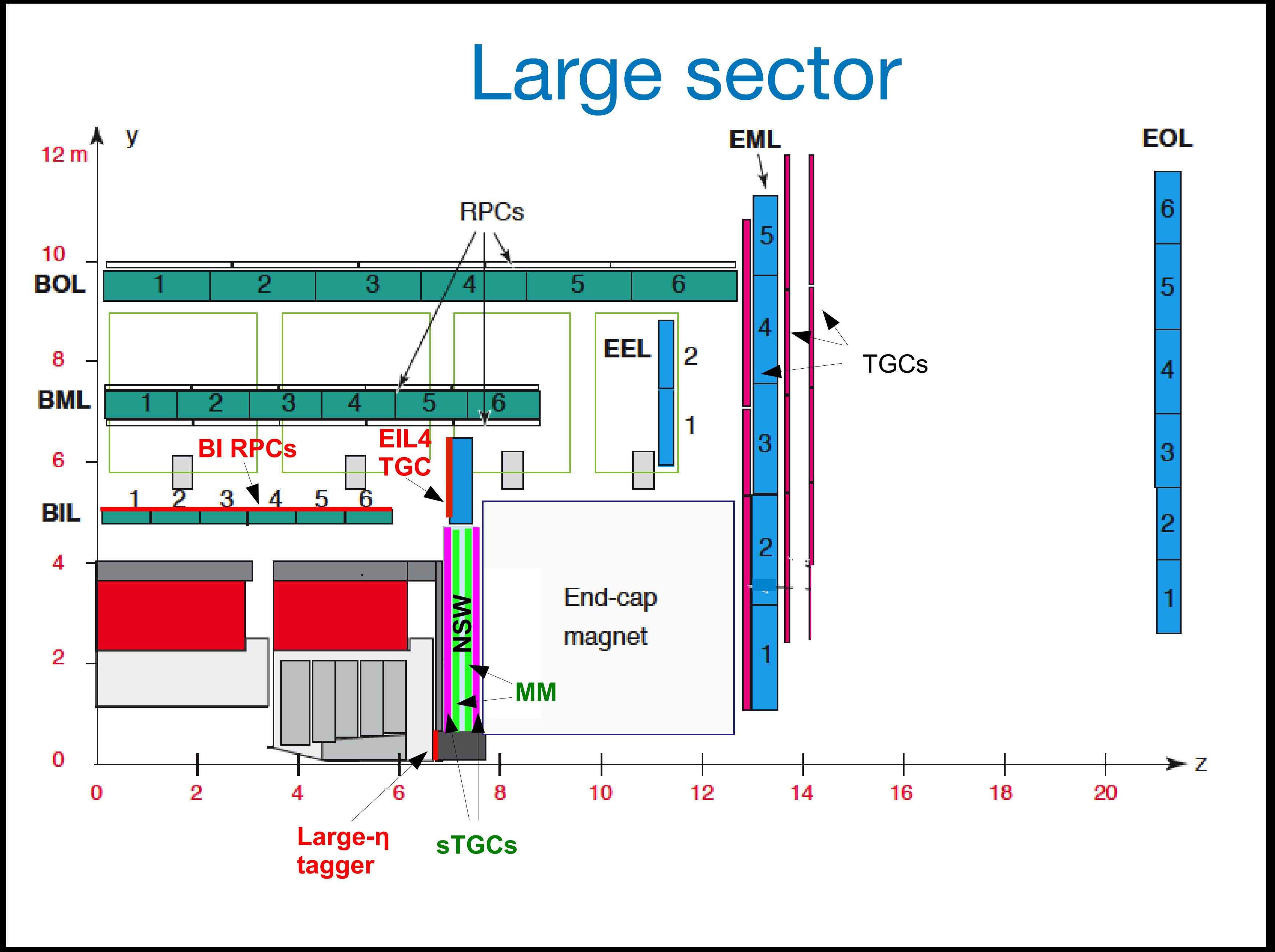




Muon detectors

- New RPC and sMDT detectors in the inner region of the barrel:
    - current BIS MDT replaced by new (sMDT + RPC)
    - new RPC triplets installed on top of the existing BIL MDT
- New sTGC triplets in the end-cap inner region EIL4
- The new detectors allow to:
    - reduce the trigger fake rate in barrel and end-cap regions
    - increase the trigger performances
    - increase the geometrical coverage in the barrel





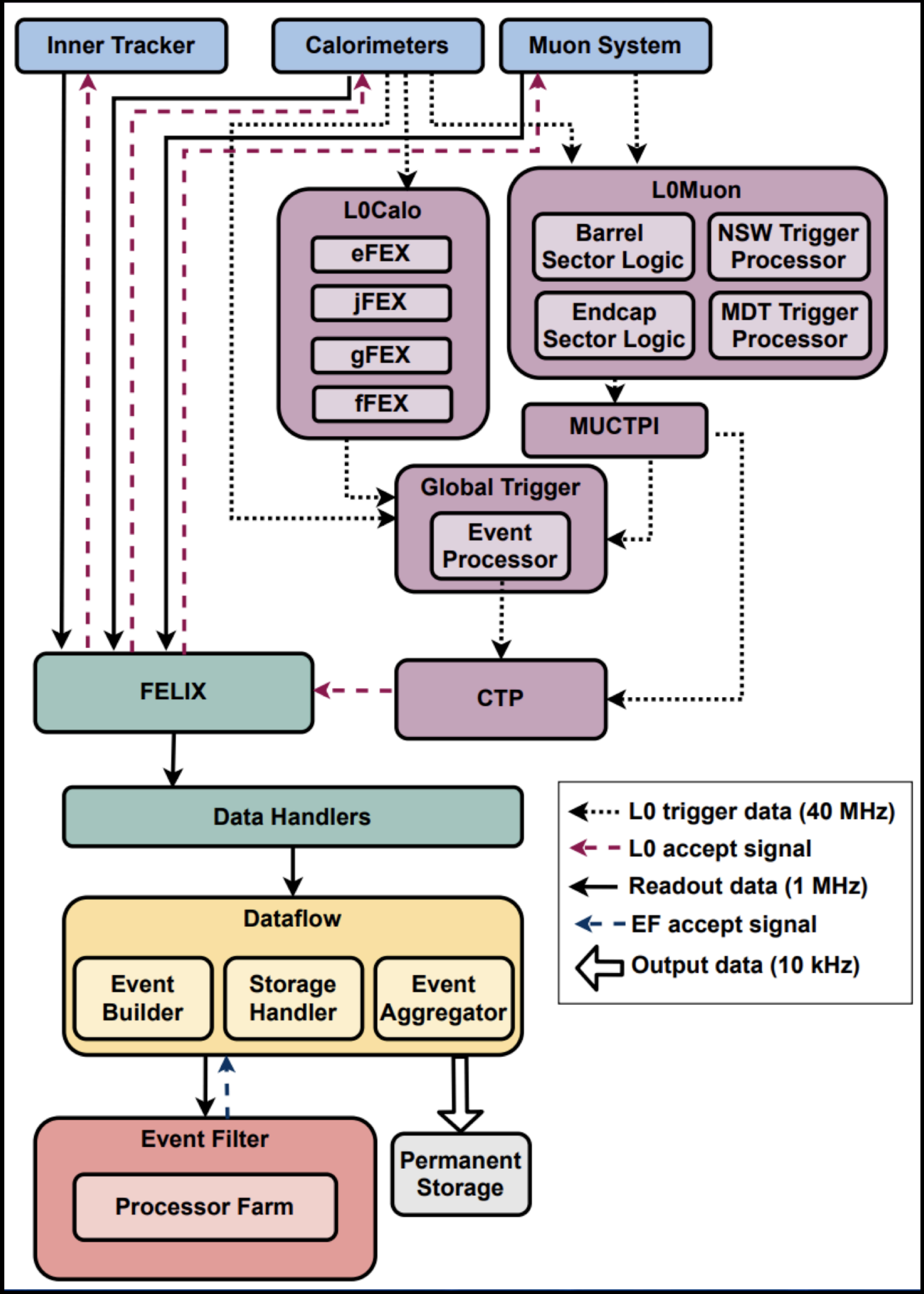
ATLAS Trigger and Data Acquisition upgrade generalities

- TDAQ upgrade components:
  - hardware-based low-latency real-time Trigger system, running at 40 MHz
  - 4.6 TB/s Data Acquisition system (event size ~5 MB), based on custom readout with commodity hardware and networking
  - 1 MHz Event Filter running offline-like algorithms on commodity servers, possibility to use commercial hardware accelerators
- Hardware: commodity servers and networks, custom ATCA boards, high speed links, FPGAs
- Algorithms: offline-style clustering and jet-finding in FPGAs in the Trigger, accelerated track reconstruction in the Event Filter

Trigger and Data Acquisition schema

ATLAS Phase-II TDAQ Upgrade TDR

- Single level Level-0 hardware trigger with an output rate of 1 MHz, (100 kHz today) Level-0 readout latency is 10 μs (2.5 μs today)
  - Calorimeters and muons front-end full granularity readout at 40 MHz
  - New Global Event processor integrates topological functions with additional selection algorithms using information from muons and calorimeters
- Readout based on FELIX system for all detectors
- DAQ throughput 4.6 TB/s (200 GB/s today)
- FPGA-based boards off-detector, on-detector where possible
- Possible hardware accelerator system for tracking at the Event Filter
- Goal of better e, γ, τ, jet identification and measurement, at hardware and software trigger levels and offline
- Event Filter output is 10 kHz (~3 kHz today)

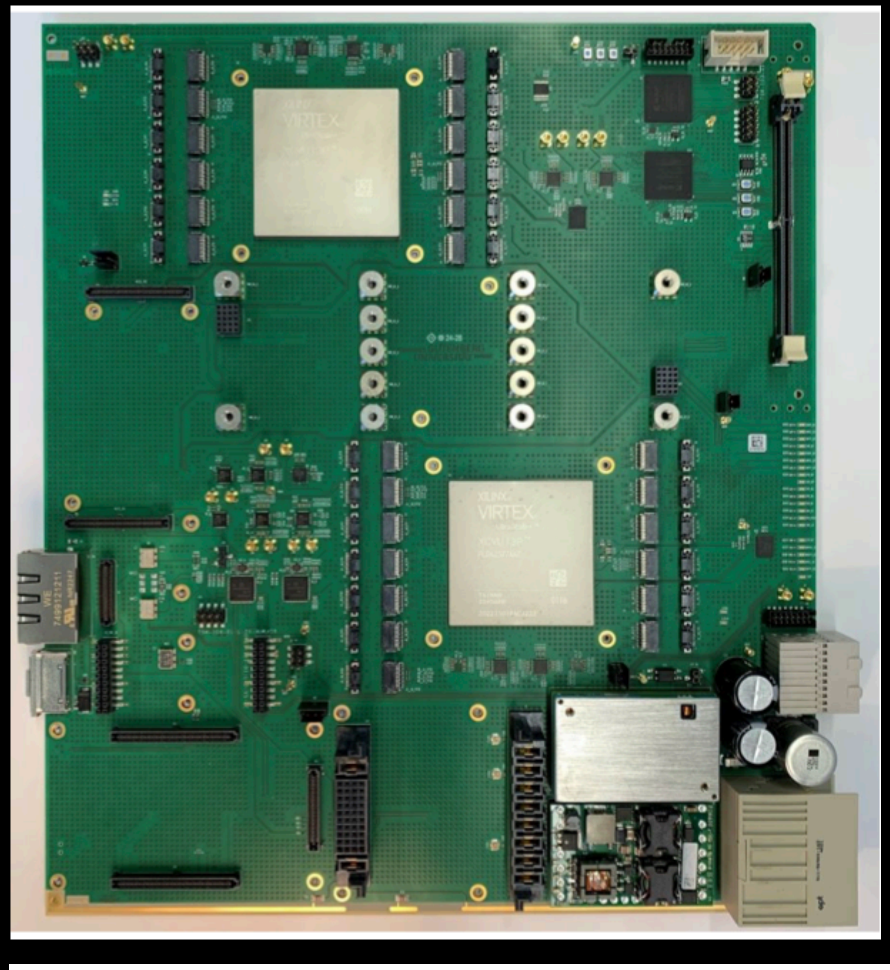


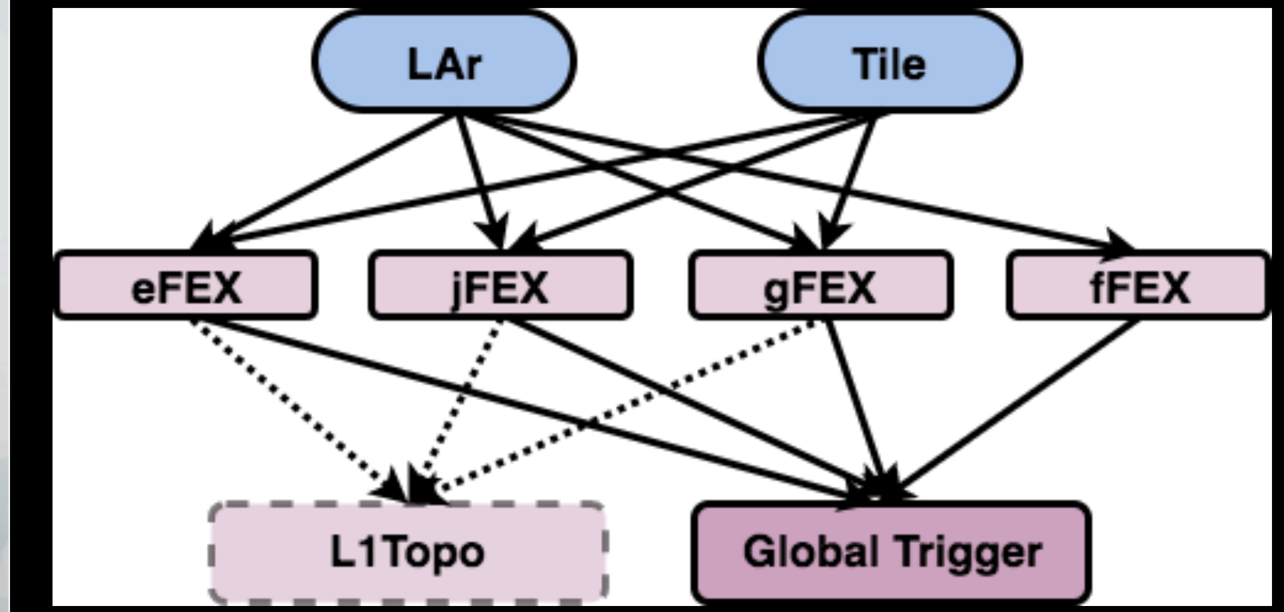
Level-0 Calorimeter trigger

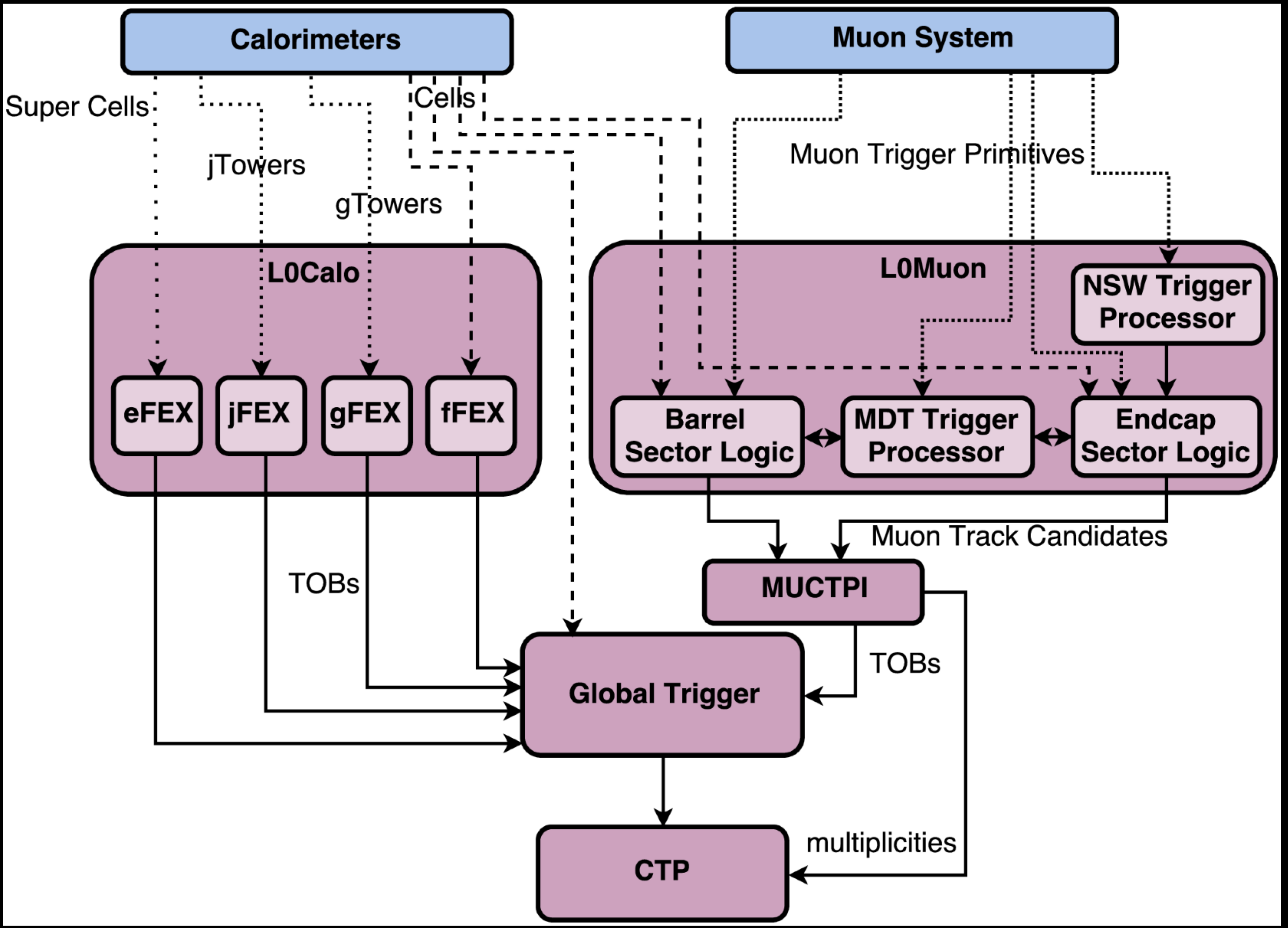
- High granularity full digital data from calorimeters sent at 40 MHz
- Feature Extractor (FEX) FPGA-based boards perform different trigger algorithms for different physics objects
- LAr and Tile calorimeter are sent separately to each FEX board
- Legacy FEXs identify electron/photon/tau candidates (eFEX), jets and ETmiss (jFEX) and large-R jets (gFEX)
- Current hardware retained with upgraded firmware (upgraded firmware possible due to increased latency allowance)
- New fFEX processors allows triggering also in the forward region (EM triggers at |η| > 2.5, Jet triggers at |η| > 3.3)
- L0 Calo output sent to L0 Global processor

ATLAS TDAQ Phase-II Upgrade TDR

fFEX prototype





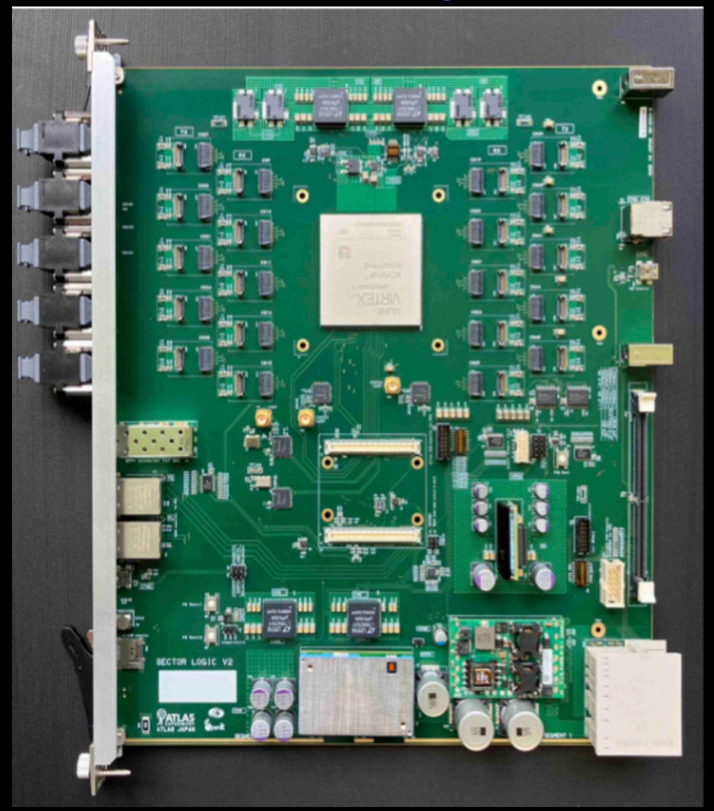


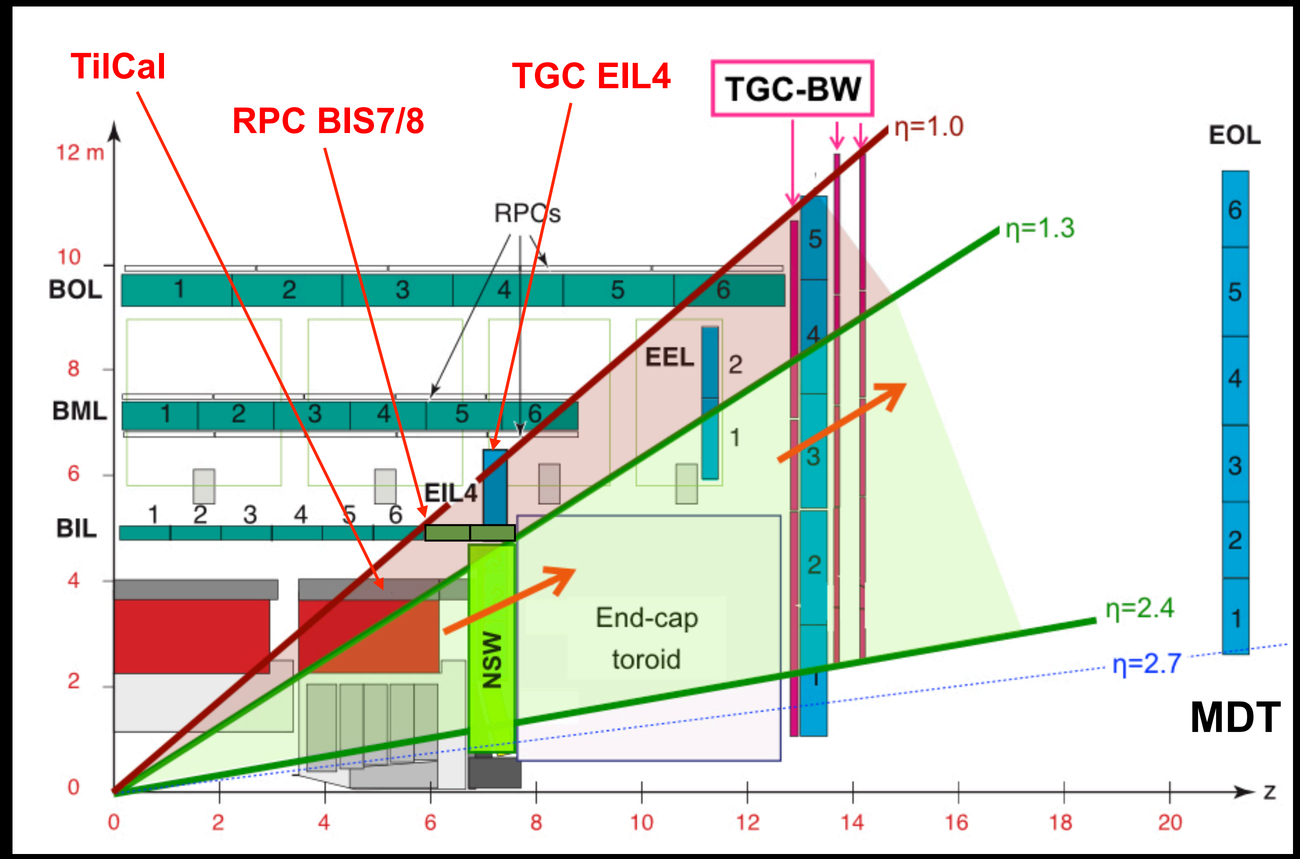
Level-0 Muon trigger

- The data from the RPC, TGC, and NSW detectors used in the Run3 system will be complemented with BI RPC, Tile calorimeter and MDT
- Increased selection efficiency and reduced fake trigger rate
- New MDT trigger sharpens turn-on curve and increases the rejection power
- Possibility to loosen RPC trigger selection to increase the geometrical acceptance in the barrel, from ~70% to ~95%
- Rate suppression of ~50% for muons with p_T < 20 GeV
- New on-detector electronics full digital readout to off-detector @ 40 MHz
- Barrel and end-cap new off-detector Sector Logic trigger boards perform the coincidence trigger algorithm and send the seed to the MDT Trigger Processors
- New MDT Trigger Processors match the MDT hits with the RPC/TGC seed vectors in space and time
- New NSW Trigger Processor performs trigger algorithms in the small wheel region to lower end-cap fake trigger rate
- Large use of FPGAs on and off-detector

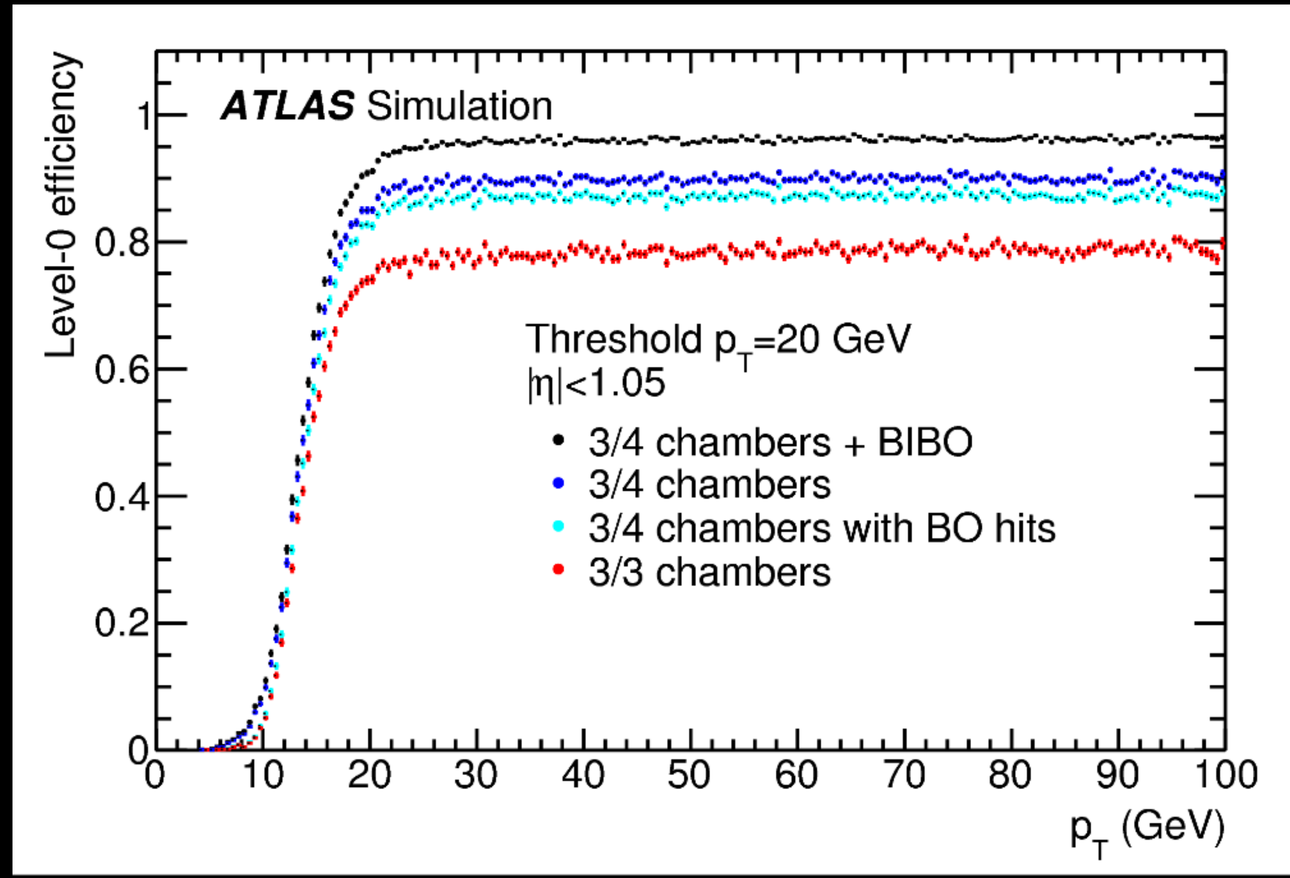
MDTTP CM prototype

SL prototype



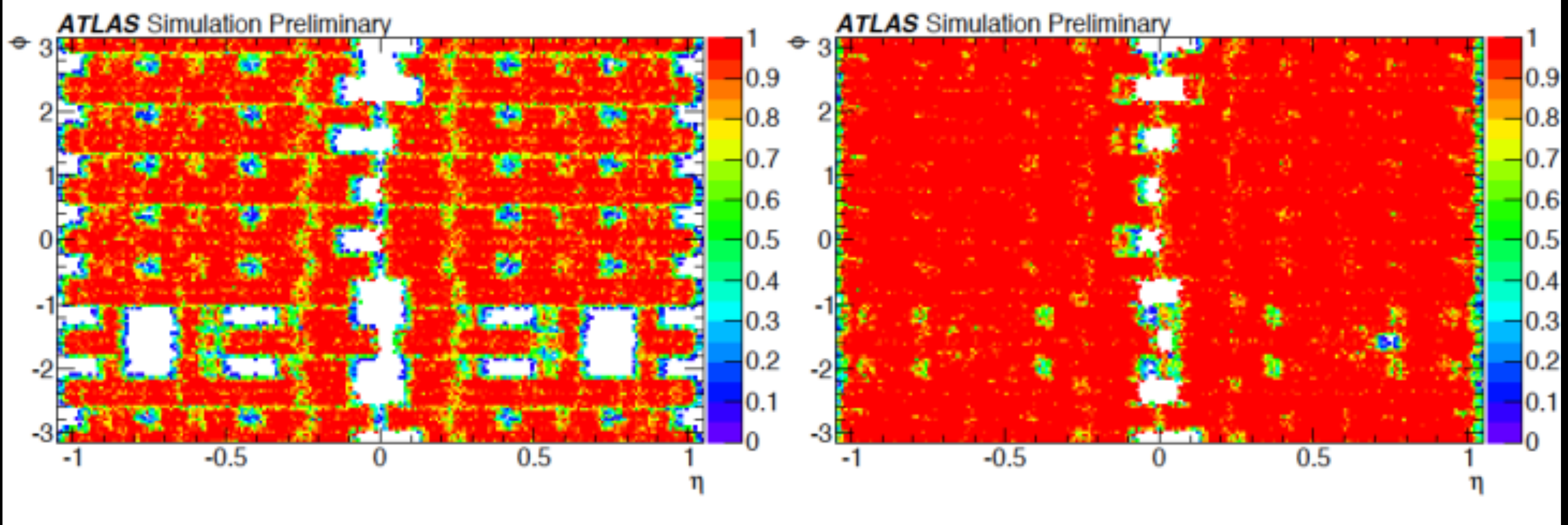


ATLAS Muon Spectrometer Phase-II TDR plots



ATL-PHYS-PUB-2016-026

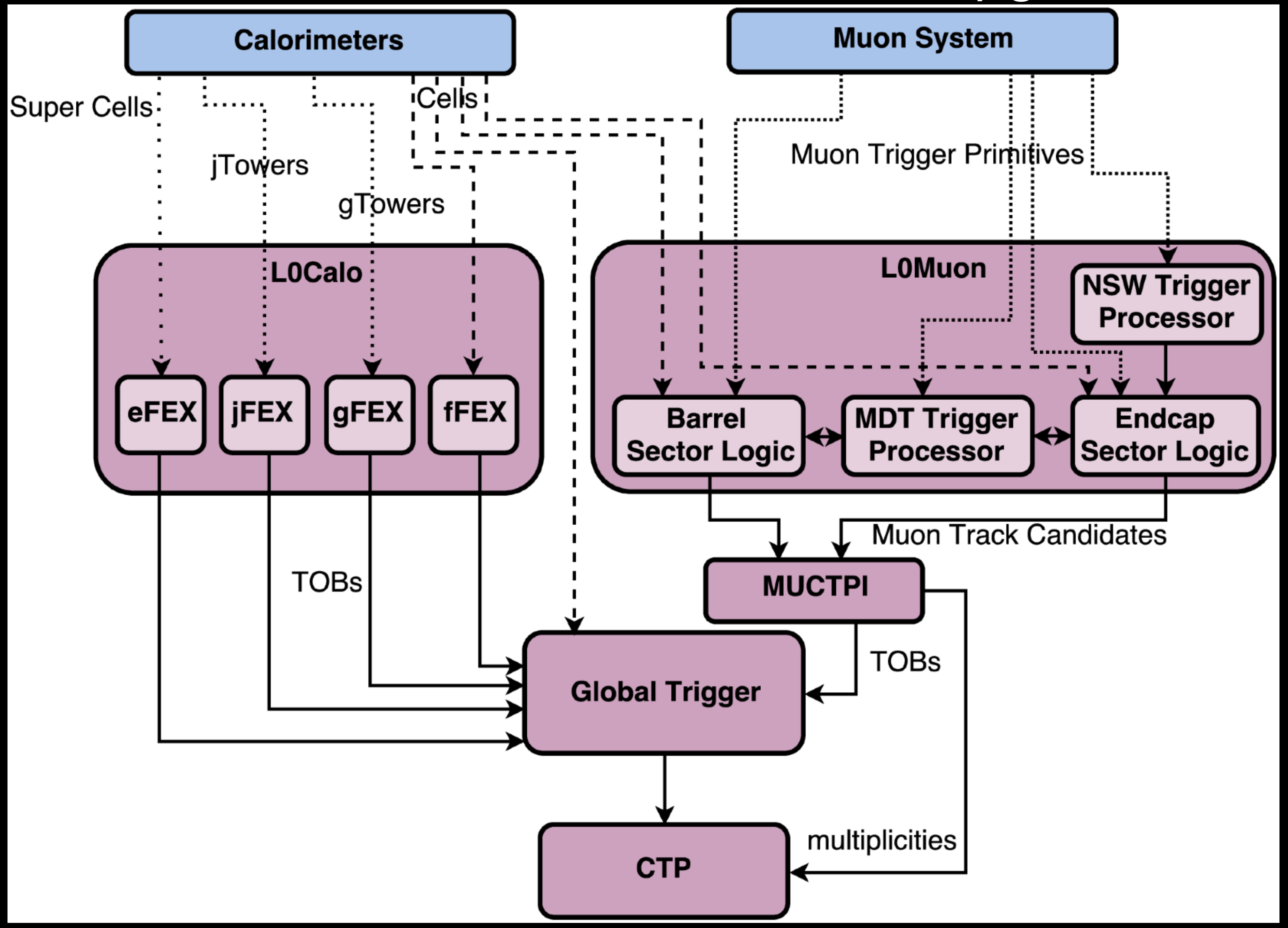
L0 barrel acceptance Run3 vs. Run4

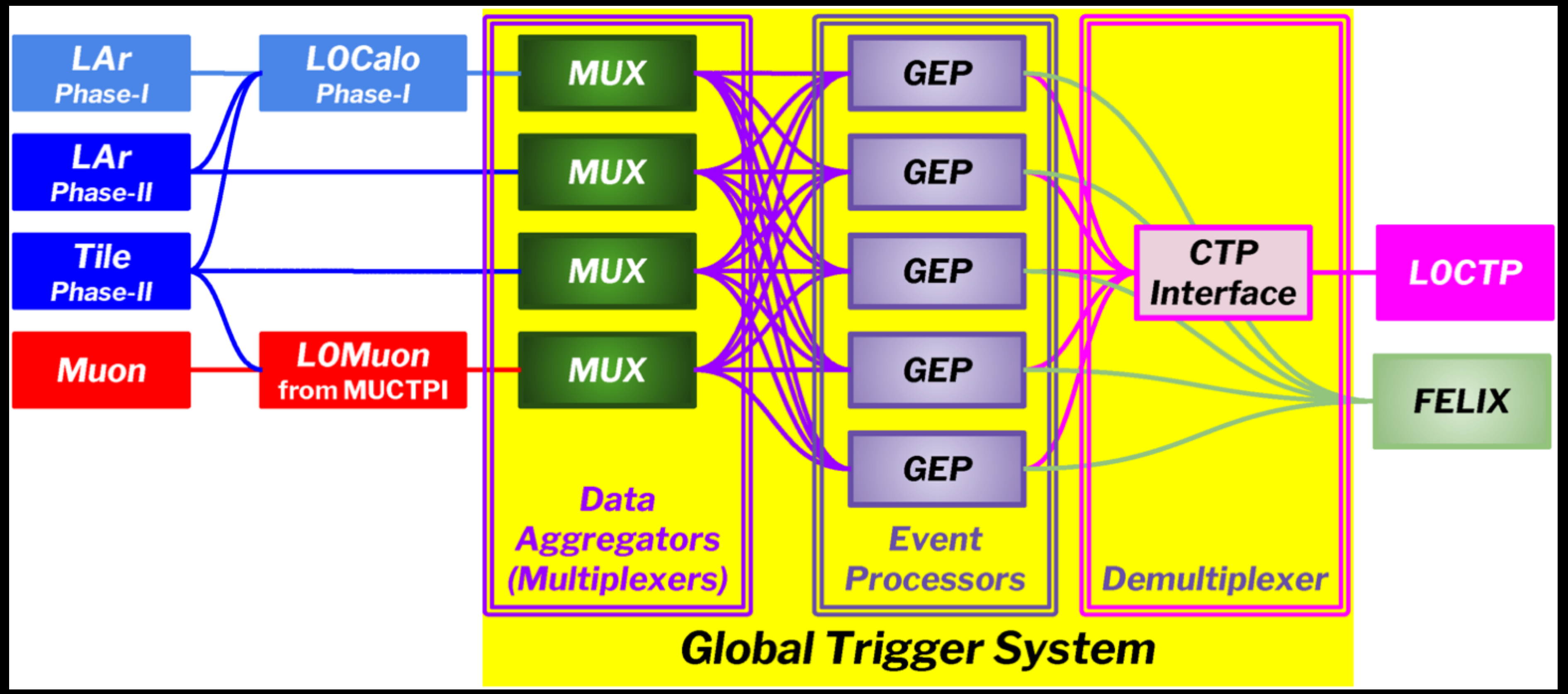


Level-0 Global trigger

- Runs trigger algorithms similar to the ones in HLT, on high granularity data
- Replaces current topological trigger
- Algorithms organised into same trigger signatures as EF (calo, muon, topological cluster, e/ɣ, τ, jets, E_T^{miss} and other topological quantities)
- FPGA-based hardware, firmware components are:
    - MUX: data aggregator and time multiplexer of events from all sub-detectors (>50 TB/s throughput)
    - GEP: Global Event Processing and trigger algorithms
    - gCTPi: demultiplexing and Central Trigger Processor interface
- Latency is a critical parameter for this project
- All of the firmware components are implemented on a common hardware module (the Global Common Module, GCM) prototypes of which are under test

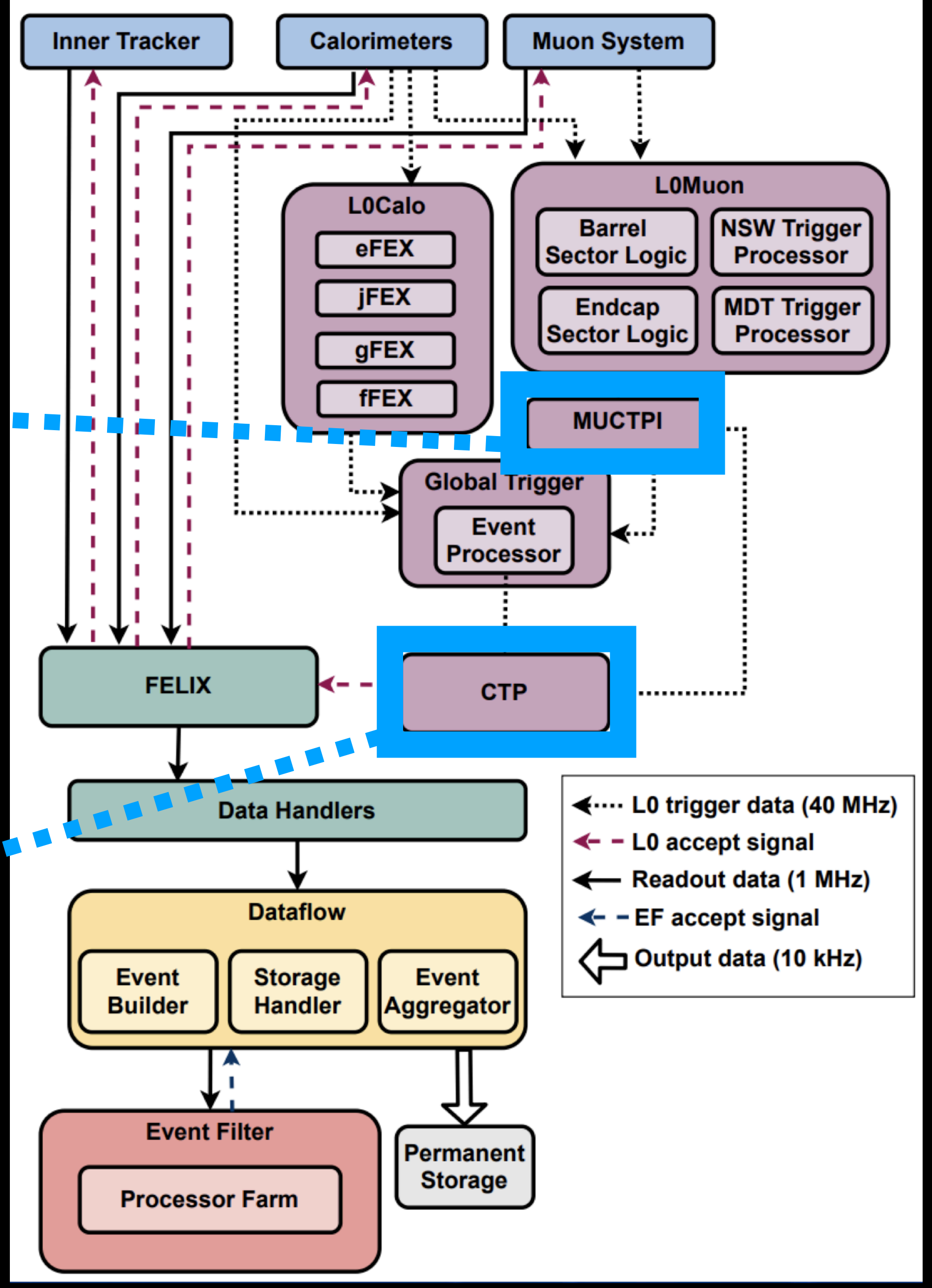
ATLAS TDAQ Phase-II Upgrade TDR



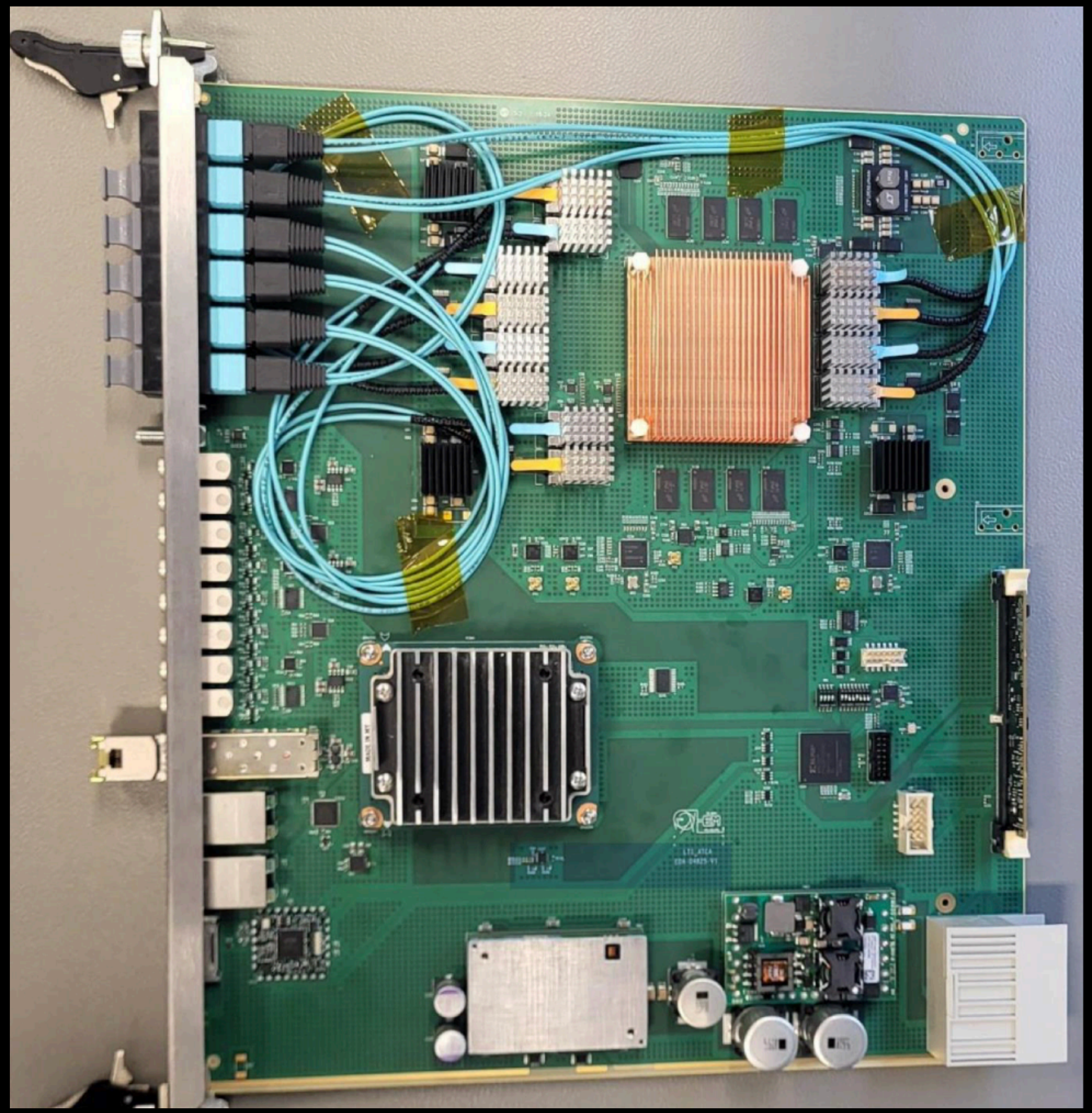


Central Trigger

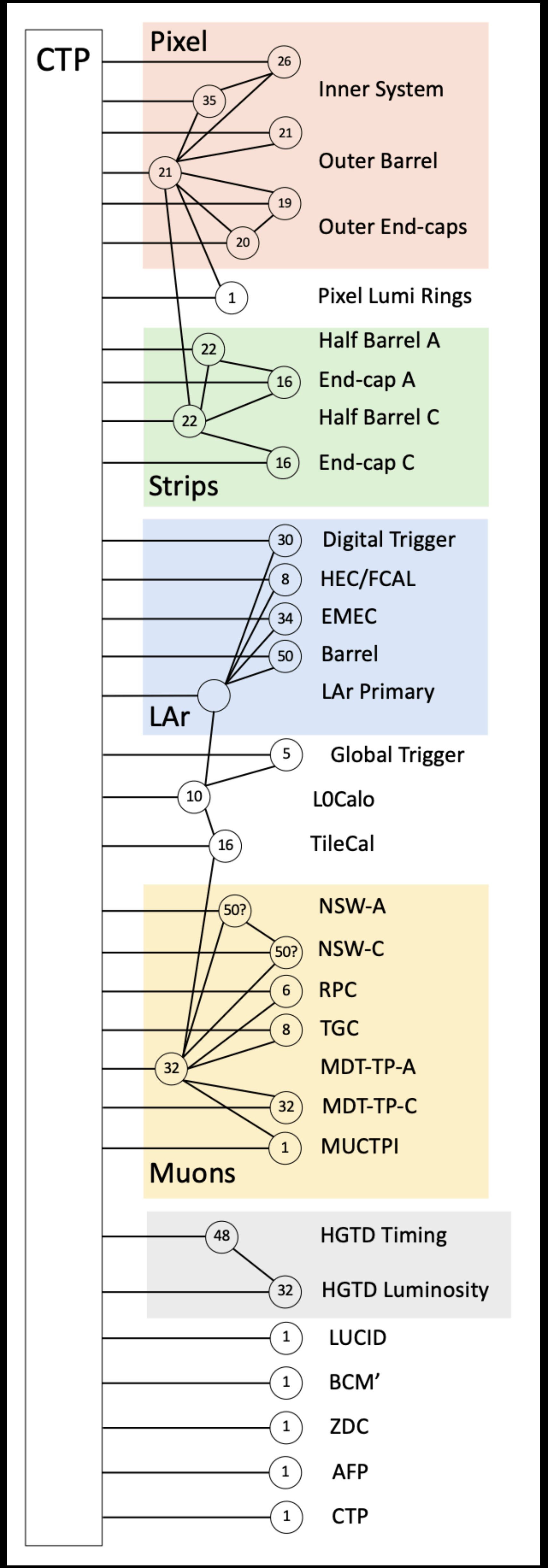
- Muon to CTP interface board (MUCTPI) board
  - Combines muon systems candidates and distributes L0 Muon candidates
- Central Trigger Processor (CTP) board:
  - Takes the final decision and delivers L0 candidates
  - Distributes LHC Timing, Trigger, Control (TTC) signals through the LTI modules
- LTI board: distributes TTC signals to FELIX
- MUCTPI and CTP are based on common hardware with different firmware versions



LTI prototype



TTC network in USA15



Readout, Dataflow and Online software

FELIX FLX-182 prototype

- FELIX (Front-End LInk eXchange)
  - PCIe I/O board, FPGA-based
  - Interfaces optical links to community network
  - Receives readout detector data from front-end and off-detector boards and distributes to Readout
  - Receives TTC data from LTI board and distributes to front-end and off-detector boards

- Dataflow:
  - Aggregates data from Readout
  - Transfers full granularity events to Event Filter
  - Records the accepted events and transfers events to offline
  - Network studies ongoing

- Online software:
  - configuration, control, monitoring of the DAQ system

Event filter

- Event Filter farm runs:
  - core software: interfaces to dataflow, online control, monitoring, L0 trigger, configuration
  - tracking, calorimeter, muon: reconstruction from raw data, accelerators and algorithms, including ML
- Evaluating EF tracking performances with CPU / GPU / FPGA
  - comparison done with different hardware pipeline options
  - cost comparison also under evaluation
- Athena framework integration ongoing
- EF commodity computing technology decision in 2025

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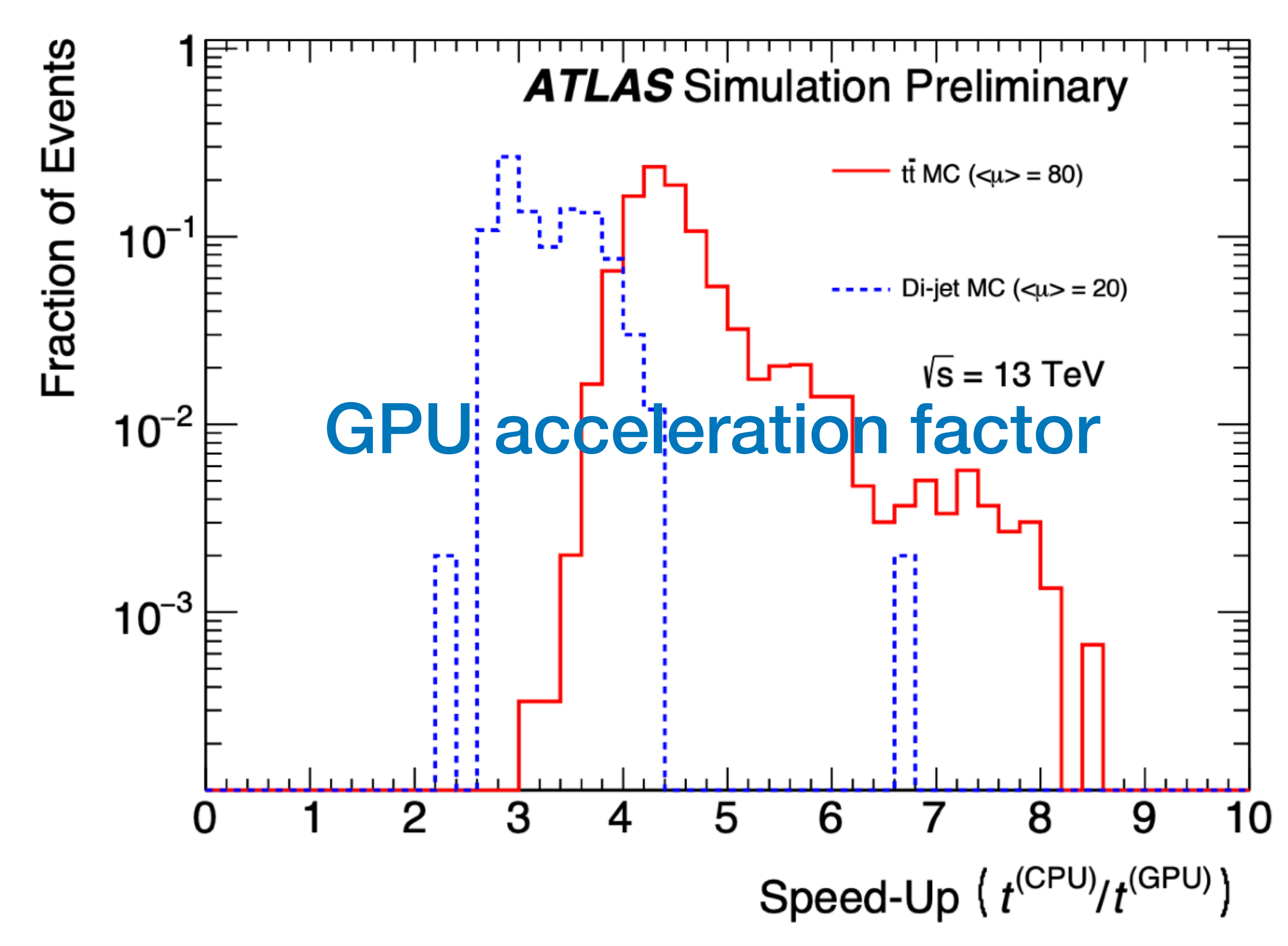
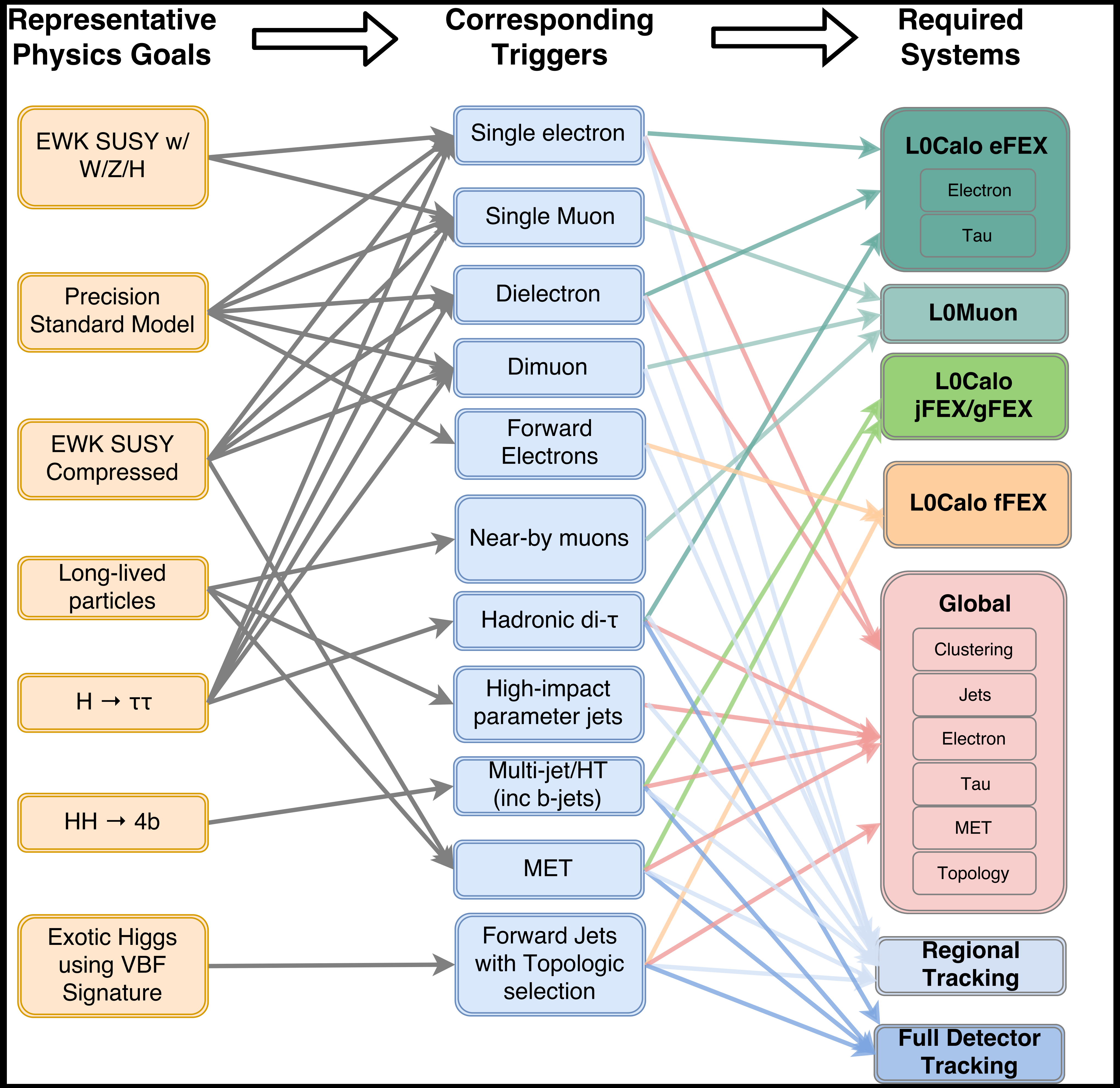


Conclusions

- The large datasets that can be collected with the High-Luminosity LHC will allow us to perform Higgs and SM precision measurements, the search for rare Higgs boson decay modes and the study of low production cross section Standard Model processes, as well as the search for new phenomena beyond Standard Model
- ATLAS experiment will improve its trigger and readout capabilities thanks to new detectors and new electronics
- New electronics based on FPGA and commodity hardware
- ATLAS Run4 TDAQ upgrade projects status:
    - Detector and electronics prototypes available, moving towards pre-production for most of the systems
    - Prototype integration (hardware and firmware) progressing
    - Some strategic choices still to be made (commodity hardware accelerators for EF)
- Additional info available in the ATLAS upgrade public web page

ATLAS TDAQ Phase-II Upgrade TDR



Flow from the representative set of physics goals to the hardware systems