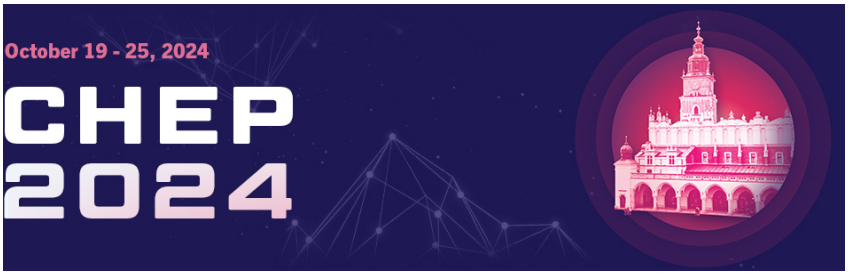

Contribution ID: **164** Type: **Talk**

Development of an FPGA based track reconstruction pipeline for the ATLAS Event Filter

Thursday 24 October 2024 14:24 (18 minutes)

For the upcoming HL-LHC upgrade of the ATLAS experiment, the deployment of GPU or FPGA co-processors within the online Event Filter system is being studied as a measure to increase throughput and save power. End-to-end track reconstruction pipelines are currently being developed using commercially available FPGA accelerator cards. These utilize FPGA base partitions, drivers and runtime tools supplied by the manufacturer to reduce design effort. Algorithms are implemented both in hardware description language (HDL) and high-level synthesis (HLS), and integrated as kernels into an OpenCL host software interfacing with the ATLAS main software framework Athena. This contribution summarizes the algorithmic developments, the integration workflow and status.

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