Measurement of propagation time with the use of FPGA devices in ALICE experiment at CERN

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MOTIVATION AND OBJECTIVES

Used technologies:

Time-to-Digital Converters (TDC) are widely used in various fields such as physics, medical imaging, and automotive systems, where precise time measurements are crucial. The higher the resolution of a TDC, the better the accuracy in detecting and recording time intervals, which is essential for improving the performance and precision of systems in these applications.

Improving Resolution:

Using two Serializer/Deserializer instead of one doubles the resolution, improving it from 200 ps to 100 ps, at a clock frequency of 625 MHz for Xilinx 7 series FPGAs. This solution is suitable for creating multi-channel TDCs with better time resolution or for using the FPGA in combination with an ASIC TDC as a coarse measurement stage, where the results from both devices are combined into one.

IMPLEMENTATION IN FPGA

Introduction:

TDC is an electronic device that converts digital time pulses into a digital code representing the duration or delay of a signal. In 7-series FPGAs, ISERDES2 blocks are used to simplify the implementation of high-speed source-synchronous applications, which can be applied in the development of a TDC.

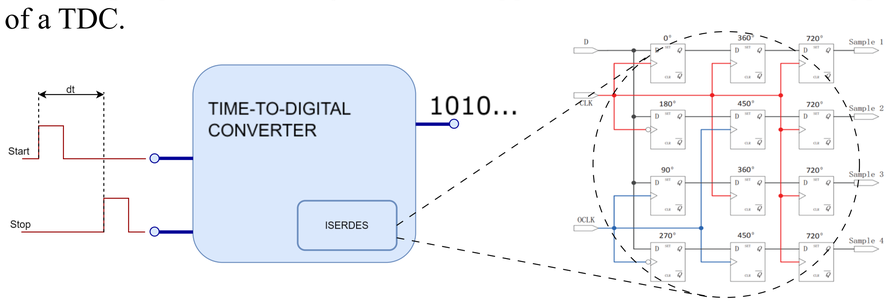

Figure 1: Basic Concept of a Time-to-Digital Converter (TDC)

The ISERDES2 block in the TDC system converts a serial signal into a parallel one, functioning as a SIPO (Serial-In, Parallel-Out) circuit. Clock signals are supplied to it by the MMCM module. ISERDES2 operates in oversample mode, allowing for precise sampling and data collection at double the clock speed (DDR). The resulting 4-bit parallel signal at the output indicates the moment when the Stop signal was registered.

To reduce metastability and synchronize the output samples to a single clock edge, the internal ISERDES2 block contains three sequential flip-flops.

Dual SERDES:

[1] To improve the resolution of the Time-to-Digital Converter, two ISERDES2 blocks can be used with a 45° phase shift between them. The incoming differential signal is split using an IBUFDS buffer. The phase shift can be achieved in two methods.

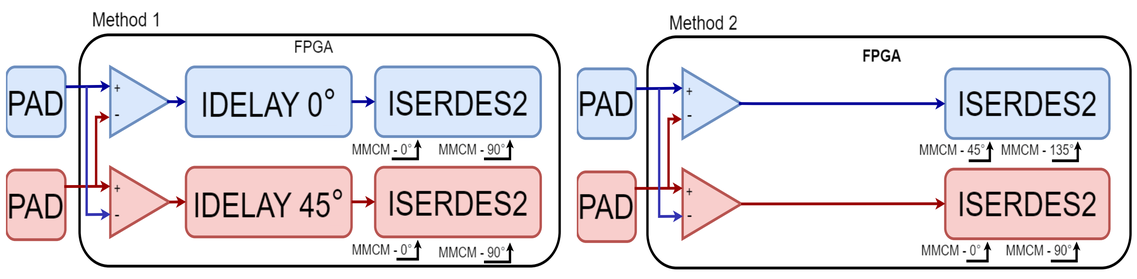

Figure 2: Dual SERDES Configurations for Time-to-Digital Conversion

Method 1:

Using additional IDELAY blocks. The phase shift between ISERDES2 blocks is achieved by delaying the input signal with IDELAY2 blocks, which provide a programmable delay line with 32 taps. Each tap adds a delay of 78 ps, 52 ps, or 39 ps depending on the clock frequency. For proper operation, the IDELAYCTRL module must be connected, which continuously calibrates the individual delay taps (IDELAY/ODELAY) to minimize the impact of variations in process, voltage, and temperature.

Method 2:

Using two additional clock signals generated by the MMCM. One ISERDES2 operates at 0° and 90°, while the other operates at 45° and 135°.

Multi-channels:

The use of ISERDES2 enables the implementation of multi-channel TDCs with a single FPGA. In 7 series devices, an I/O bank consists of 50 input/output blocks (IOBs). The number of banks depends on the device size and package pinout. For Kintex 7, 12 TDCs can be implemented in a single bank.

TEST SETUP AND RESULTS

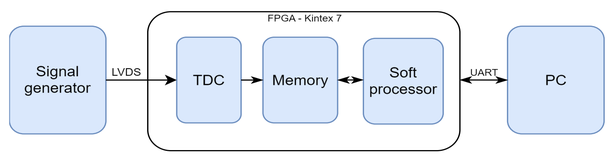

Figure 3: Test Setup and Data Processing Flow

The Tektronix AWG710 generator (jitter 25 ps) sent pulses of known duration to the KC705 board (XC7K325T-2FFG900C) via LVDS. The incoming signal was processed by the TDC block (using two methods) at a frequency of 625 MHz, after which the data was stored in BRAM. After collecting 4092 events, the data was transferred to the Microblaze via the AXI bus and sent to a computer through UART for analysis using Python.

The histogram shows how often each time the difference between the measured and actual signals occurred. The data is approximated by a Gaussian curve. The histogram shows that Method 1 is more accurate, with approximately 68% of the time differences (events) falling within the range to which μ belongs: <-138, 138> ps.

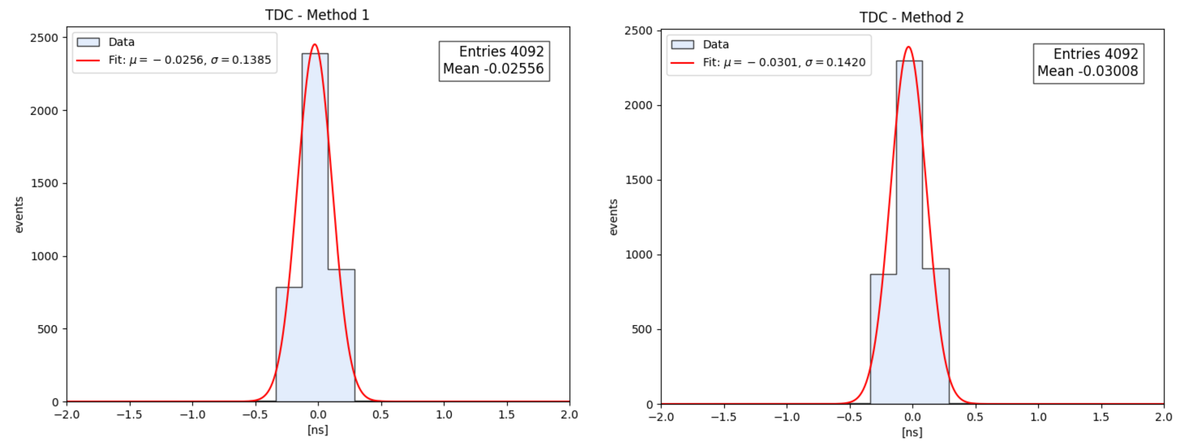

Figure 4: Comparison of TDC Measurement Accuracy Using Two Methods

DNL MEASURMENTS

MMCM and Control Block:

[2] The MMCM block was used to generate test signals with high-precision dynamic phase adjustment. The phase shift step depends on the VCO frequency and is 1/56 of the VCO period. For Kintex 7, one phase step equals 11 ps.

A finite state machine controls phase shifting and data collection. It shifts the phase after collecting 1000 values from the ISERDES block and stops once the phase shift reaches one clock cycle (1600 ns), corresponding to 8 BINs.

Graphs:

The graph presents normalized bin width results. From the graph, we can observe that the first four bins for both methods show identical deviations, which is expected since they are clocked by the same 0° and 90° signals. Additionally, we can see that the last four bins in the second method exhibit greater nonlinearity compared to the first method. This can be explained by the additional clock skew between the signal pairs of 0°/90° and 45°/135°.

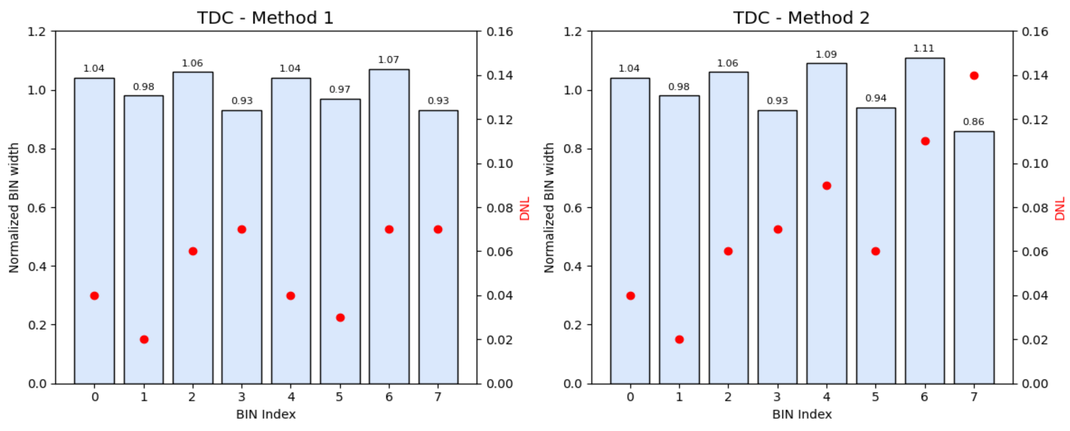

Figure 5: Differential Non-Linearity (DNL) Measurements for Two TDC Methods

CONCLUSION

Based on the obtained results, it can be concluded that the first method is more accurate. Additionally, this method does not require generating an additional pair of clock signals, which reduces the FPGA's routing resources.

REFERENCE

[1] Xilinx, XAPP523 - LVDS 4x Asynchronous Oversampling Using 7 Series FPGAs and Zynq-7000 AP SoCs

[2] Tian Xiang, Lei Zhao, Xi Jin, Tianqi Wang, Shaoping Chu, Cong Ma, Shubin Liu, Qi An, "A 56-ps Multi-phase Clock Time-to-Digital Converter Based on Artix-7 FPGA,"

ACKNOWLEDGEMENT

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