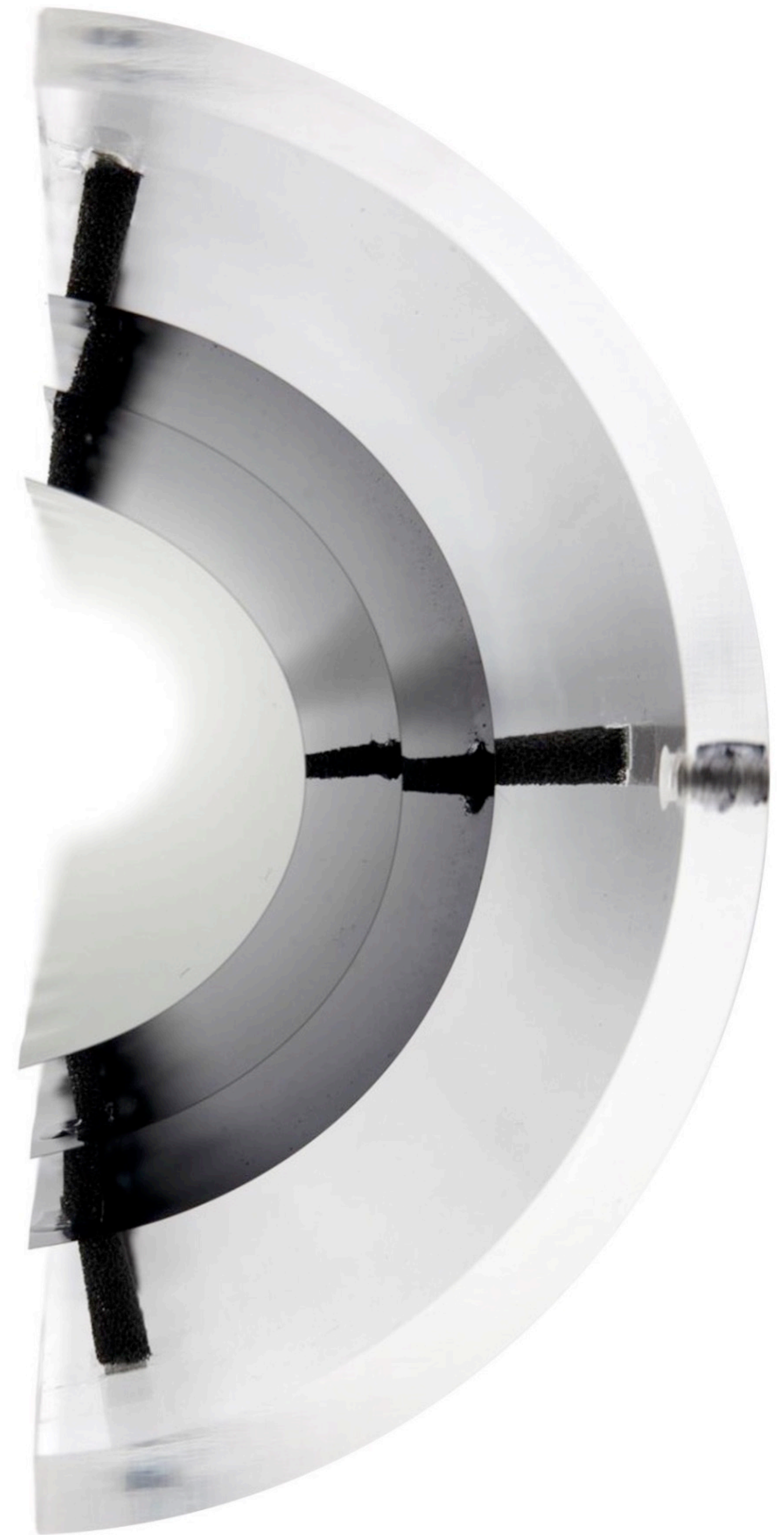




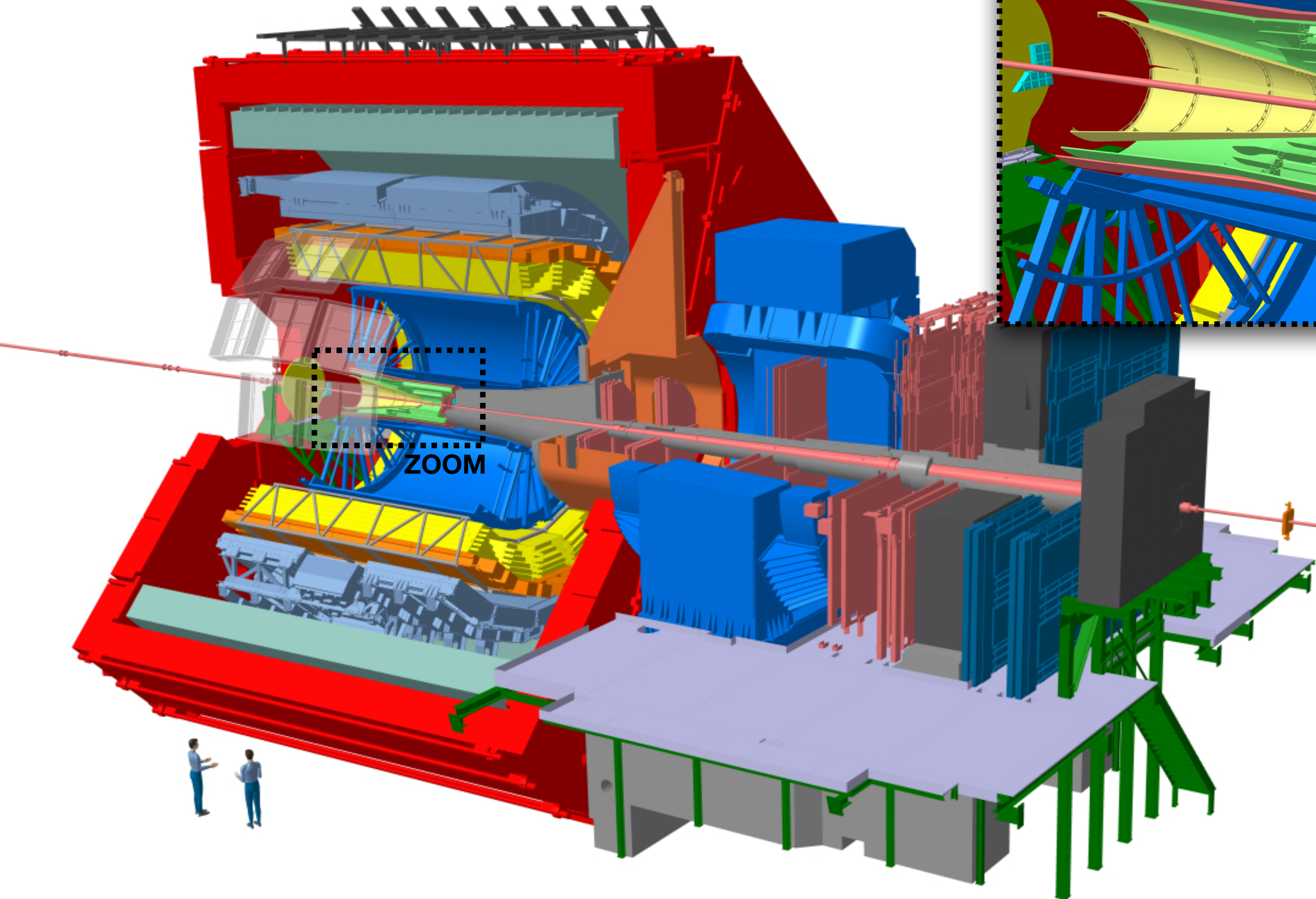
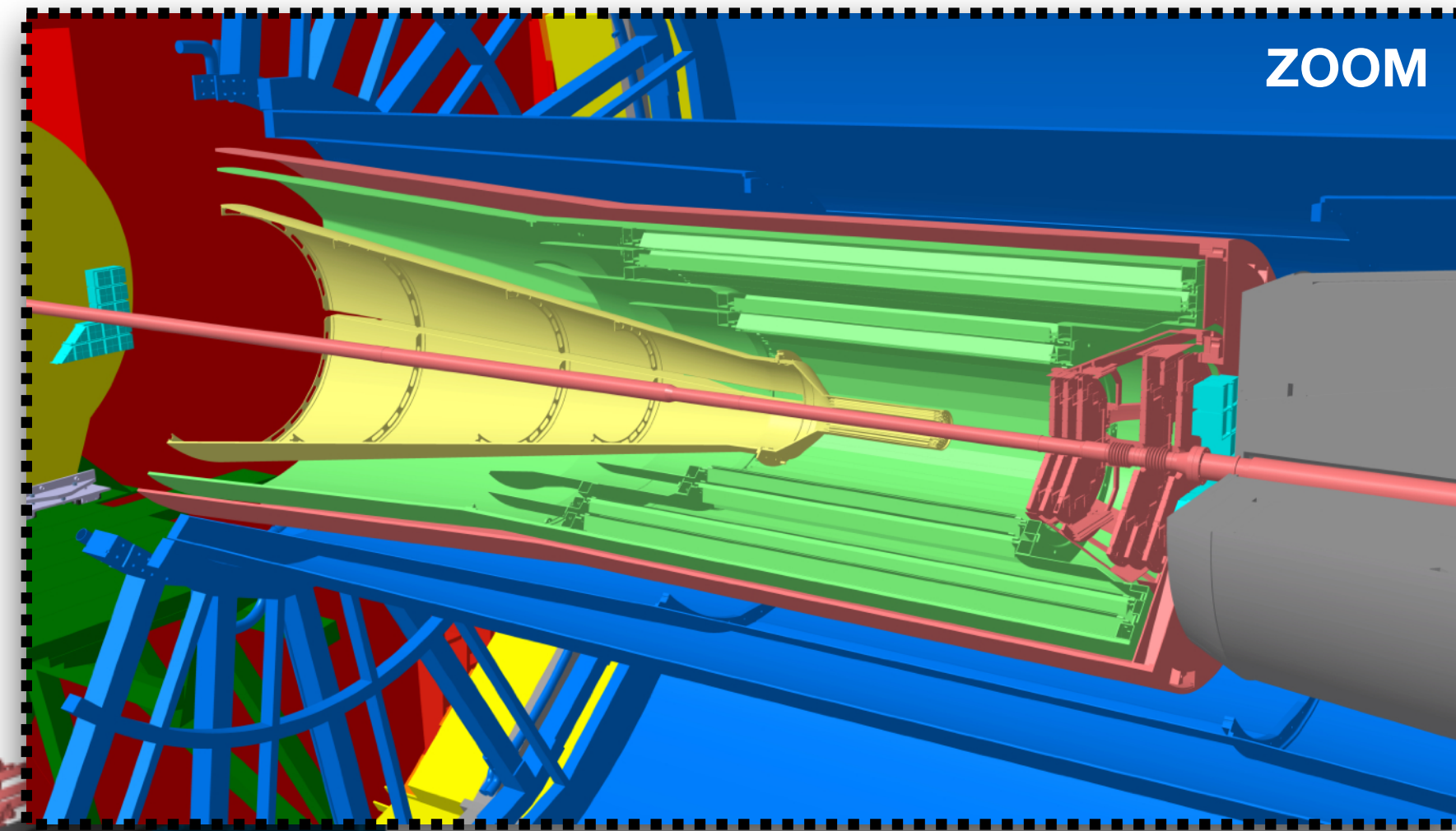
Design and expected performance of the **ALICE ITS3** tracker upgrade

Bong-Hwi Lim (INFN Torino)
on behalf of **ALICE** collaboration

24/09/2024

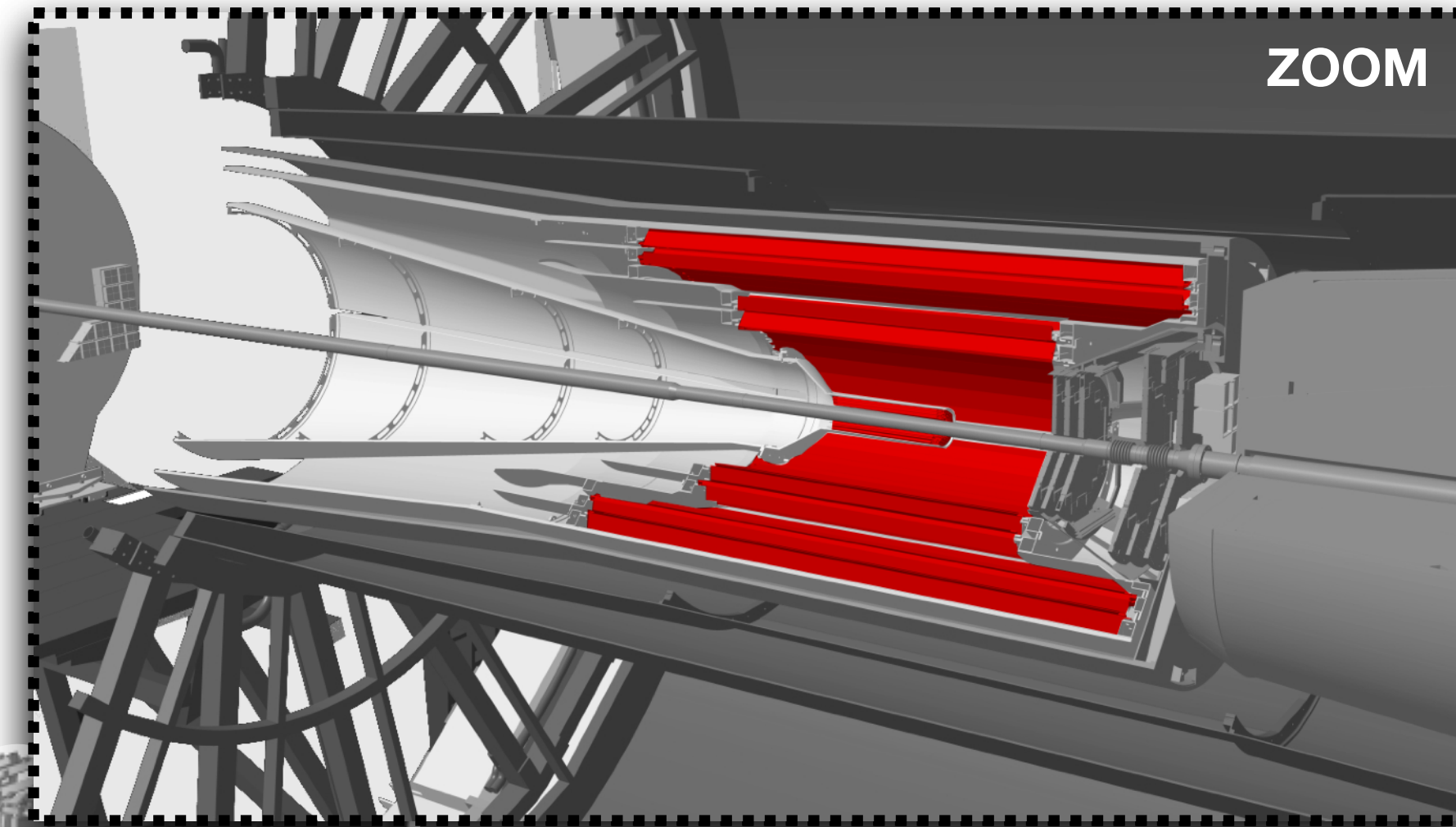


The ALICE experiment



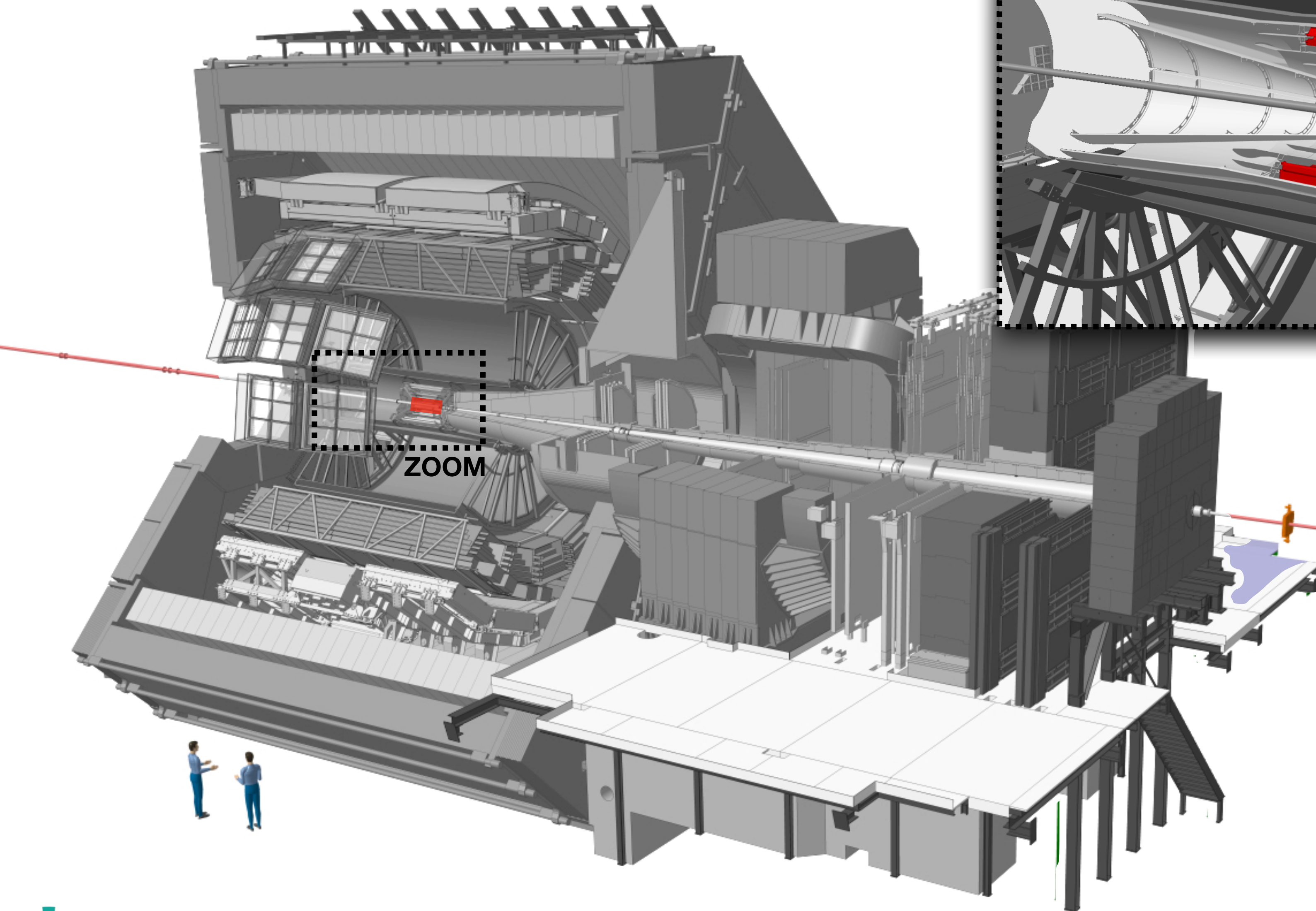
- Study of **strongly interacting matter at extreme densities (QGP)** in heavy-ion collisions at the LHC (CERN)
- **Very high multiplicities:** tracking of up to O(10k) particles in single event
- Charm and beauty hadron reconstruction
- Low momentum ($\approx 1\text{ GeV}/c$) particle reconstruction

The ALICE experiment



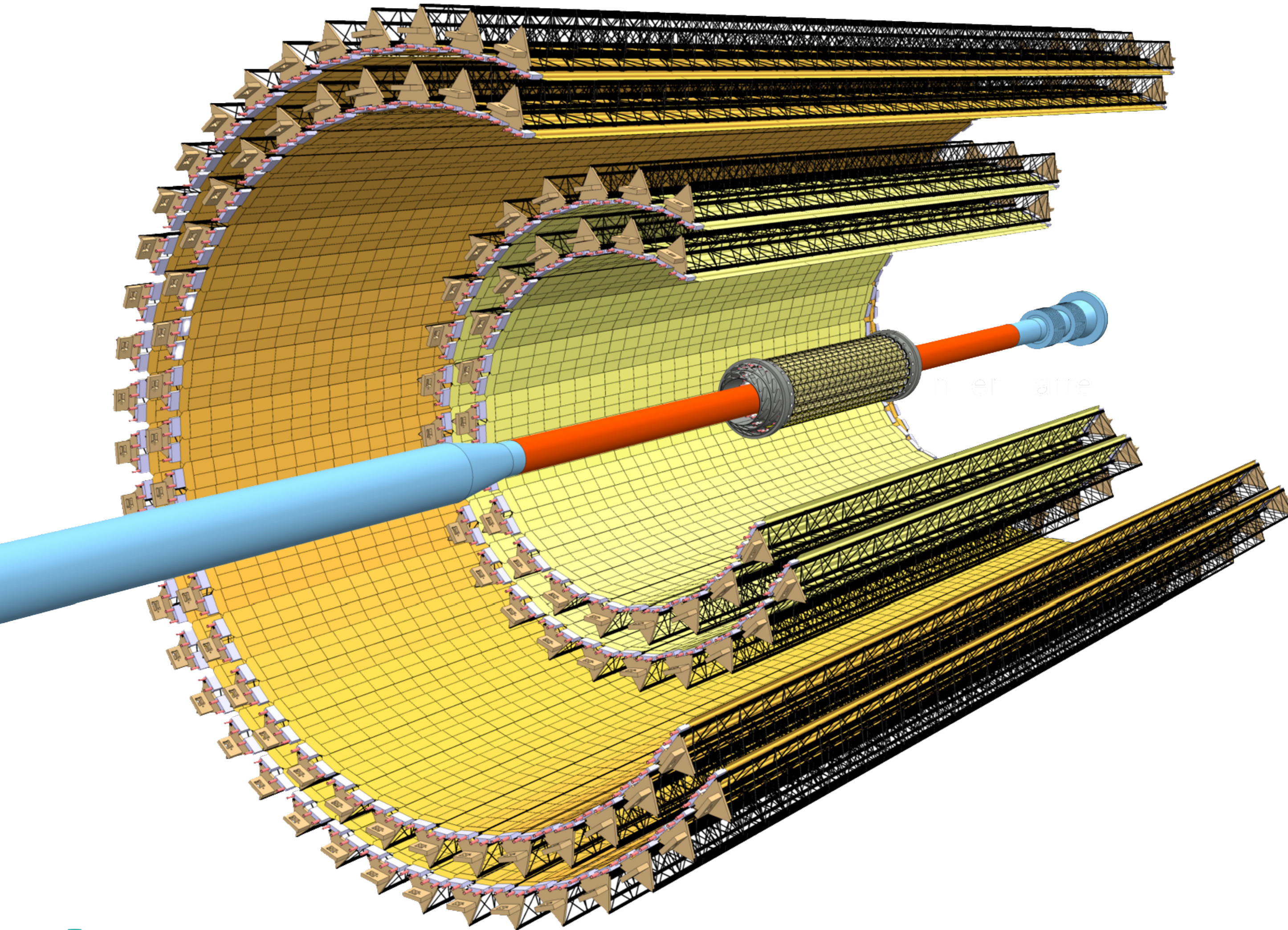
Inner Tracking System (ITS)

- Study of **strongly interacting matter at extreme densities (QGP)** in heavy-ion collisions at the LHC (CERN)
- **Very high multiplicities:** tracking of up to $O(10k)$ particles in single event
- Charm and beauty hadron reconstruction
- Low momentum ($\approx 1\text{ GeV}/c$) particle reconstruction



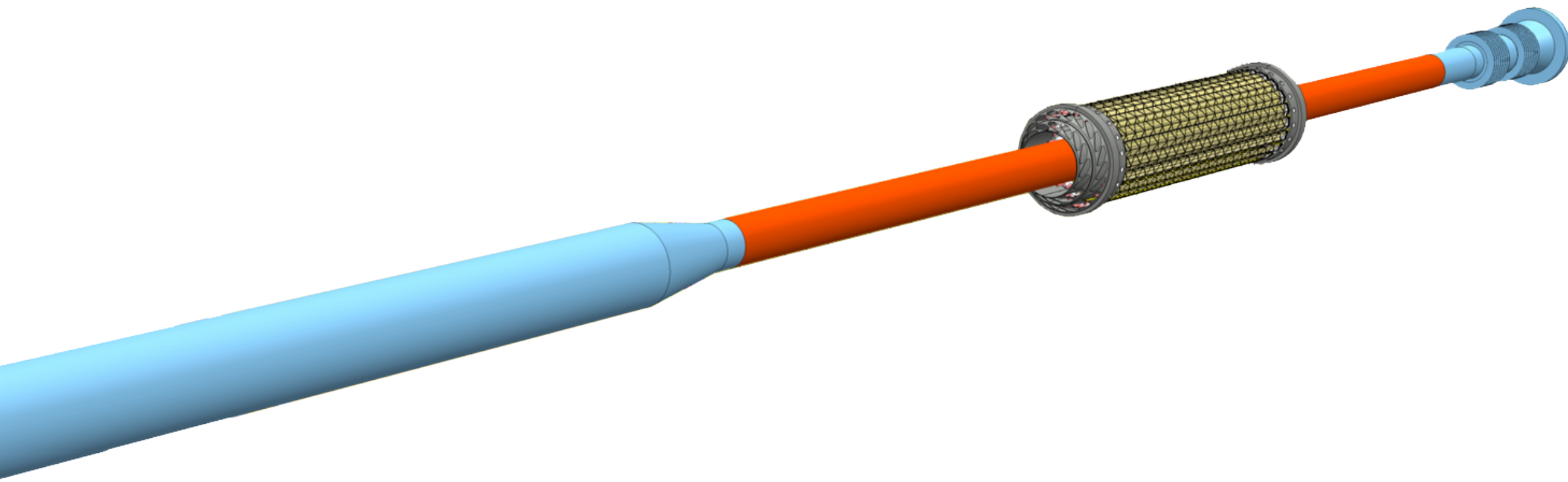
What will be changed?

Conceptual understanding of ITS3



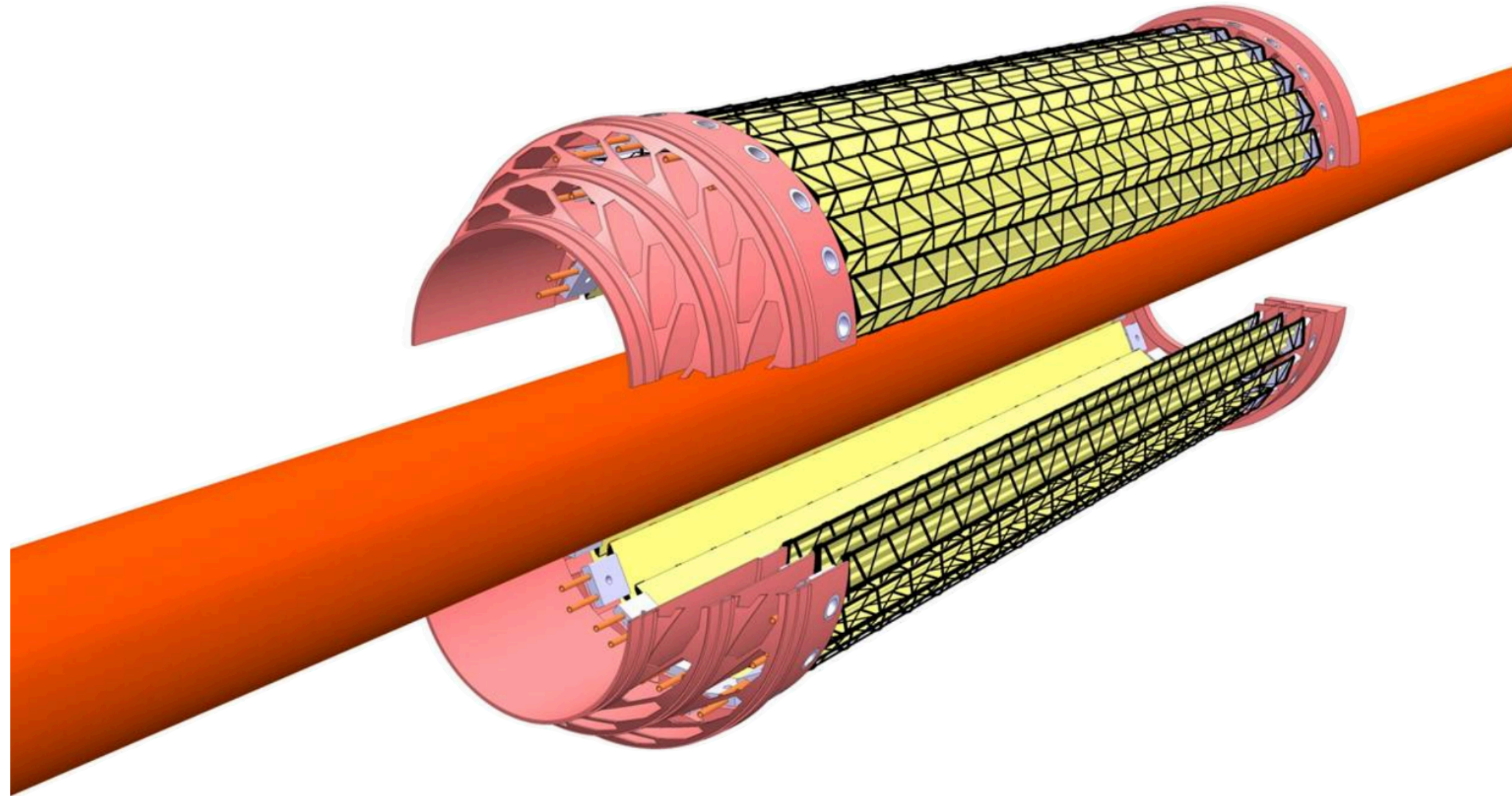
What will be changed?

Conceptual understanding of ITS3



What will be changed?

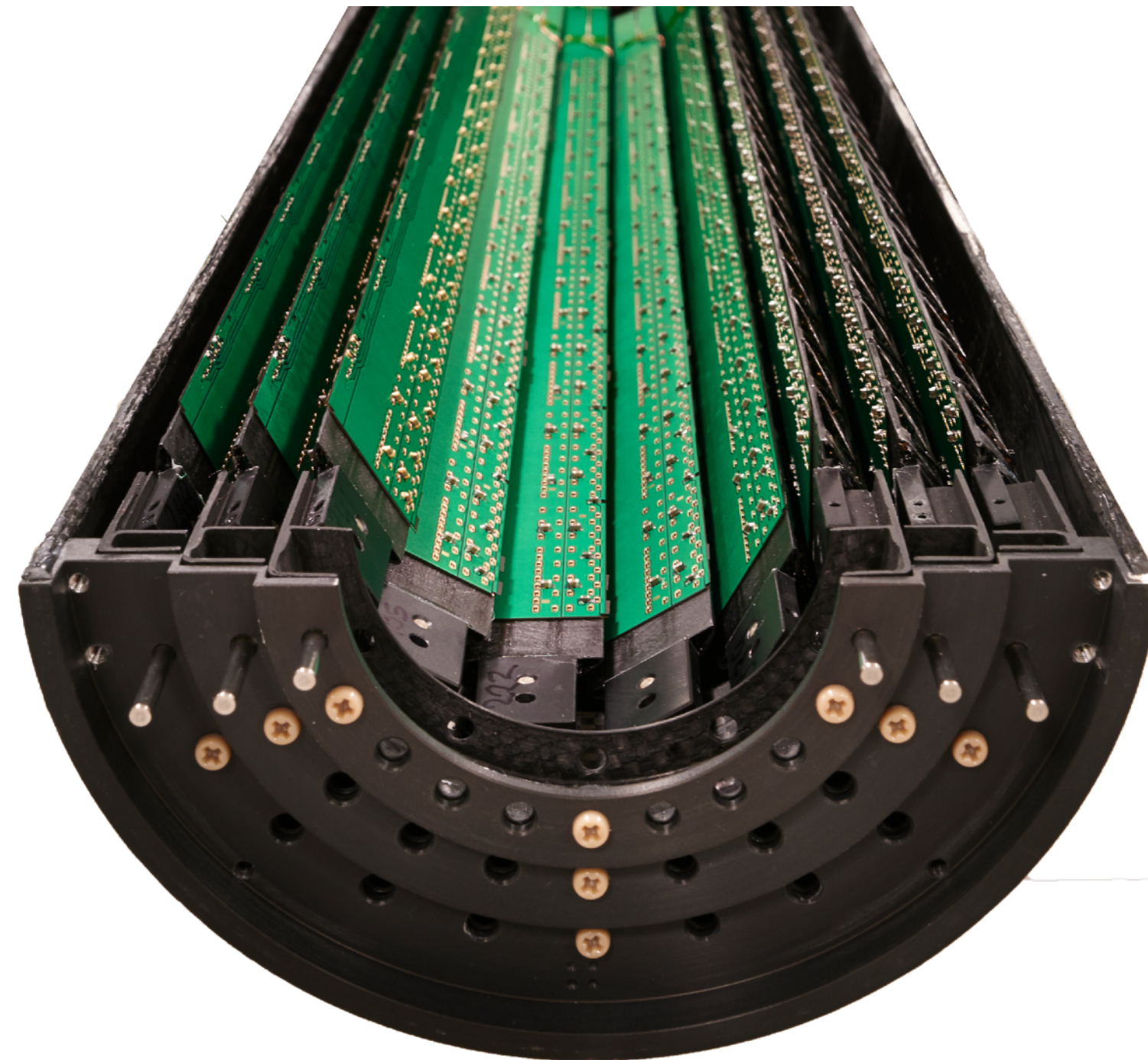
Conceptual understanding of ITS3



ITS Inner barrel

What will be changed?

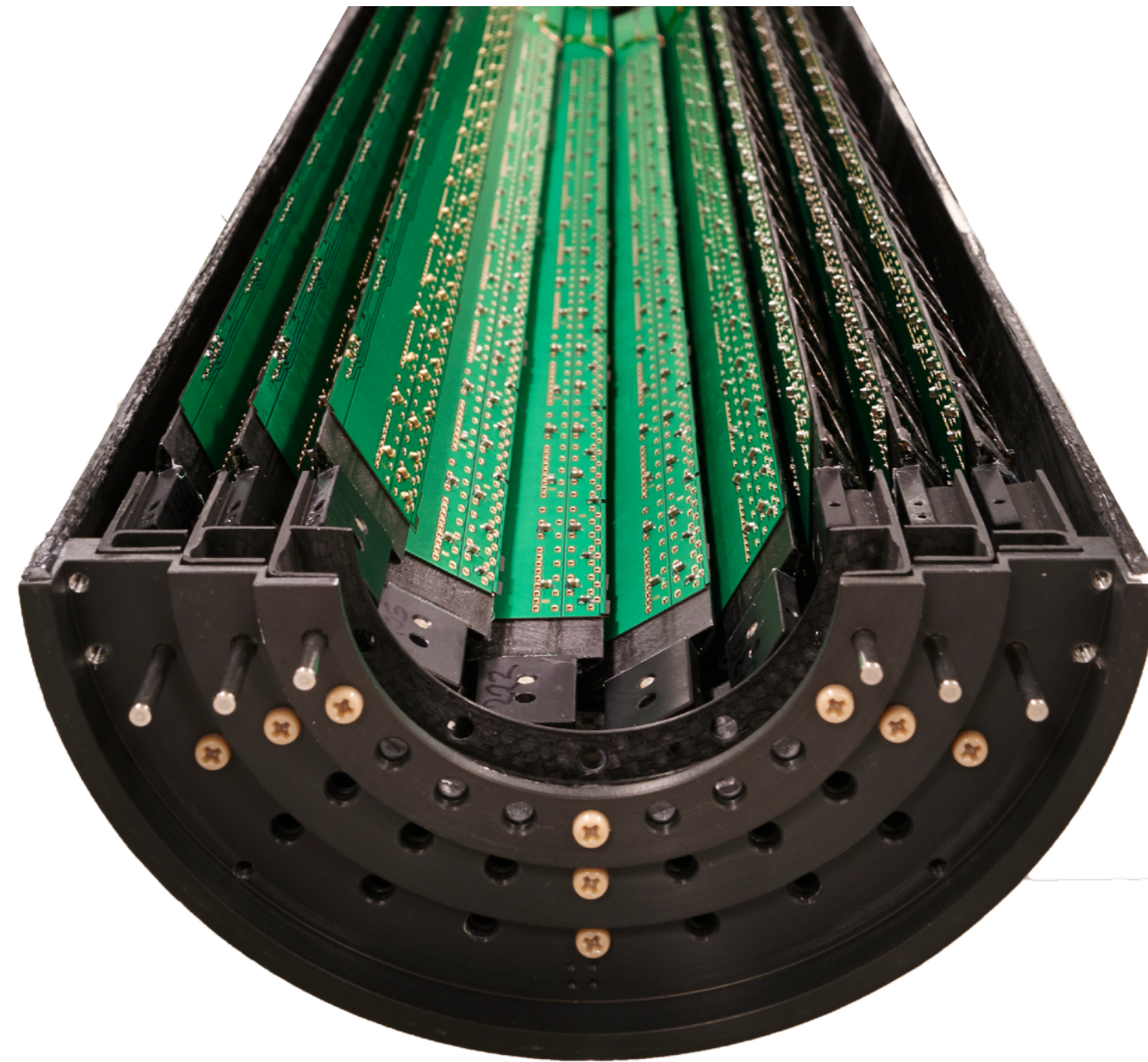
Conceptual understanding of ITS3



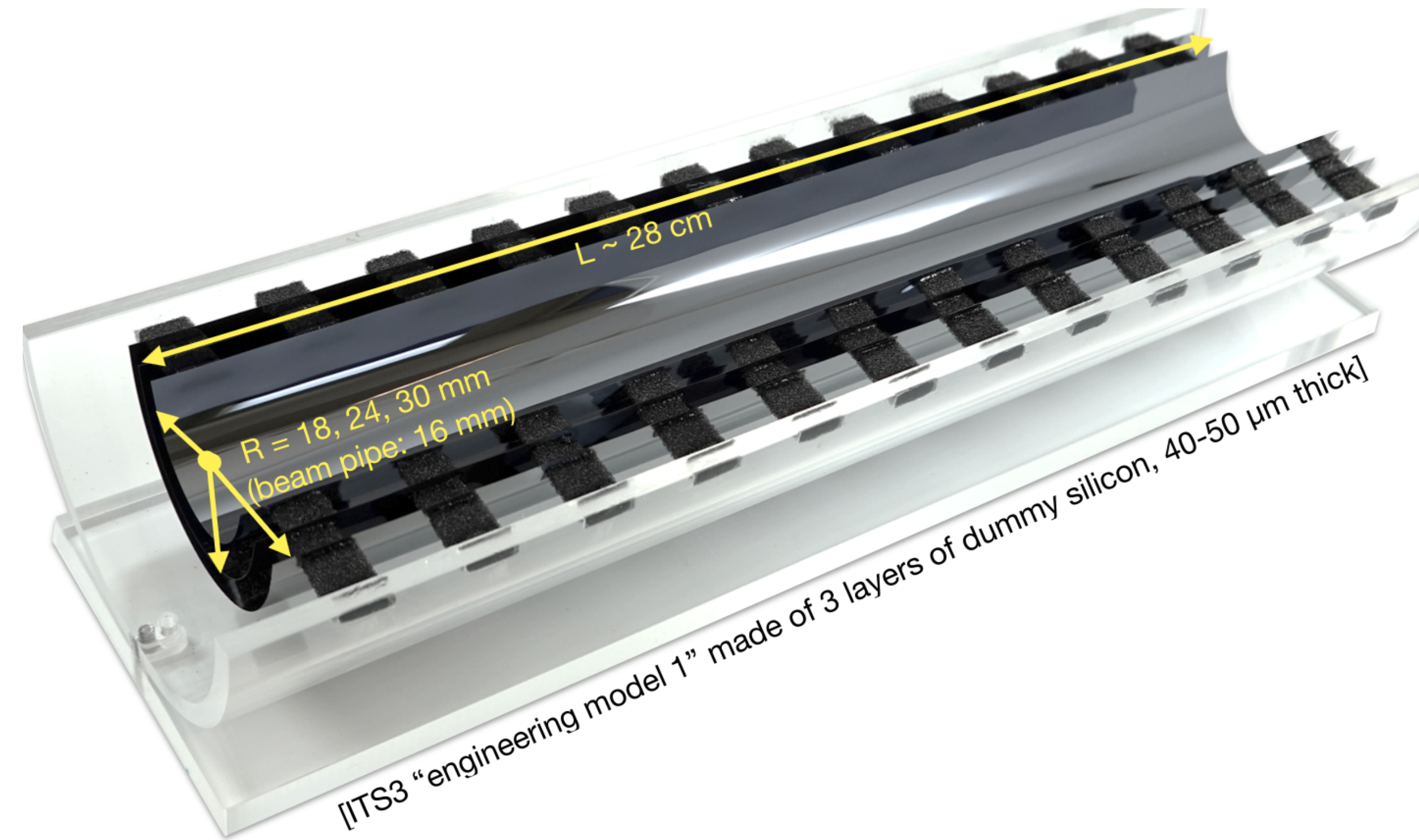
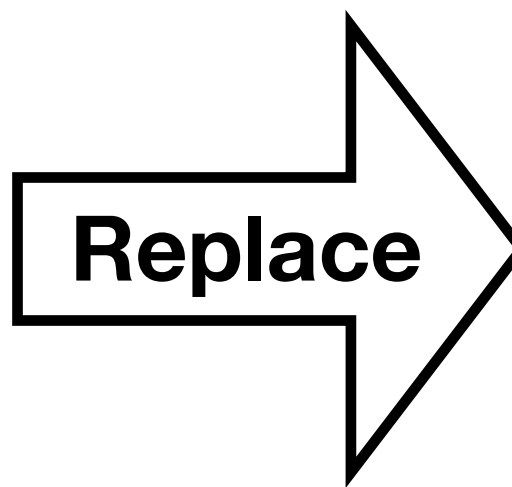
ITS half IB

What will be changed?

Conceptual understanding of ITS3



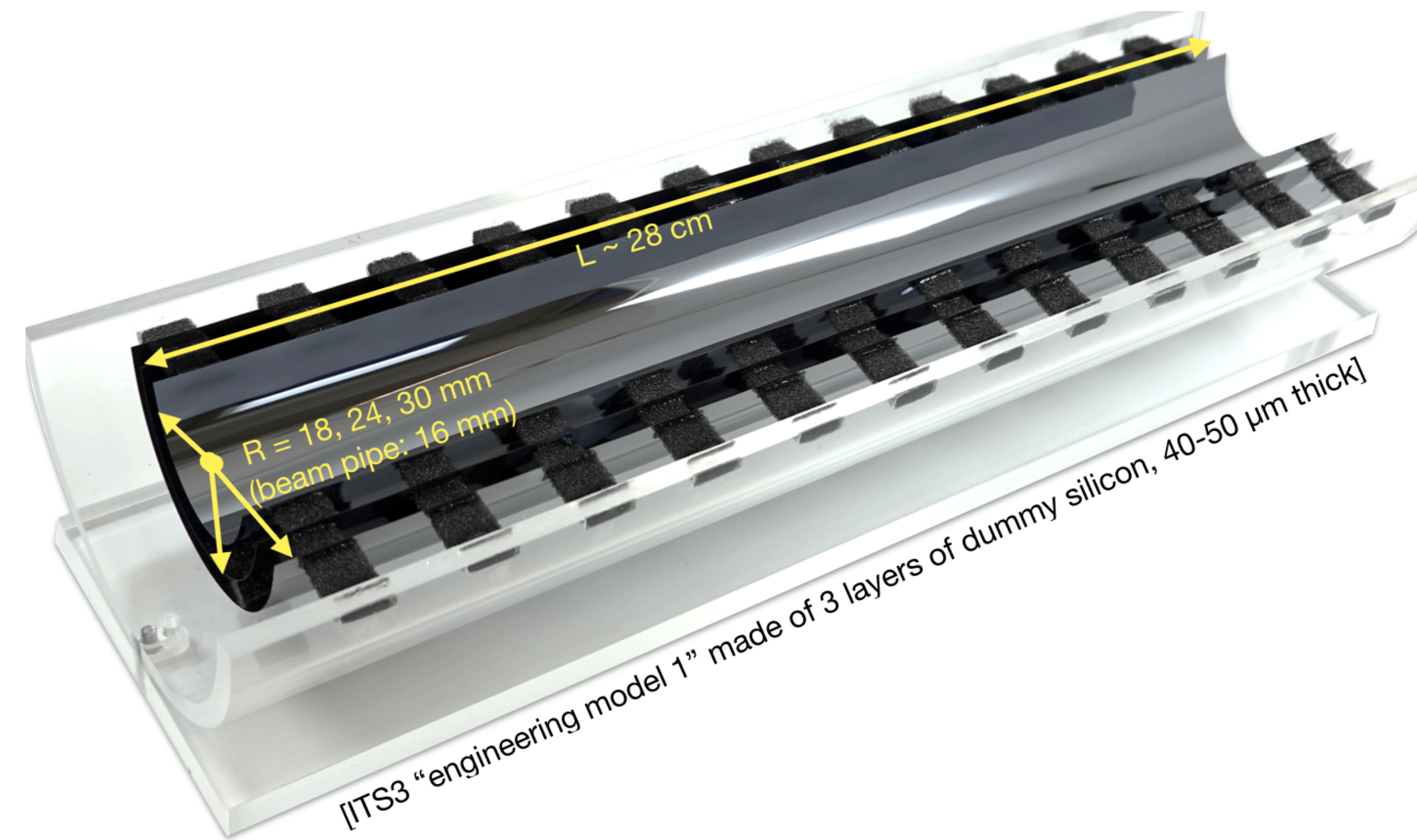
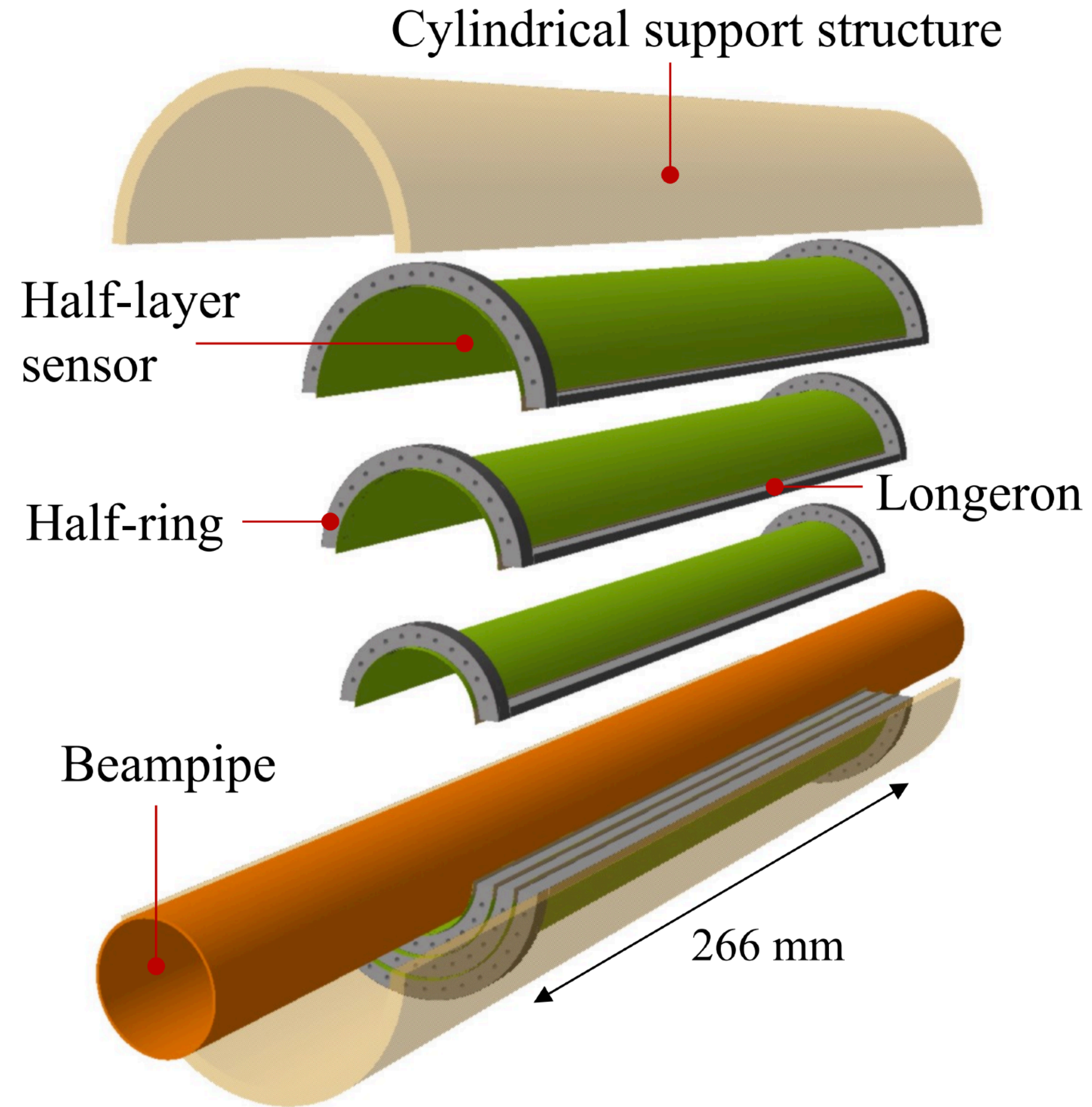
ITS half IB



- Replace the inner barrel (3 layers) of the current ITS
→ new 3 layers of ITS3 (wafer-scale size one chip)

What will be changed?

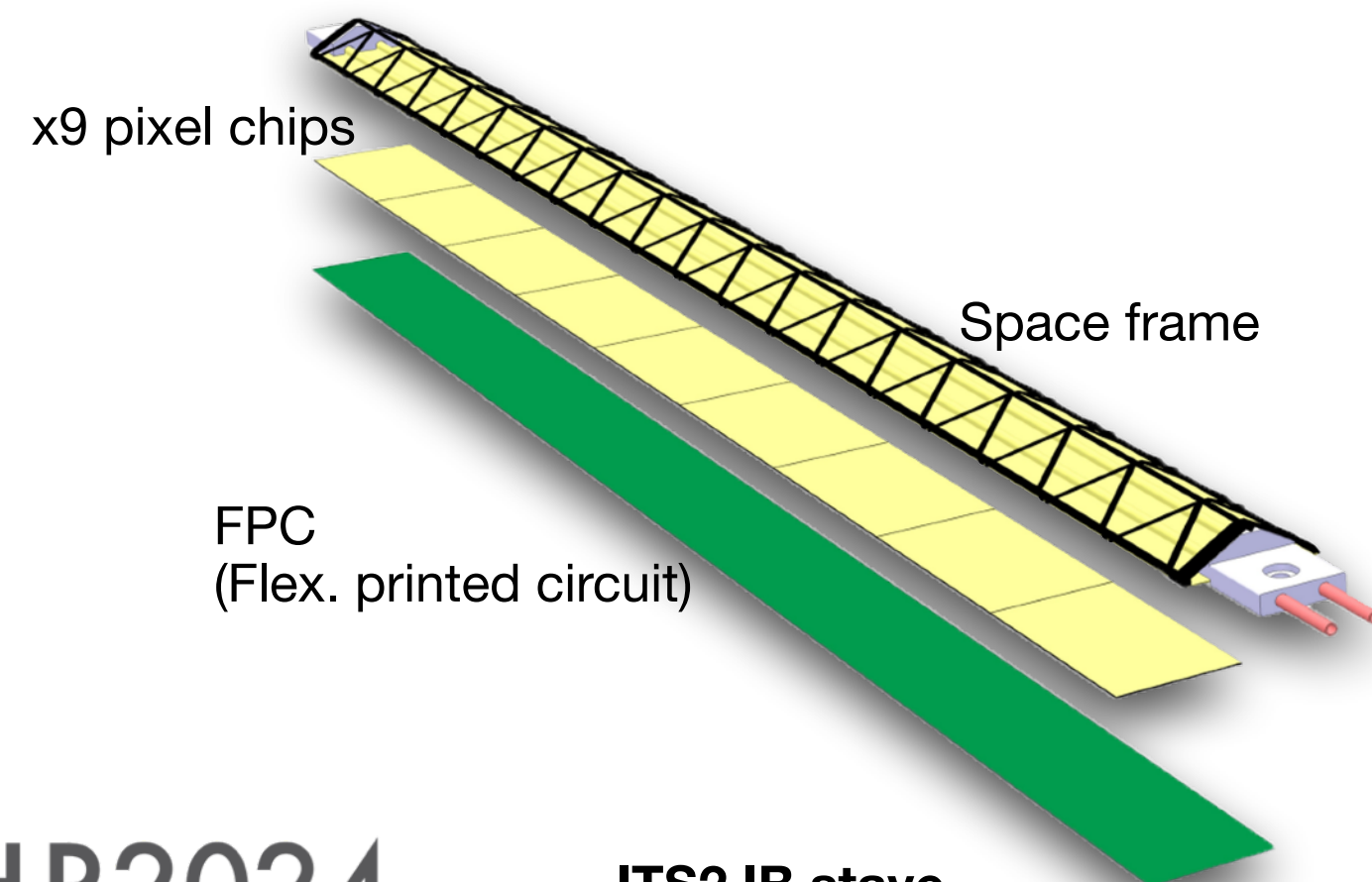
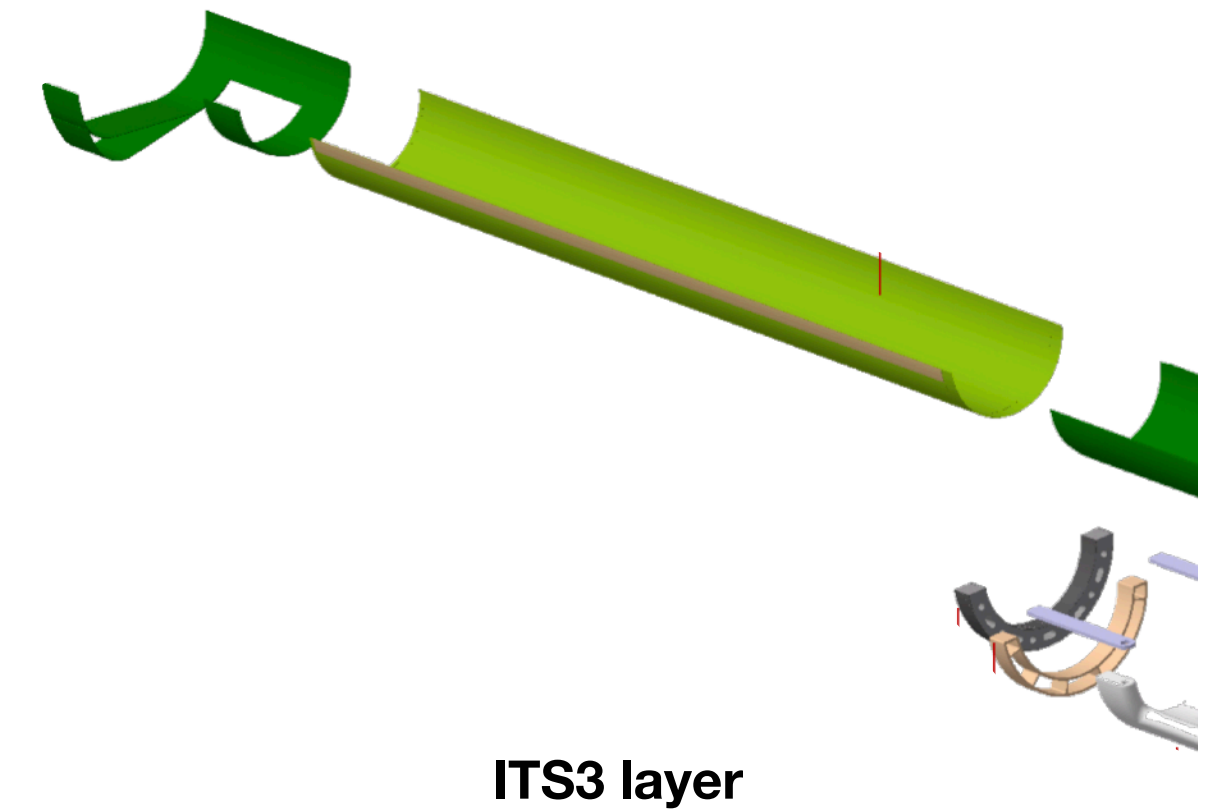
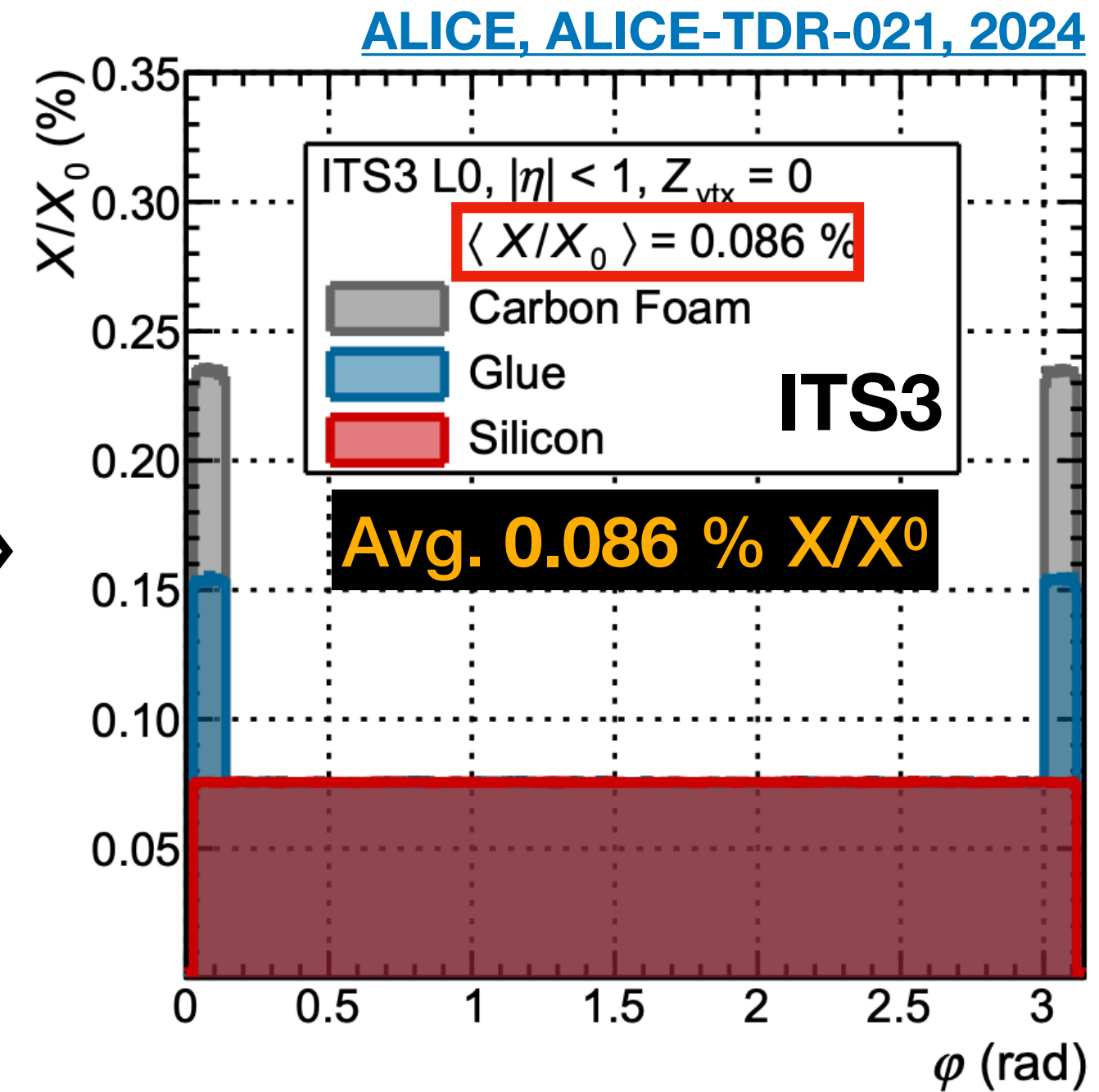
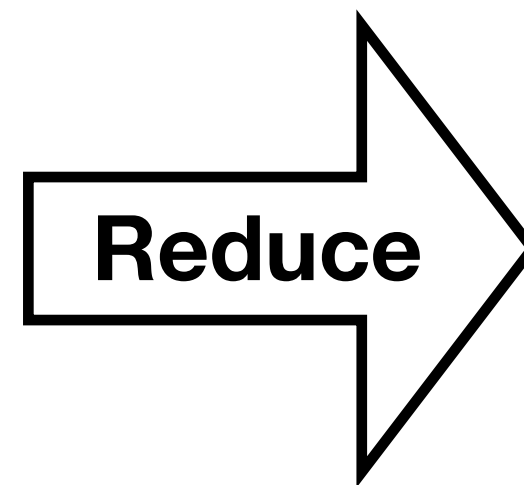
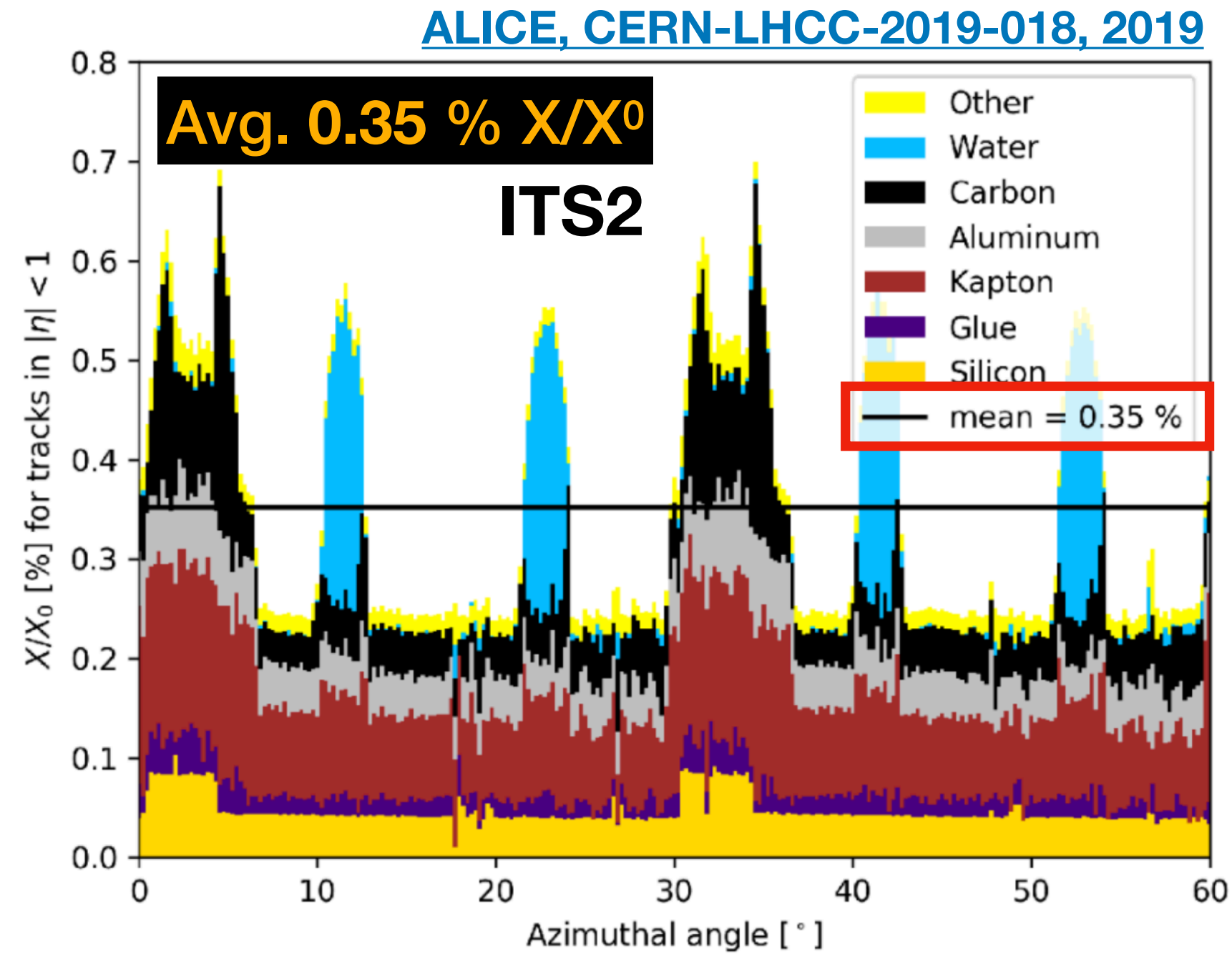
Conceptual understanding of ITS3



- Replace the inner barrel (3 layers) of the current ITS
→ new 3 layers of ITS3 (wafer-scale size one chip)

How can we achieve?

Possible improvements



1. Removal of water cooling:

- Possible if reduction of **power consumption** $< 40 \text{ mW/cm}^2$

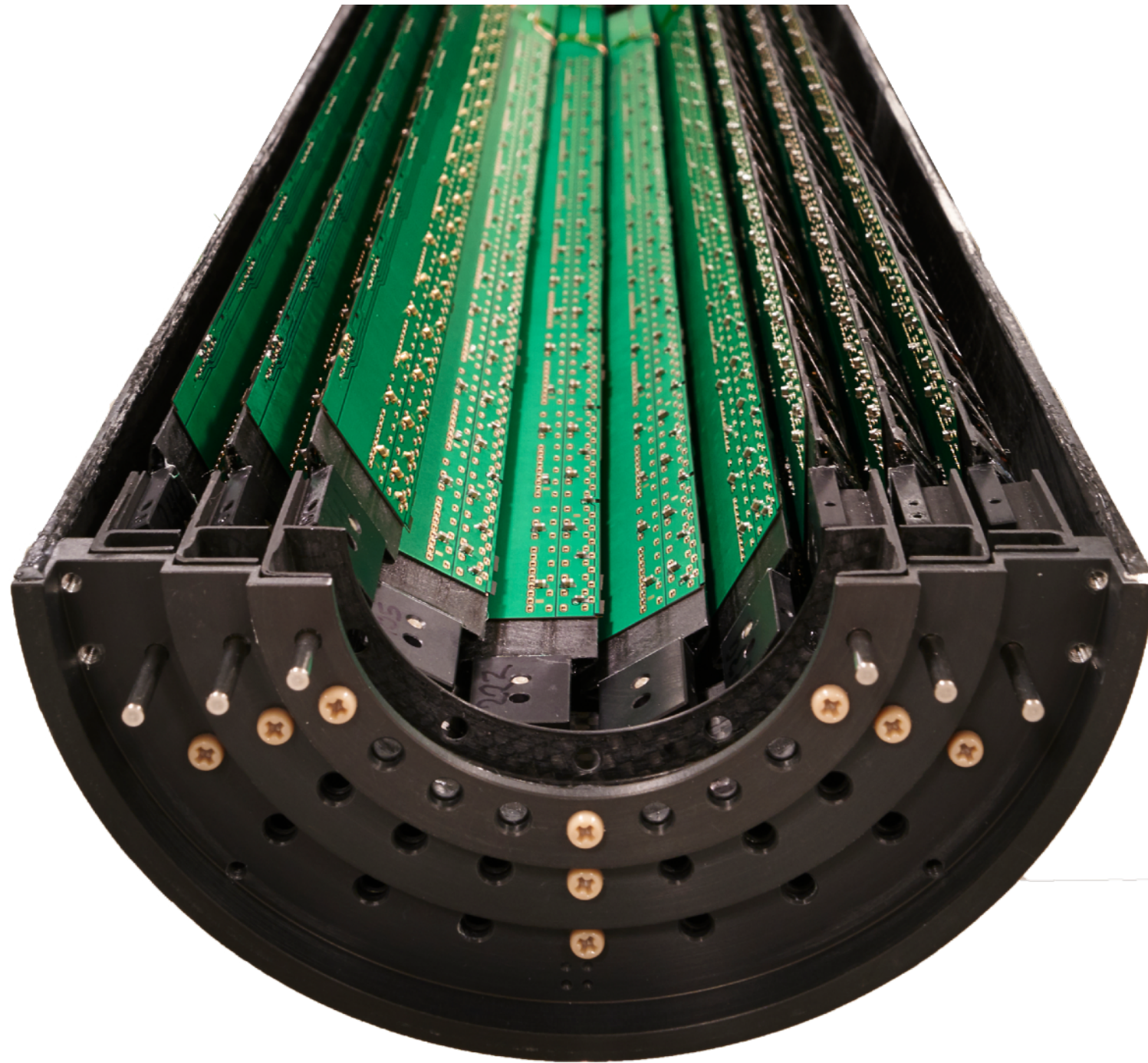
2. Removal of the Flexible Printed Circuit (FPC)

- **Integrate** it on the chip (data & power)

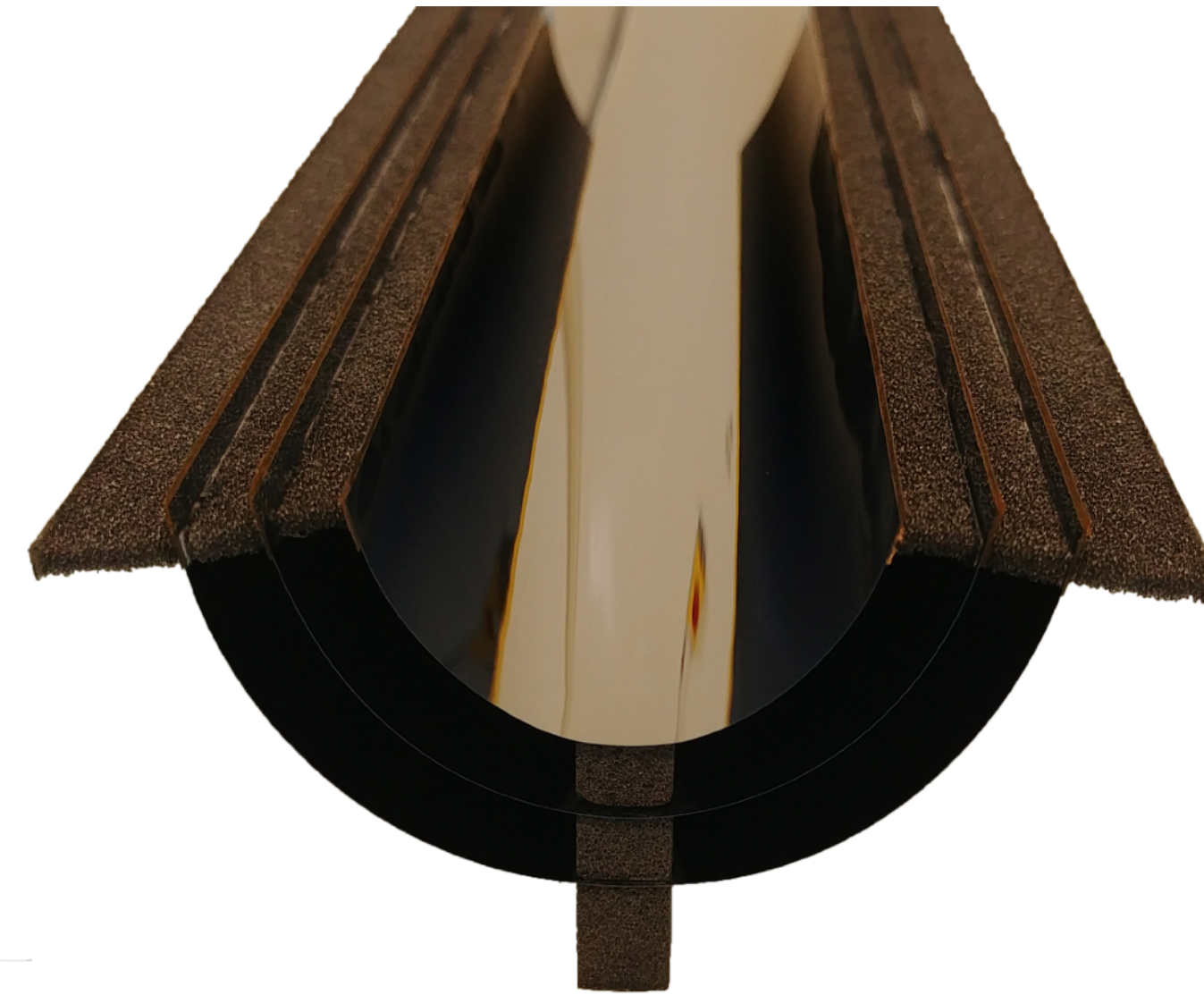
3. Removal of the mechanical support

- Thinned silicon [$\leq 50 \mu\text{m}$] \rightarrow **bending**

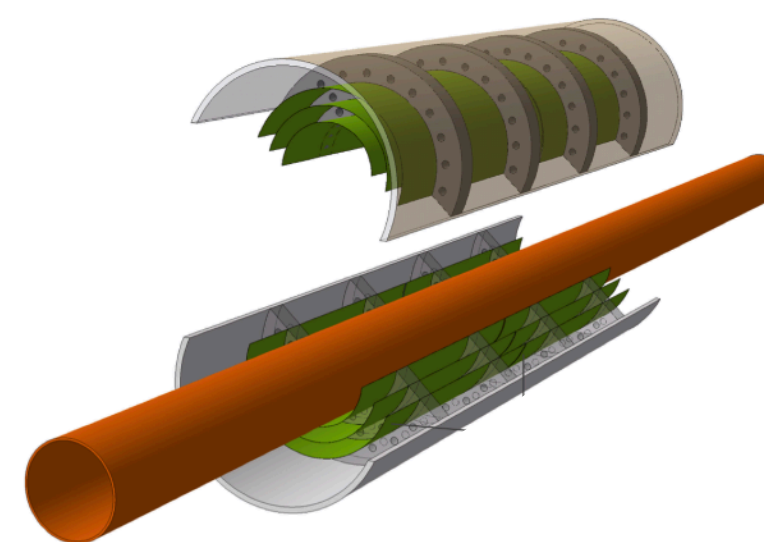
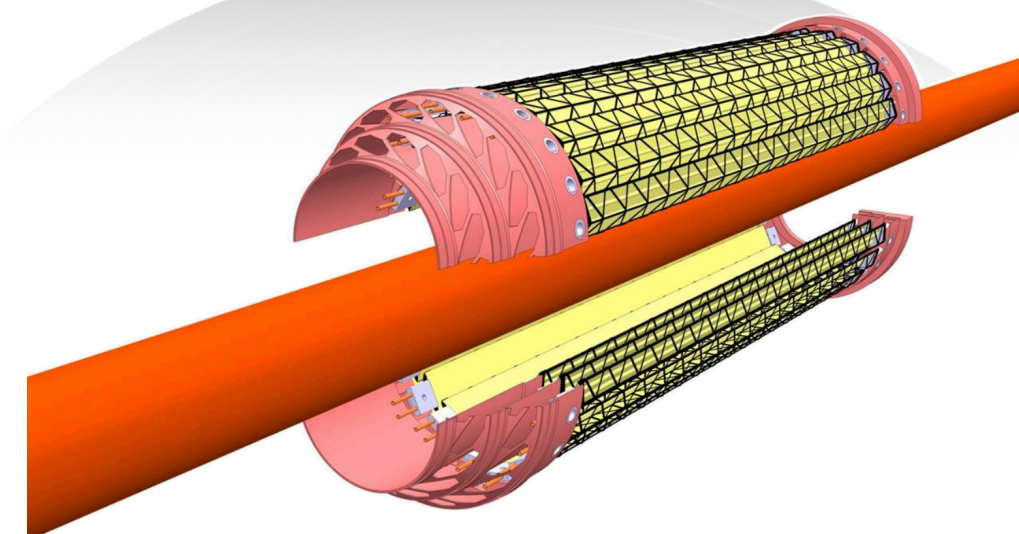
Some key points of ITS3 upgrade



ITS half IB



ITS3 engineering model



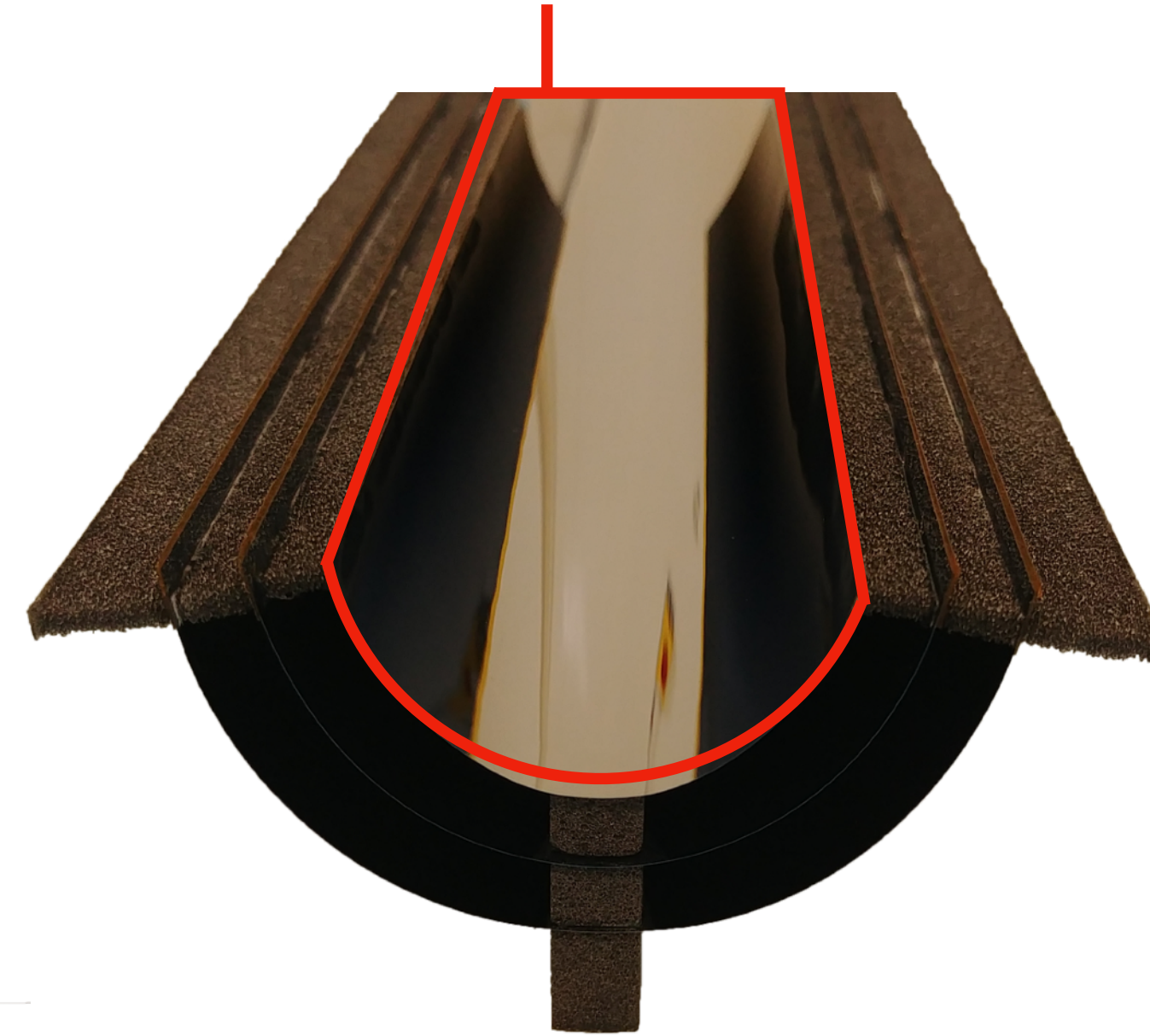
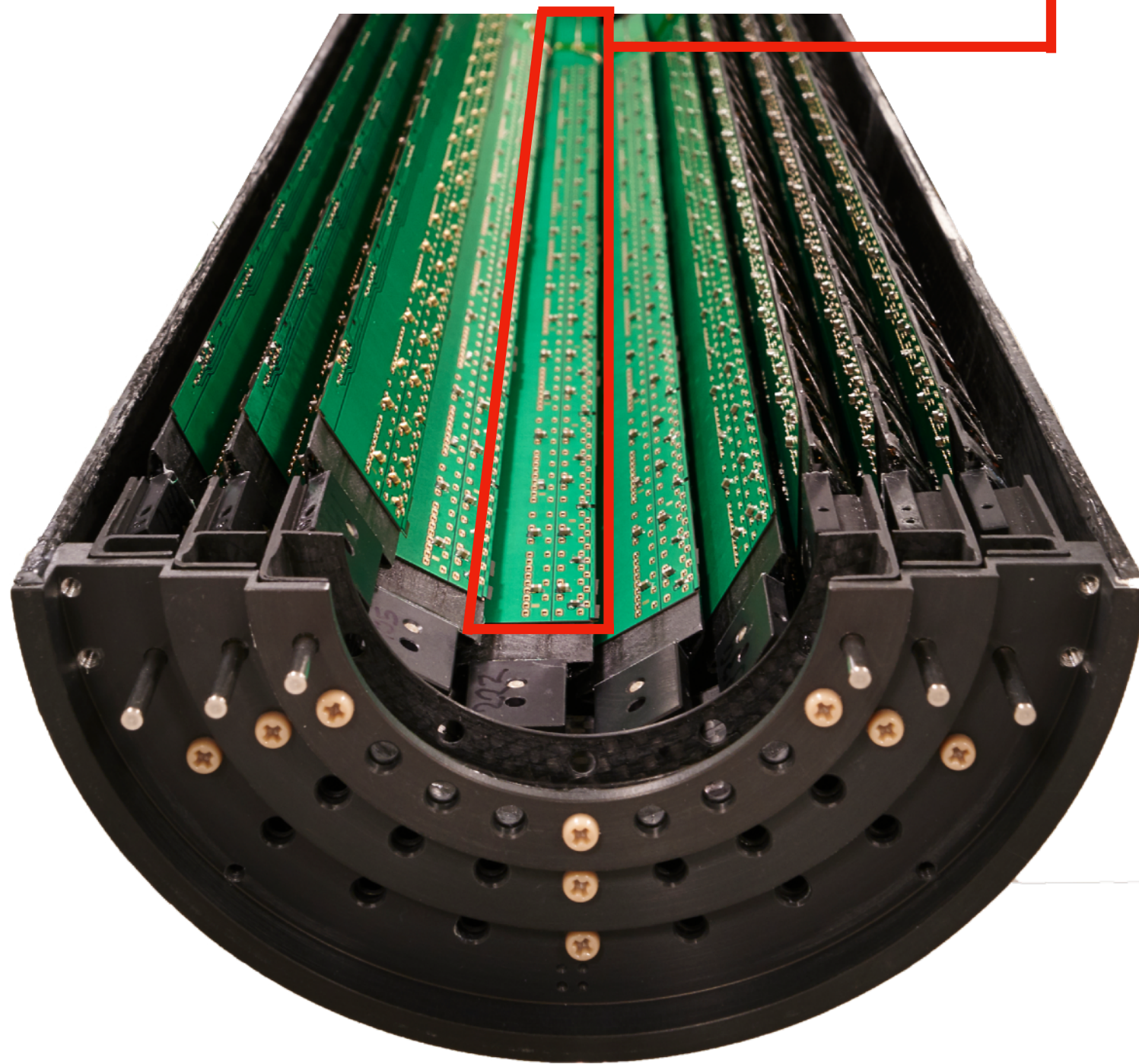
	ITS2	ITS3
Technology	180 nm	65 nm
Chips	432	6
Pixel size	29 x 27 μm^2	20.8 x 22.8 μm^2
Material budget / layer	0.35 % x/X^0	0.086 % x/X^0
r_{Lo}	24 mm	19 mm
$r_{\text{Beam pipe}}$	18.2 \pm 0.8 mm	16 + 0.5 mm

- **3 wafer-scaled bent CMOS active silicon sensor for half barrel**
- **~26 x ~10 cm size for last layer**

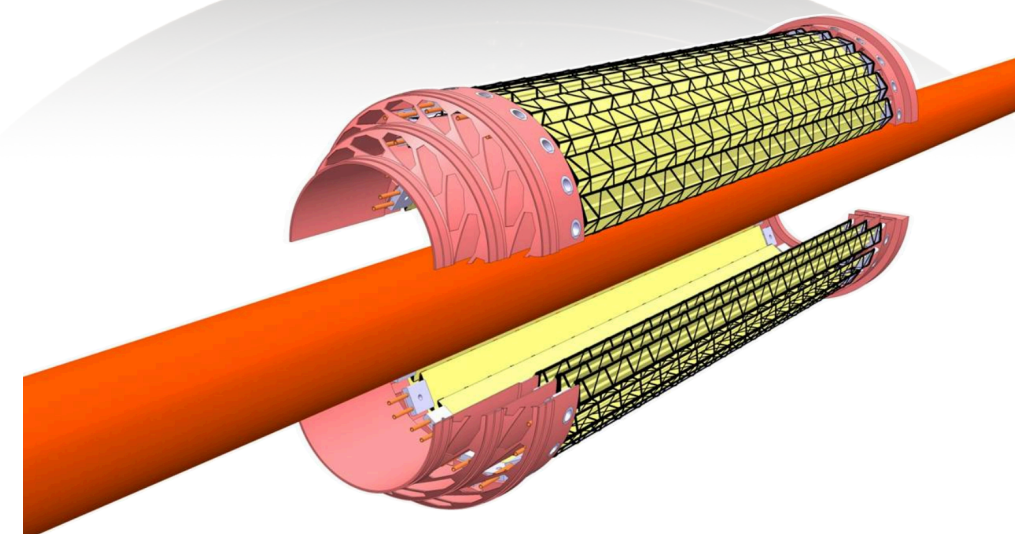
Some key points of ITS3 upgrade

Module structure (stave)

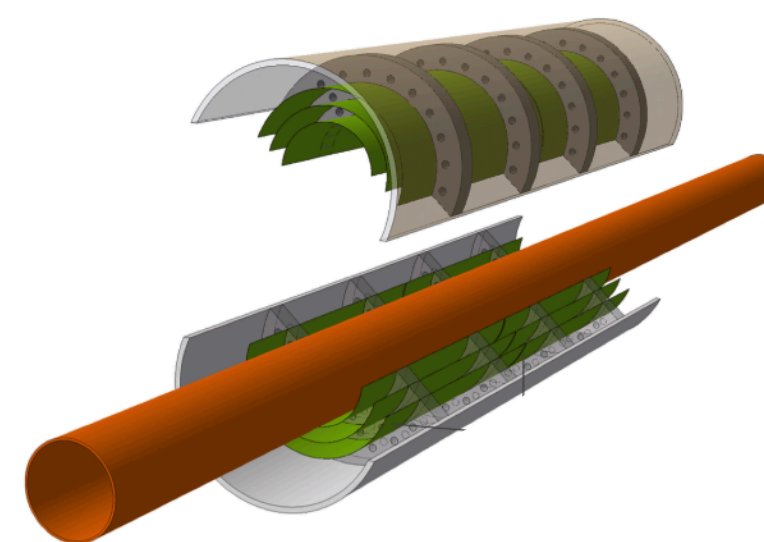
Wafer-scaled sensor (1chip)



ITS half IB



ITS3 engineering model



	ITS2	ITS3
Technology	180 nm	65 nm
Chips	432	6
Pixel size	29 x 27 μm^2	20.8 x 22.8 μm^2
Material budget / layer	0.35 % x/X^0	0.086 % x/X^0
r_{Lo}	24 mm	19 mm
$r_{\text{Beam pipe}}$	18.2 \pm 0.8 mm	16 + 0.5 mm

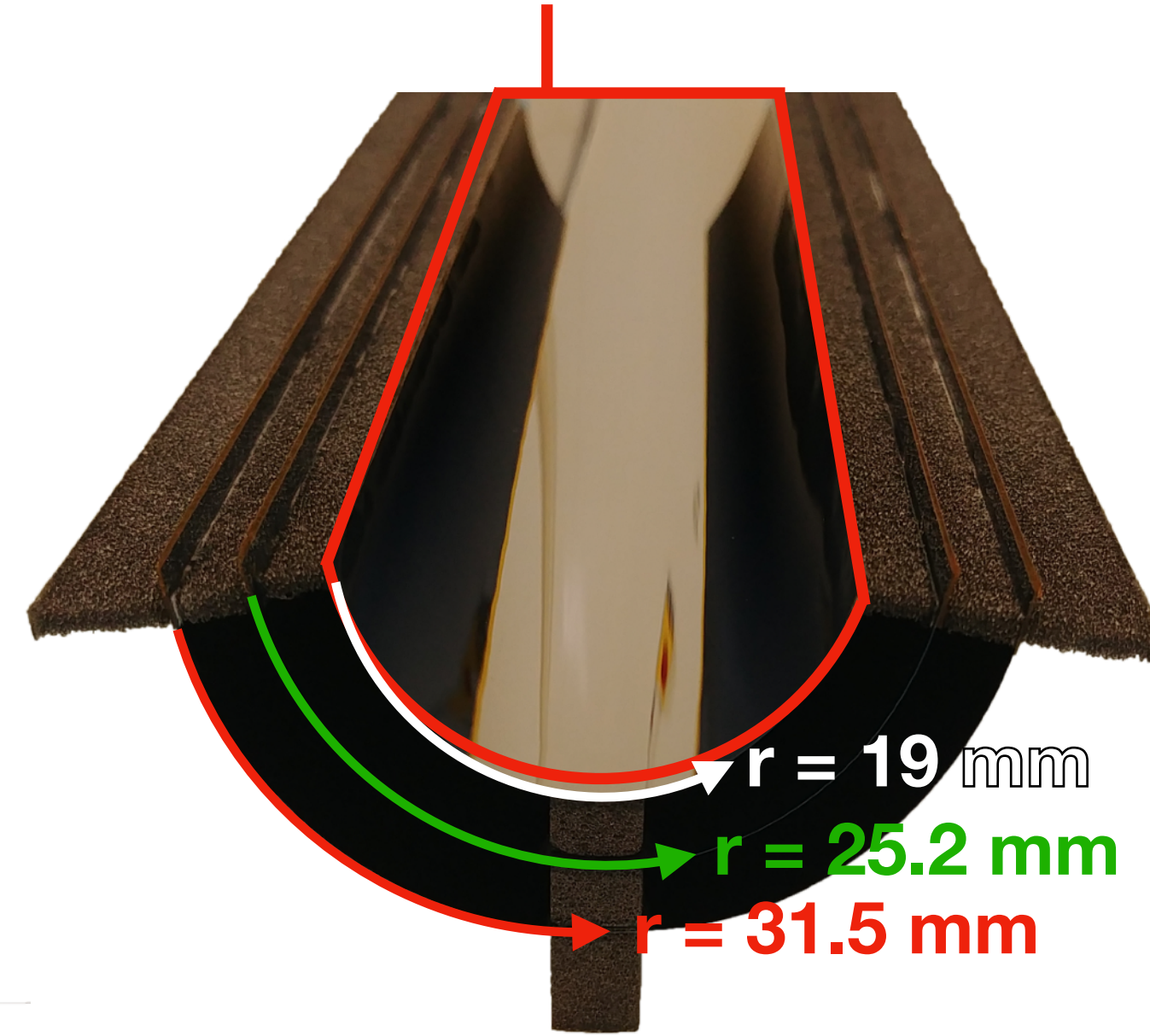
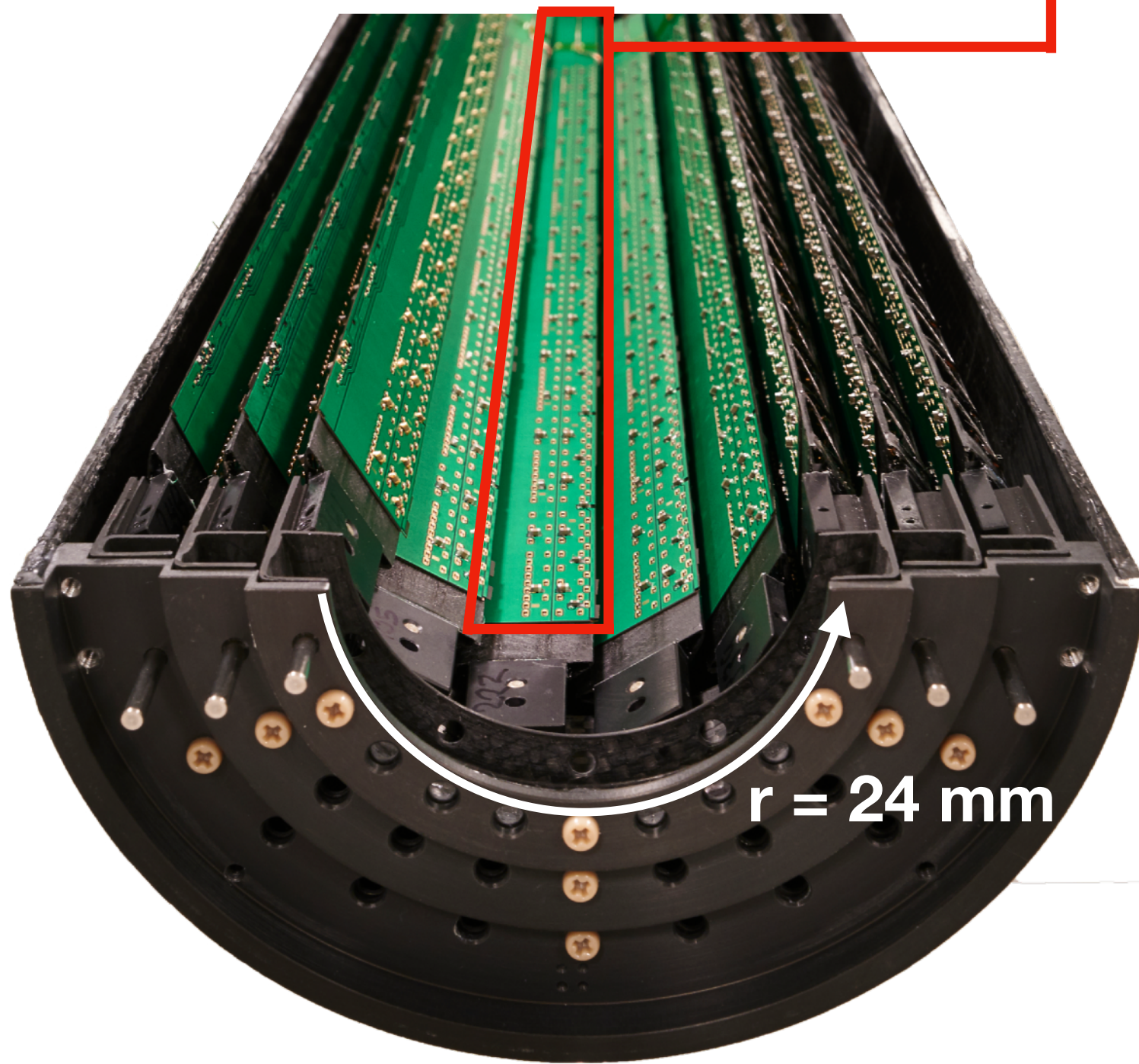
- **3 wafer-scaled bent CMOS active silicon sensor for half barrel**
- **~26 x ~10 cm size for last layer**

Some key points of ITS3 upgrade



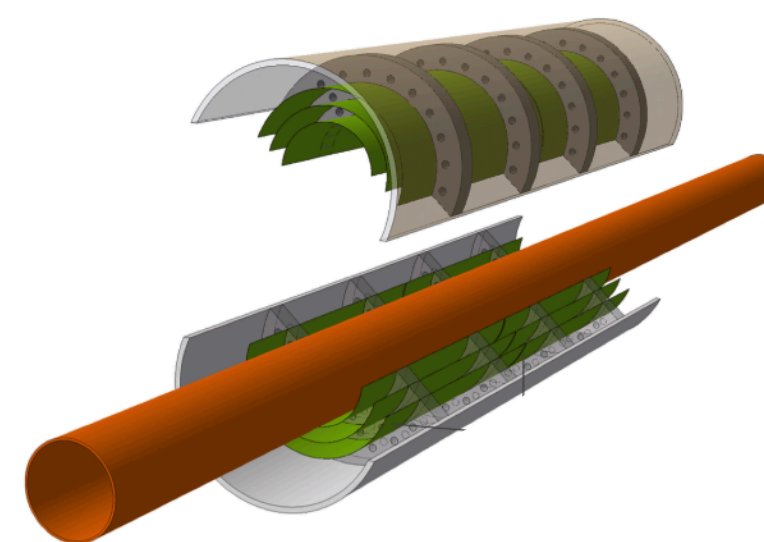
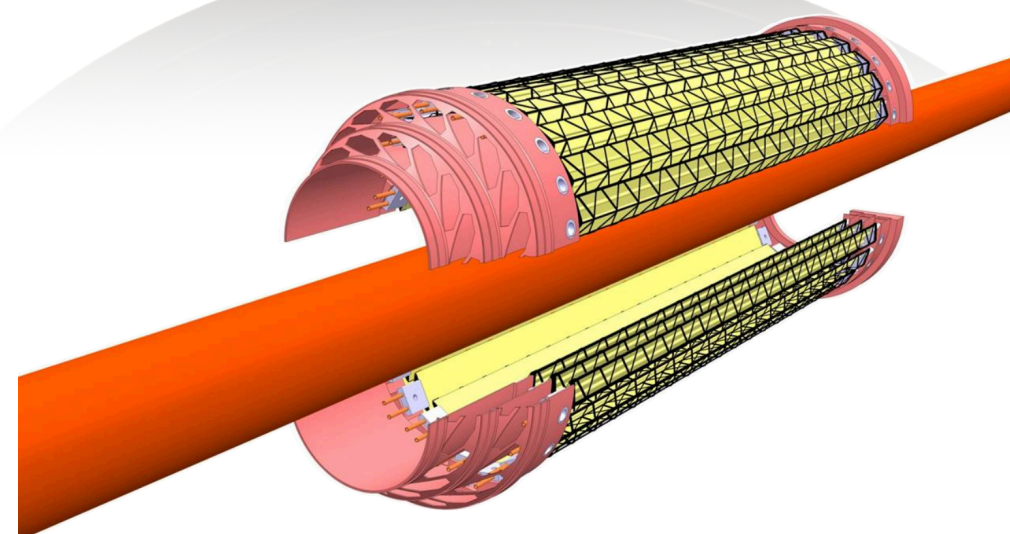
Module structure (stave)

Wafer-scaled sensor (1 chip)



ITS half IB

ITS3 engineering model



	ITS2	ITS3
Technology	180 nm	65 nm
Chips	432	6
Pixel size	29 x 27 μm^2	20.8 x 22.8 μm^2
Material budget / layer	0.35 % x/X^0	0.086 % x/X^0
r_{Lo}	24 mm	19 mm
$r_{Beam\ pipe}$	18.2 \pm 0.8 mm	16 + 0.5 mm

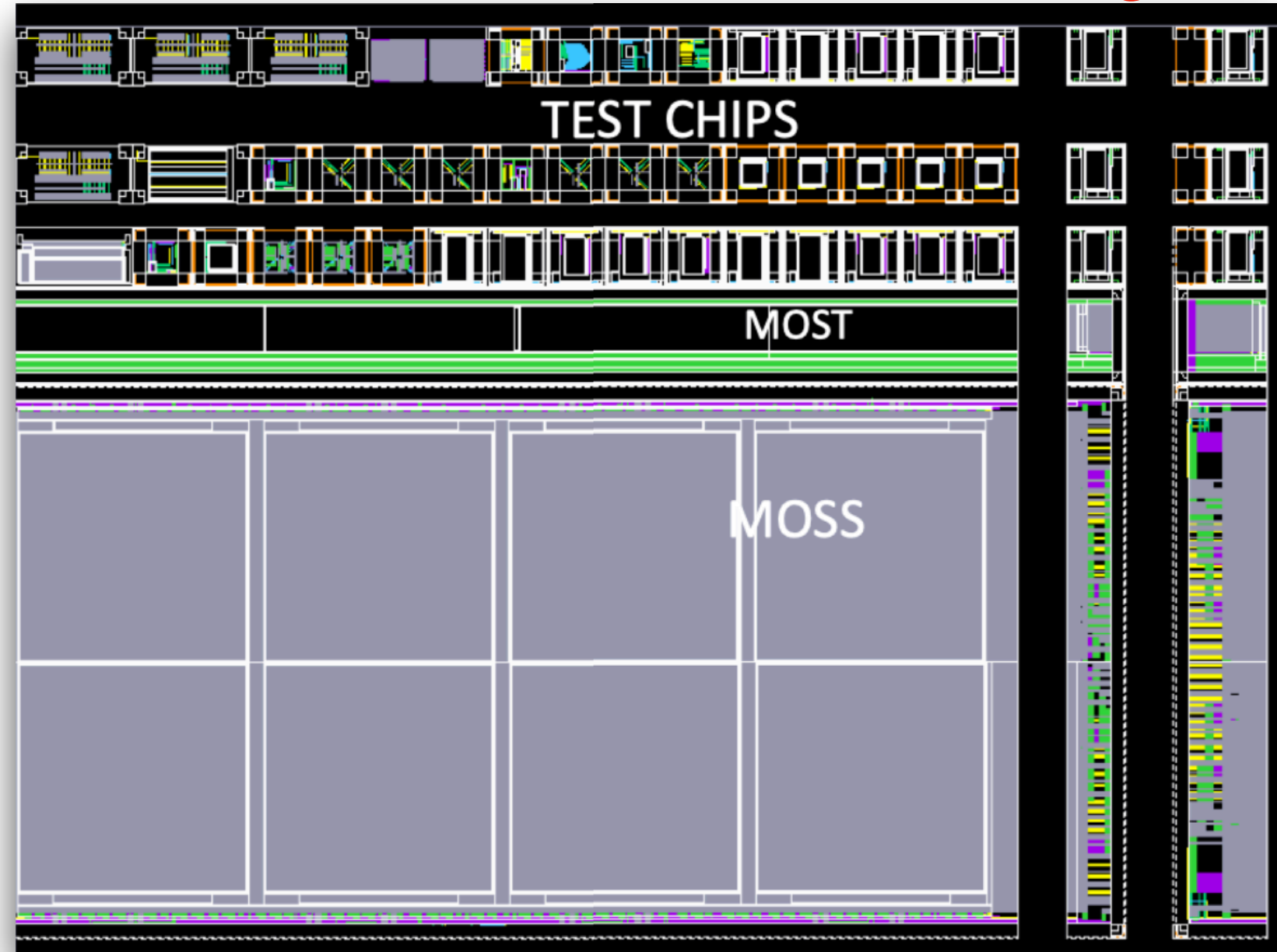
- **3 wafer-scaled bent CMOS active silicon sensor for half barrel**
- **~26 x ~10 cm size for last layer**

How can we make such a large sensor?

Stitching (simplified)

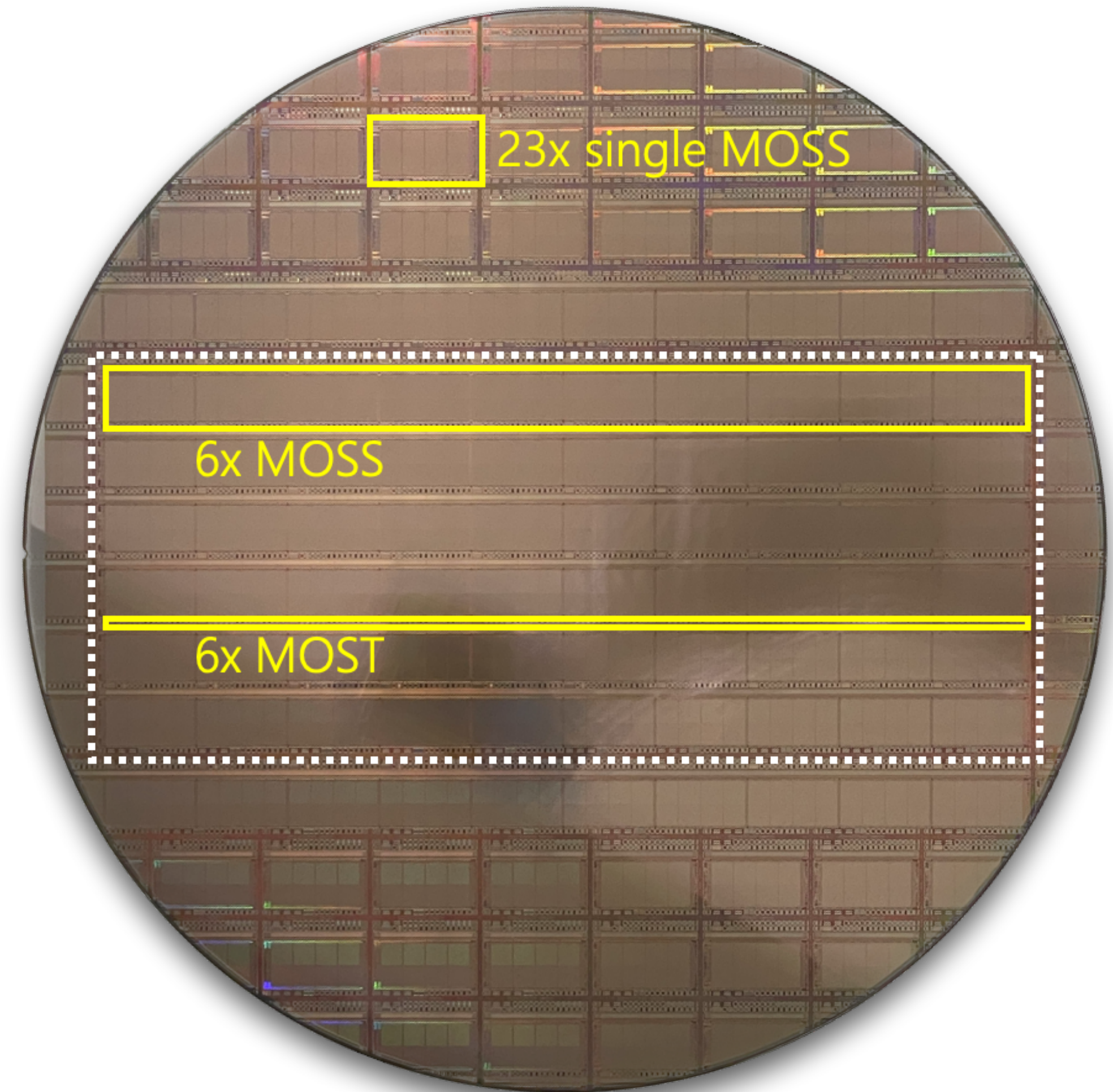


"What we designed"



Reticle (mask)

"What we want to fabricate"



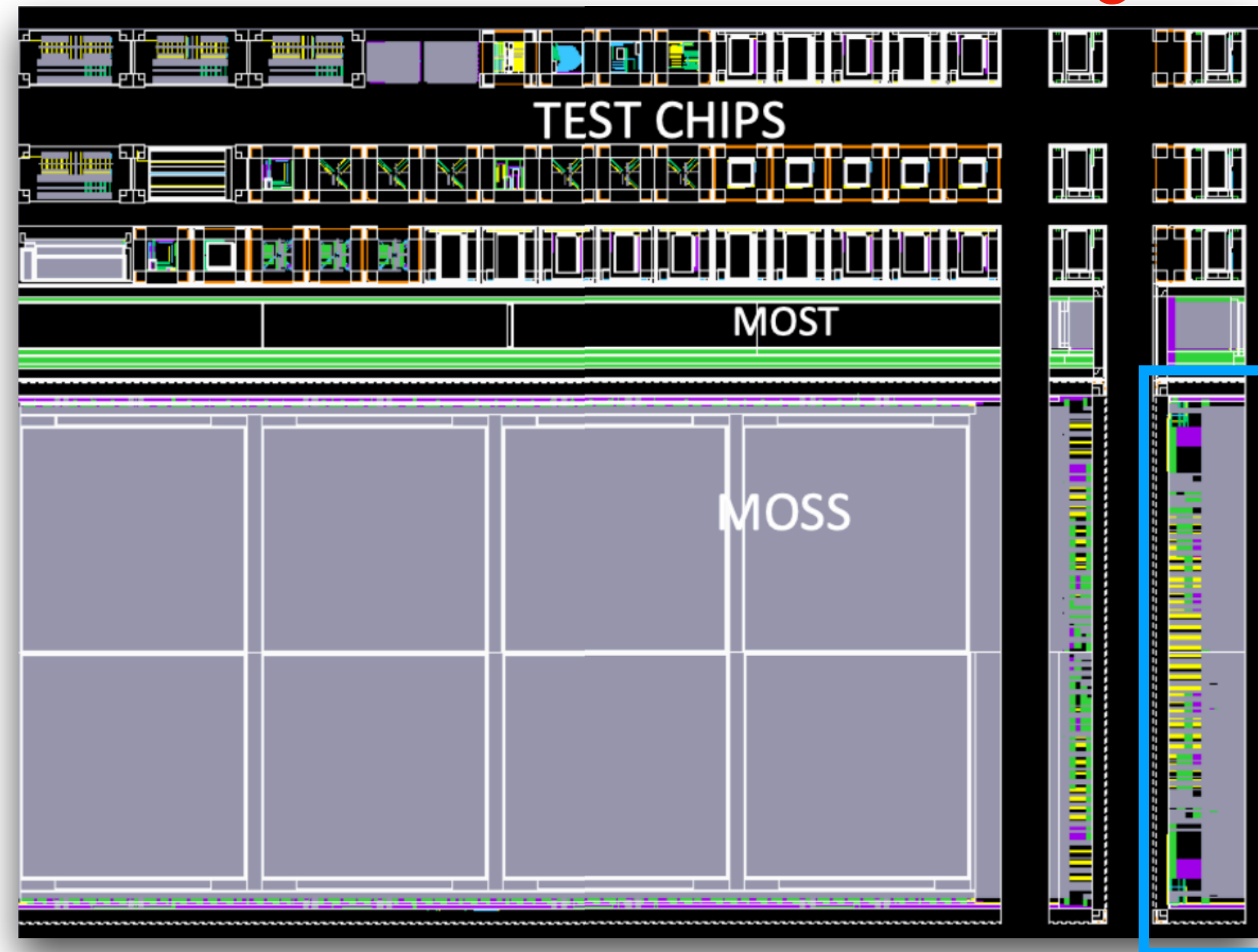
Wafer ($\phi=300\text{mm}$)

How can we make such a large sensor?

Stitching (simplified)

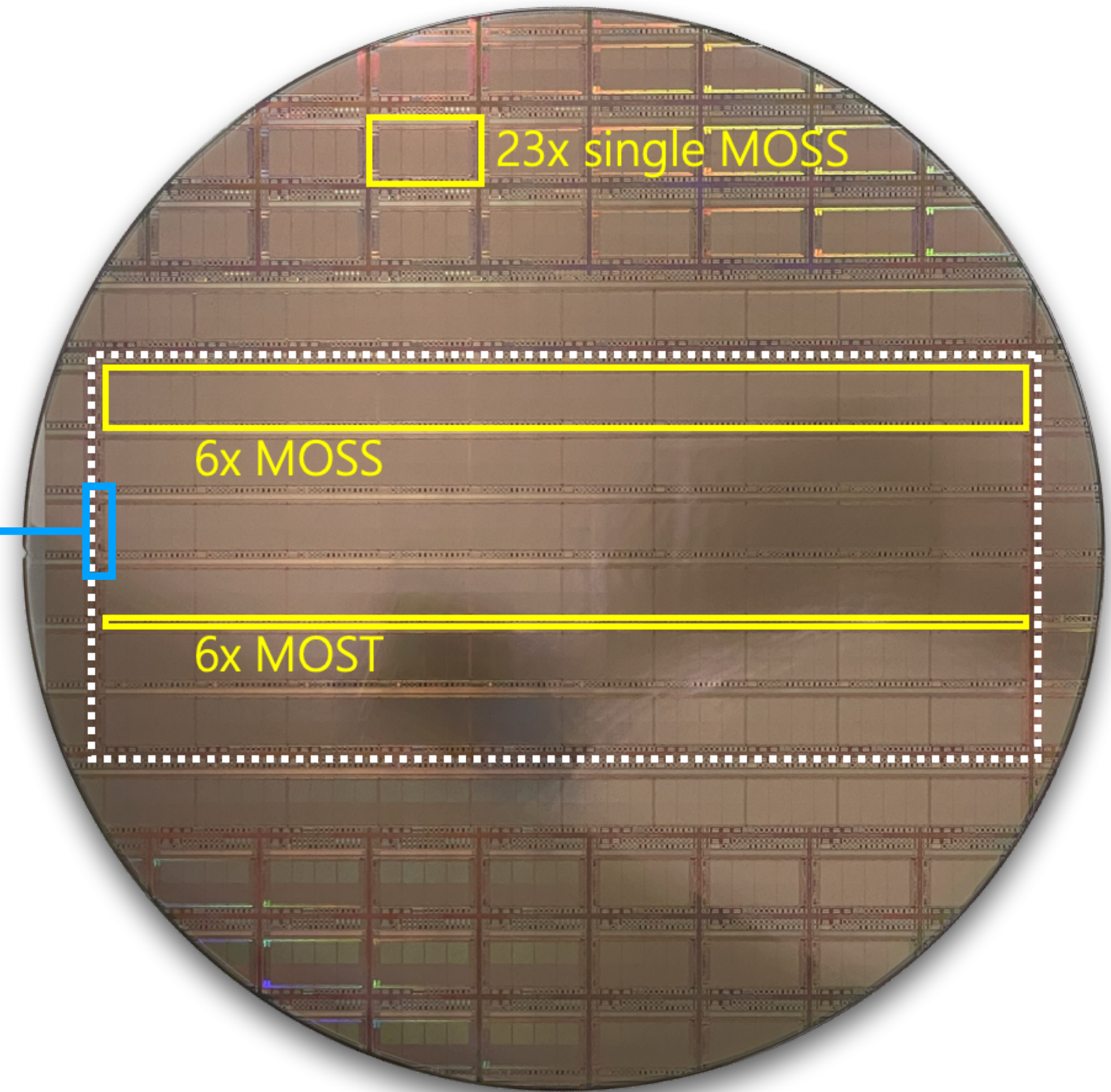


"What we designed"



Reticle (mask)

"What we want to fabricate"



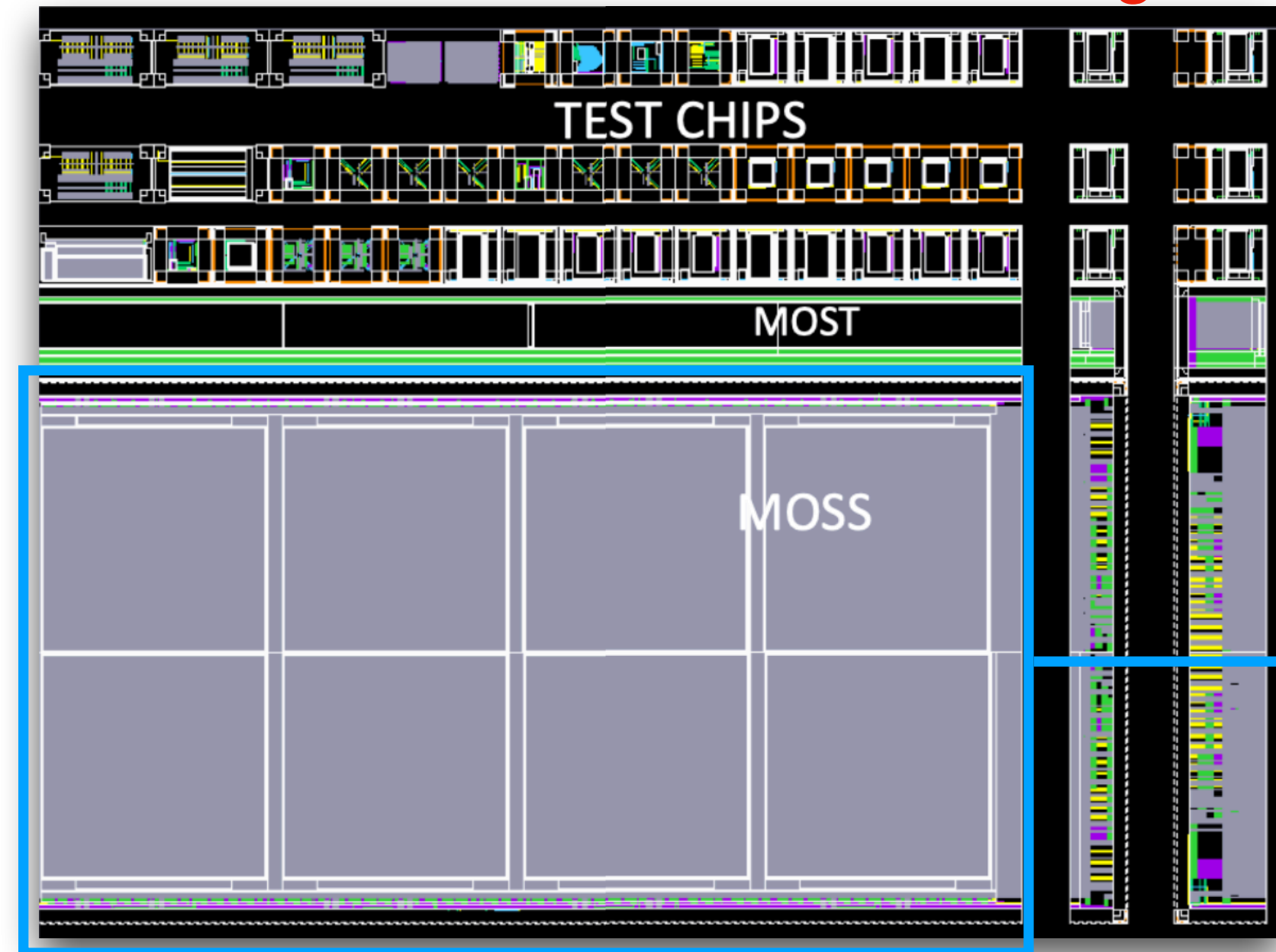
Wafer ($\phi=300\text{mm}$)

How can we make such a large sensor?

Stitching (simplified)

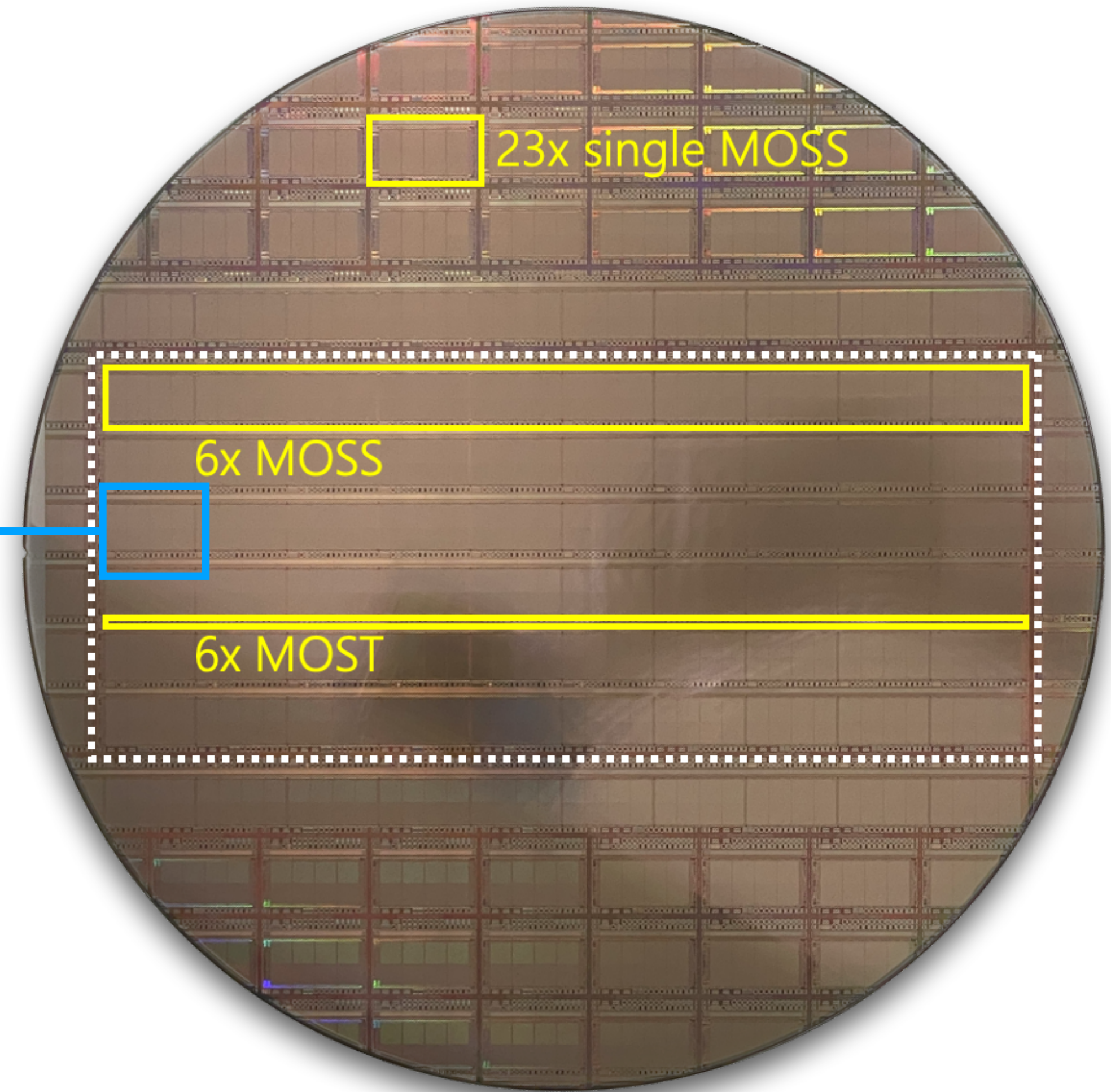


"What we designed"



Reticle (mask)

"What we want to fabricate"



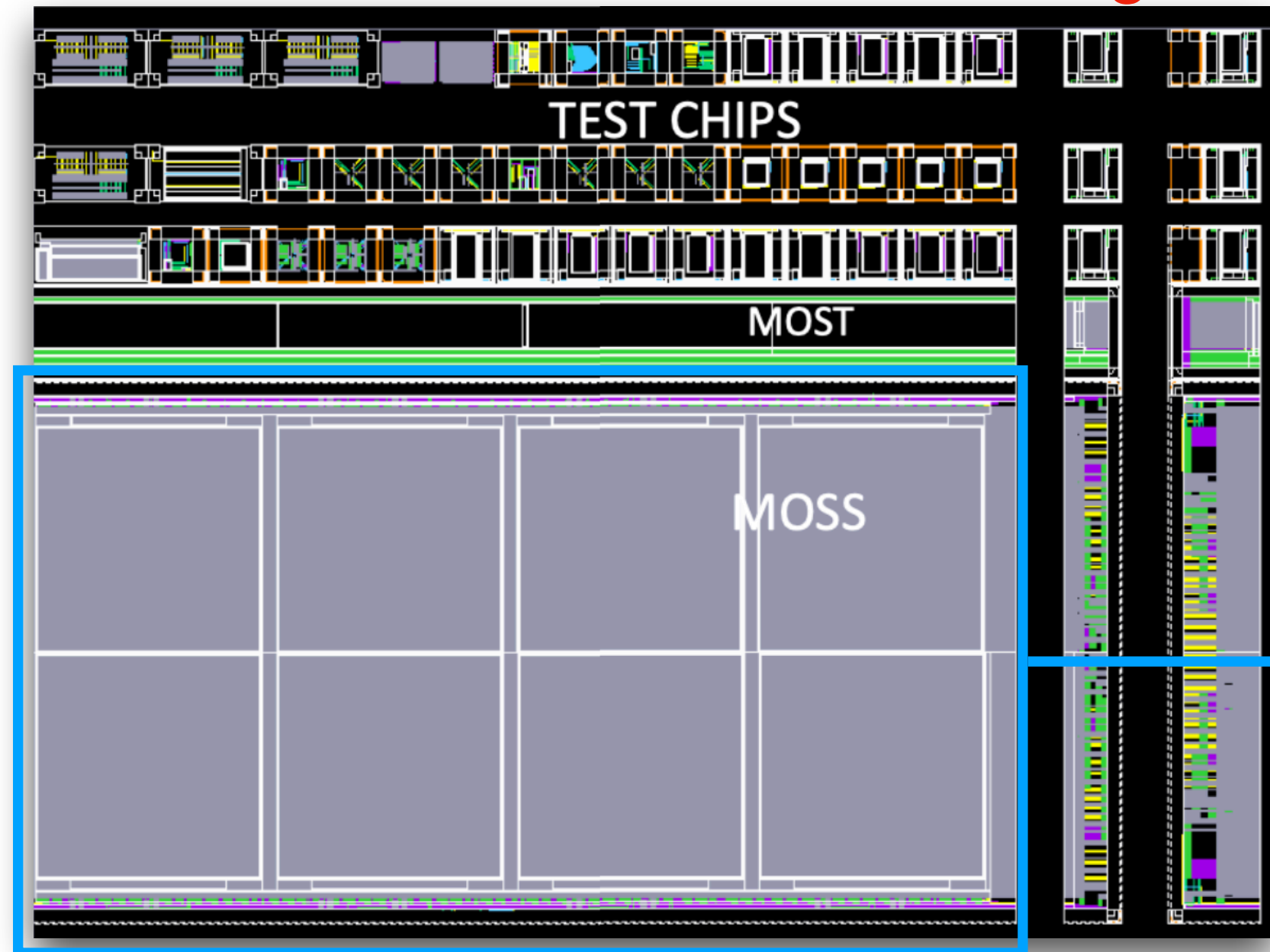
Wafer ($\phi=300\text{mm}$)

How can we make such a large sensor?

Stitching (simplified)

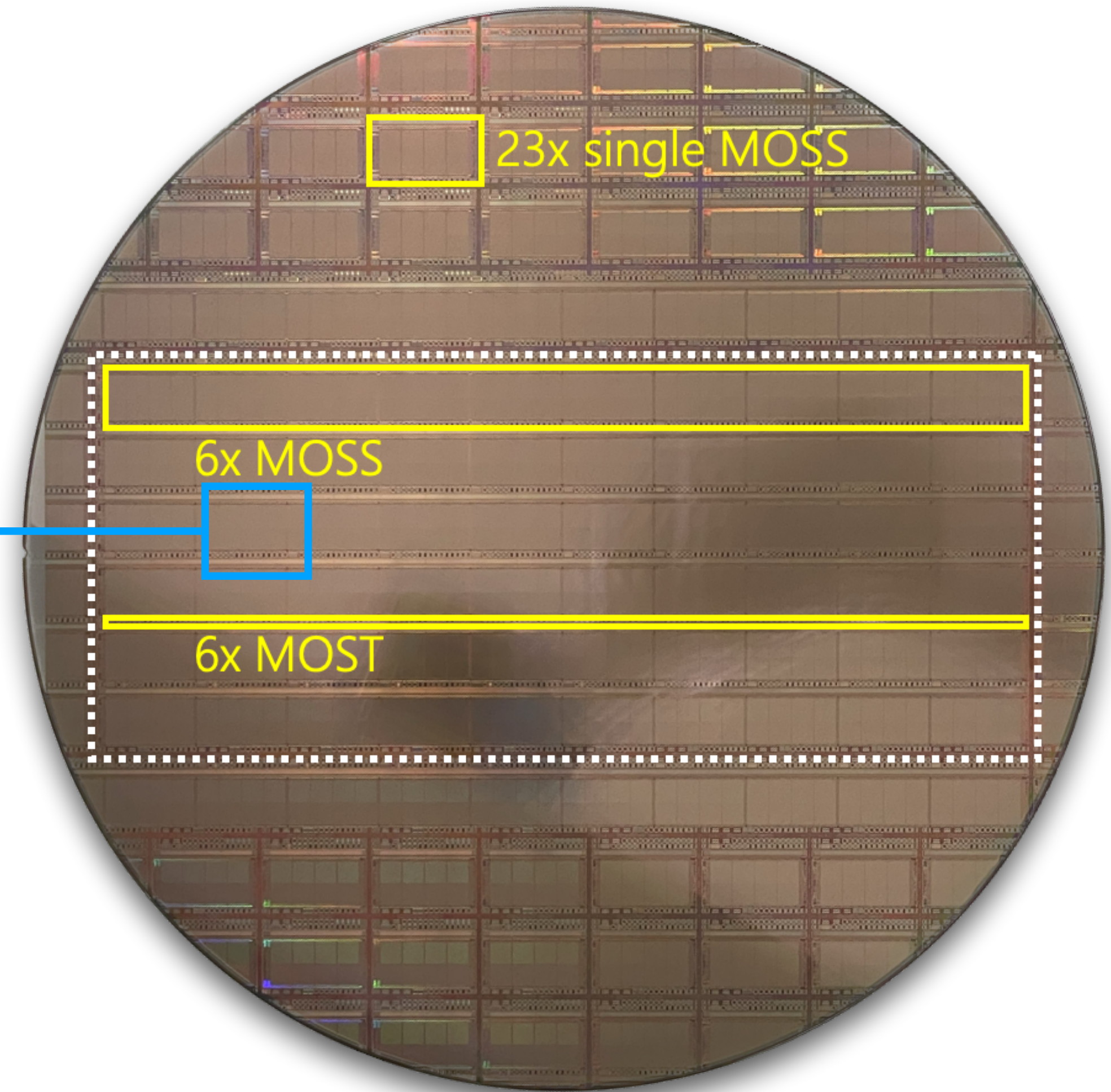


"What we designed"



Reticle (mask)

"What we want to fabricate"



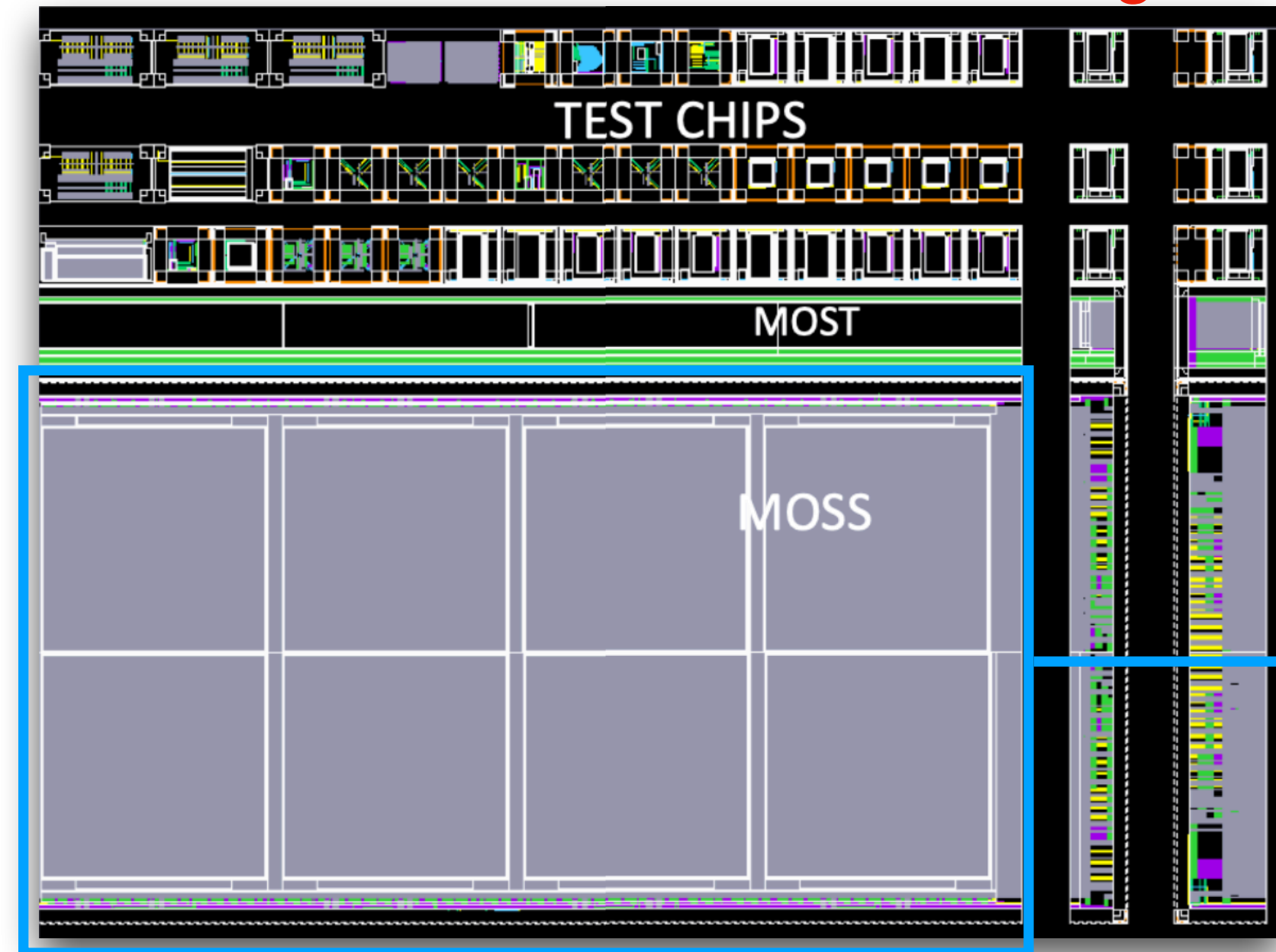
Wafer ($\phi=300\text{mm}$)

How can we make such a large sensor?

Stitching (simplified)

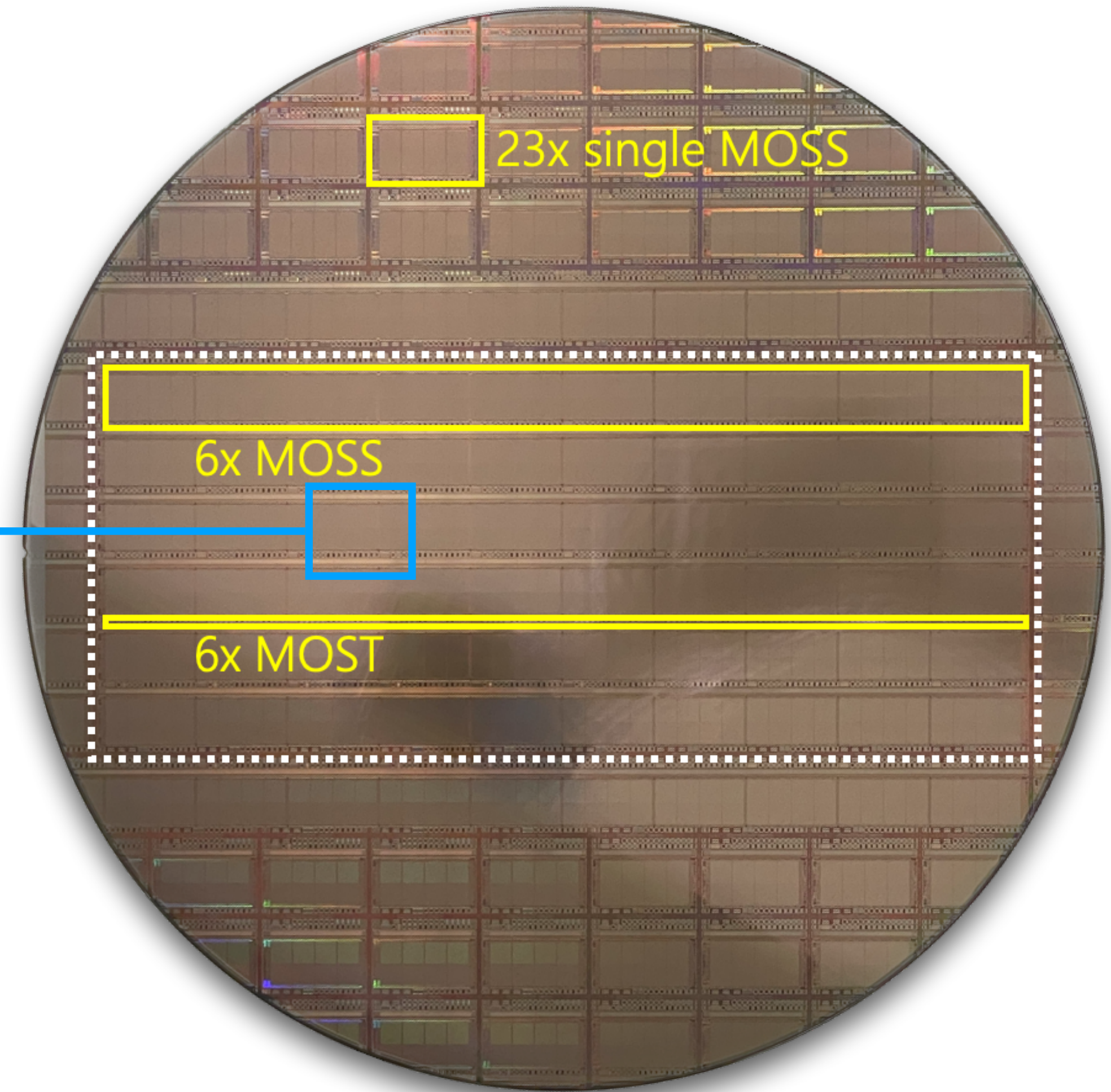


"What we designed"



Reticle (mask)

"What we want to fabricate"



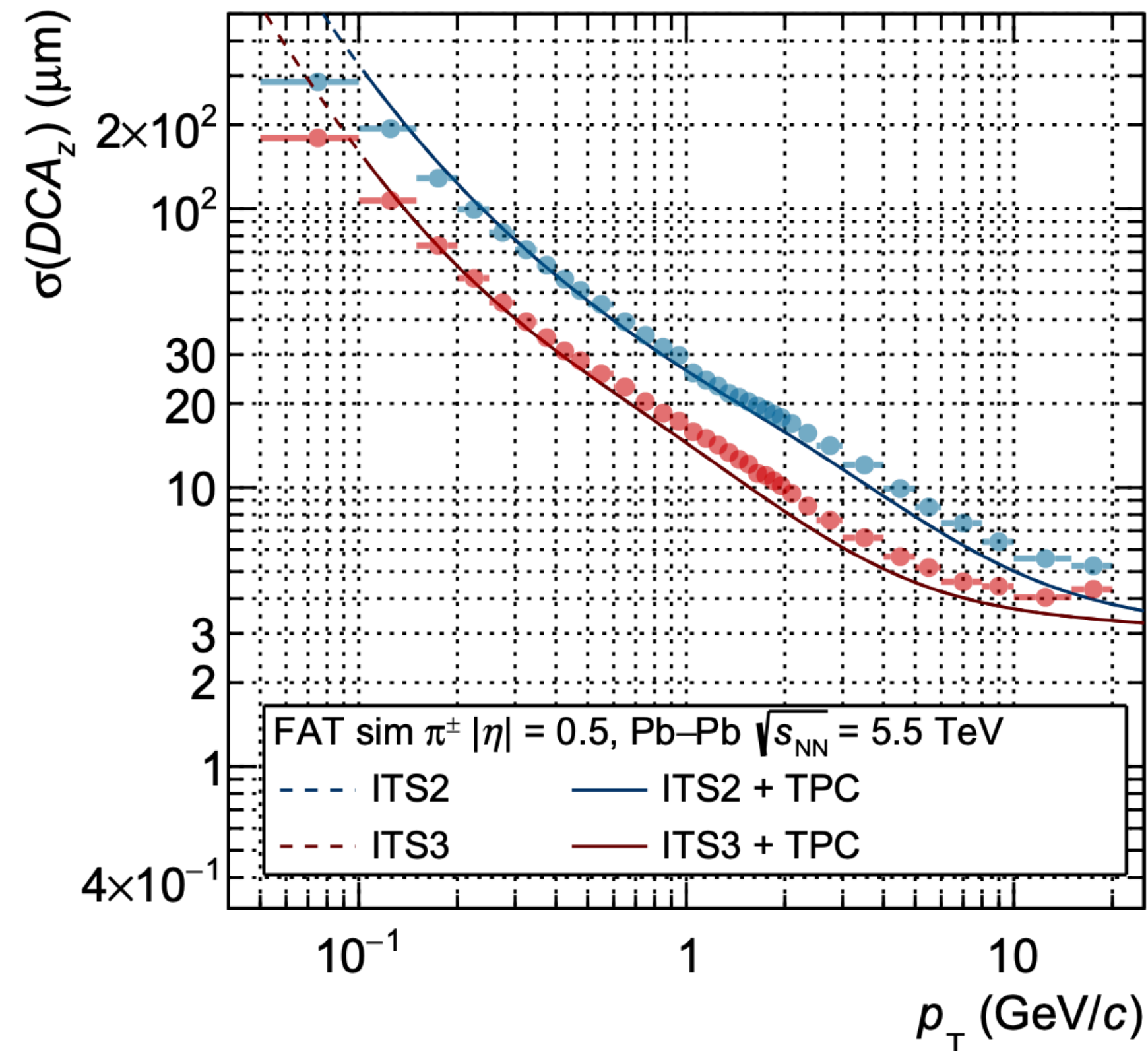
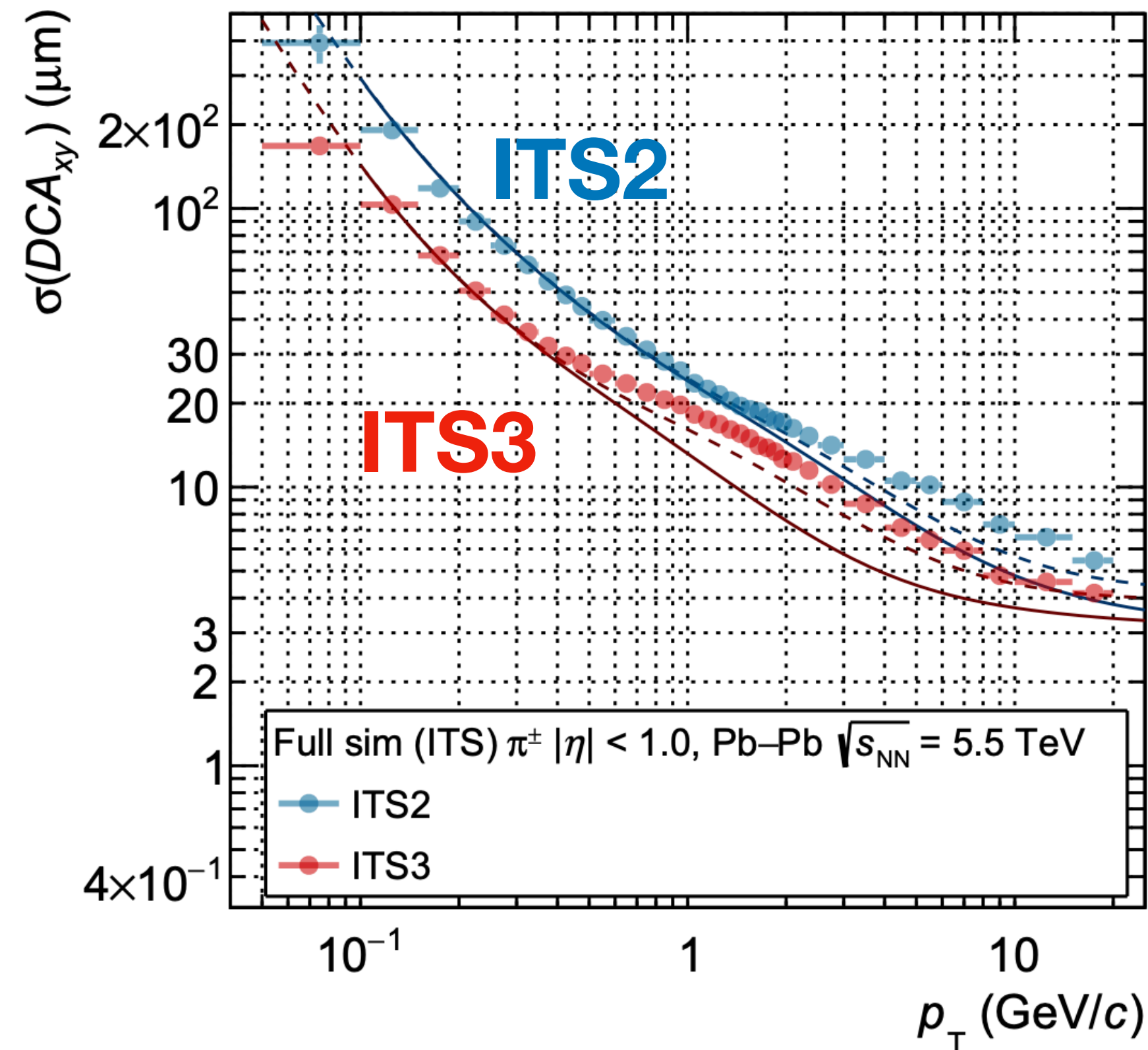
Wafer ($\phi=300\text{mm}$)

What we can get?

ITS3 performance improvements



ALICE, ALICE-TDR-021, 2024



- **2x improvement** in the pointing resolution (left: $r\phi$, right: z) of primary charged pion

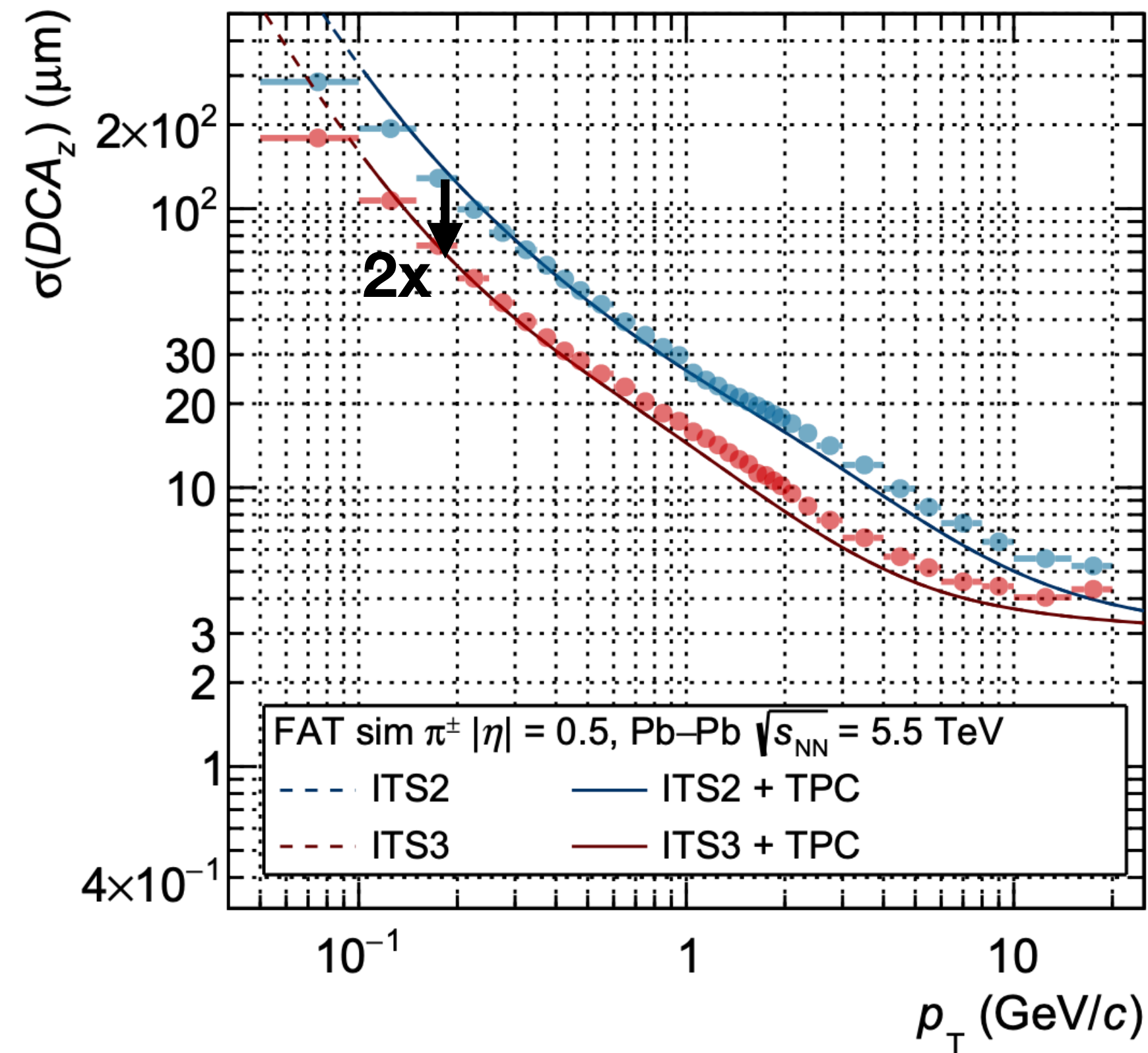
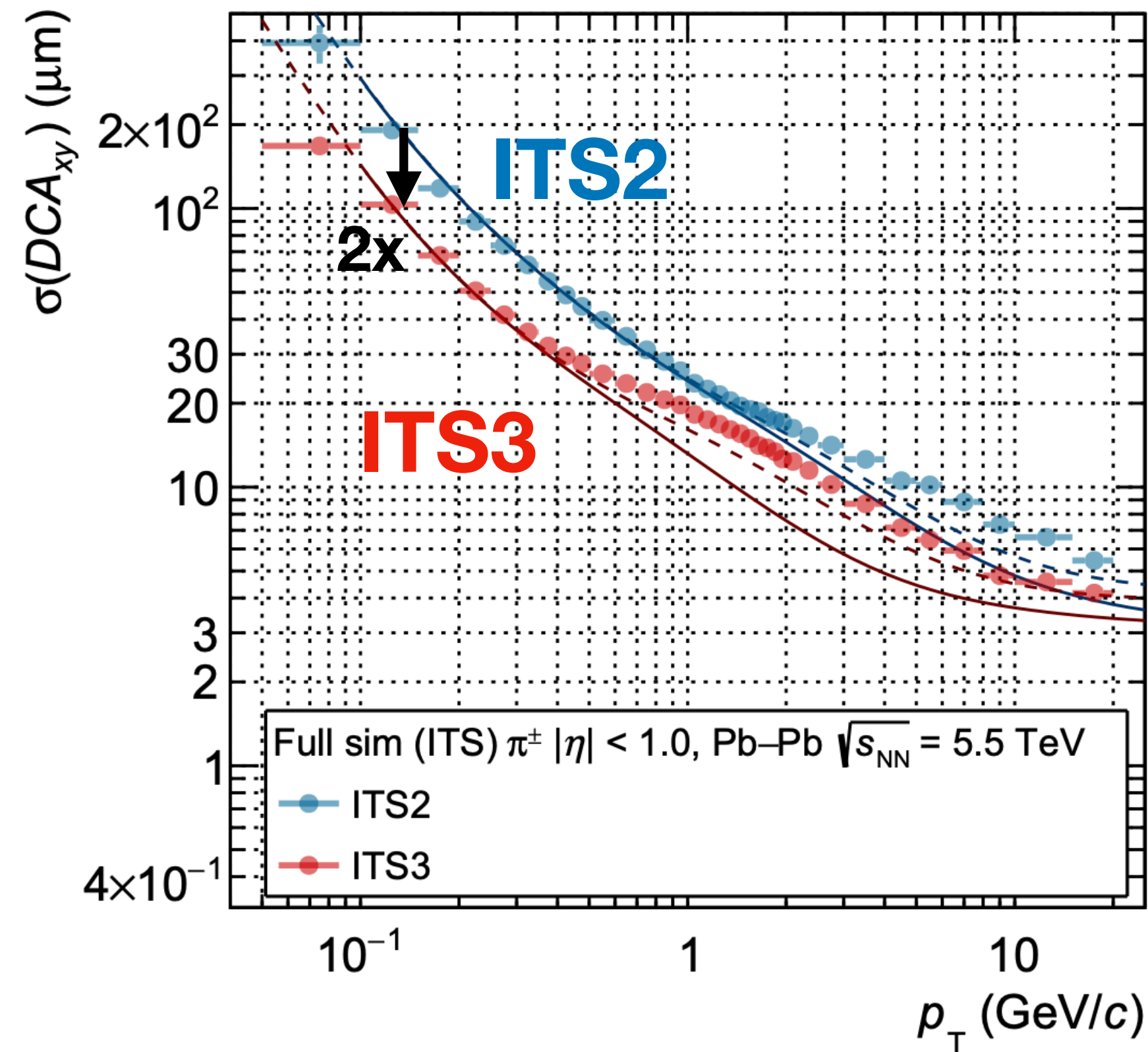
- Drastic reduction of material budget (0.35 \rightarrow 0.086% X_0 /layer)
- Being closer to the interaction point (24 \rightarrow 19 mm)
- Thinner and smaller beam pipe (700 \rightarrow 500 μm ; 18.2 \rightarrow 16.0 mm)

What we can get?

ITS3 performance improvements



ALICE, ALICE-TDR-021, 2024

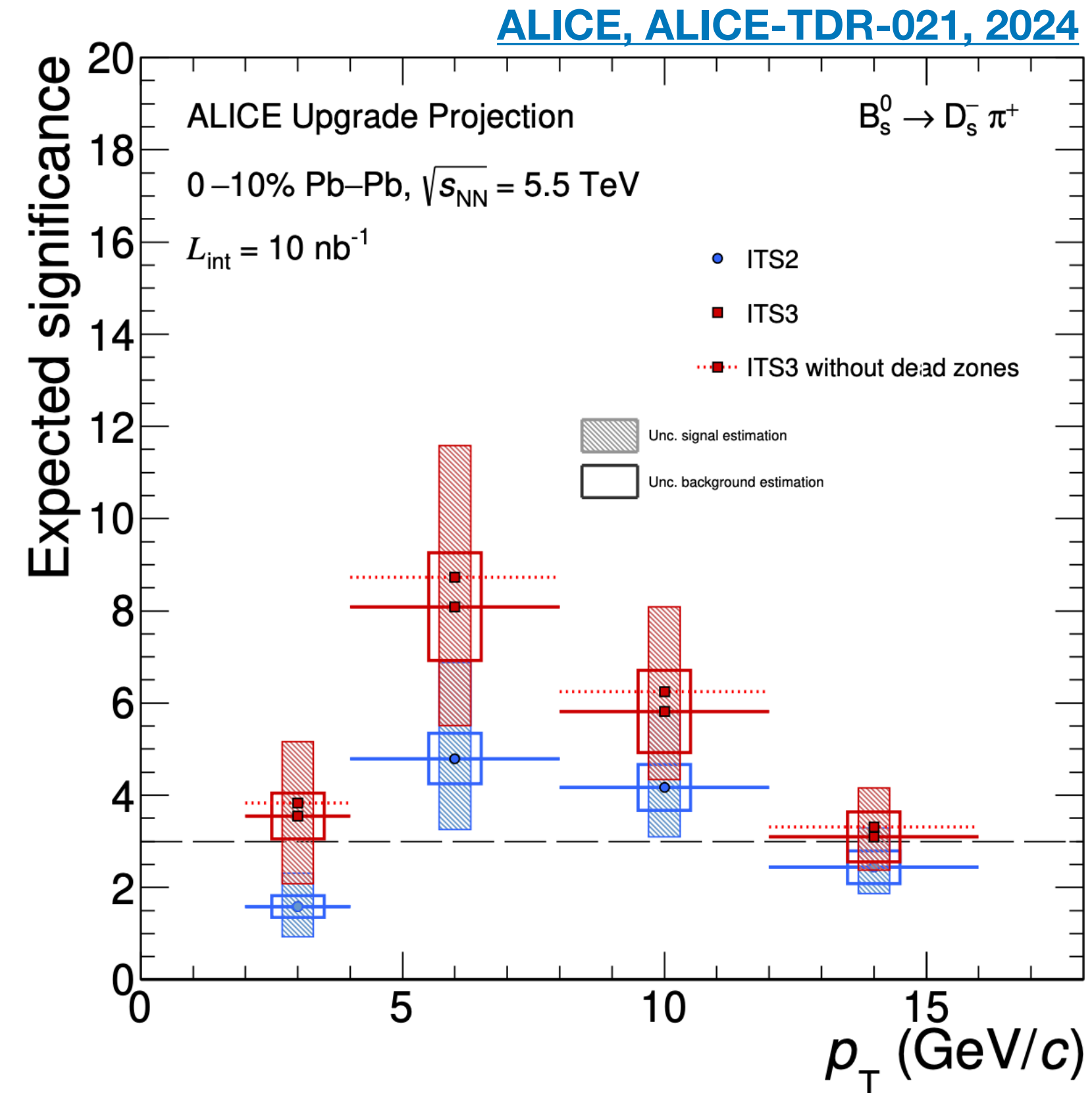
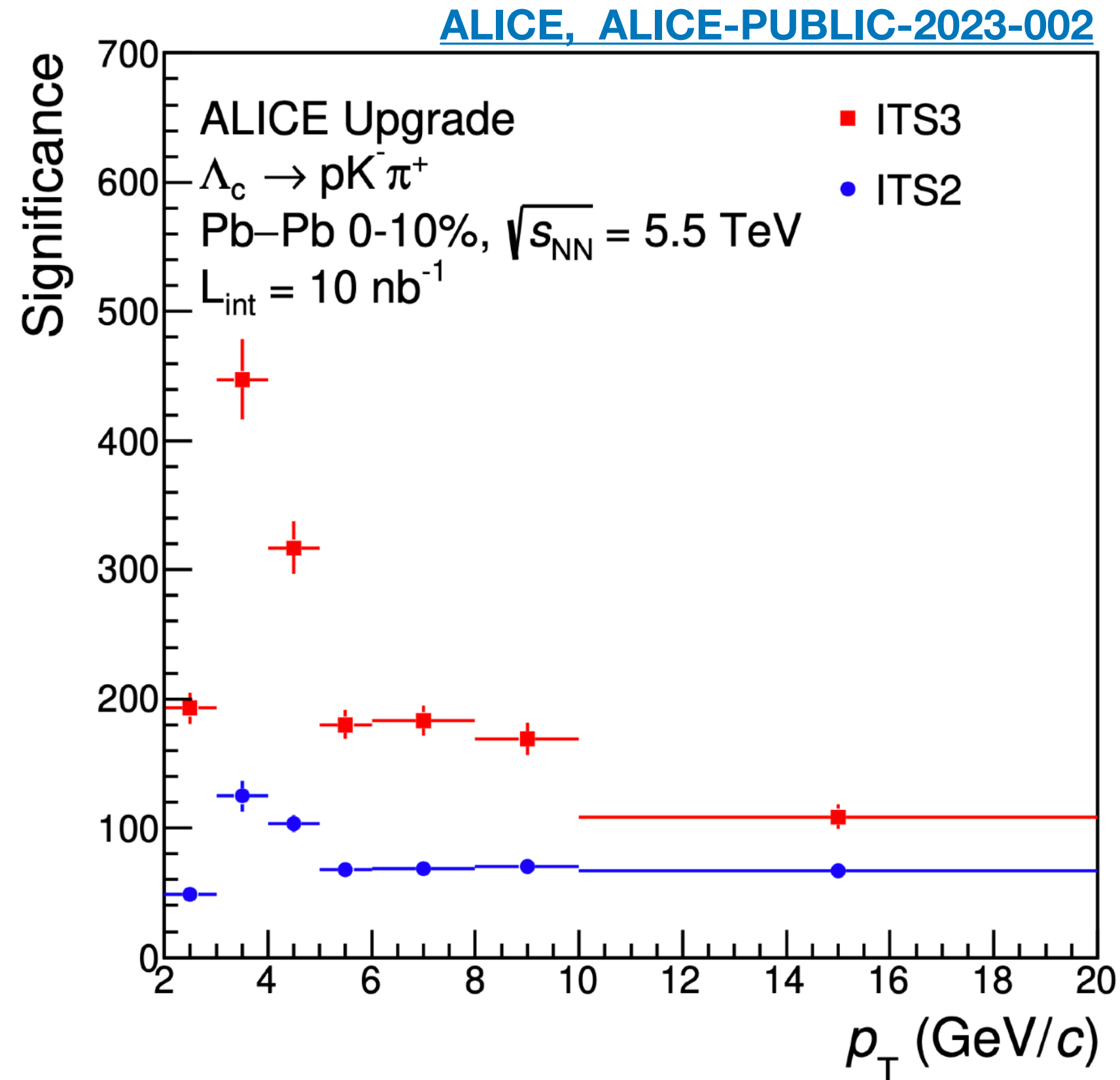


- **2x improvement** in the pointing resolution (left: $r\phi$, right: z) of primary charged pion

- Drastic reduction of material budget (0.35 \rightarrow 0.086% X_0 /layer)
- Being closer to the interaction point (24 \rightarrow 19 mm)
- Thinner and smaller beam pipe (700 \rightarrow 500 μm ; 18.2 \rightarrow 16.0 mm)

What we can get?

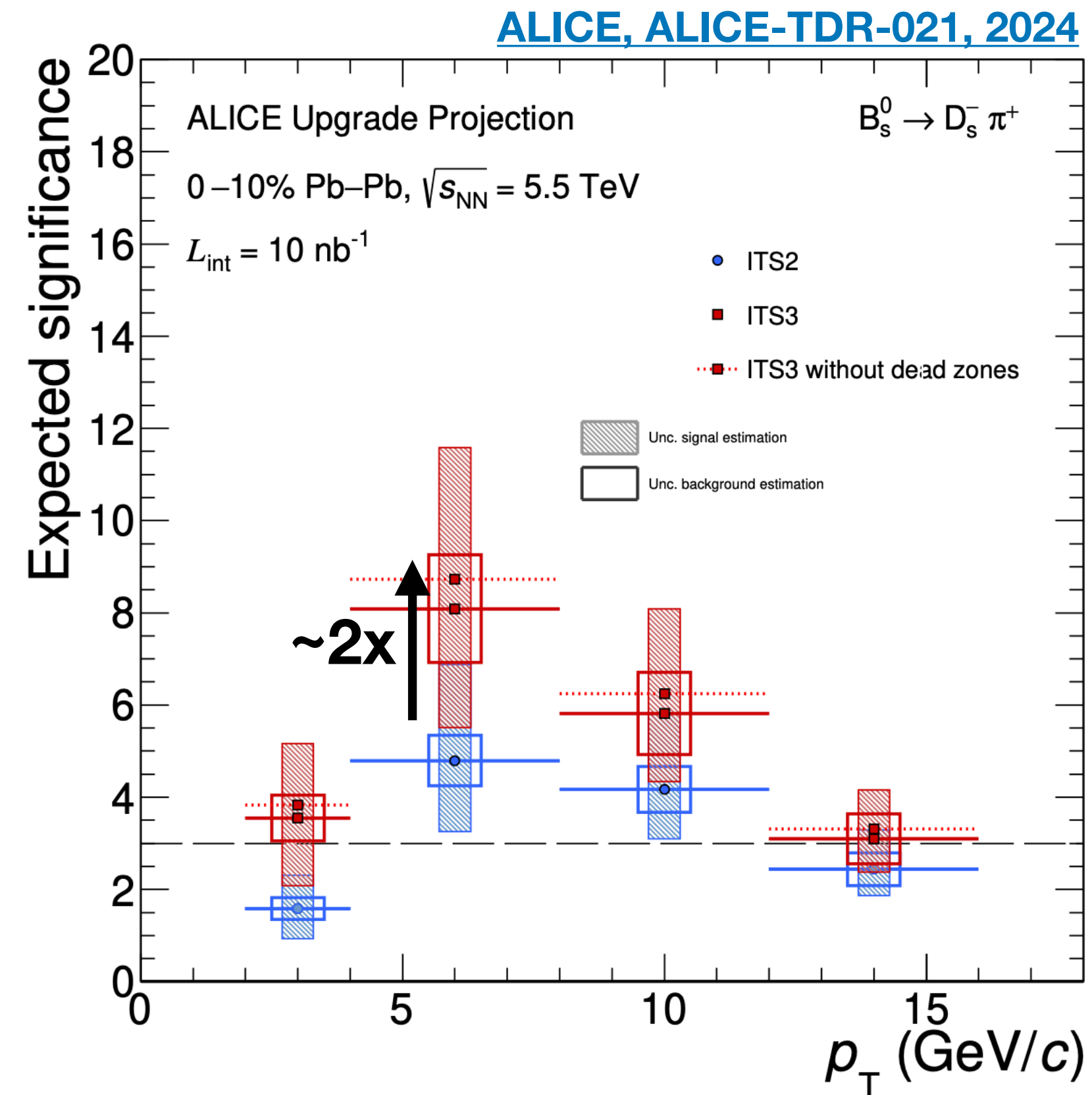
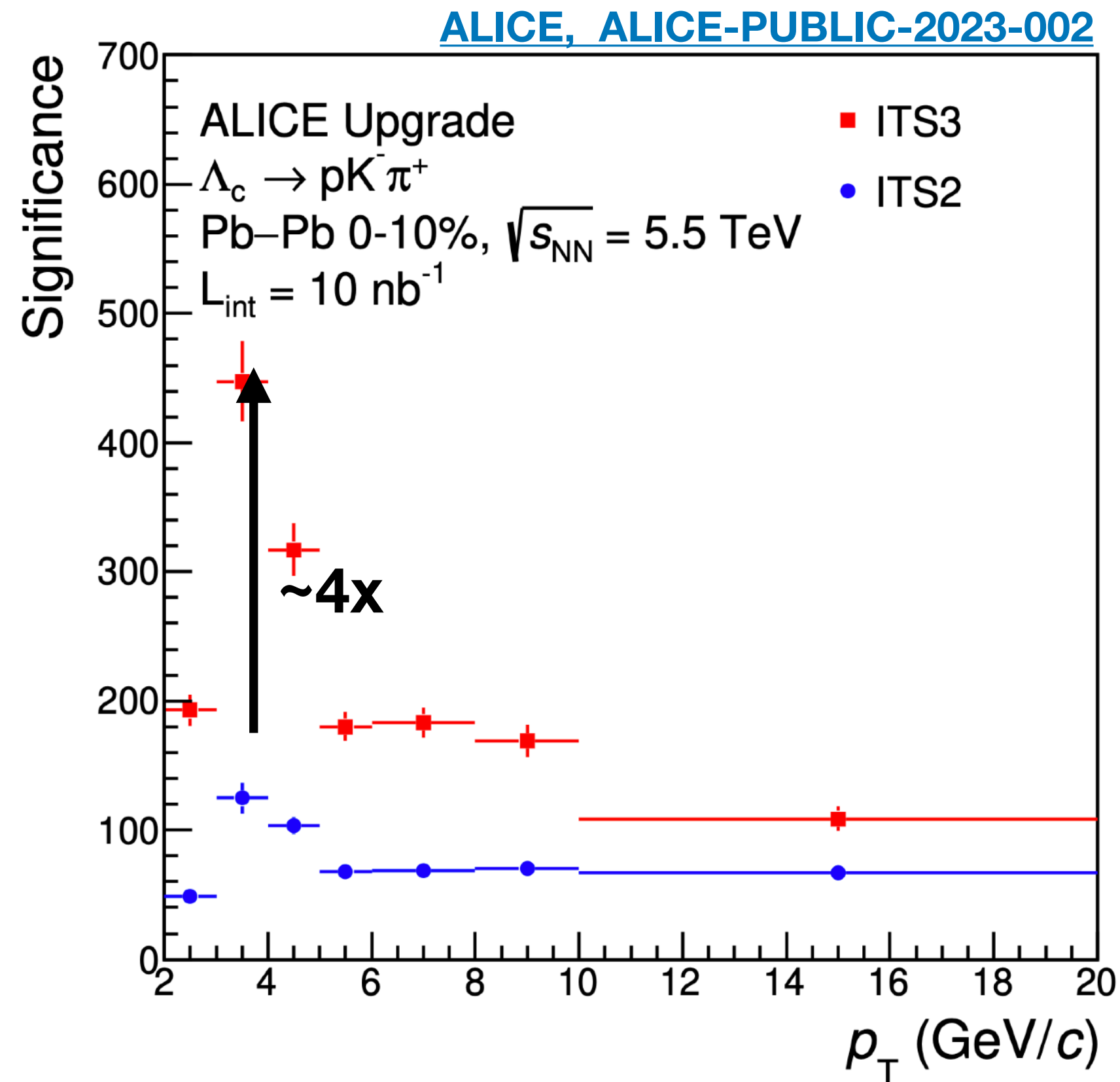
Measurements benefitting from ITS3



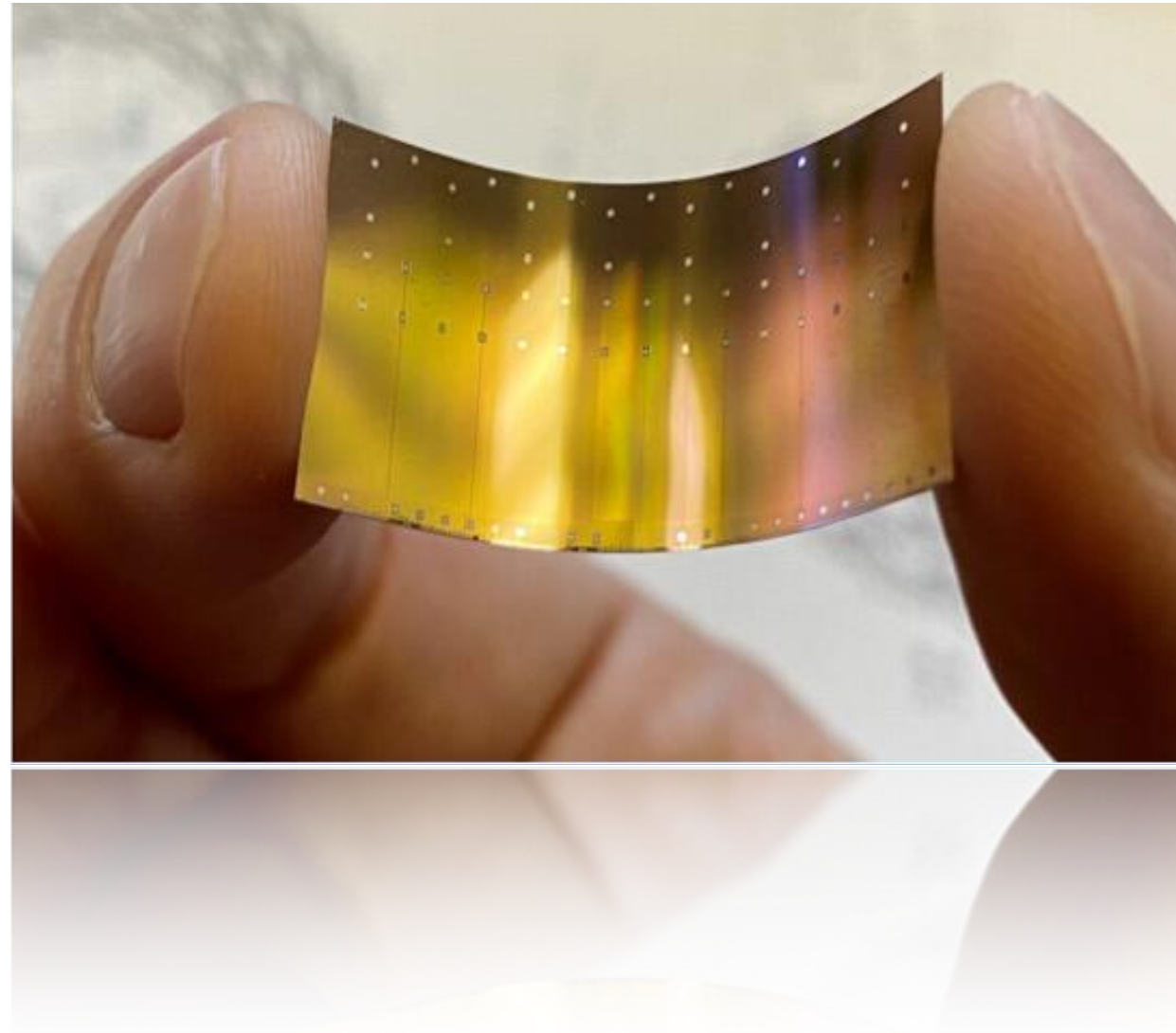
- Directly boosts the **ALICE core physics program** that is largely based on:
 - Low momenta
 - Secondary vertex reconstruction

What we can get?

Measurements benefitting from ITS3

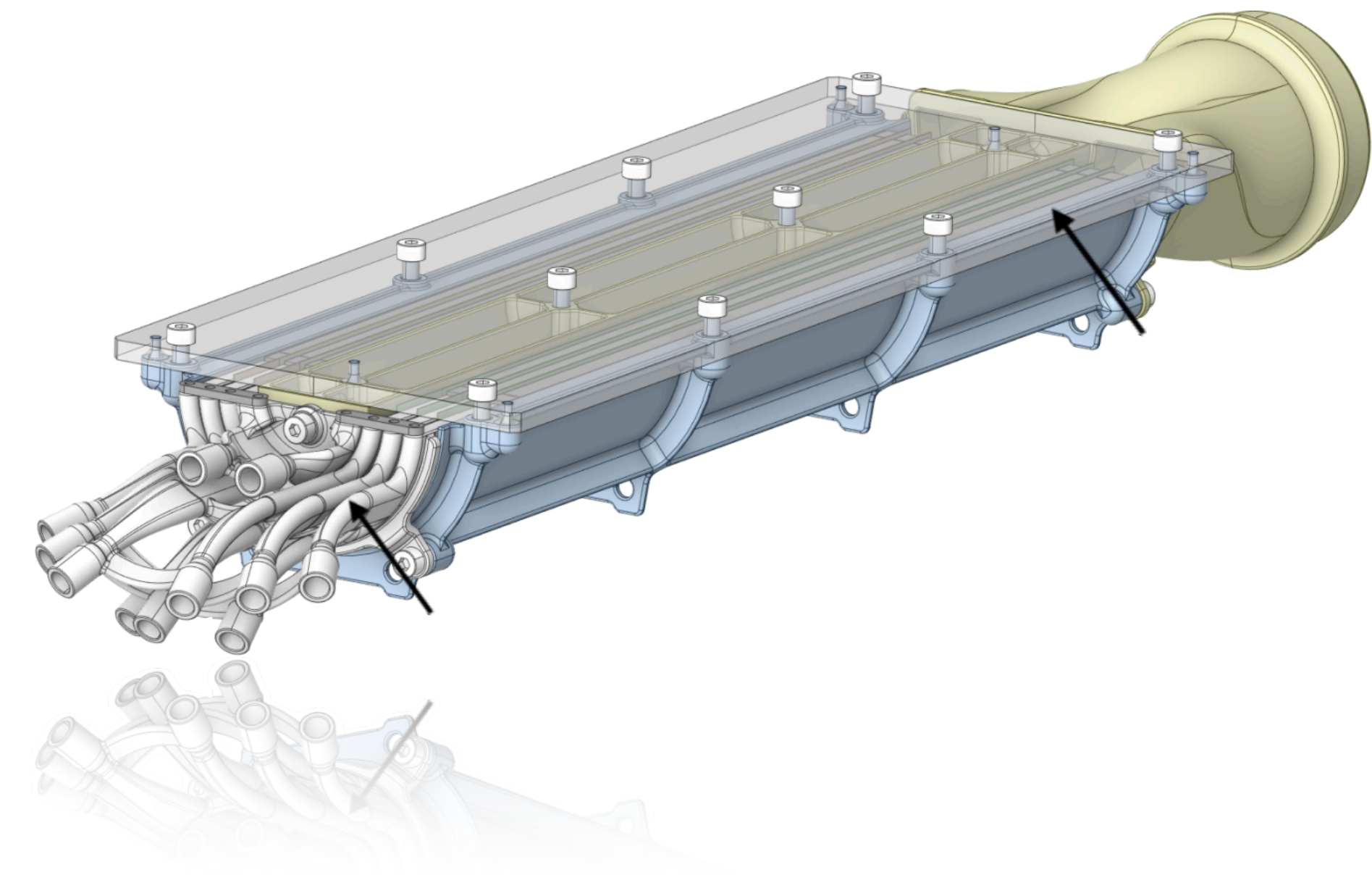


- Directly boosts the **ALICE core physics program** that is largely based on:
 - Low momenta
 - Secondary vertex reconstruction



ITS3 design and R&D Activities

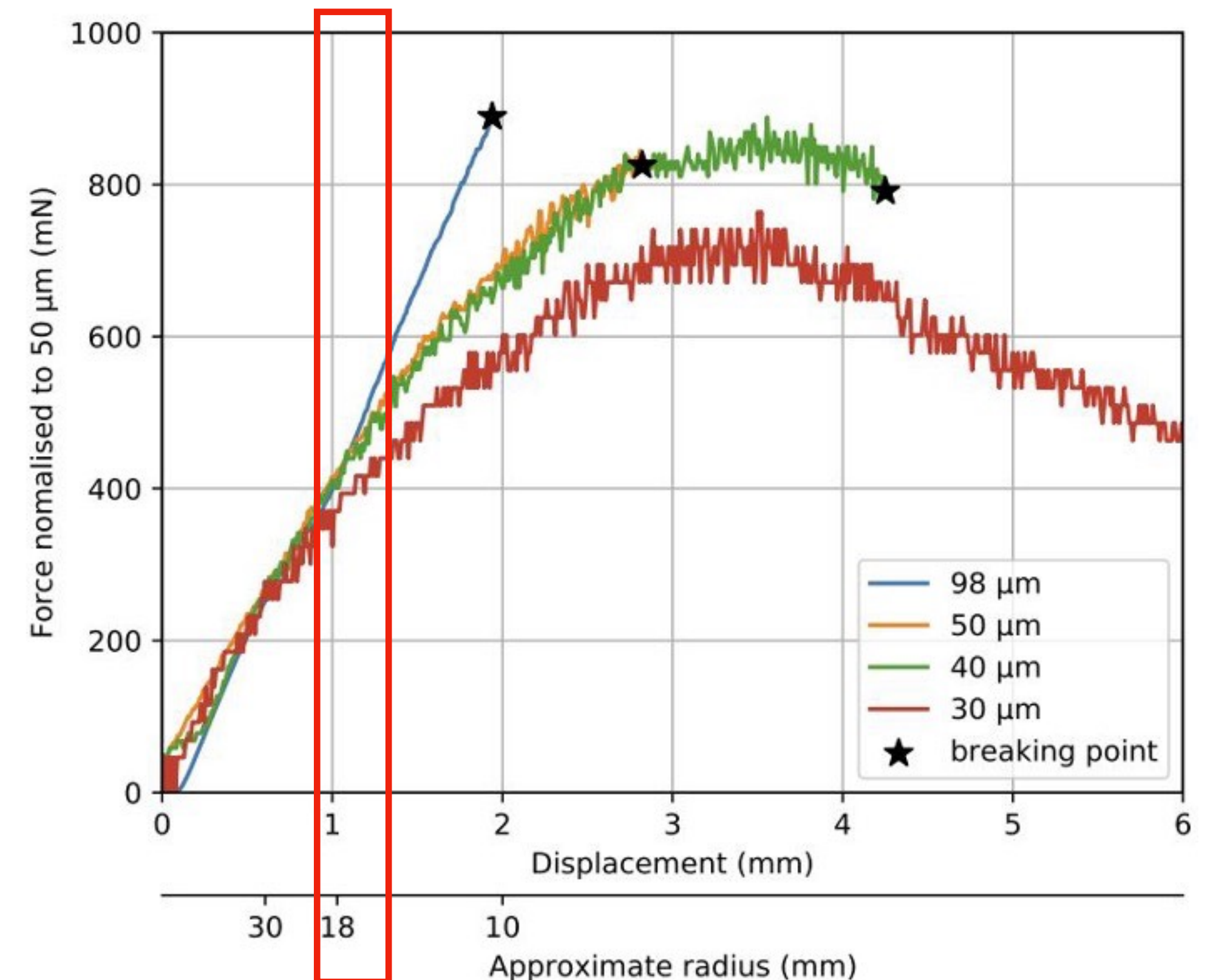
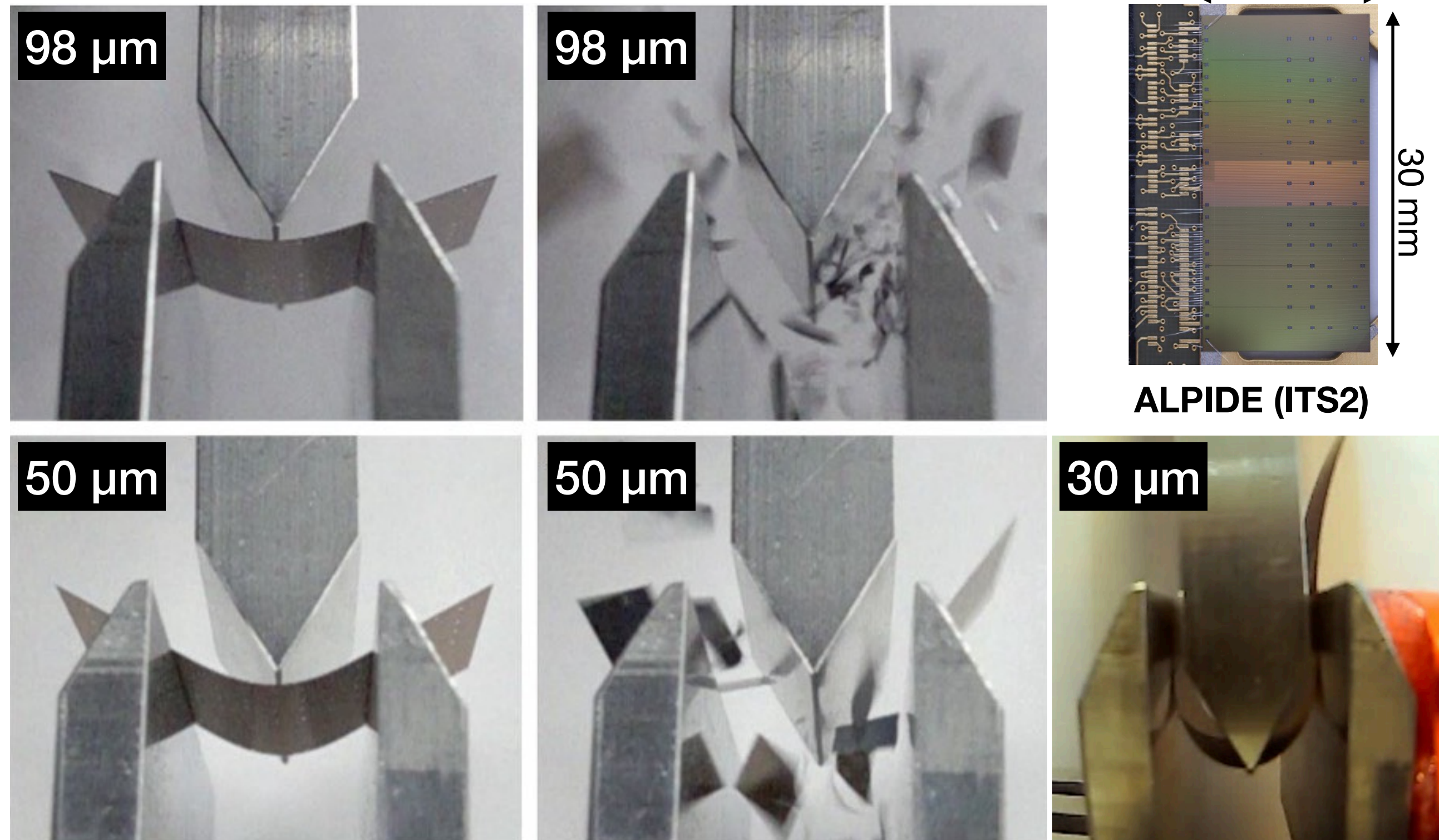
- Can we **bend it**?
- Can we **cool it down**?
- Can it **withstand vibration from cooling**?
- Can we use **65 nm technology**?
- Can we **do the stitching**?



ITS design and R&D

Flexibility of silicon

- Monolithic Active Pixel Sensors are quite flexible
- Bending force scales as (thickness)⁻³
 - Large benefit from thinner sensors

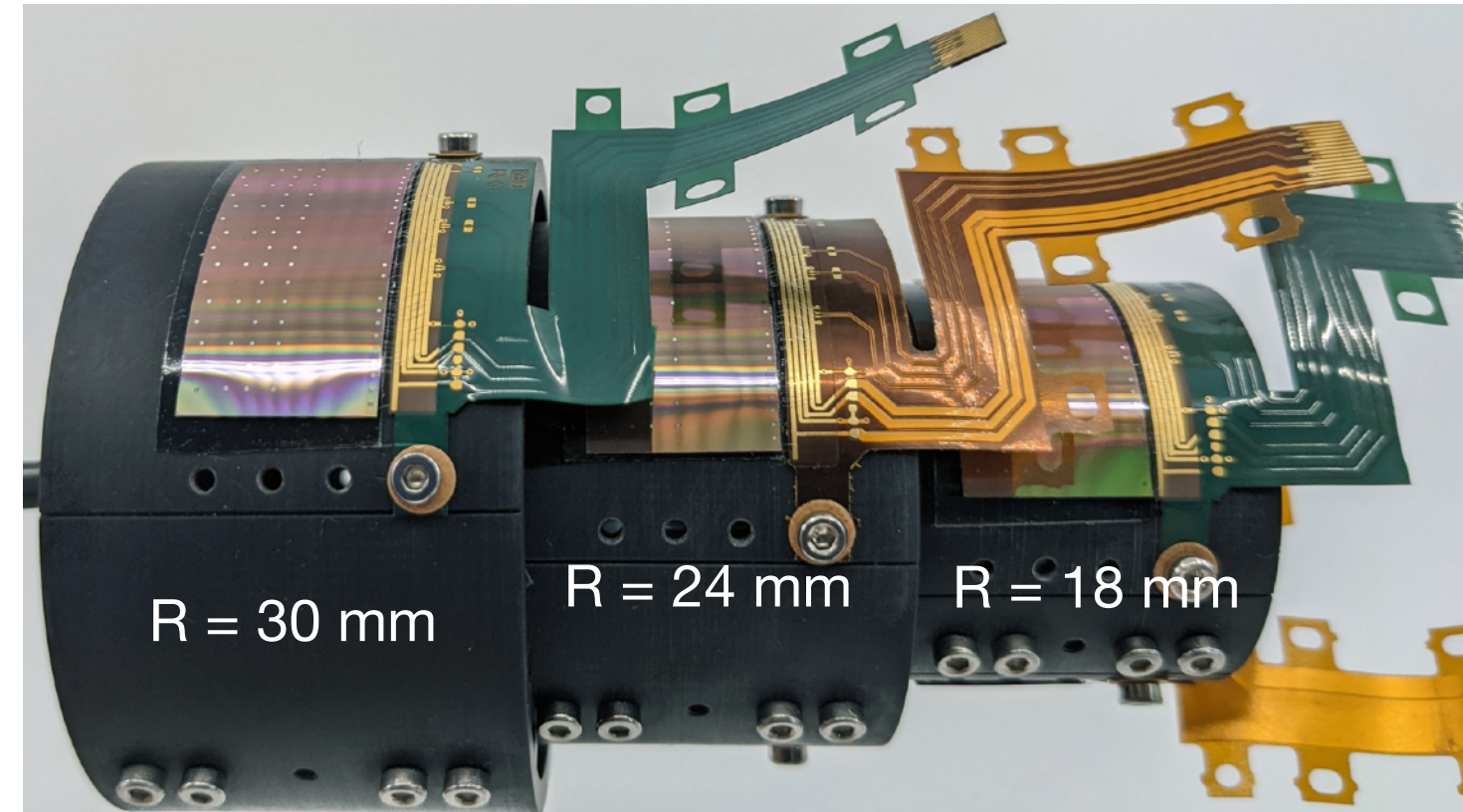
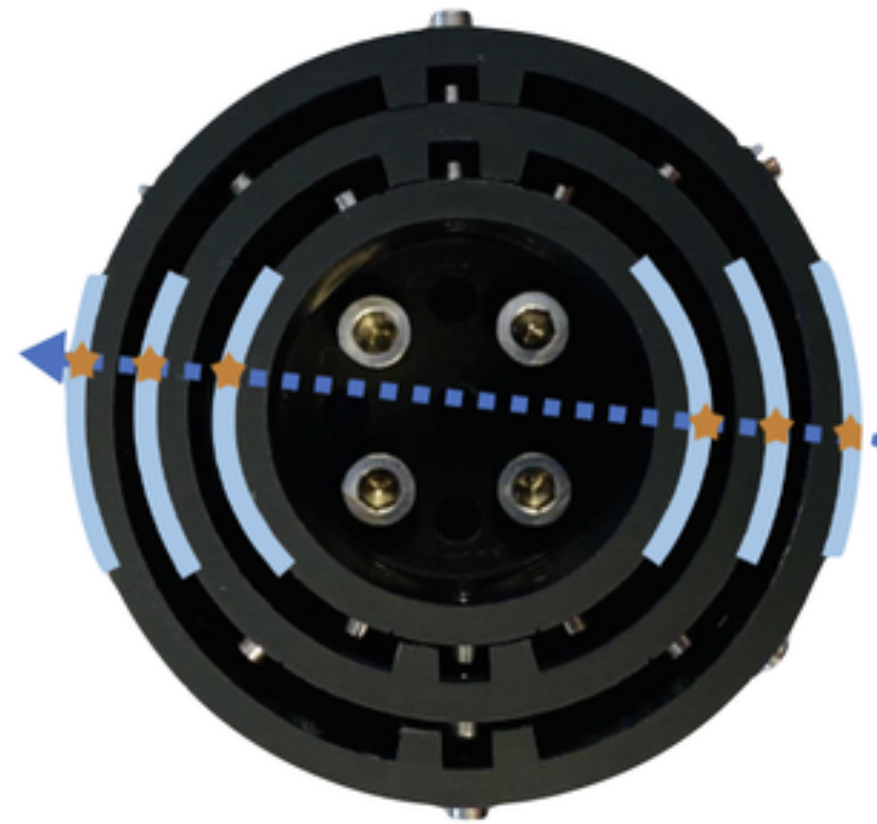


ITS3 innermost layer radius

- Bending test with ITS2 sensor:
Target radii (19 mm) easily achievable

ITS design and R&D

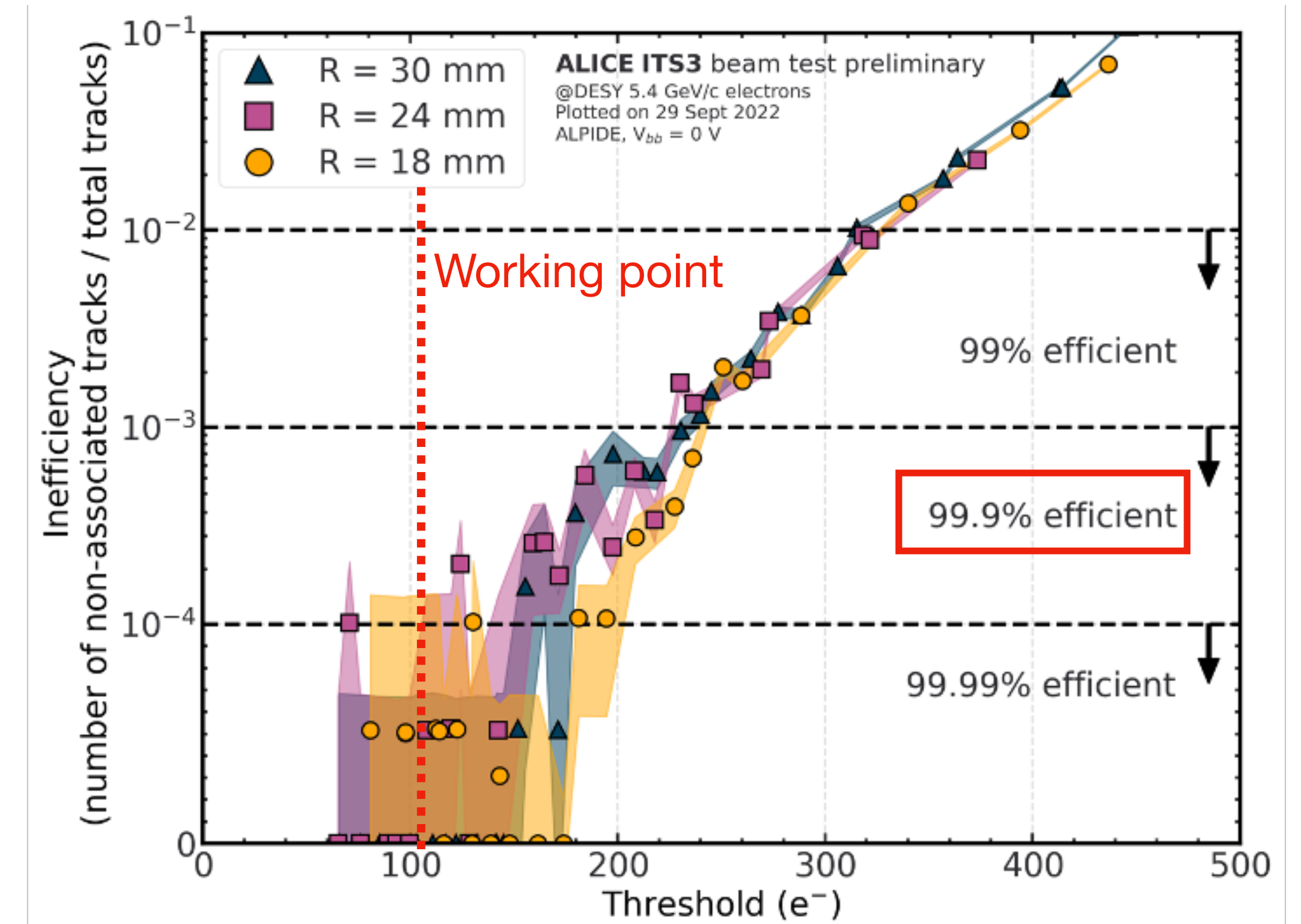
Bending ALPIDEs (ITS2) performance



[ALICE, NIM.A 1028 \(2022\) 166280](#)

μITS3

- "μITS3": 6 ALPIDEs (180 nm) bent to ITS3 target radii
- No degradation of detection efficiency observed
- Results validated on bent 65 nm pixel test structures
- Electrical interconnections to FPC after bending through wire bonding tested



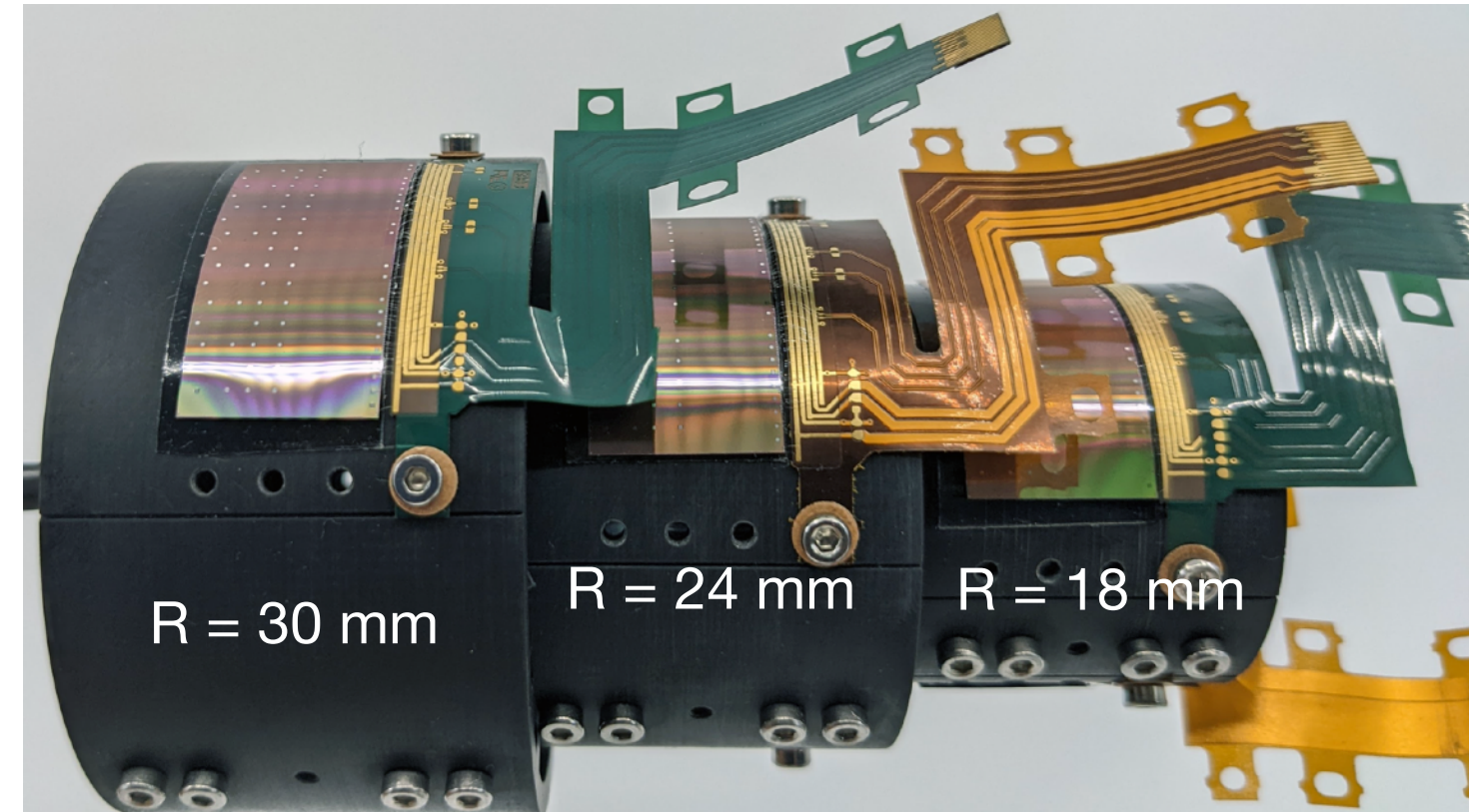
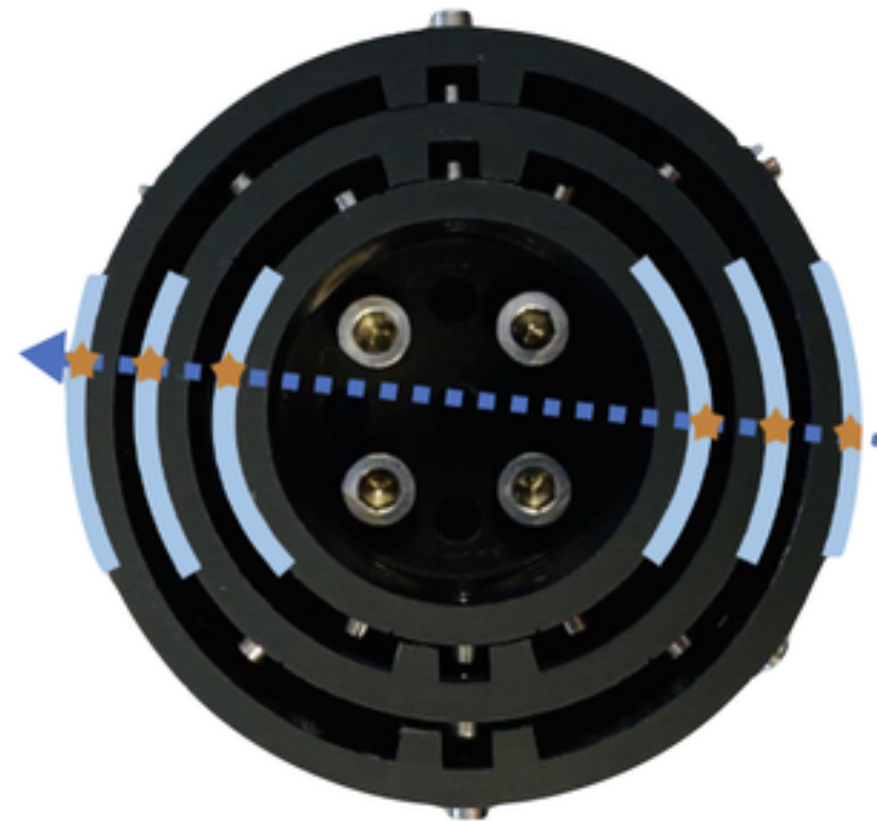
Inefficiency test results



65 nm sensor with FPC

ITS design and R&D

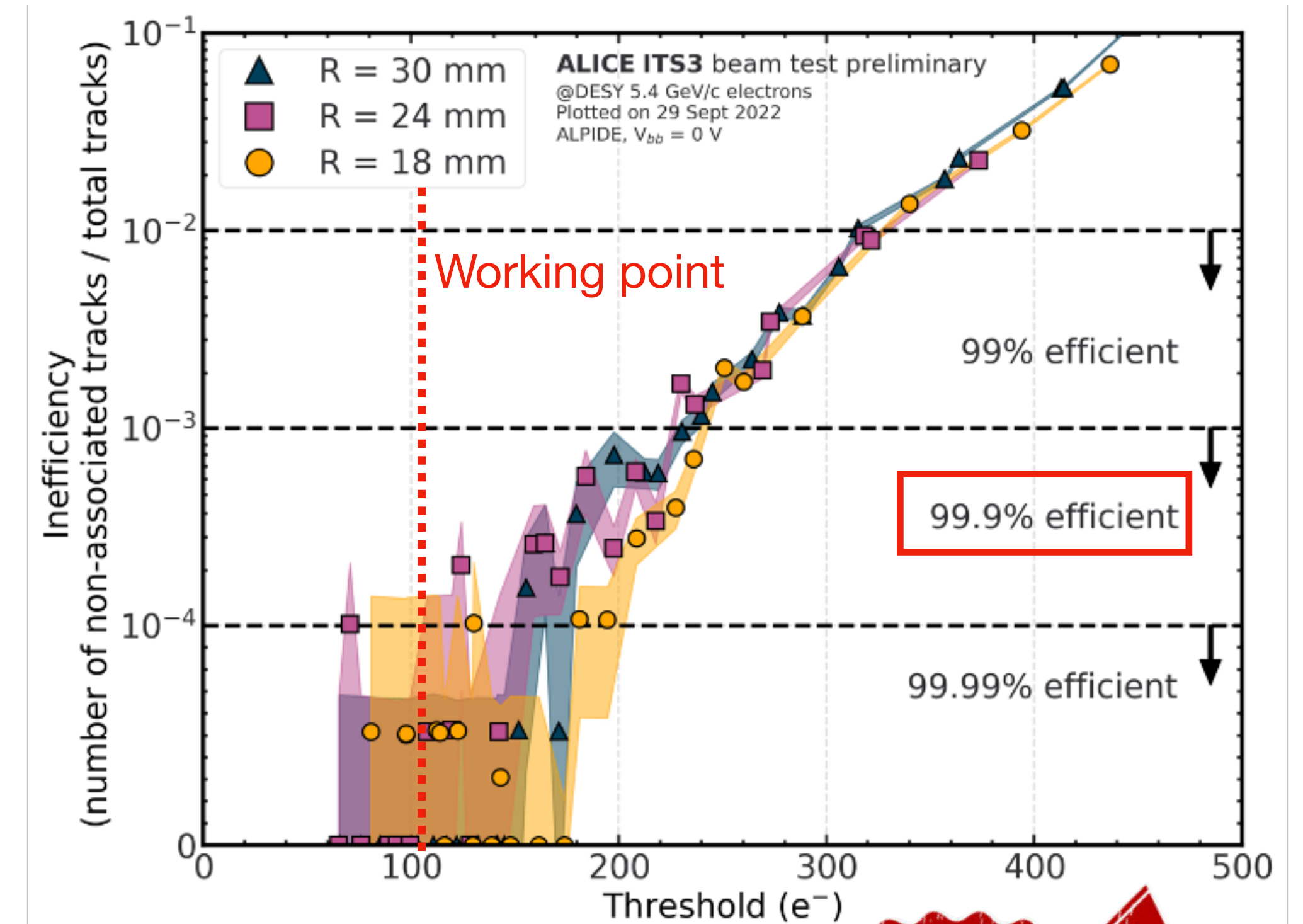
Bending ALPIDEs (ITS2) performance



[ALICE, NIM.A 1028 \(2022\) 166280](#)

μ ITS3

- " μ ITS3": 6 ALPIDEs (180 nm) bent to ITS3 target radii
- No degradation of detection efficiency observed
- Results validated on bent 65 nm pixel test structures
- Electrical interconnections to FPC after bending through wire bonding tested



Inefficiency test



We can make the bent detector !

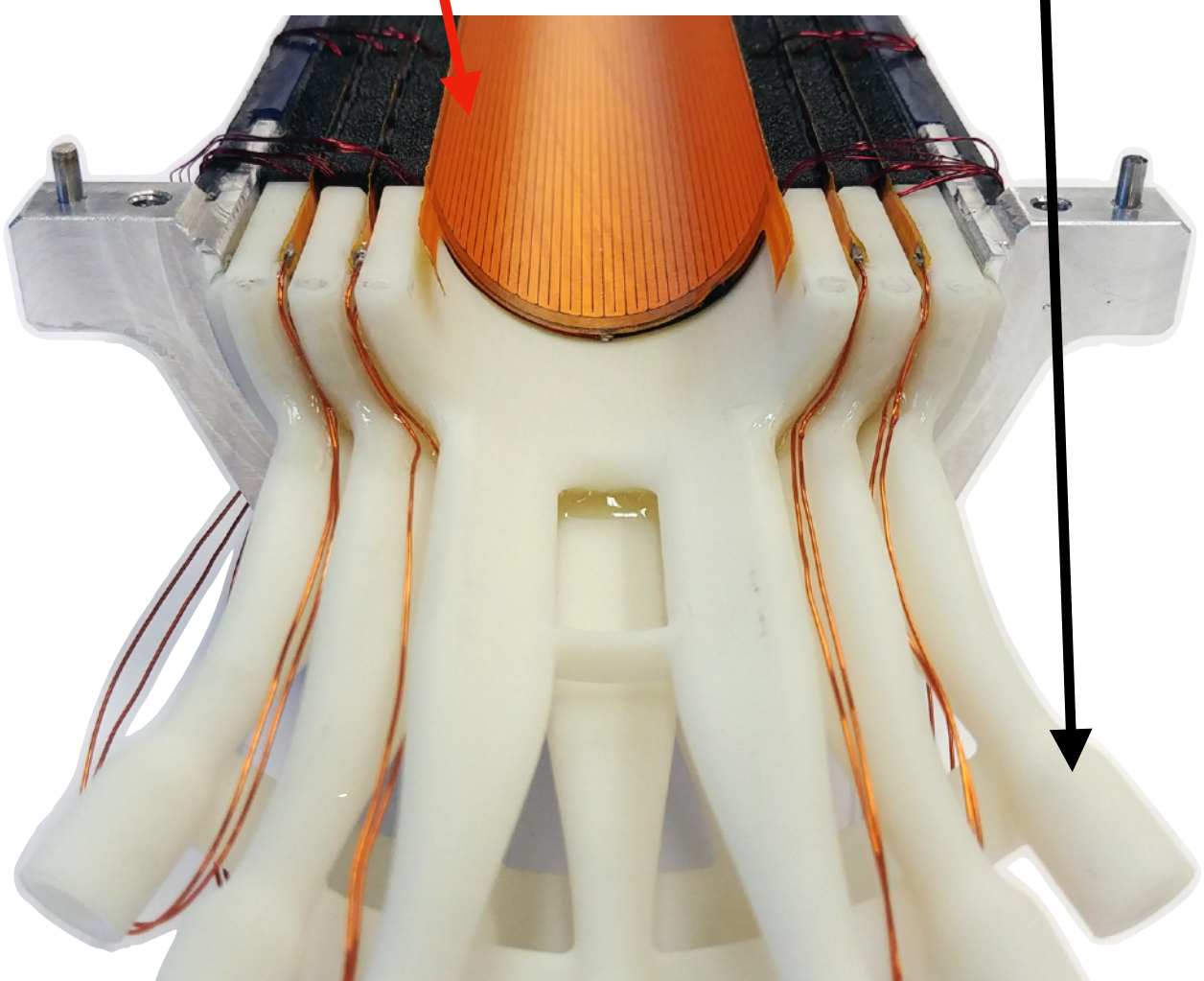
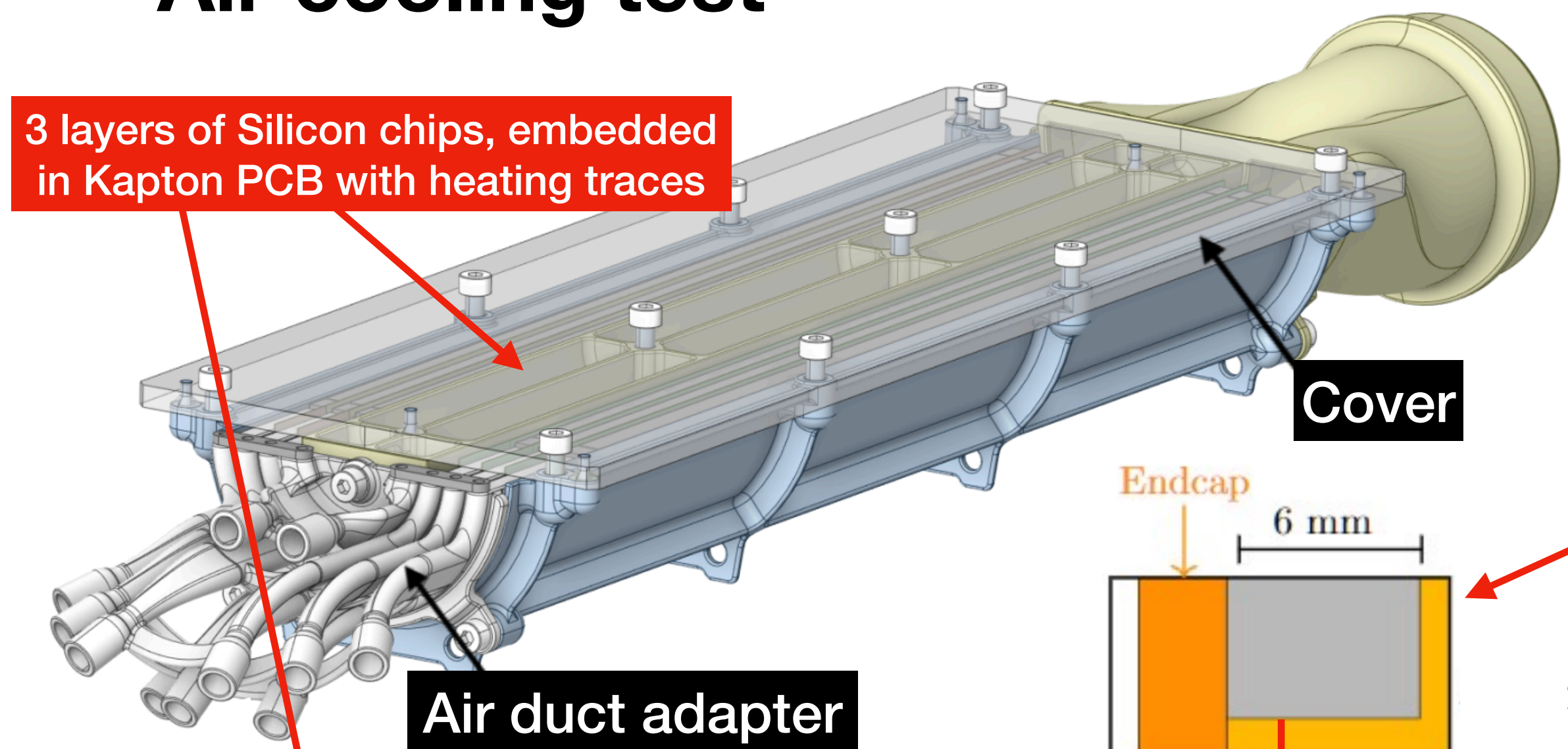
ITS design and R&D

Air cooling test

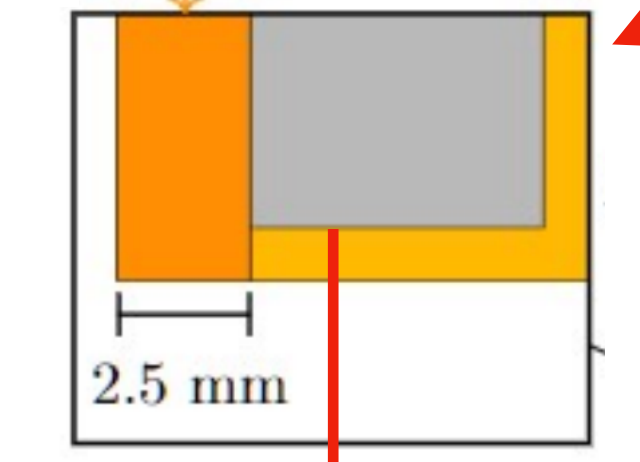
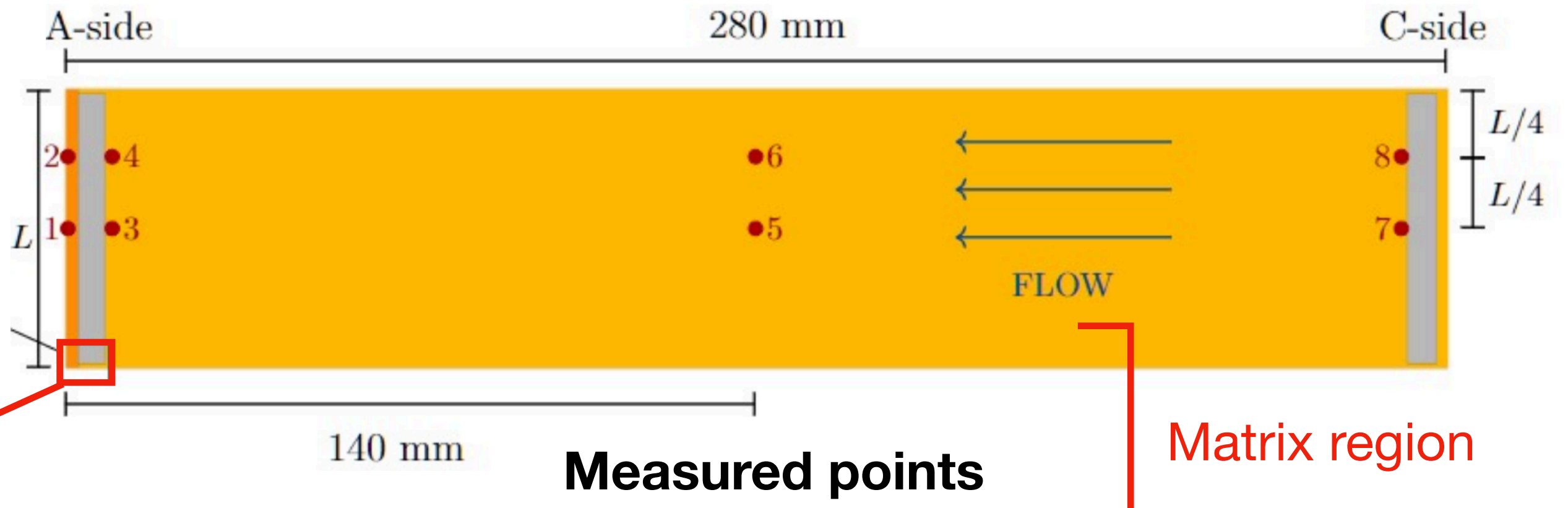


Power consumption tested:
Endcap: 1000 mW/cm², Matrix 25 mW/cm²

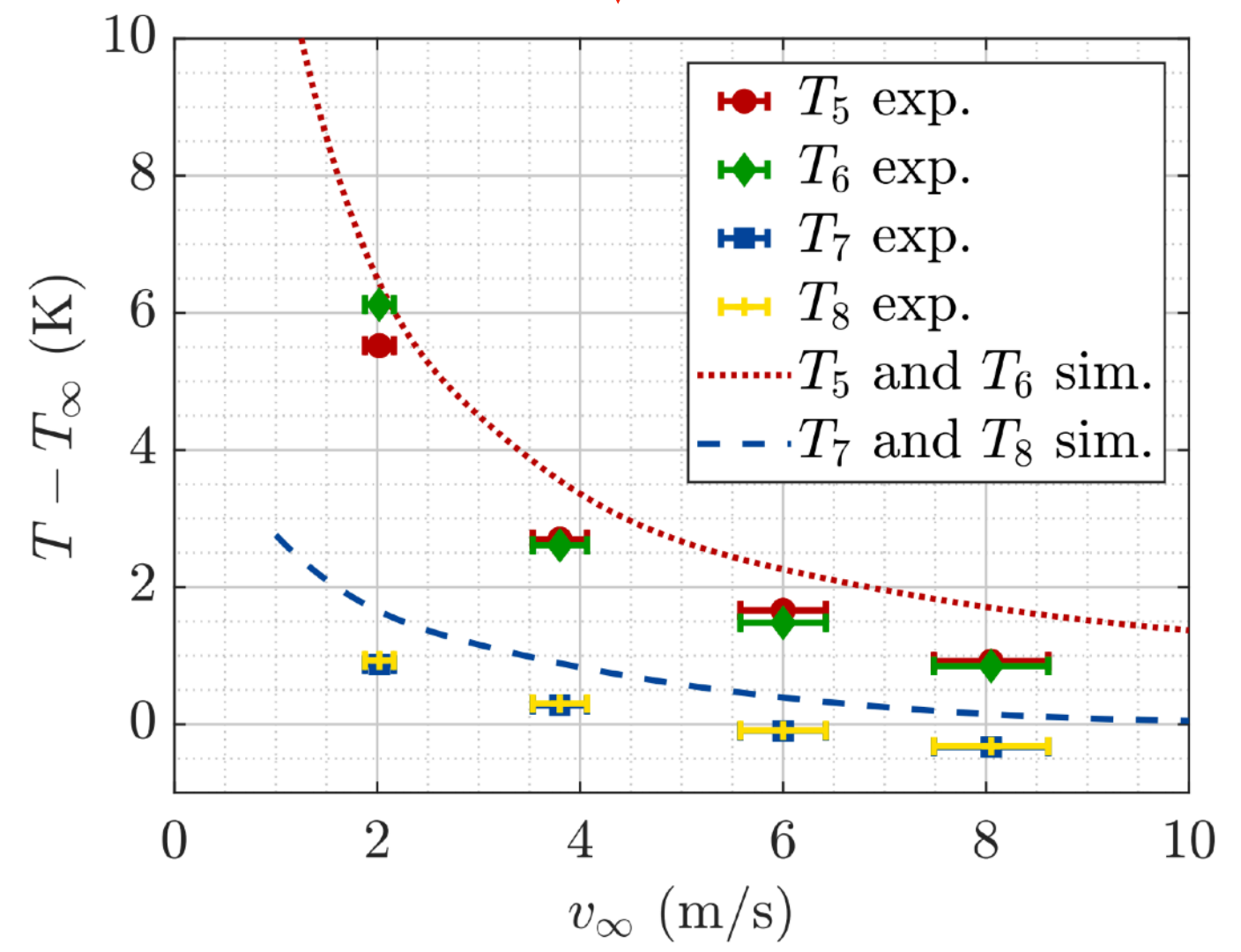
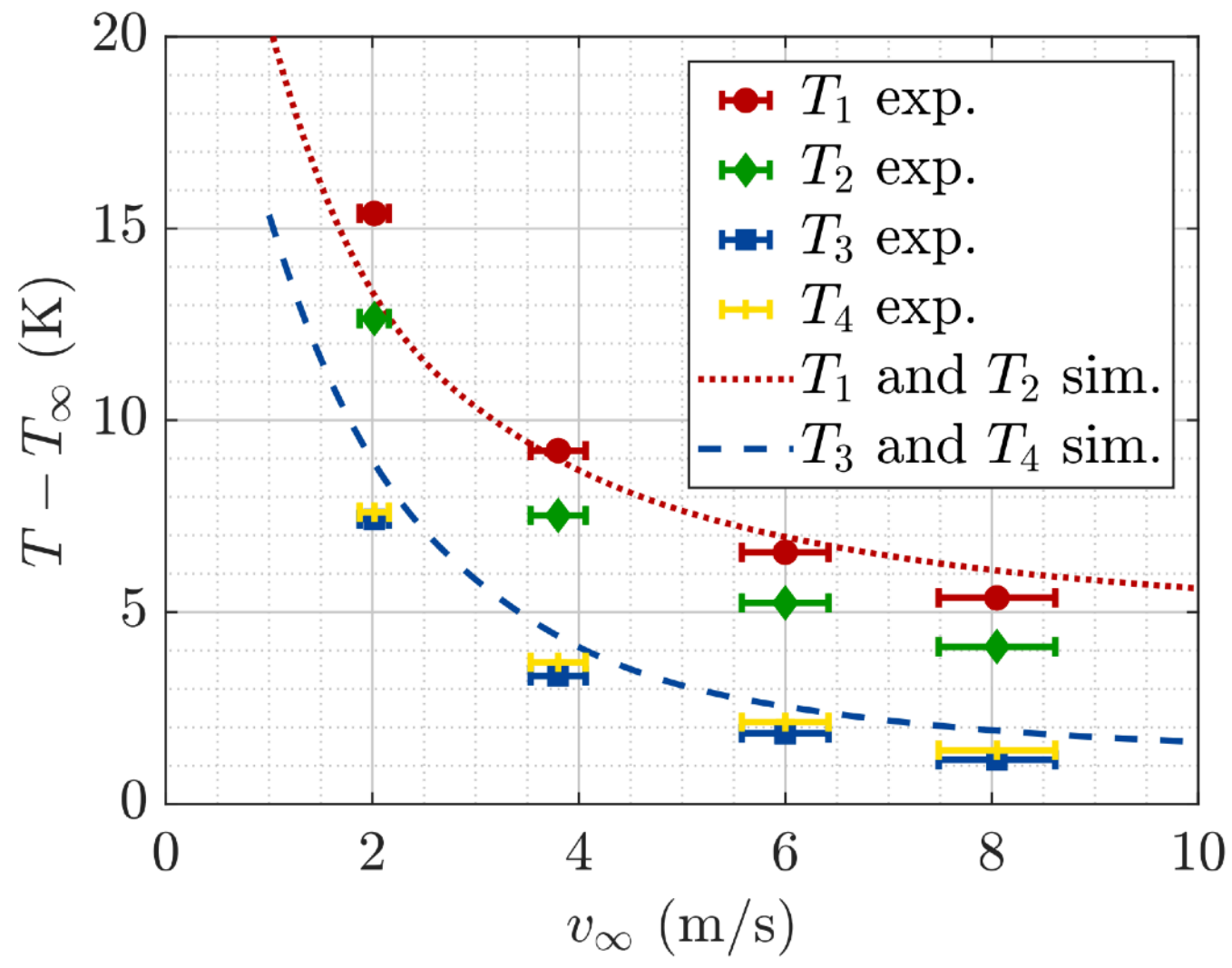
3 layers of Silicon chips, embedded in Kapton PCB with heating traces



ITS3 "bread board" model 3



Endcap region



- The CFD simulations and the experimental results agree well
- The simulations slightly over-predict the values in all cases.

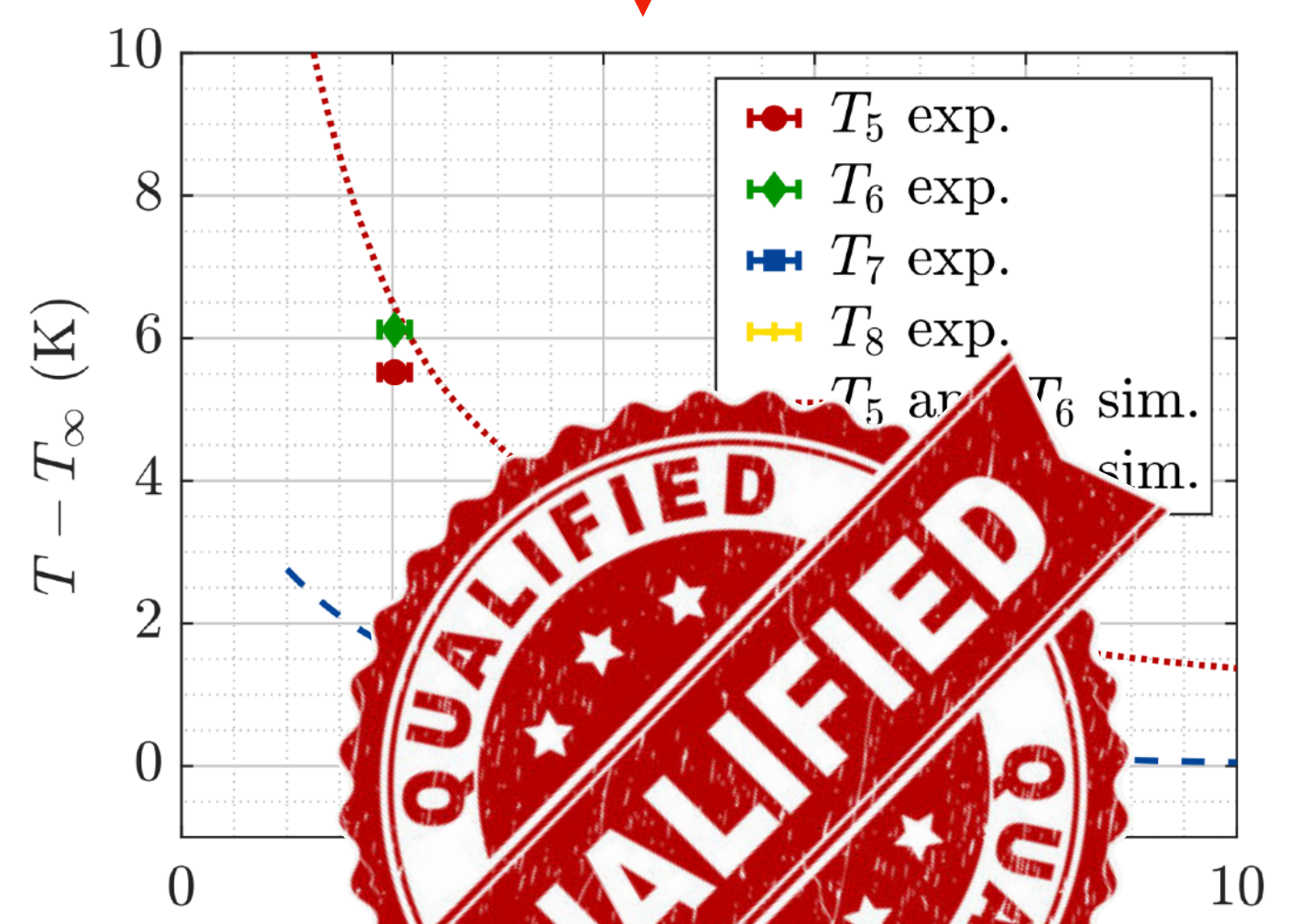
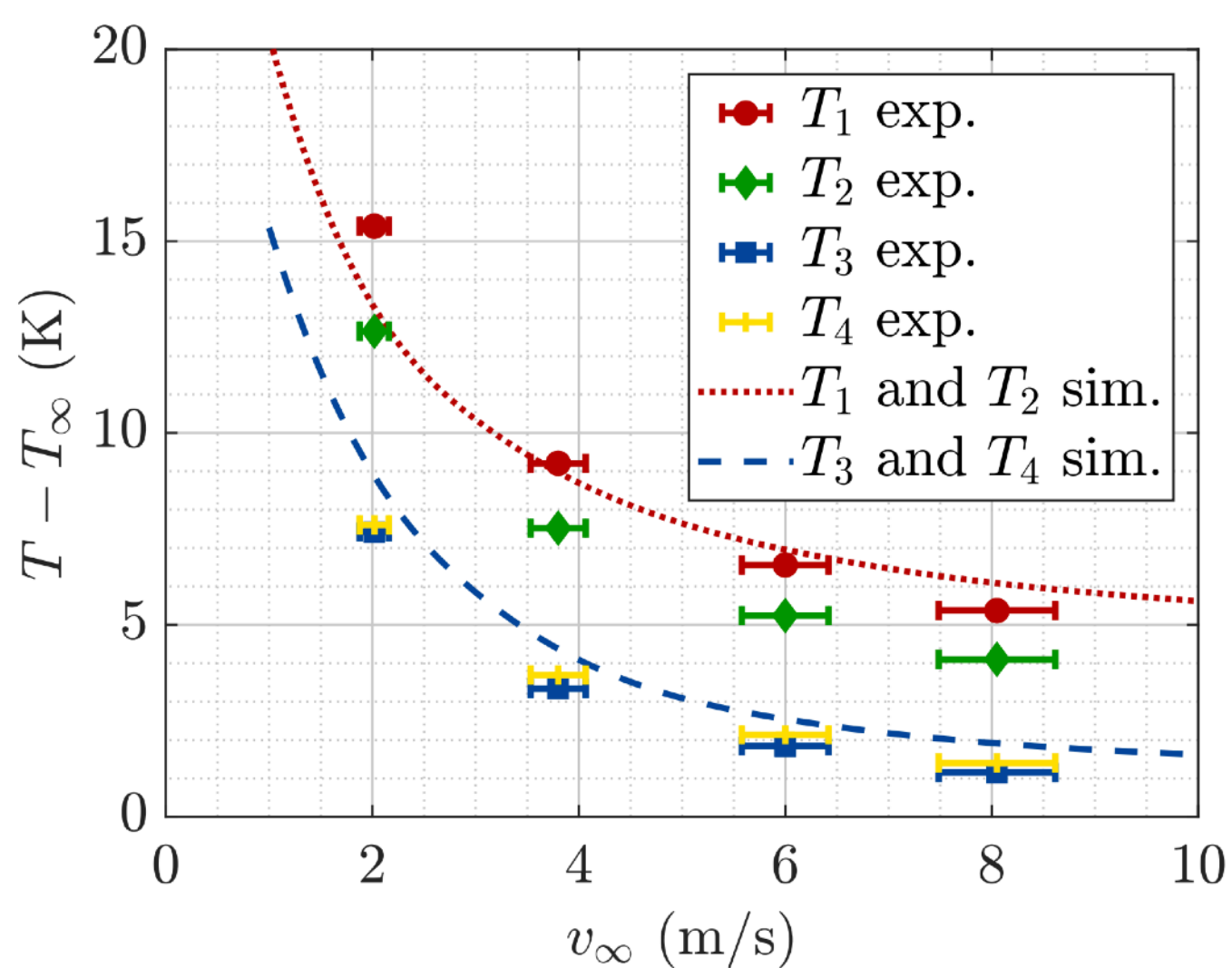
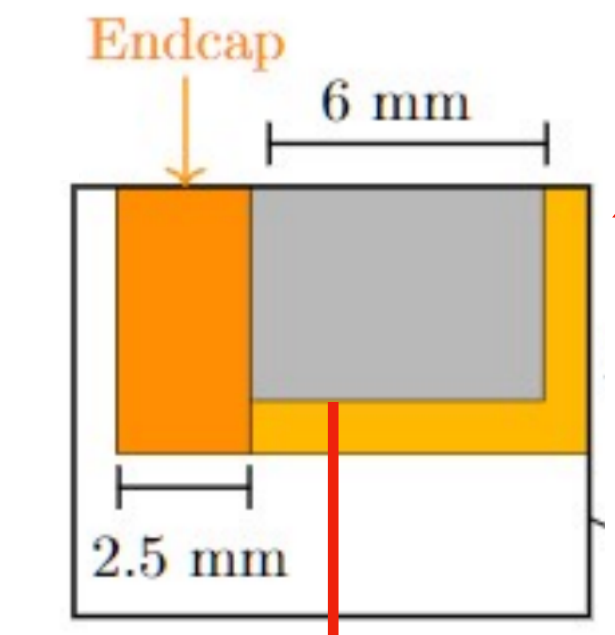
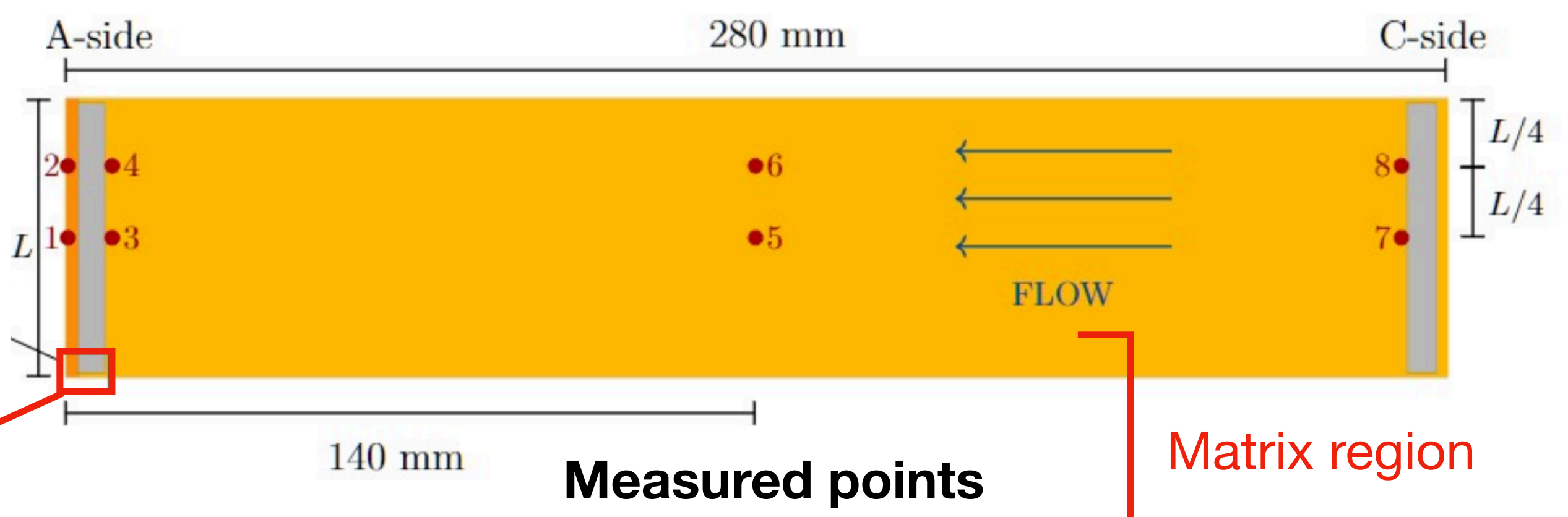
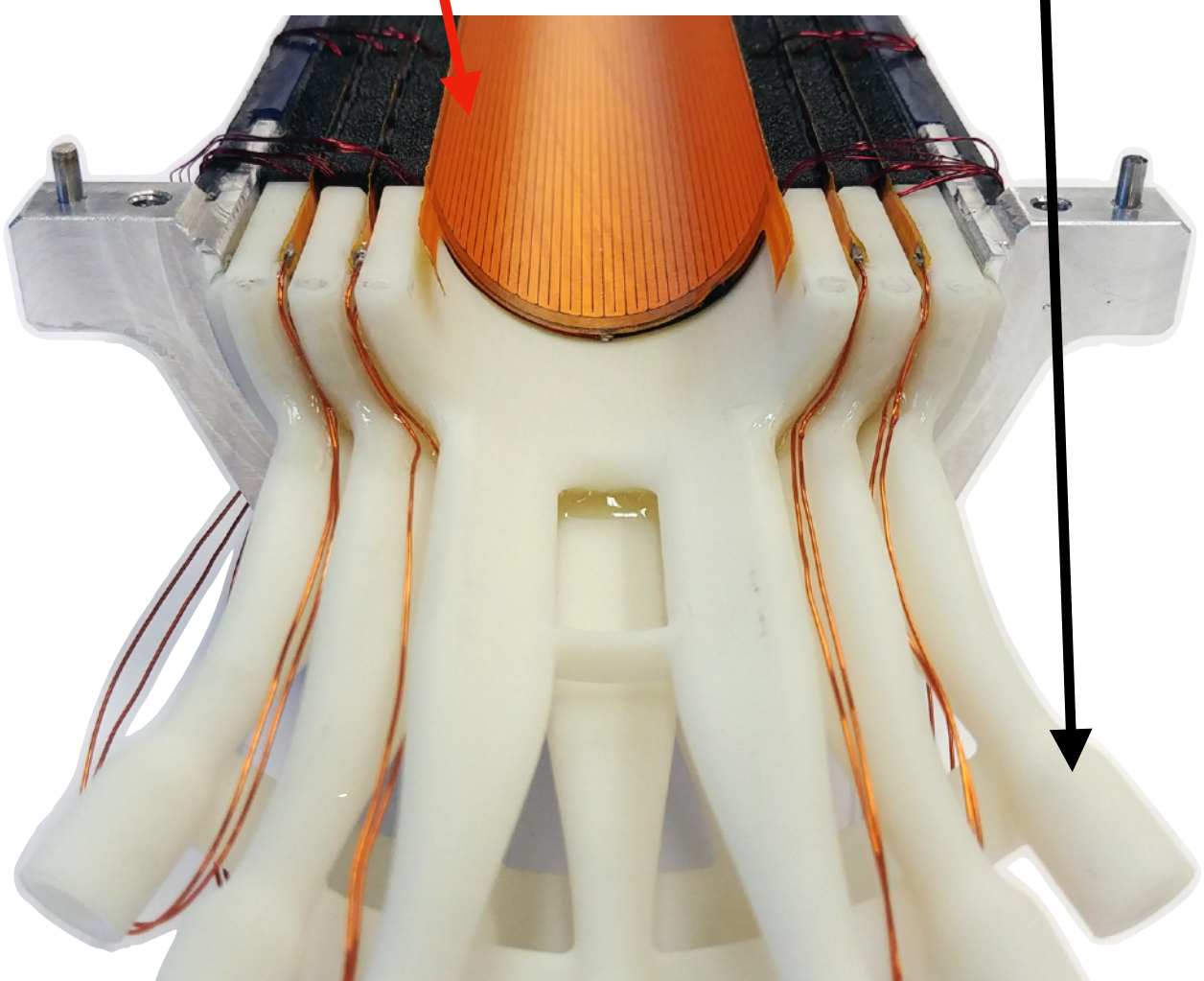
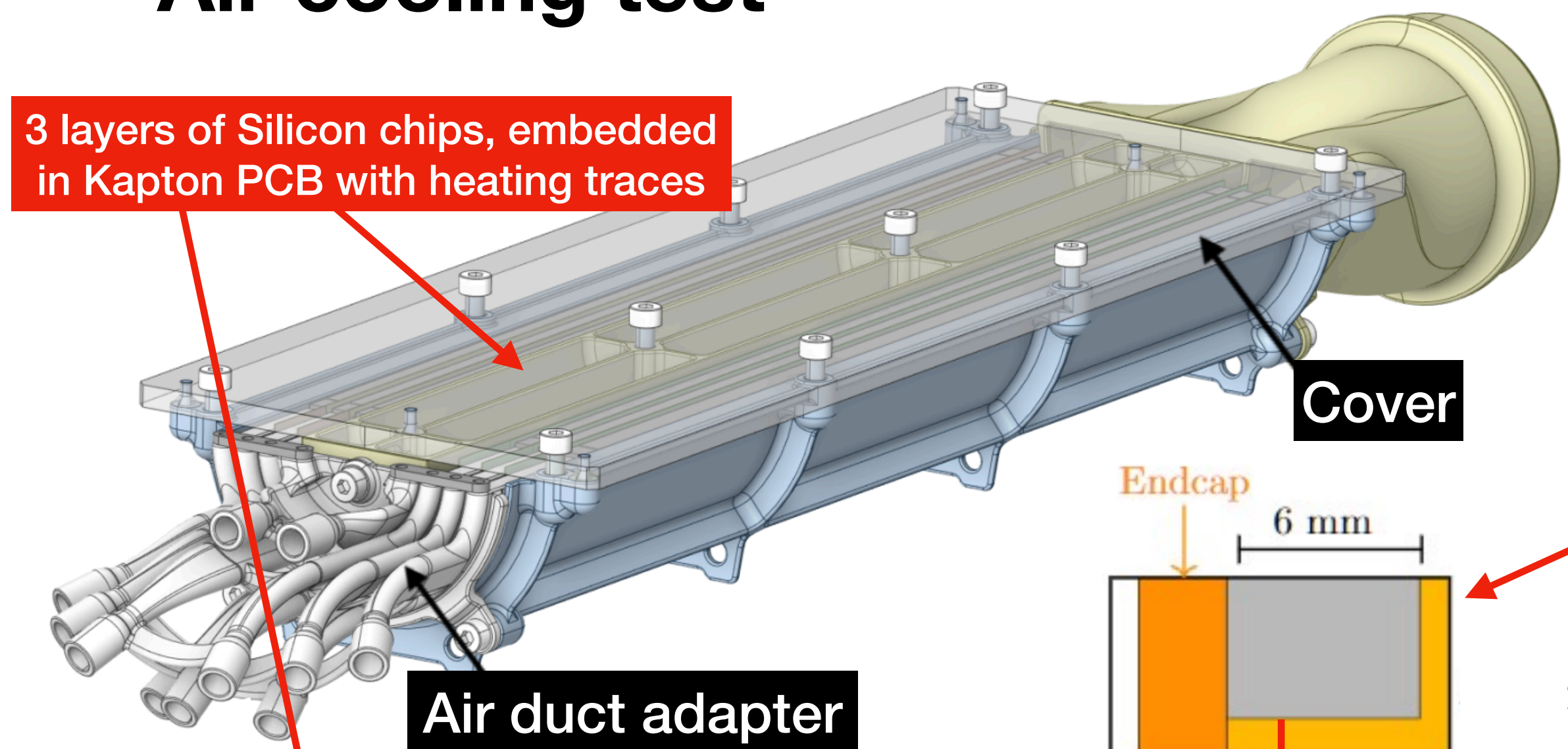
ITS design and R&D

Air cooling test



Power consumption tested:
Endcap: 1000 mW/cm², Matrix 25 mW/cm²

3 layers of Silicon chips, embedded in Kapton PCB with heating traces



- The CFD simulations and the experimental results agree
- The simulations slightly over

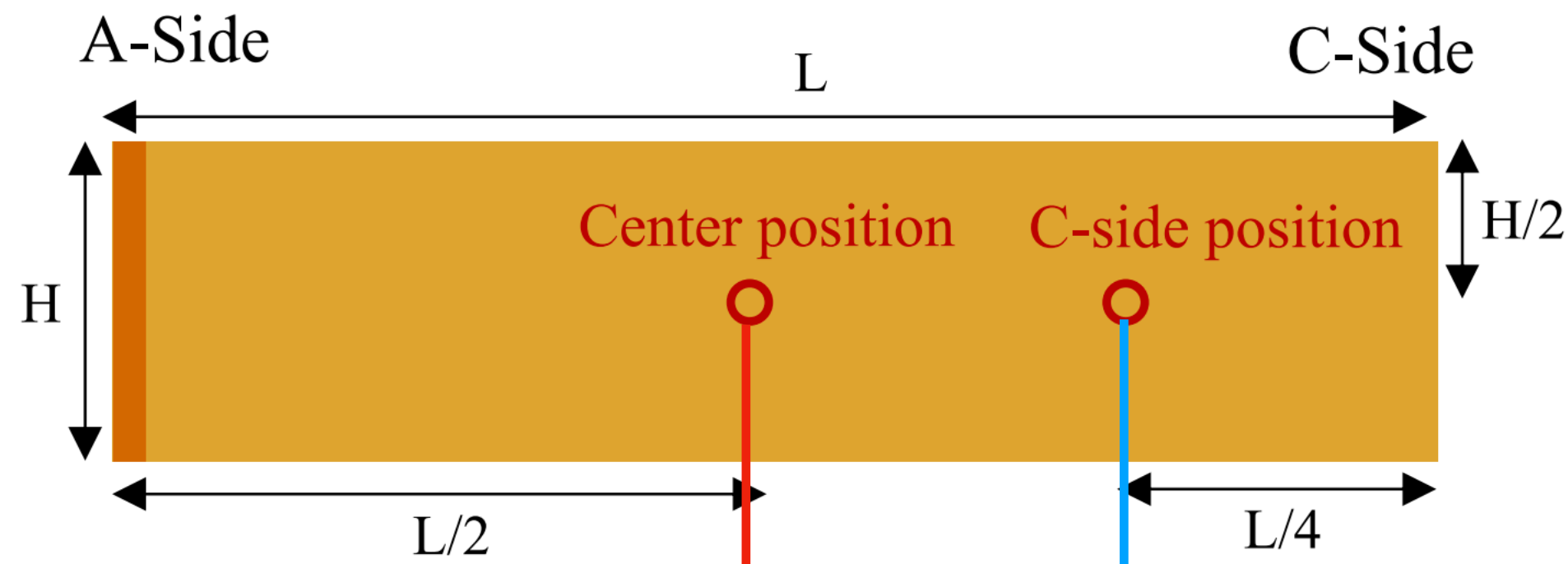
Air cooling works well !

ITS3 "bread board" model 3

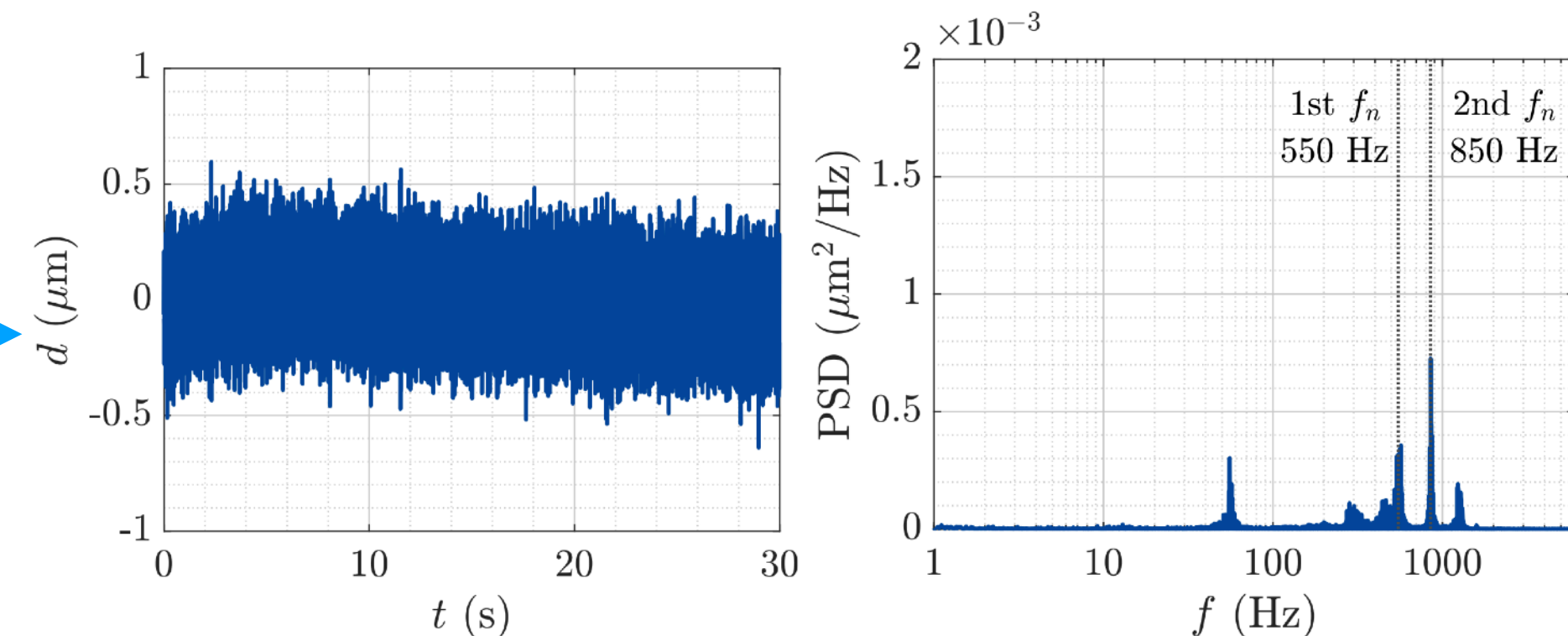
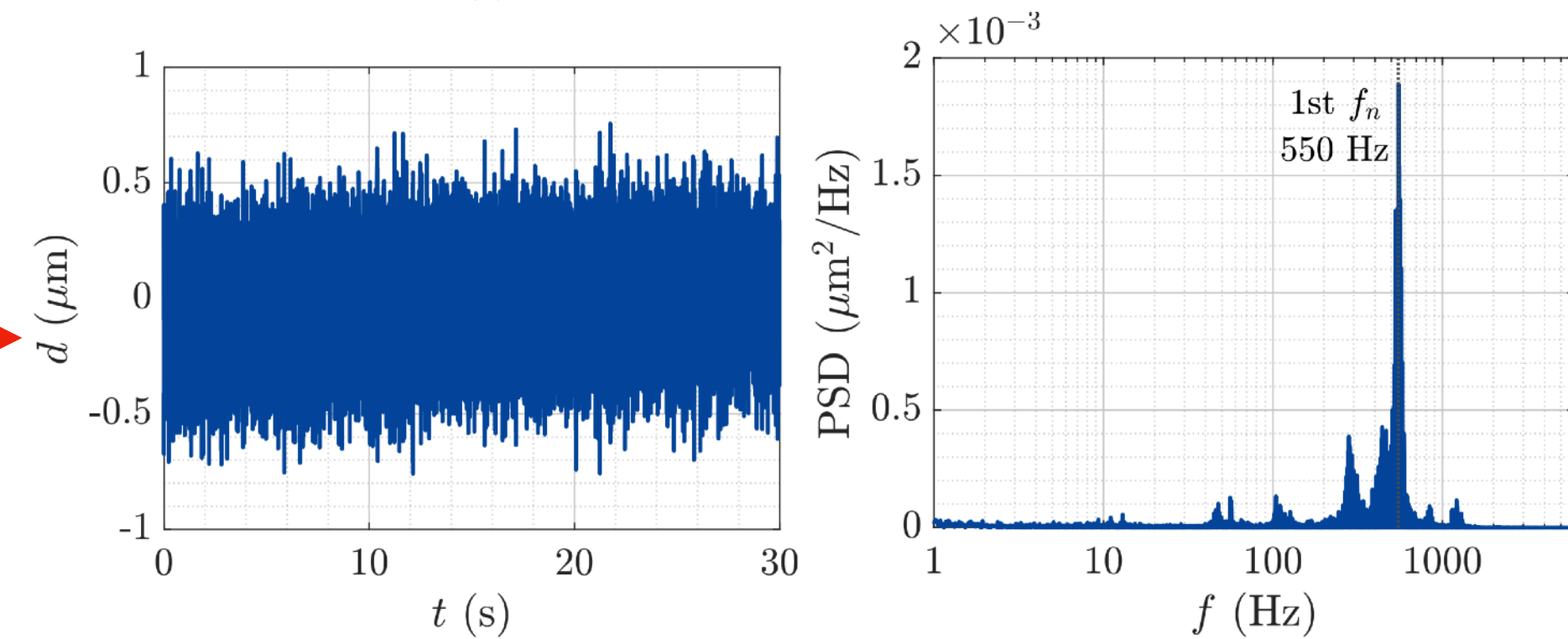
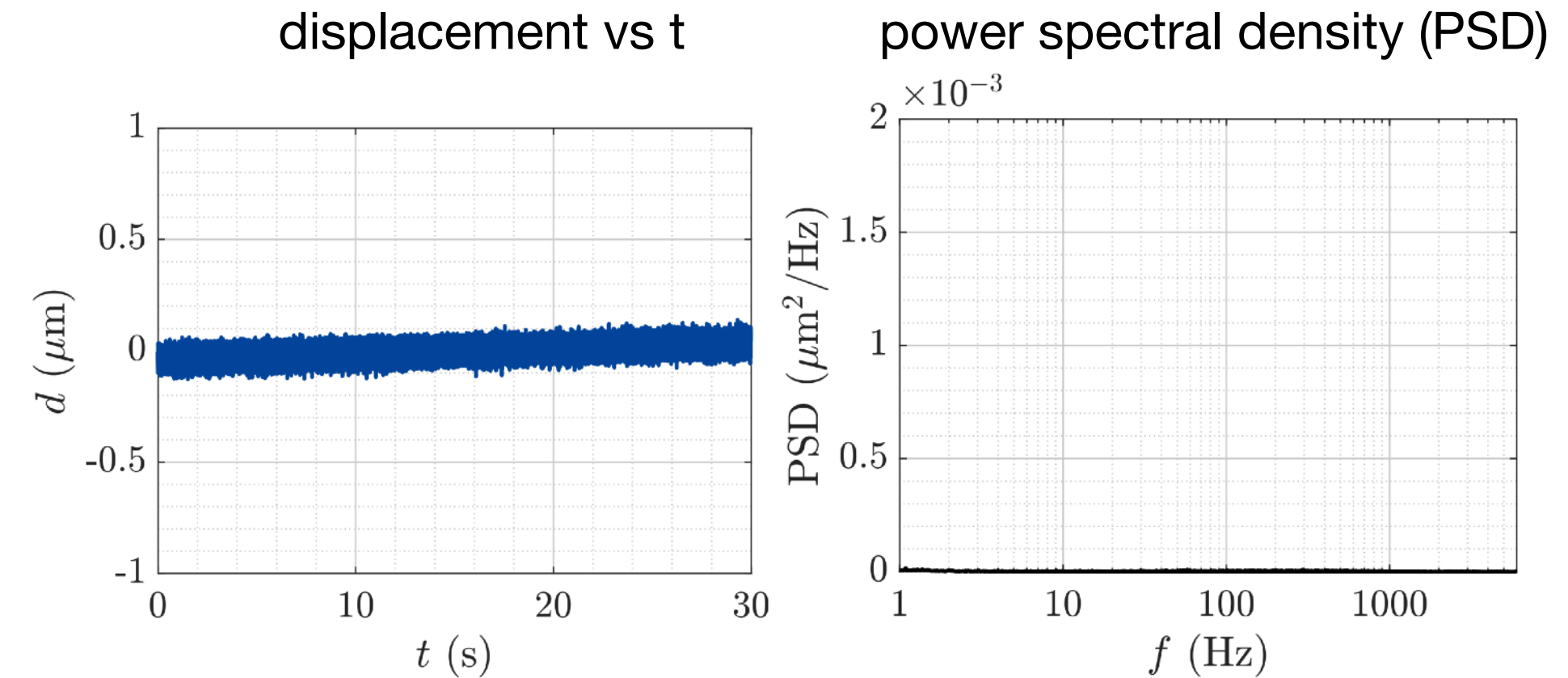


ITS design and R&D

Aeroelastic test

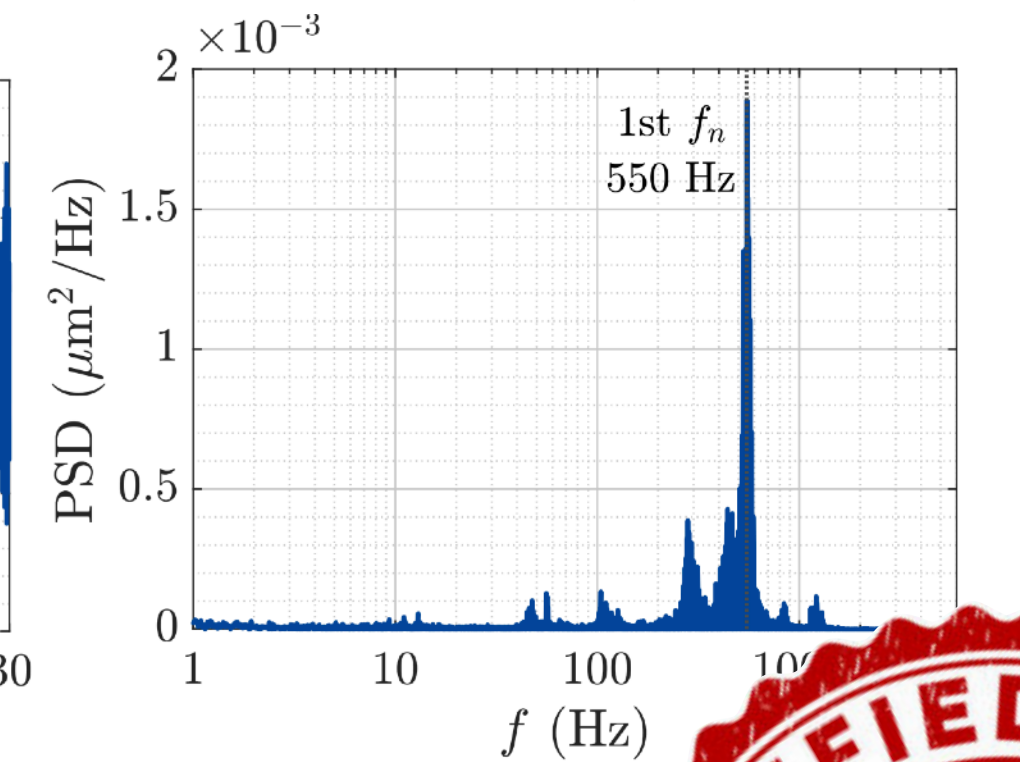
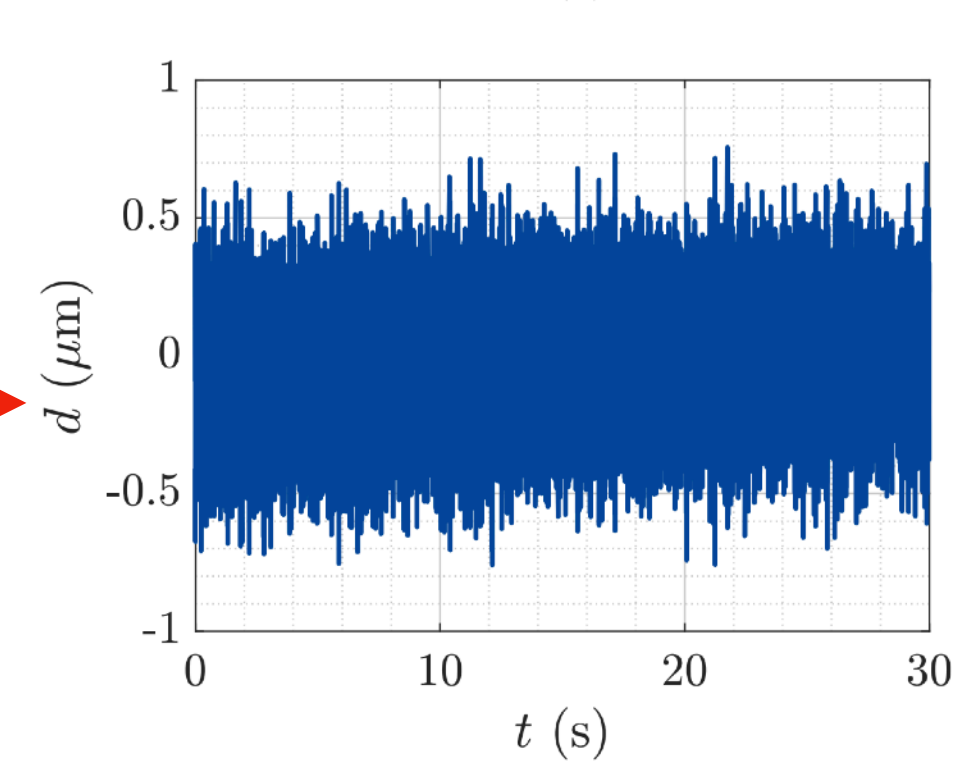
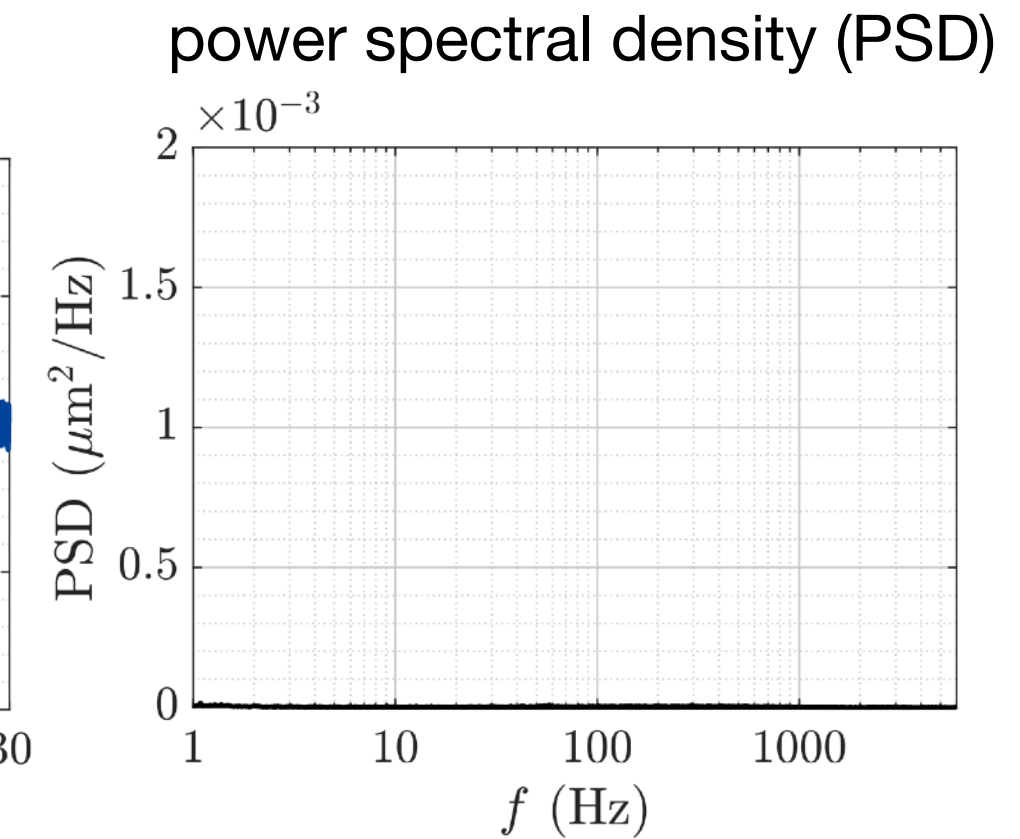
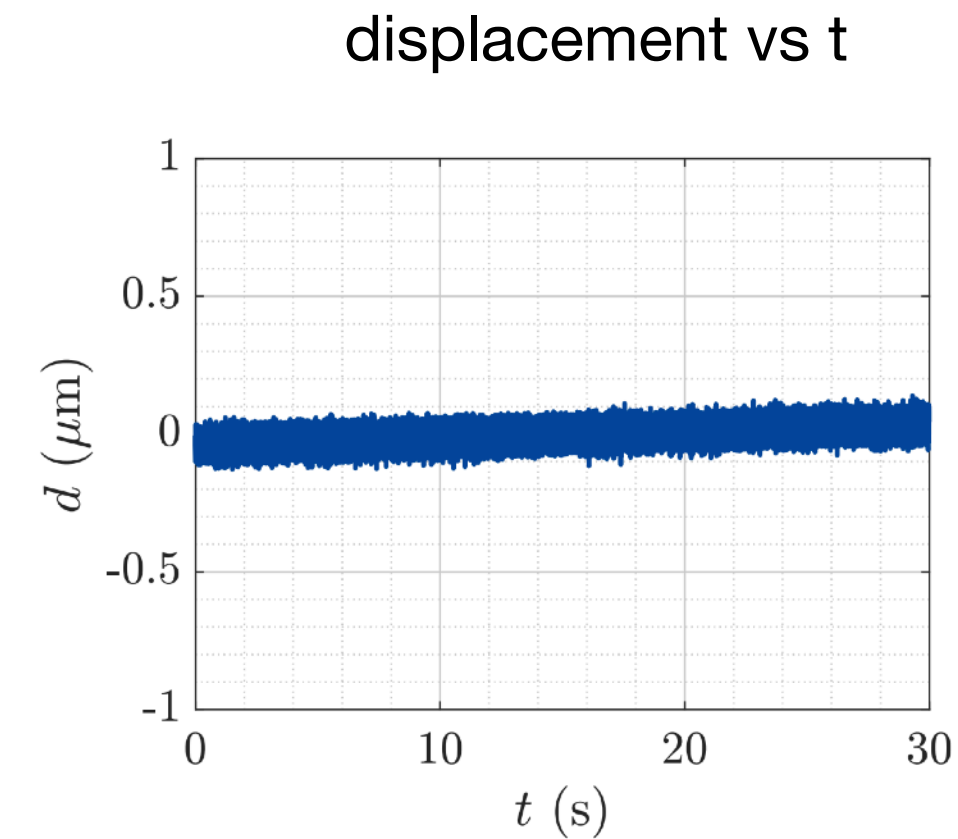
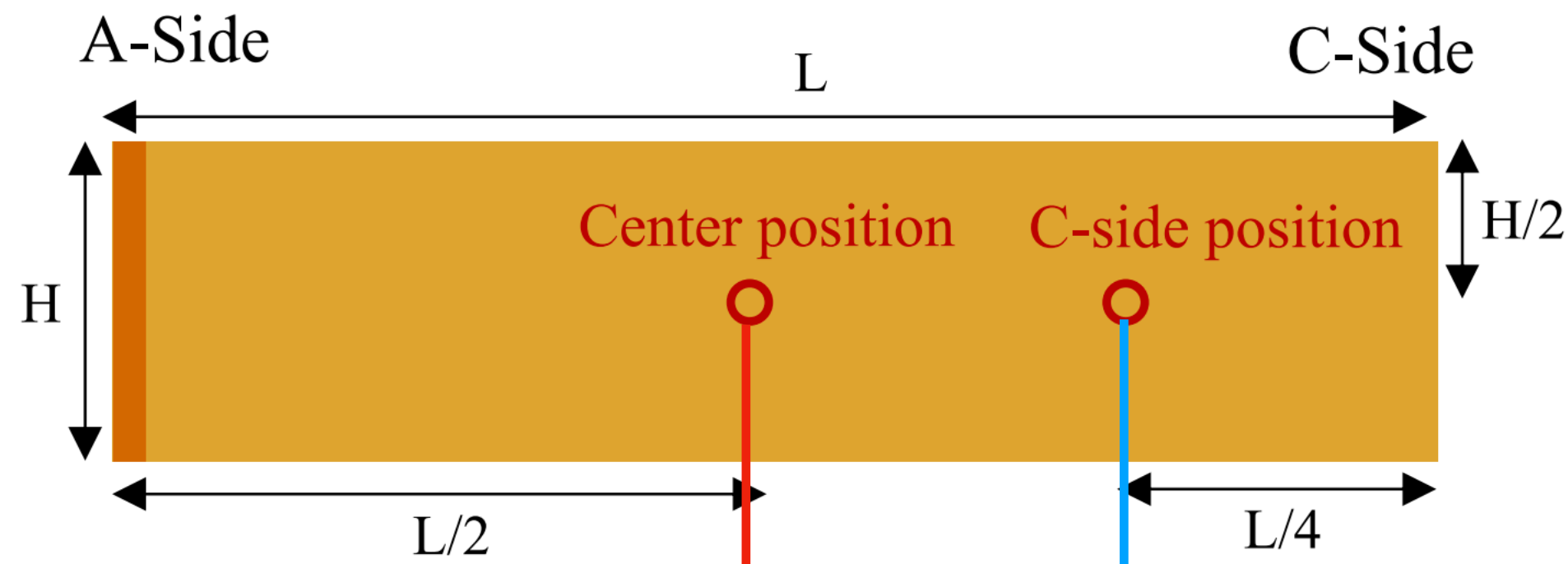


- Air flow: 8 m/s
- Measured displacement:
 - $RMS_{airflow} < 0.4 \mu m$
 - Maximum: $\sim 1.1 \mu m$
 - Requirement: $< 2 \mu m$



ITS design and R&D

Aeroelastic test



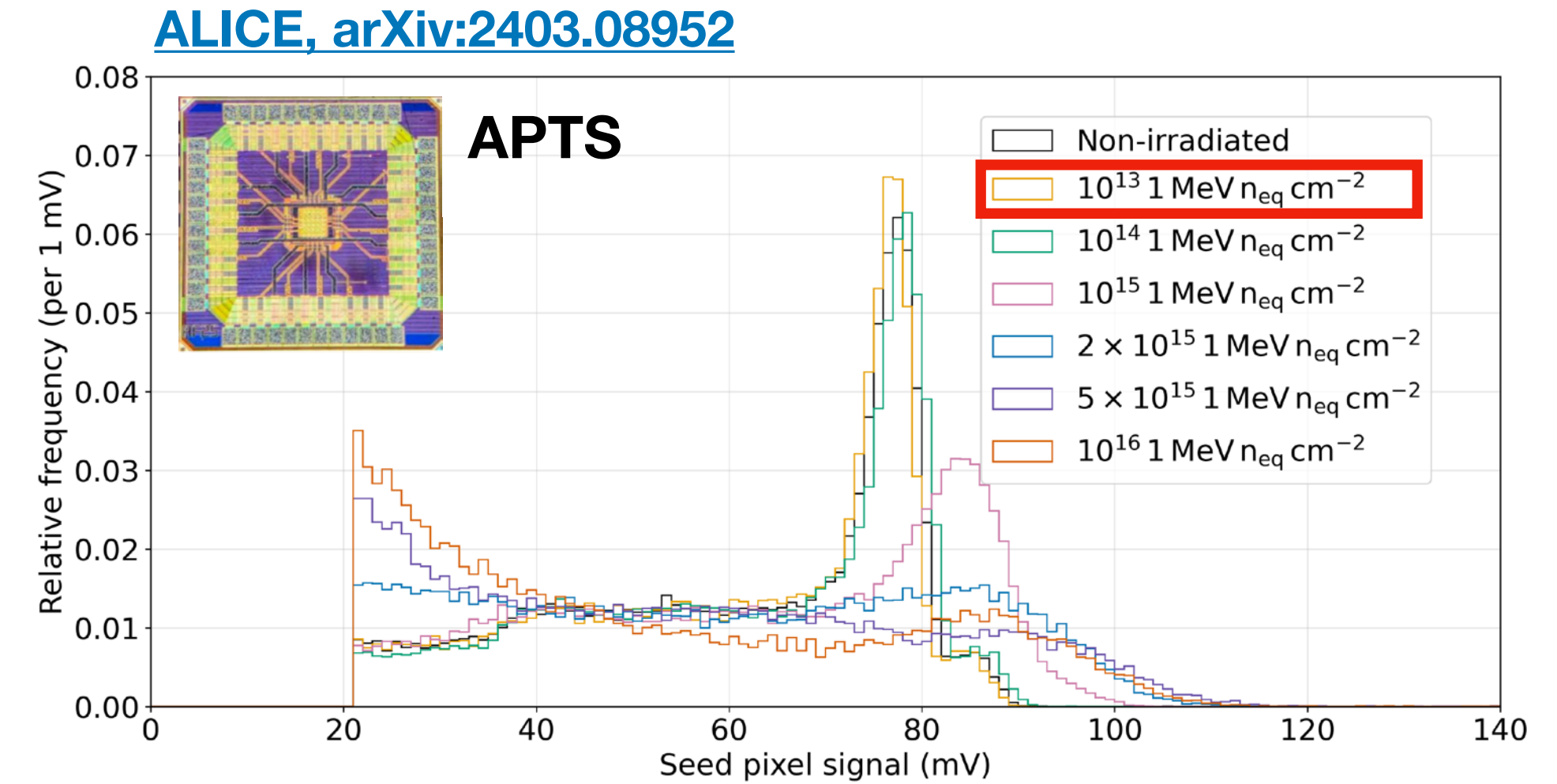
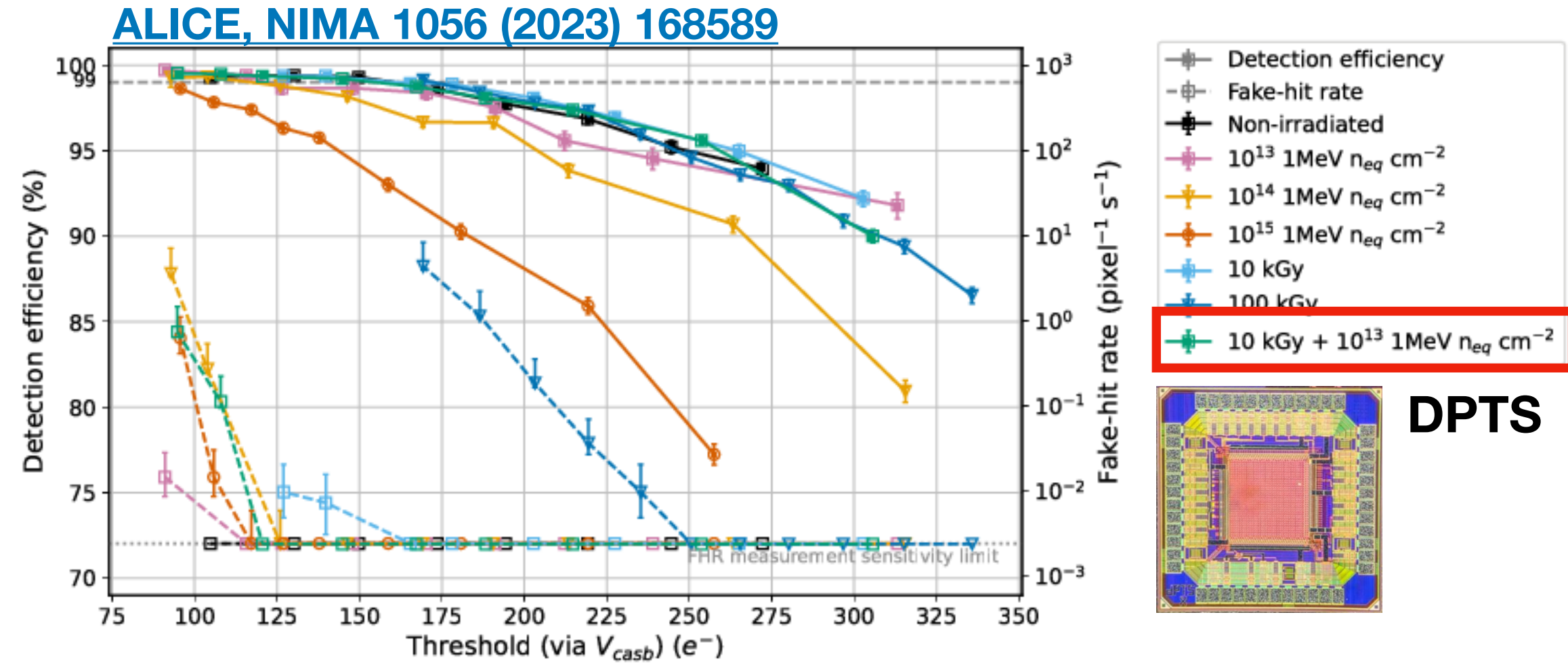
- Air flow: 8 m/s
- Measured displacement:
 - $RMS_{airflow} < 0.4 \mu m$
 - Maximum: $\sim 1.1 \mu m$
 - Requirement: $< 2 \mu m$



Aeroelastic test seems okay !

ITS design and R&D

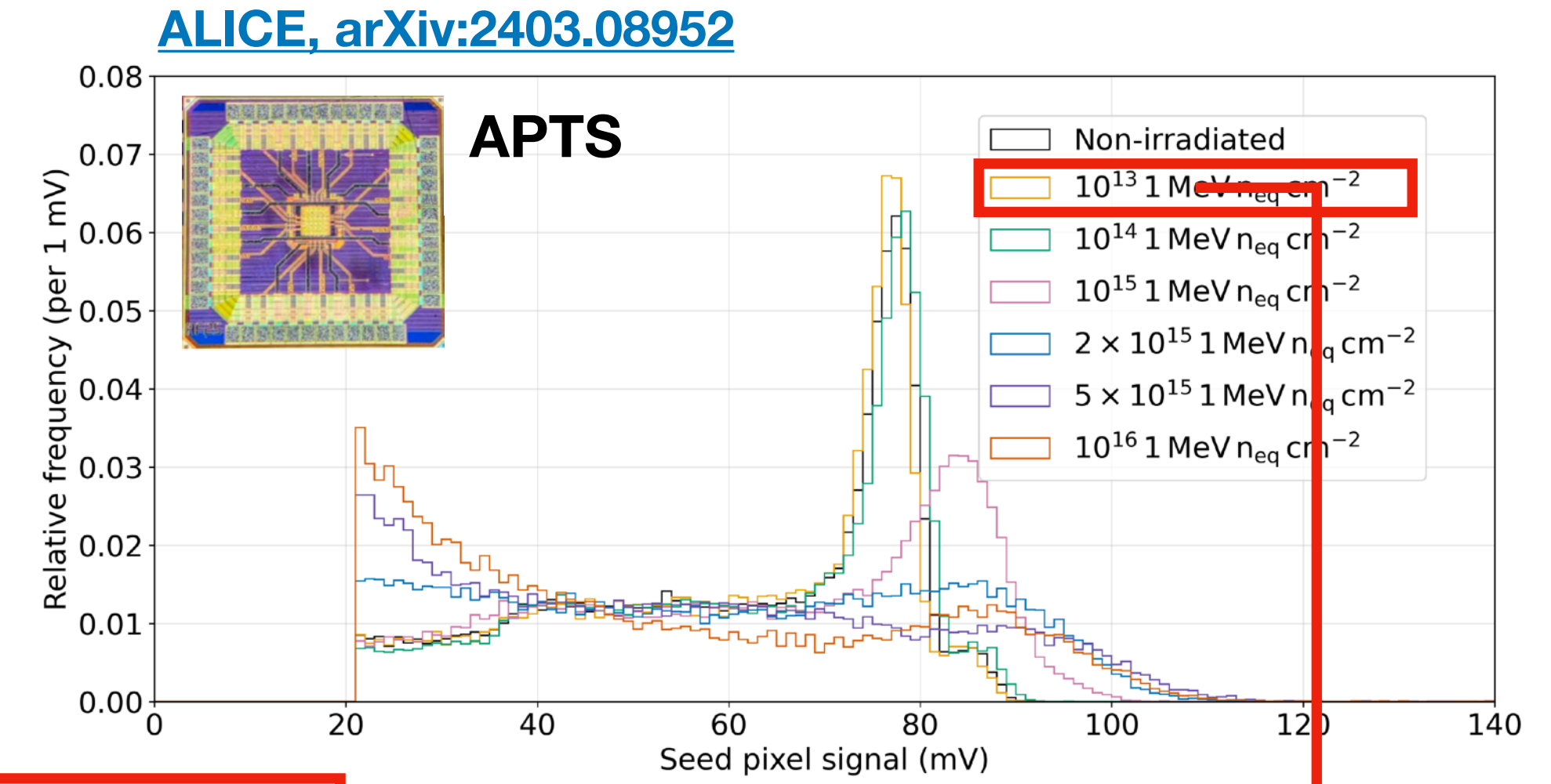
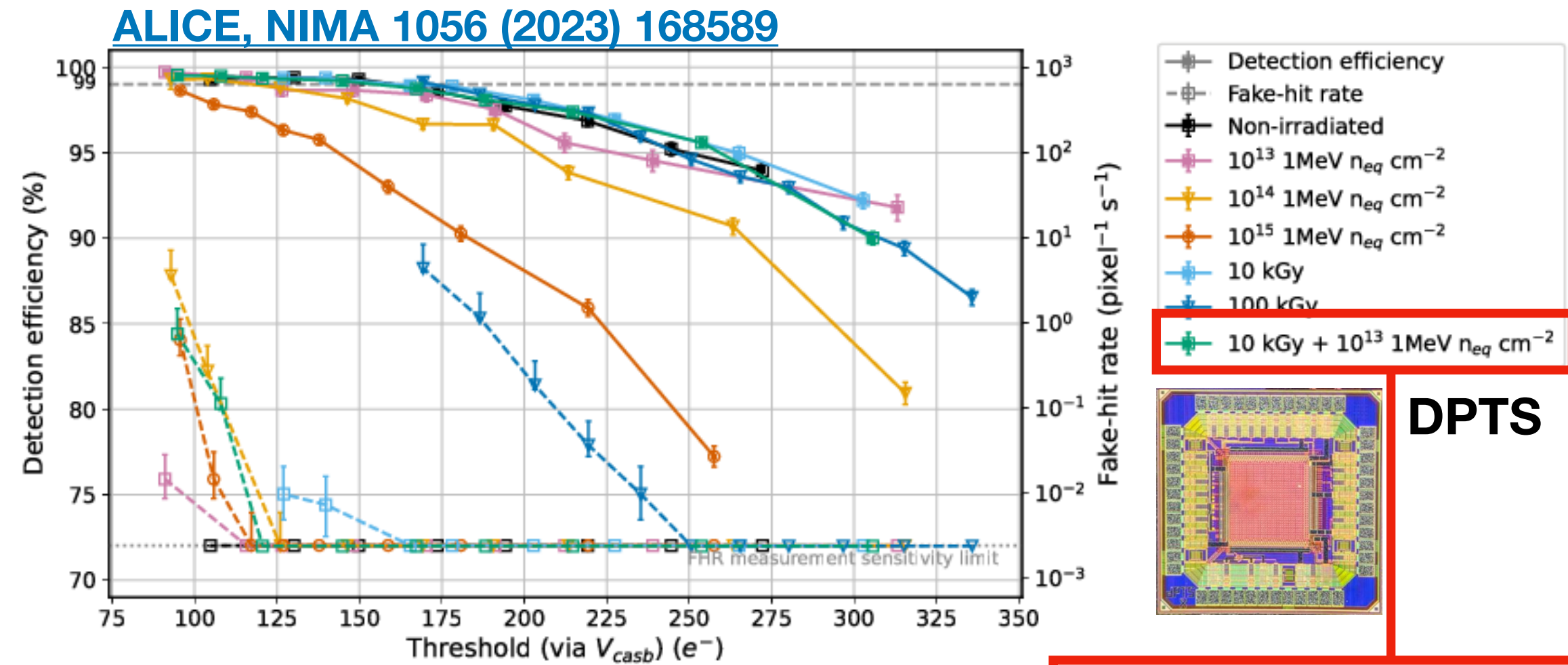
Qualification of 65nm CMOS



- Concentrated effort **ALICE ITS3** together with **CERN EP R&D**
- **Prototype sensors:** APTS (Analogue pixel test structure), DPTS (Digital pixel test structure), CE65
 - **DPTS (left):** Efficiency ($> 99\%$) with low fake-hit rate ($< 2 \times 10^{-3} \text{ pixel}^{-1} \text{ s}^{-1}$)
 - **APTS (right):** Charge collection not deteriorated by irradiation

ITS design and R&D

Qualification of 65nm CMOS

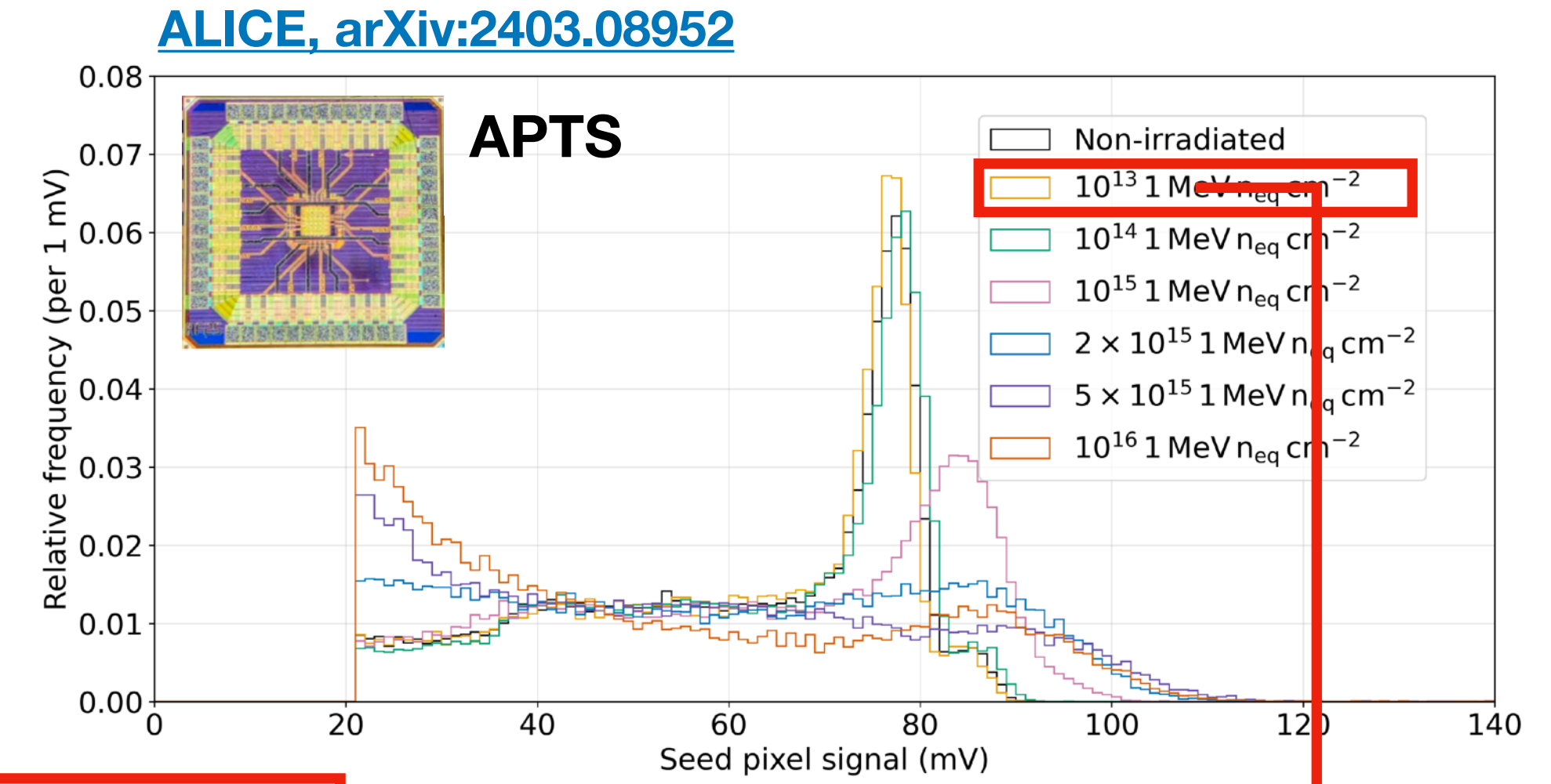
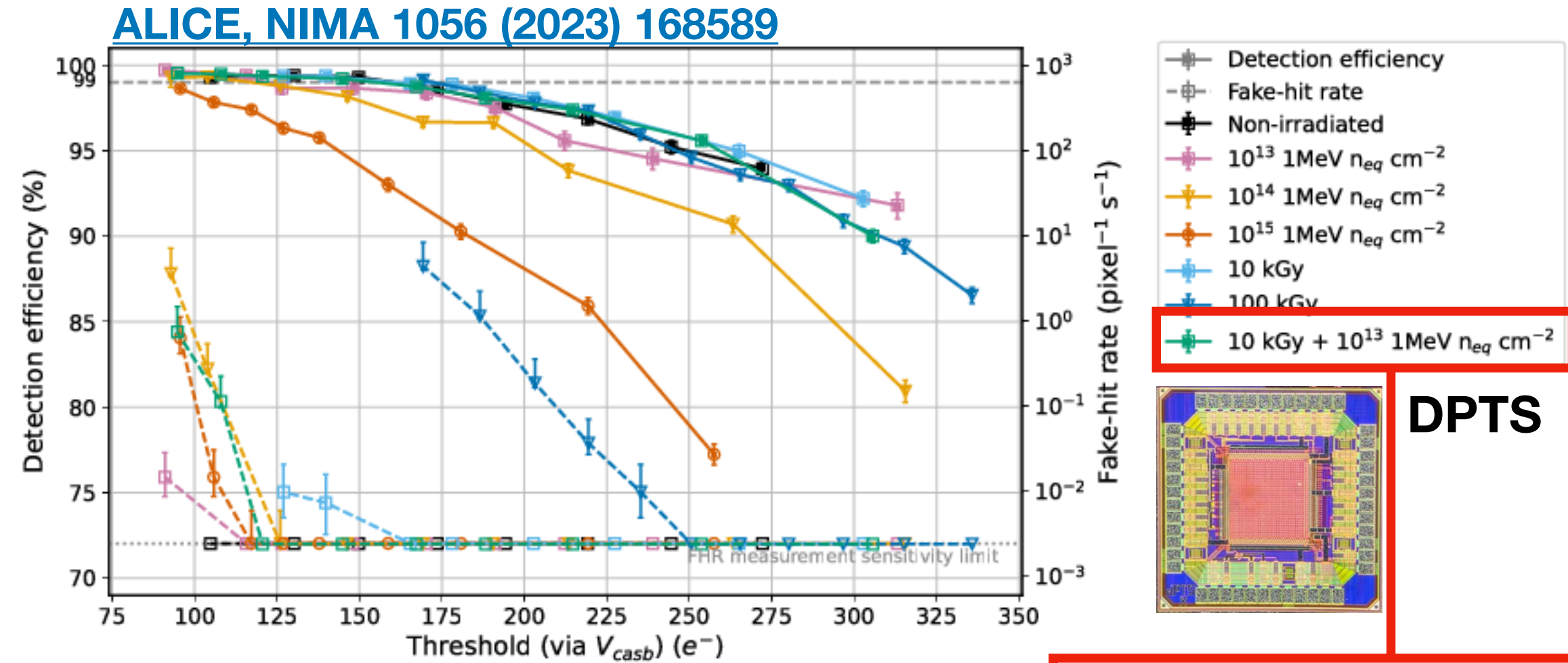


Irradiation ITS3 requirements

- Concentrated effort **ALICE ITS3** together with **CERN EP R&D**
- **Prototype sensors:** APTS (Analogue pixel test structure), DPTS (Digital pixel test structure), CE65
 - **DPTS (left):** Efficiency ($> 99\%$) with low fake-hit rate ($< 2 \times 10^{-3} \text{ pixel}^{-1} \text{ s}^{-1}$)
 - **APTS (right):** Charge collection not deteriorated by irradiation

ITS design and R&D

Qualification of 65nm CMOS



Irradiation ITS3 requirements

- Concentrated effort **ALICE ITS3** together with **CERN EP R&D**
- **Prototype sensors:** APTS (Analogue pixel test structure), DPTS (Digital pixel test structure)
 - **DPTS (left):** Efficiency ($> 99\%$) with low fake-hit rate ($< 2 \times 10^{-3} \text{ pixel}^{-1} \text{ s}^{-1}$)
 - **APTS (right):** Charge collection not deteriorated by irradiation

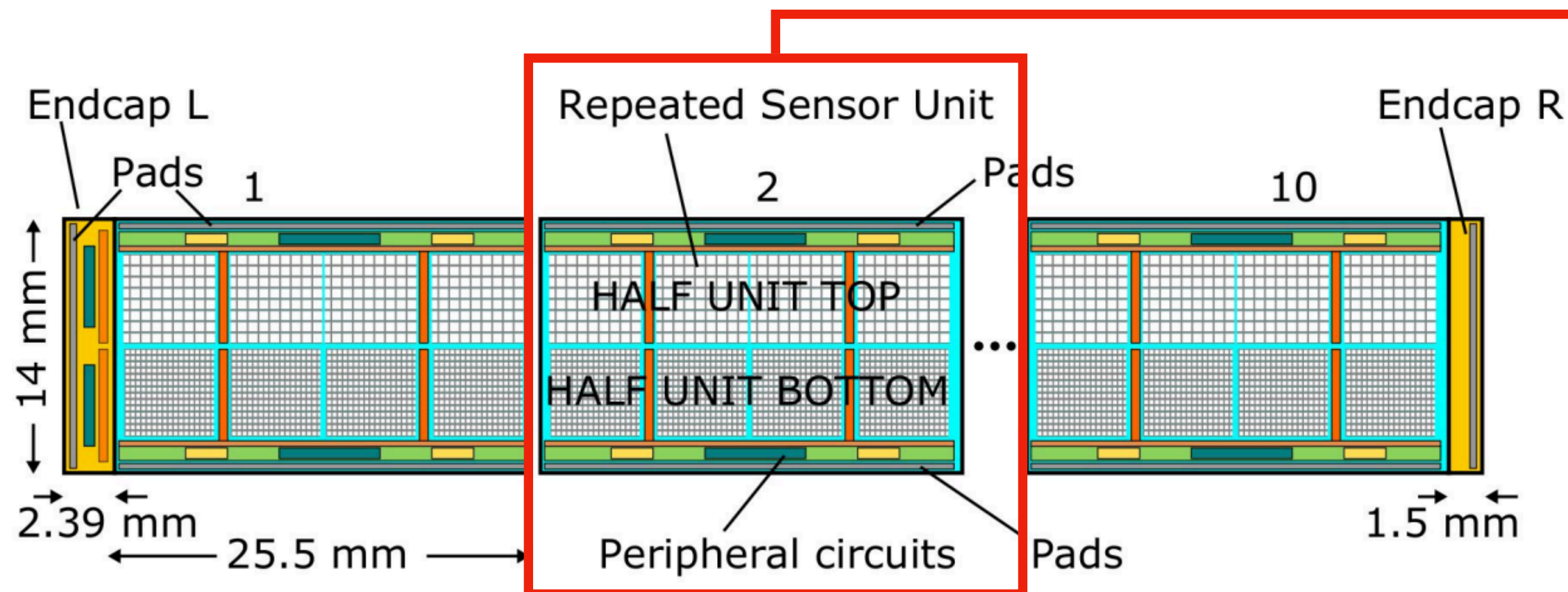
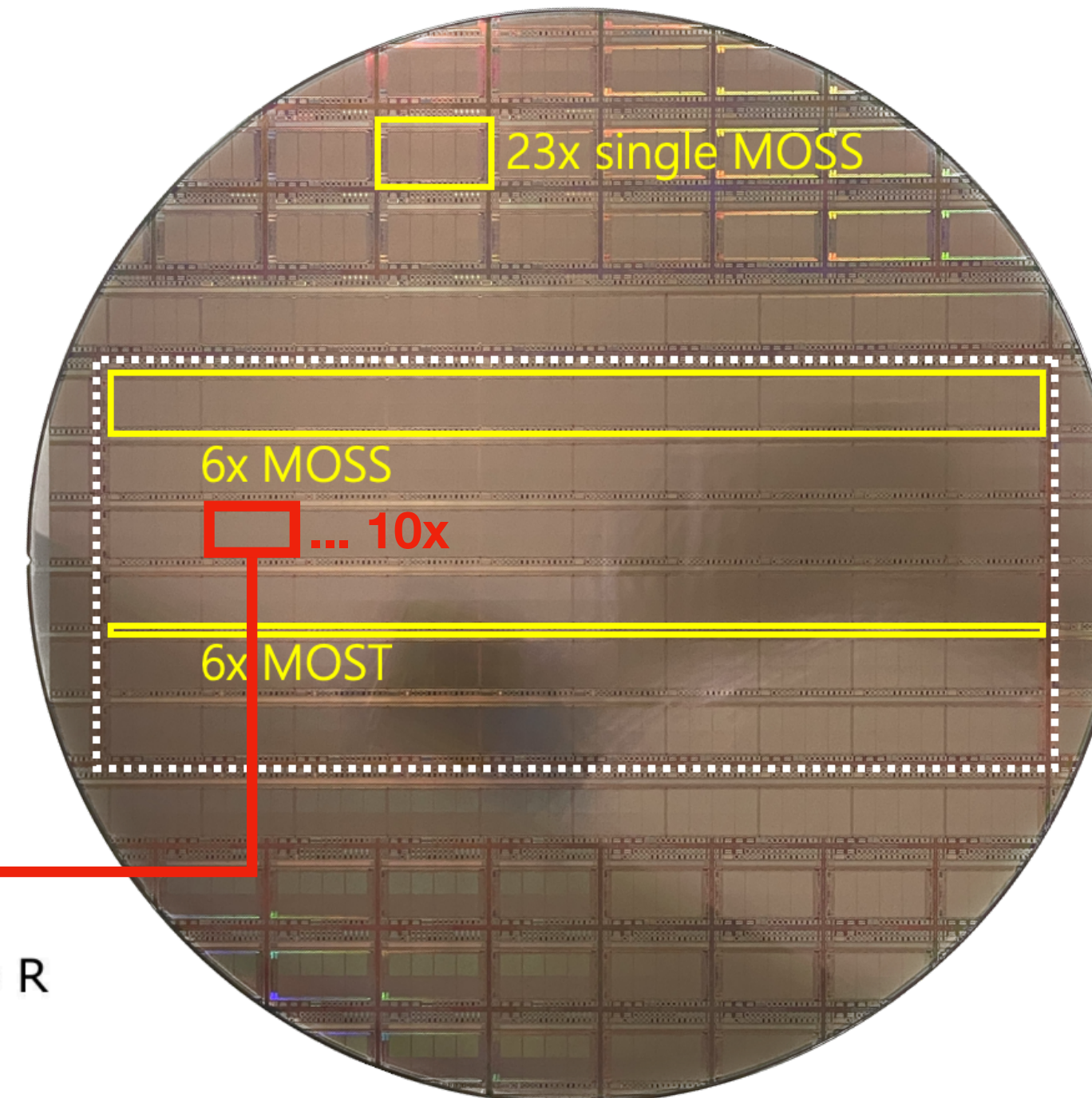


We can make the pixel sensor with this technology !

ITS design and R&D

Stitched MAPS

- **Goal:** Feasibility of stitching process
- **MO**nolithic **S**titched **S**ensor (**MOSS**):
 - 10 Repeated Sensor Units stitched together: 259 mm x 14 mm per sensor
 - 2 pixel pitches (18 μm and 22.5 μm) and 5 front-end variants



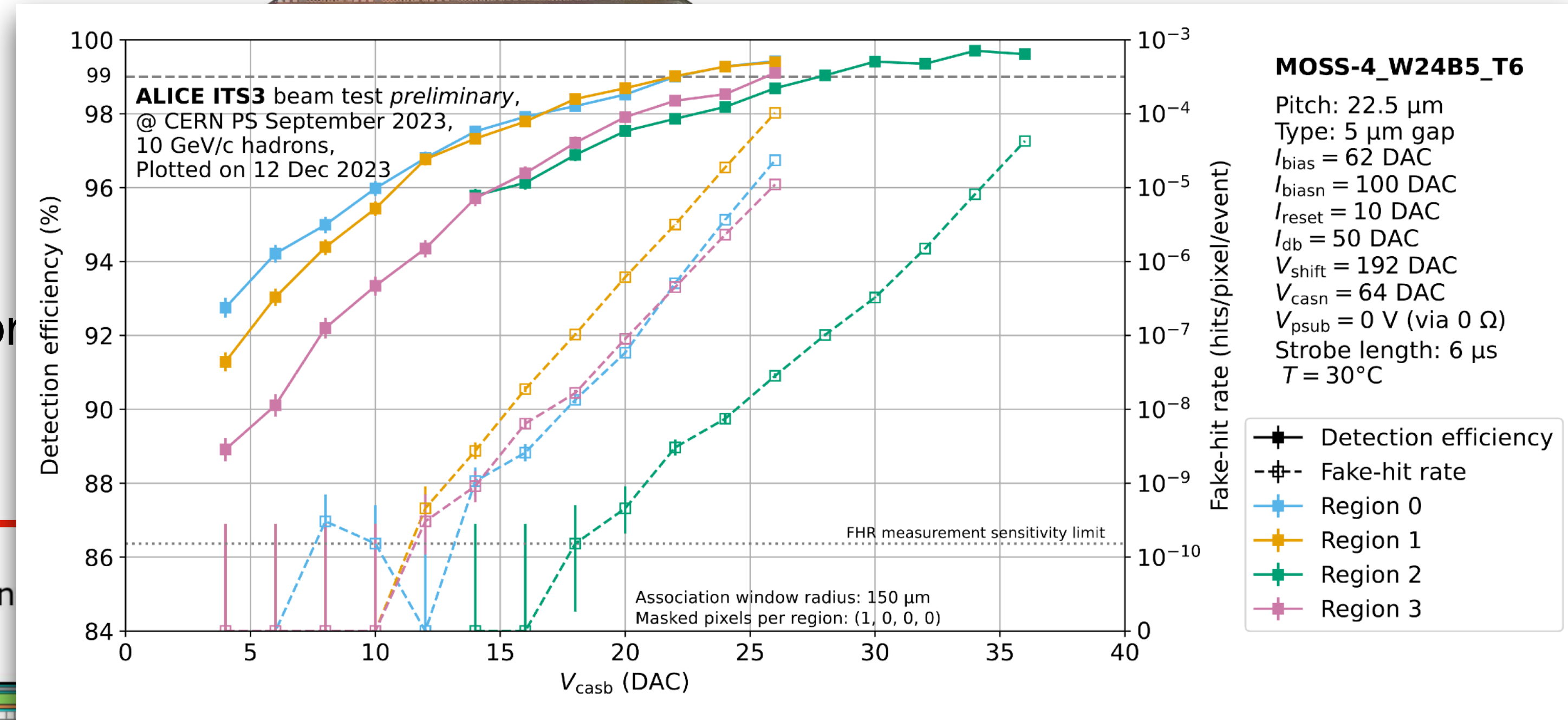
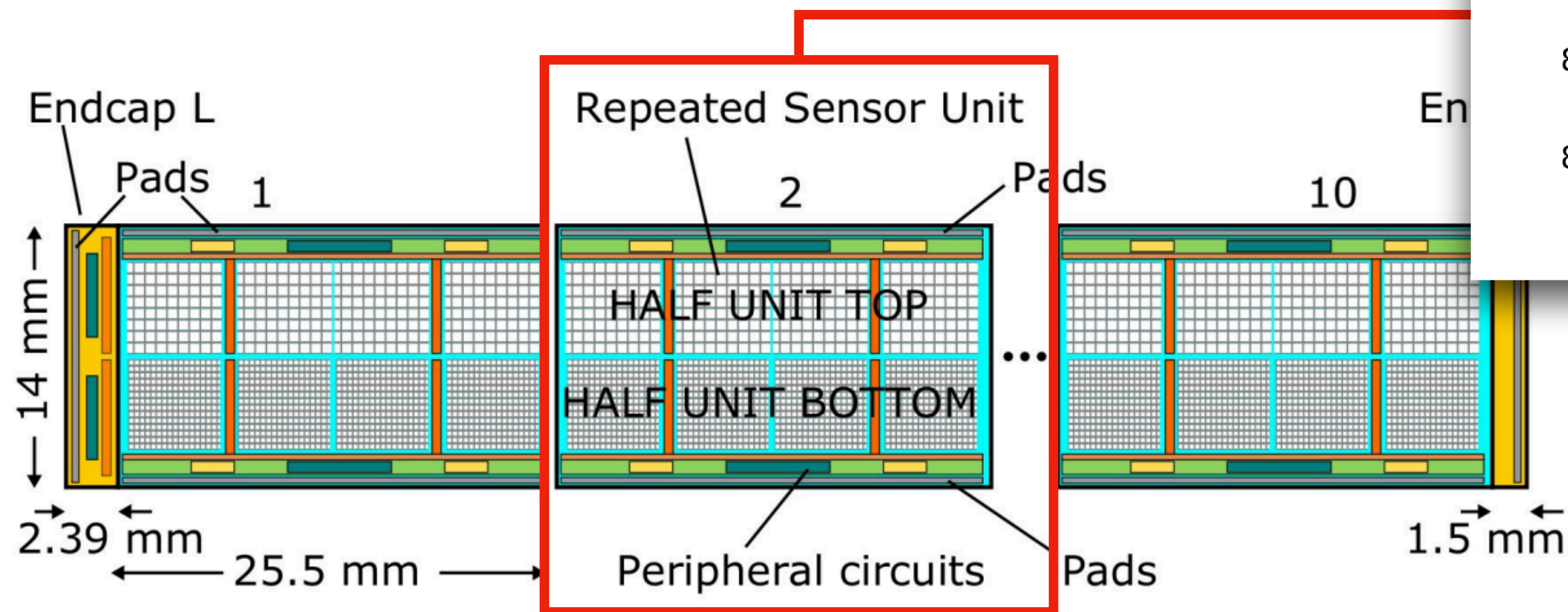
300 mm ER1 wafer

- **MOSS is operational and reaches full efficiency**
 - Yield: currently under study with extensive characterization campaign with wafer prober.
- **First beam tests performed at PS@CERN**
Detection efficiency: in line with expectations from MLR1 study

ITS design and R&D

Stitched MAPS

- **Goal:** Feasibility of stitching process
- **MO**nolithic **S**titched **S**ensor (**MOSS**):
 - 10 Repeated Sensor Units stitched together: 259 mm x 14 mm per sensor
 - 2 pixel pitches (18 μm and 22.5 μm) and 5 front-end variants



300 mm ER1 water

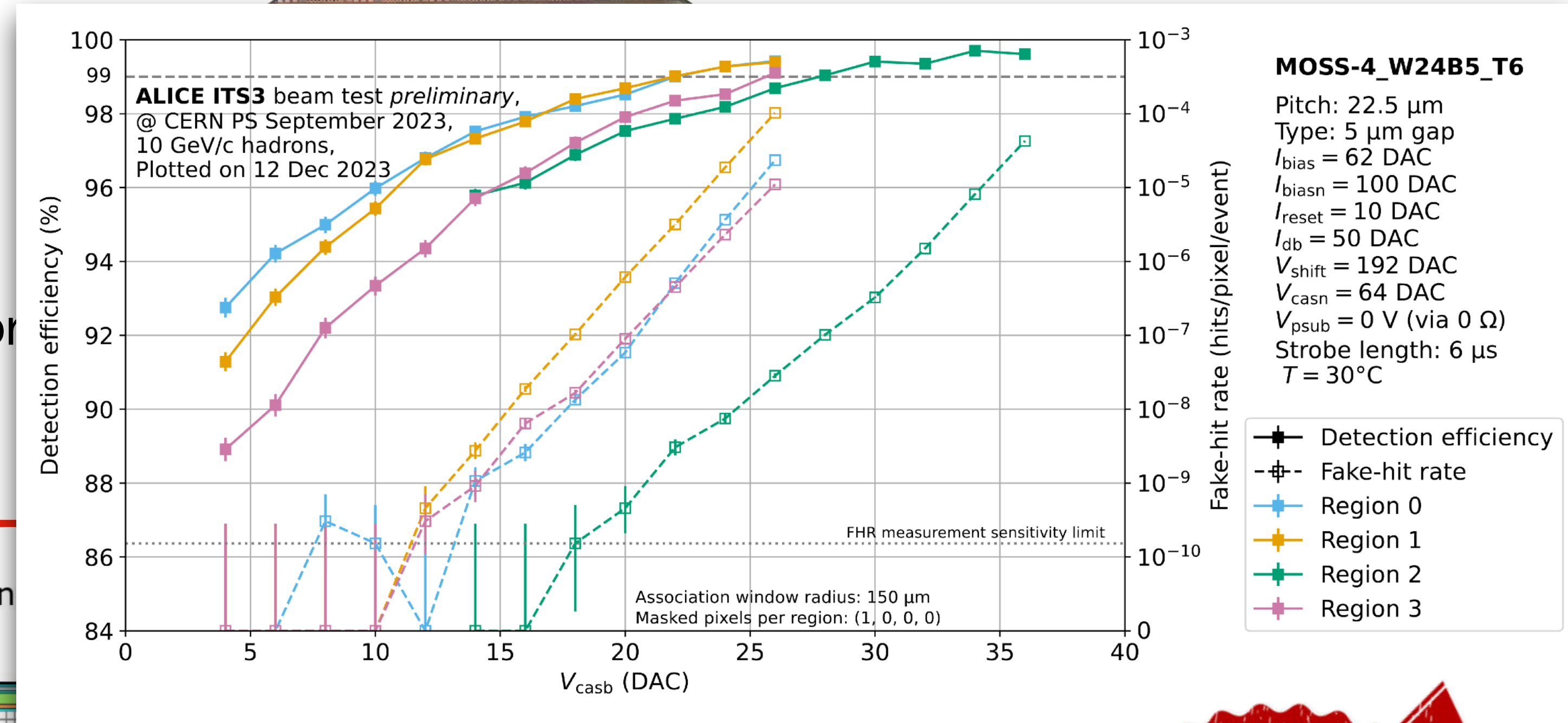
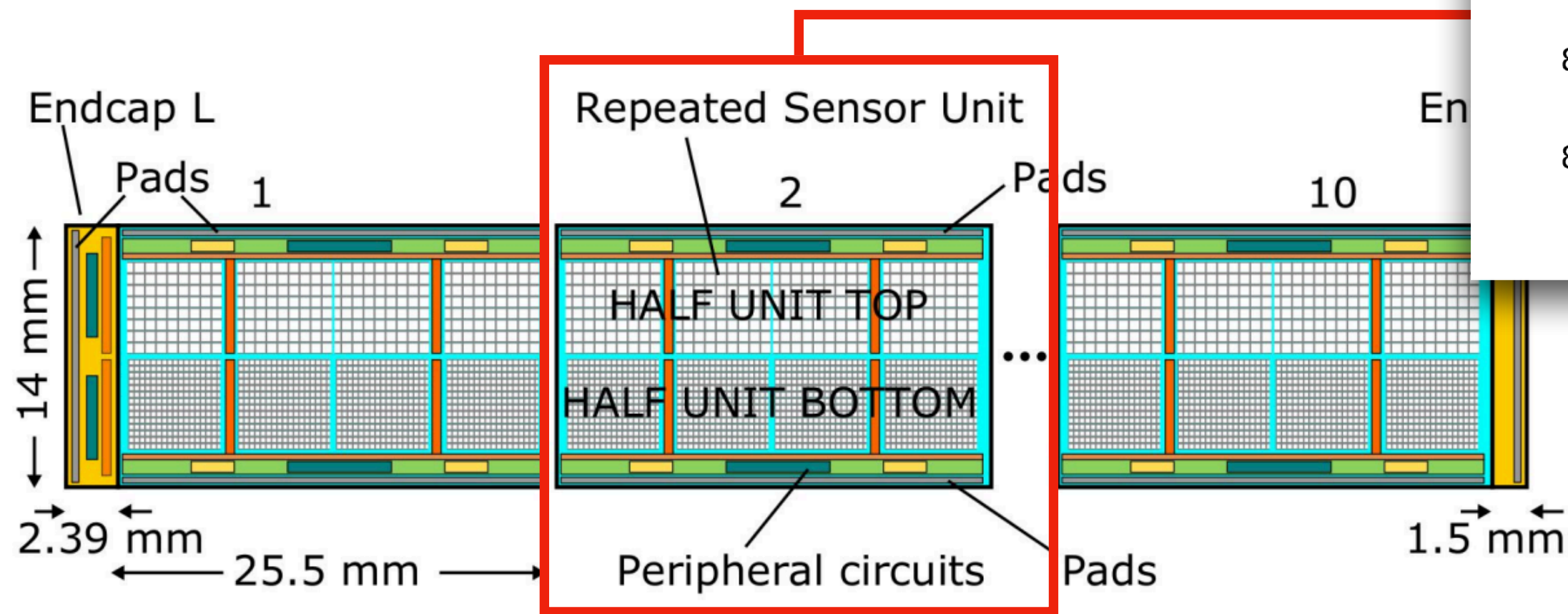
- **MOSS is operational and reaches full efficiency**
 - Yield: currently under study with extensive characterization campaign with wafer prober.
- **First beam tests performed at PS@CERN**
 Detection efficiency: in line with expectations from MLR1 study

ITS design and R&D

Stitched MAPS



- **Goal:** Feasibility of stitching process
- **MO**nolithic **S**titched **S**ensor (**MOSS**):
 - 10 Repeated Sensor Units stitched together: 259 mm x 14 mm per sensor
 - 2 pixel pitches (18 μm and 22.5 μm) and 5 front-end variants



300 mm ER1 wafer

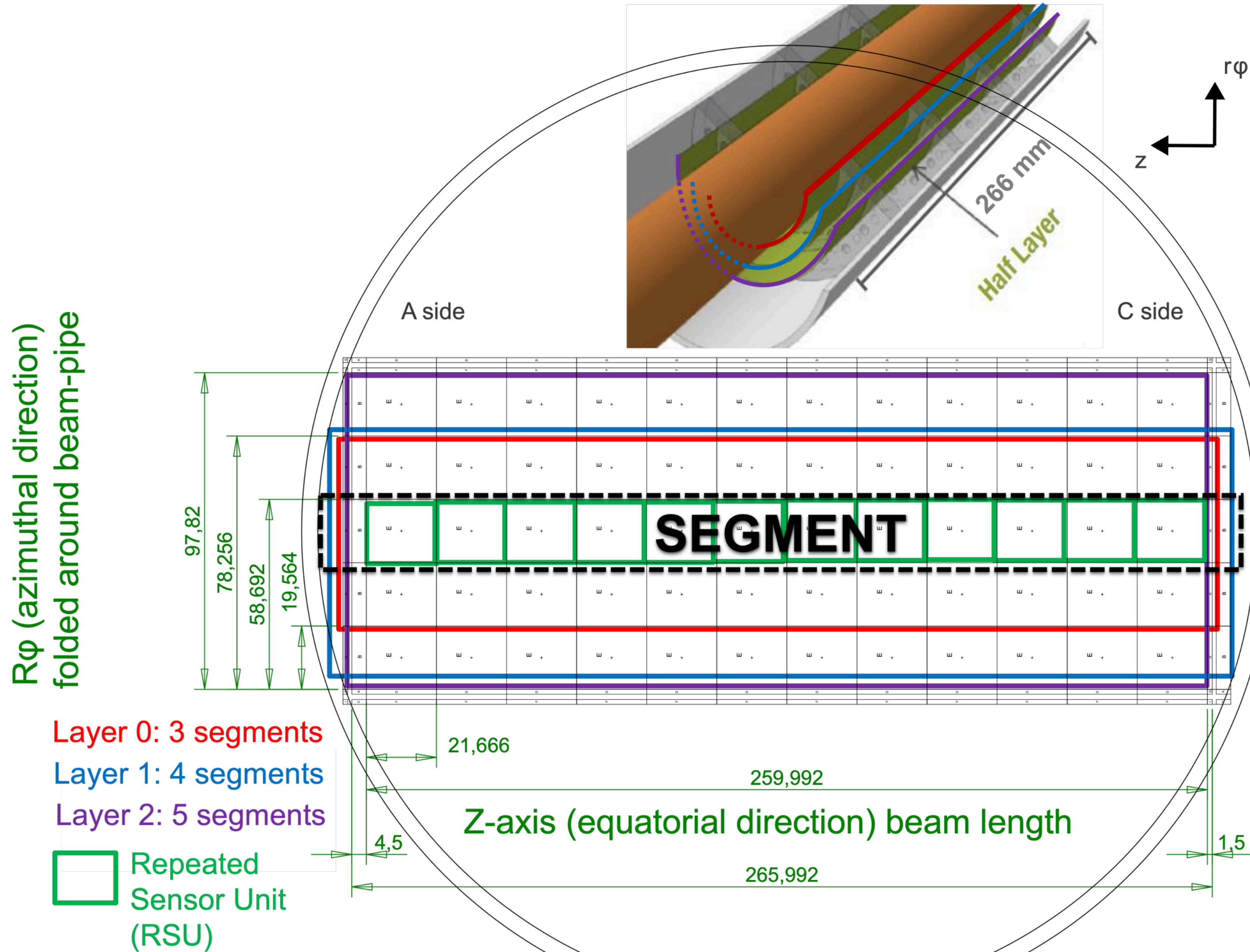
- **MOSS is operational and reaches full efficiency**
 - Yield: currently under study with extended campaign with wafer prober.
 - **First beam tests performed at PS@CERN**
Detection efficiency: in line with expectations study



We can readout the stitched sensor !

Sensor development

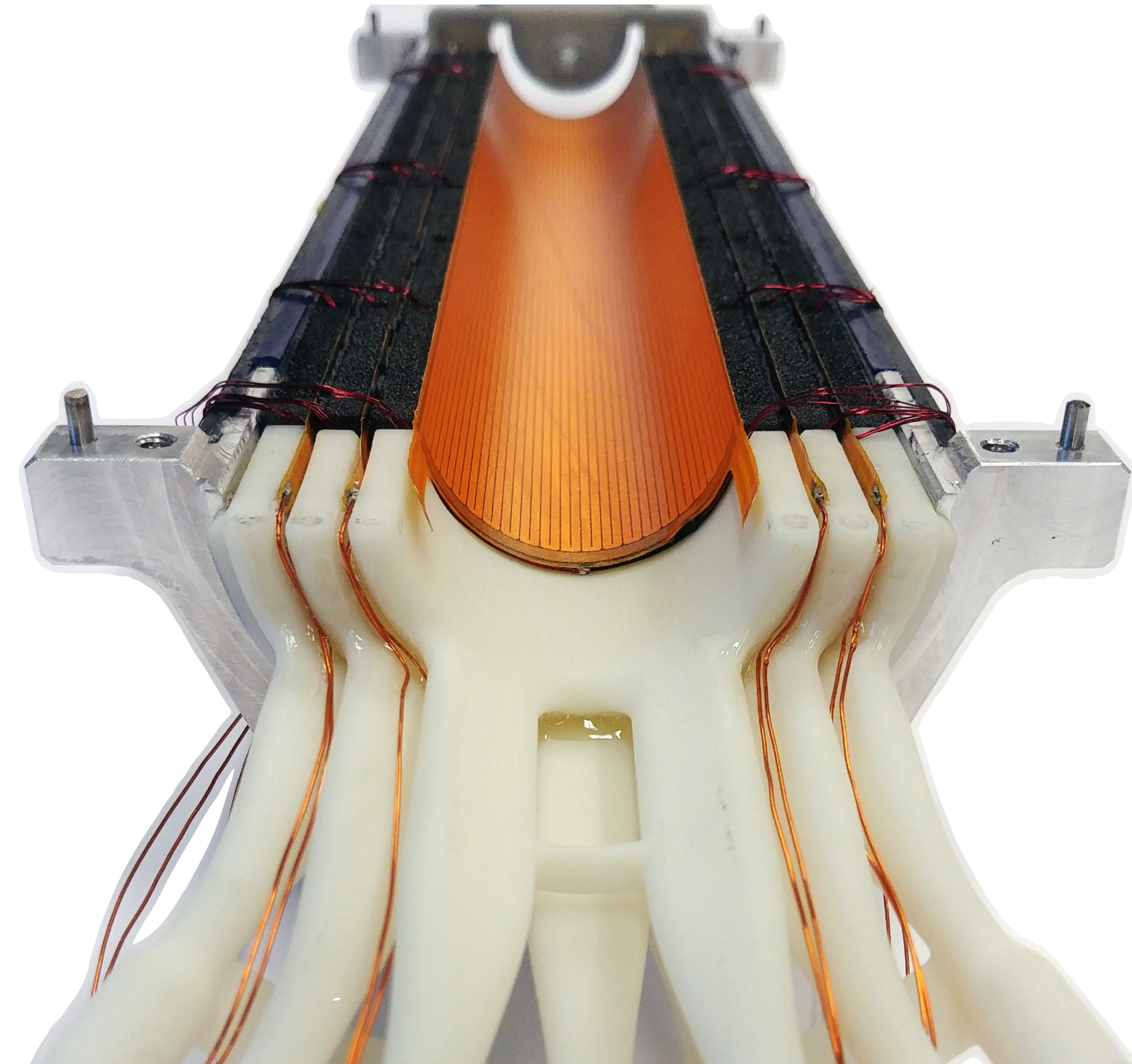
Outlook



- **MOSAIX:** Final size 2D stitched sensor
- **Modular design:** each sensor is divided into 3, 4, or 5 **segments** with 12 RSUs.
- Each RSU is divided in turn in 12 fully independent tiles (powering, control and readout)
- **Currently working to submission !**

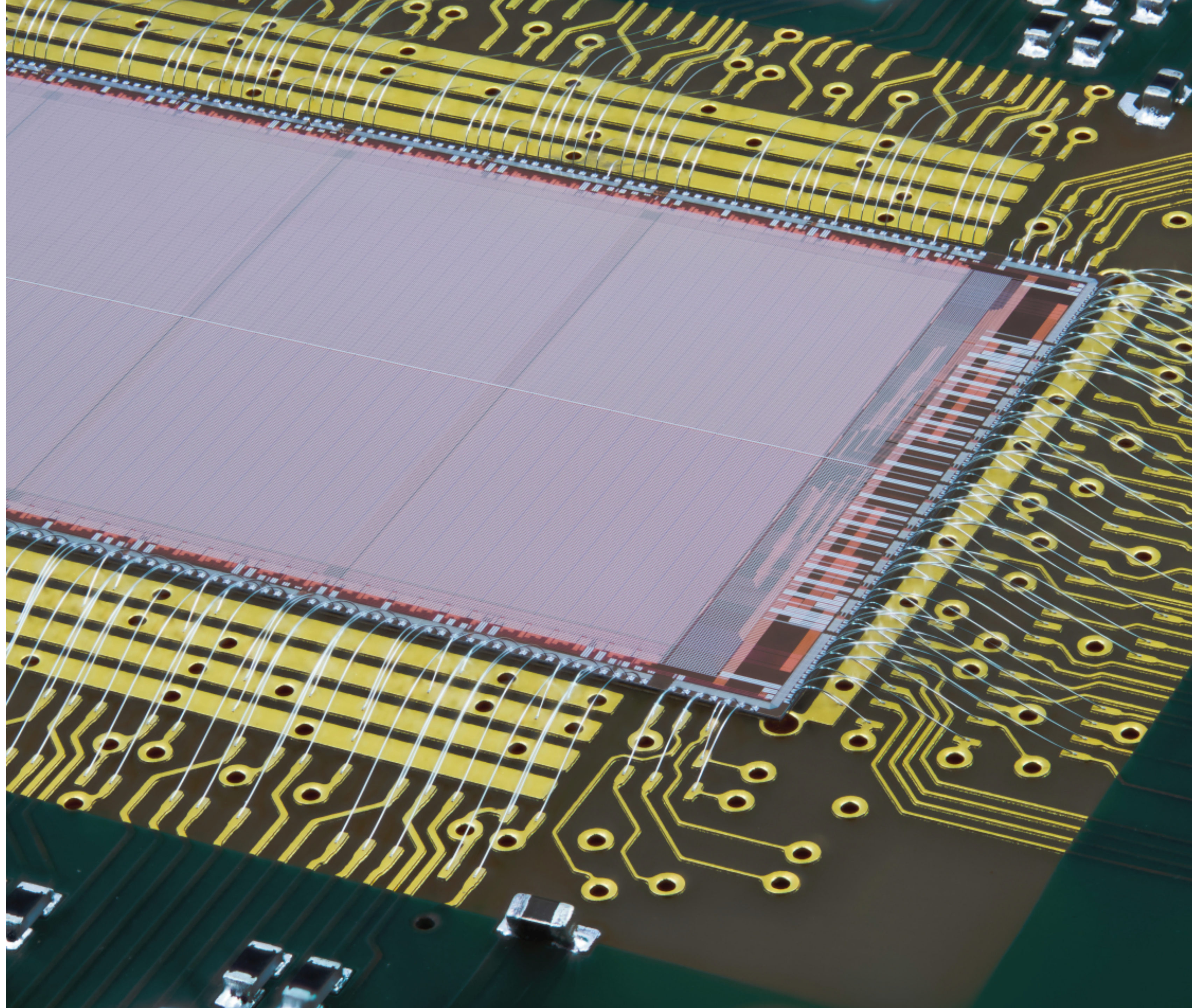
Summary

- **ALICE is preparing the new ITS upgrade:**
Truly cylindrical wafer-scale MAPS
- **ITS3 key R&D questions answered:**
 - Can we bent it?
→ Bent MAPS demonstrated in beam
 - Can we cool it down?
Can it withstand vibration from cooling?
→ Air cooling tested with aeroelastic
 - Can we use 65 nm technology?
→ 65nm process qualified with radiation
 - Can we do the stitching?
→ Stitching (MOSS) qualified
- **Next steps:**
 - Finalisation of the design and production of final prototype sensor (ER2)
- **ALICE ITS3 on track for installation in LS3 (2026-2028)**



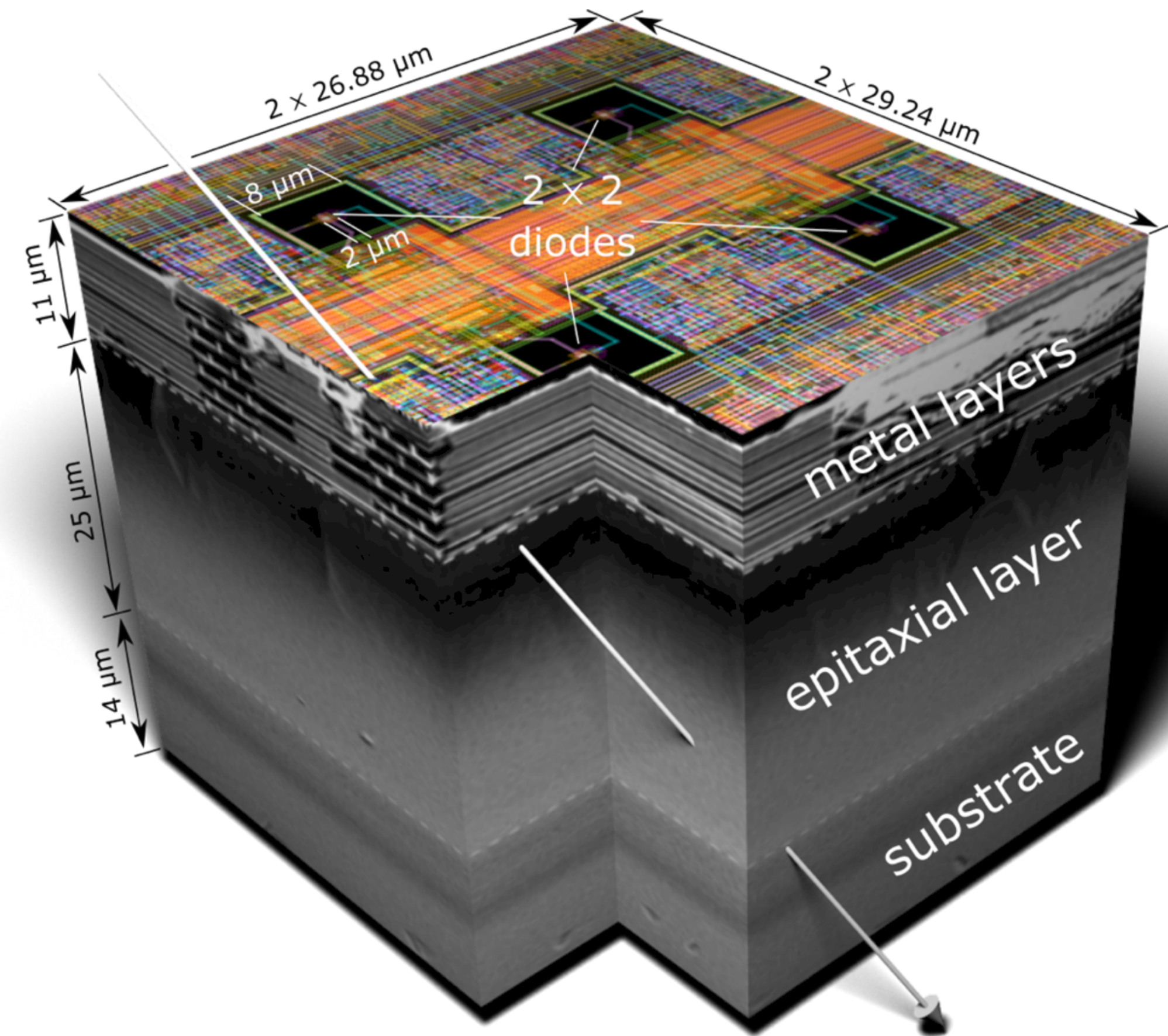
ITS3 "bread board" model 3

Back up

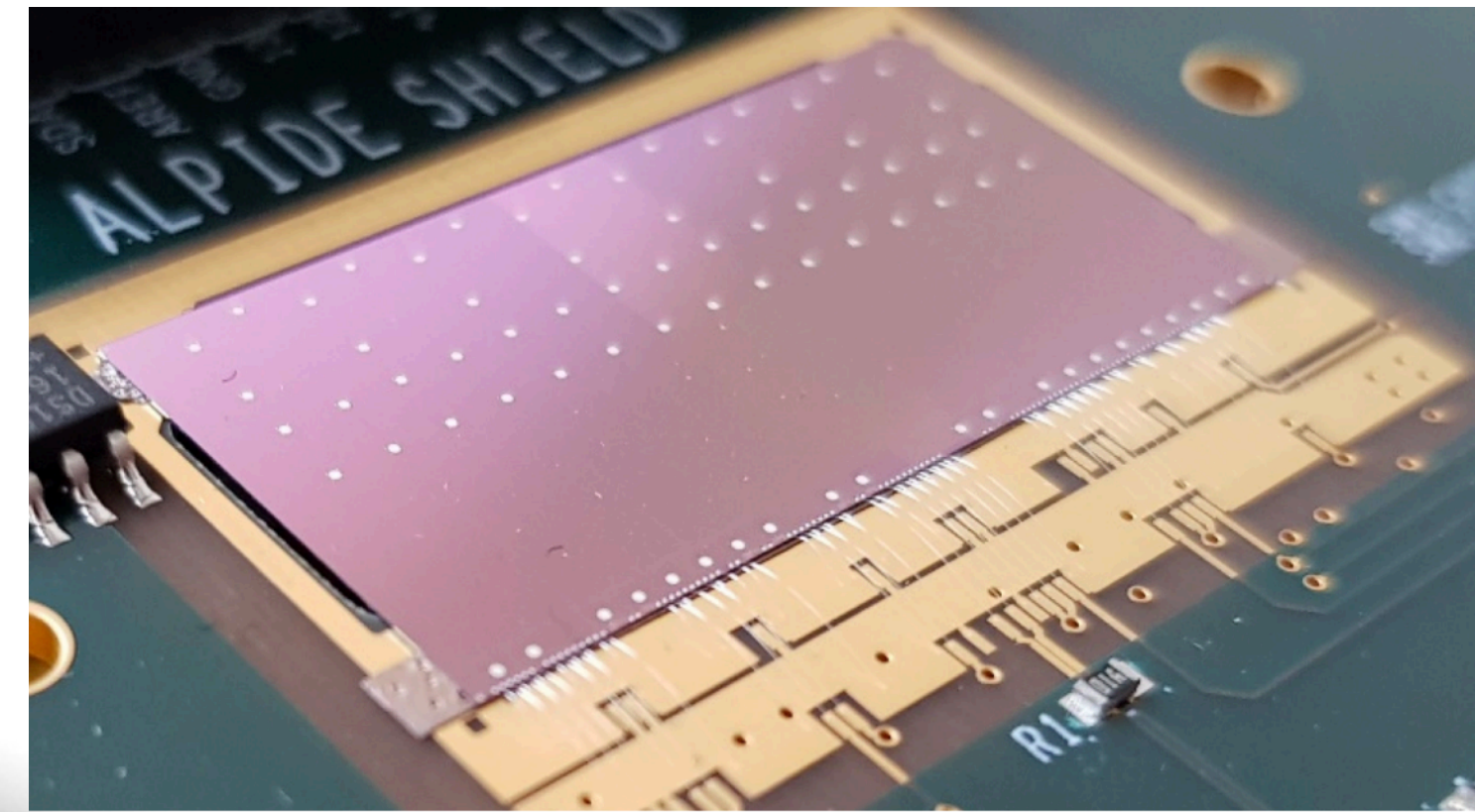


Monolithic Active Pixel Sensor (MAPS)

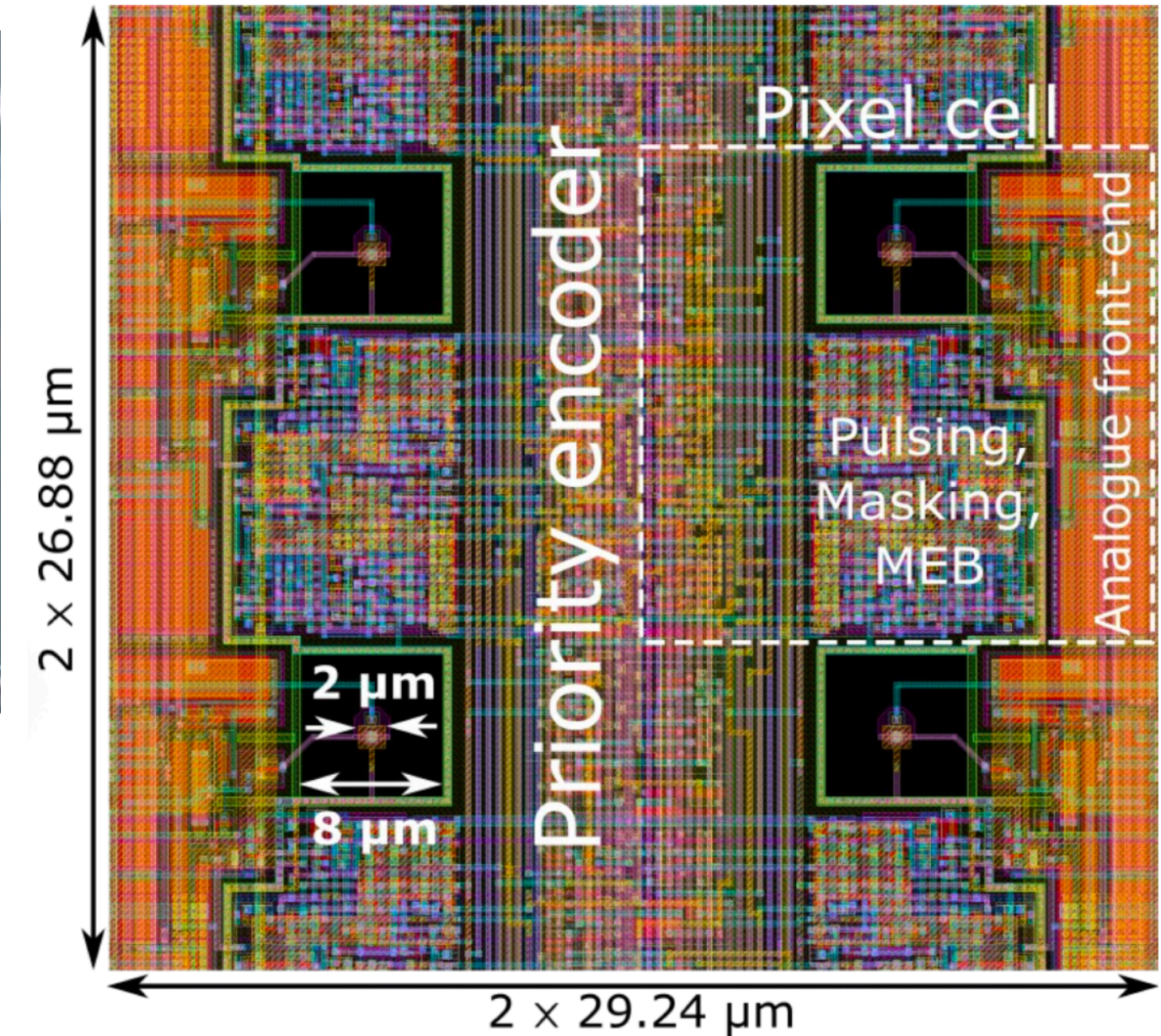
CMOS MAPS



ALPIDE (MAPS)



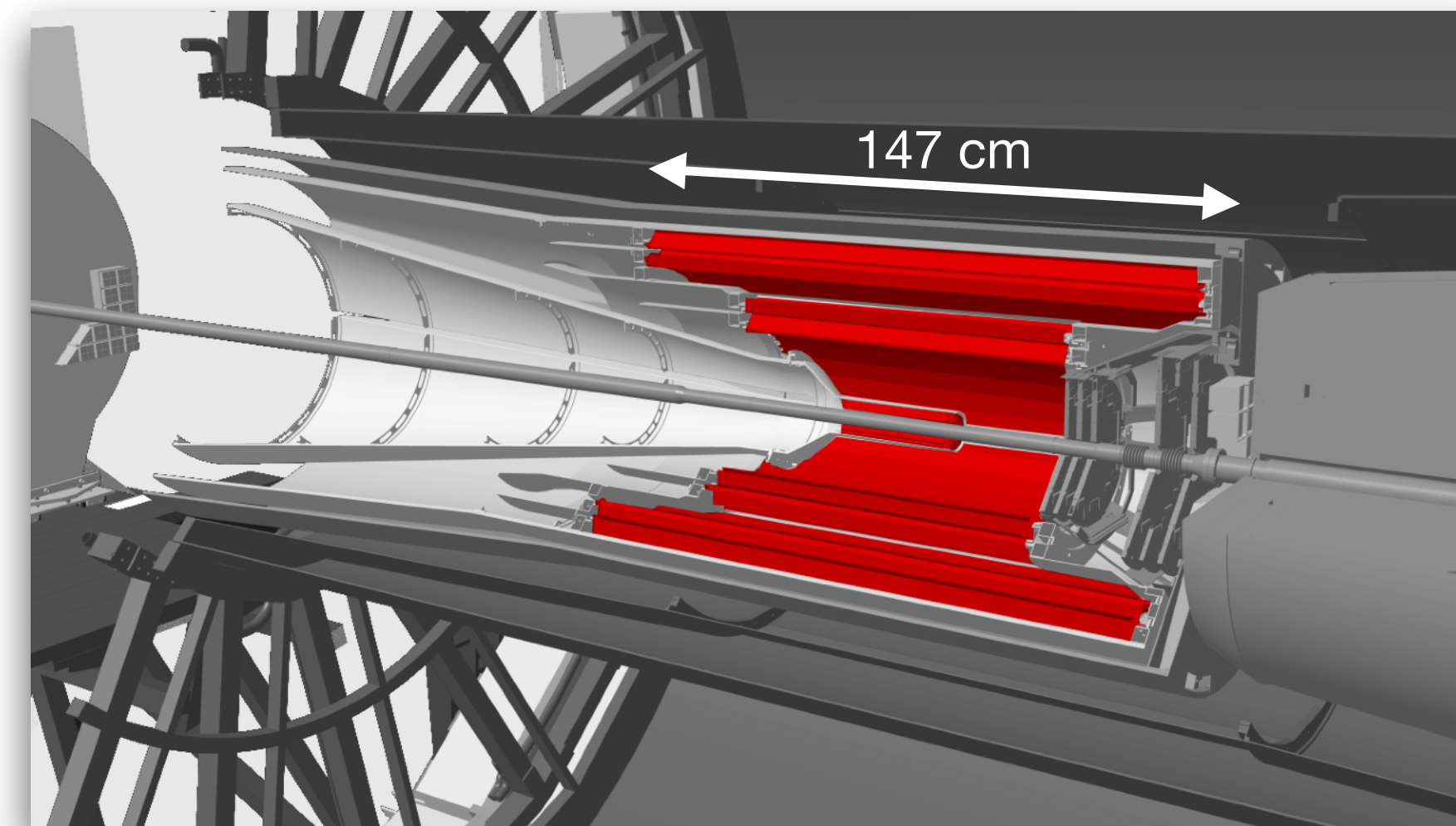
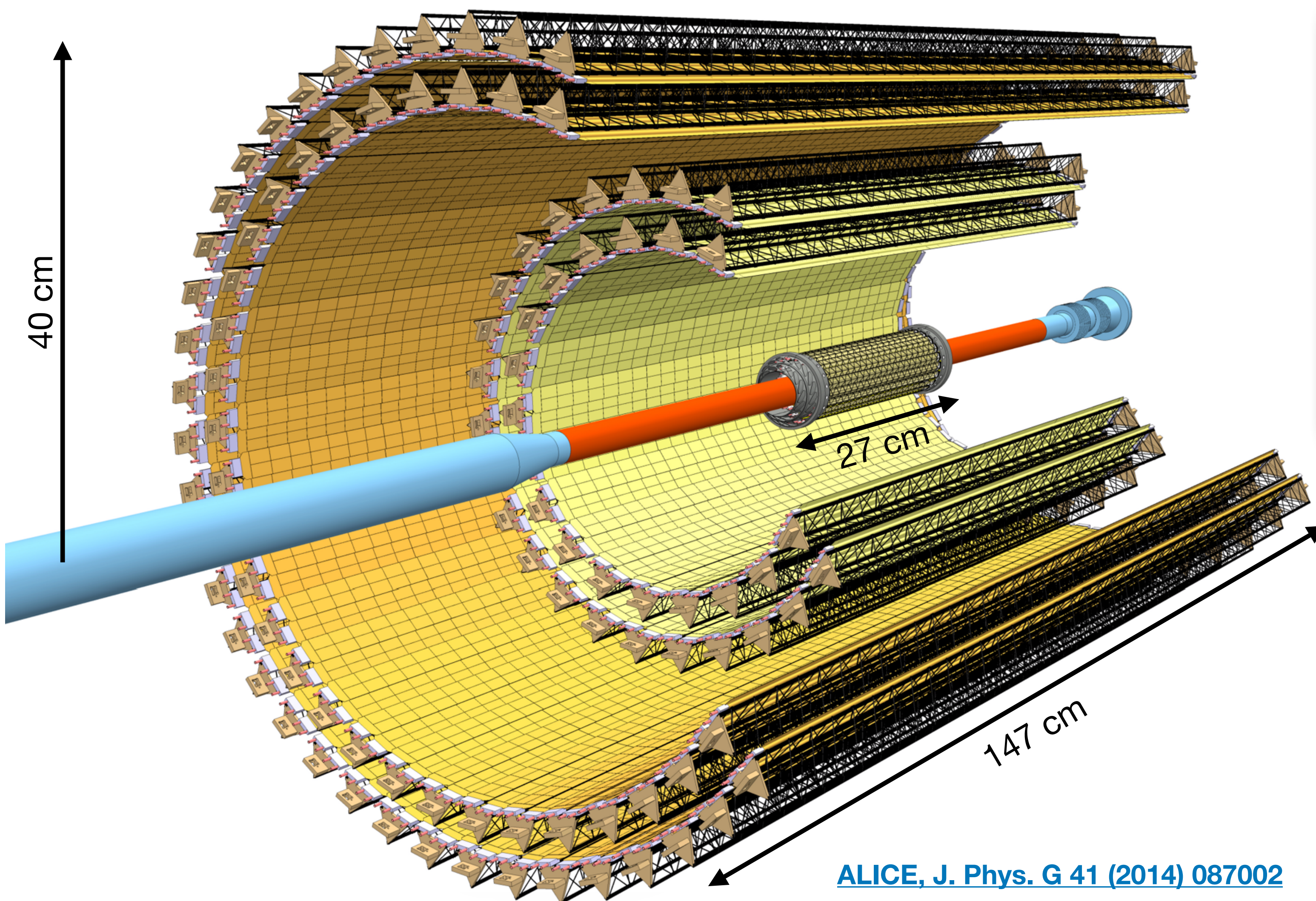
ALPIDE chip



Layout of 4 pixels

- **Single silicon chip** contains both **the detection volume and the readout electronics**
 - as opposed to hybrid pixel sensors, which use two chips that need to be interconnected
- 180 nm CMOS imaging process by TowerJazz
- 3 cm x 1.5 cm (1024 x 512 pixels) with thickness 50 μm for IB
- Size of pixel pitch: 29 μm x 27 μm

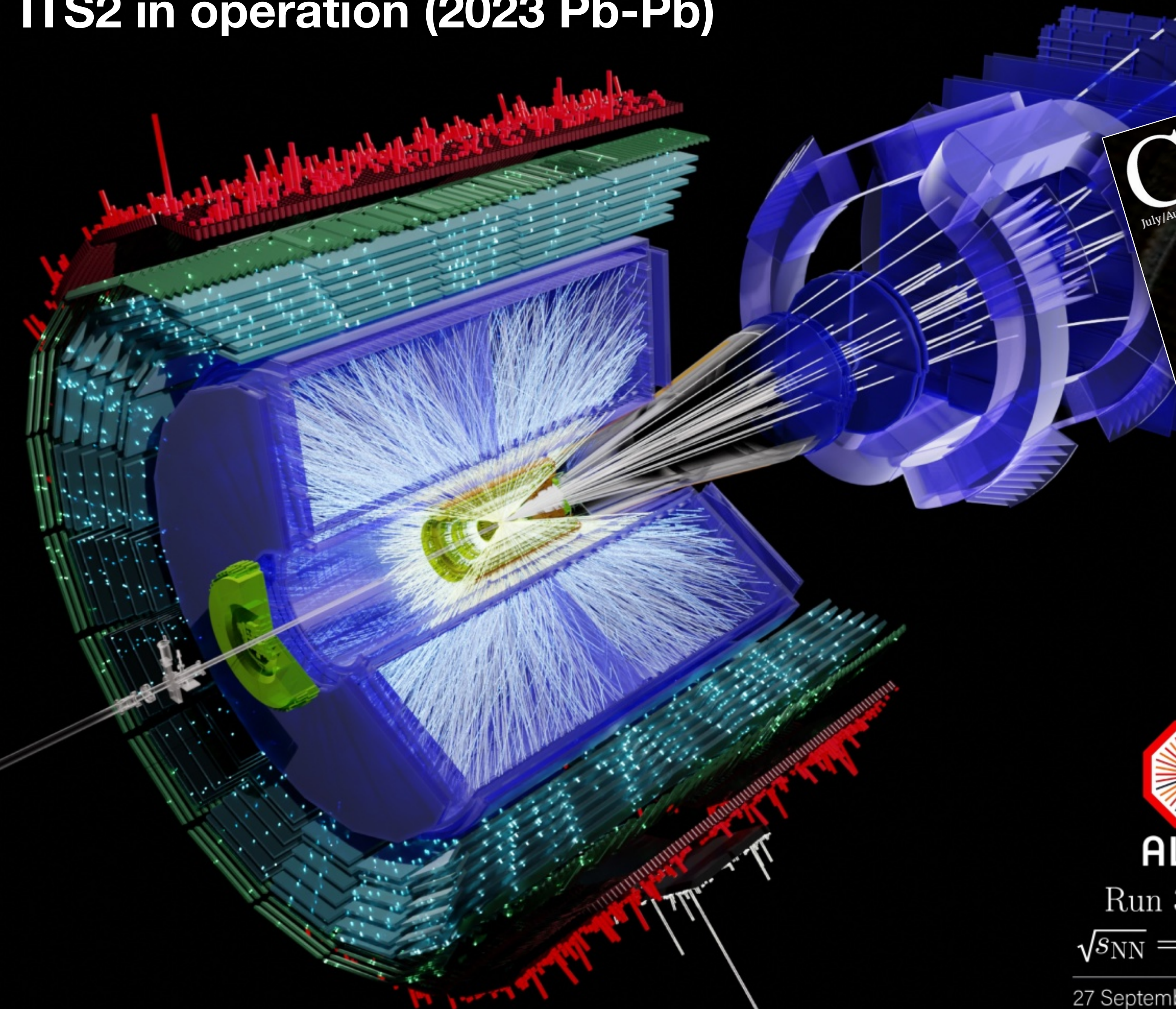
ITS; Inner Tracking System



- **7 layers** as barrel structure
- New ITS2 for ongoing Run3, fully operational (installed 2021, LHC LS2)
- **Largest MAPS** and pixel detector ever built
 - ~10 m², 24k chips, 12.5 Giga-pixels
- Fast readout rate: **100 kHz (Pb-Pb)**

[ALICE, J. Phys. G 41 \(2014\) 087002](#)

ITS2 in operation (2023 Pb-Pb)



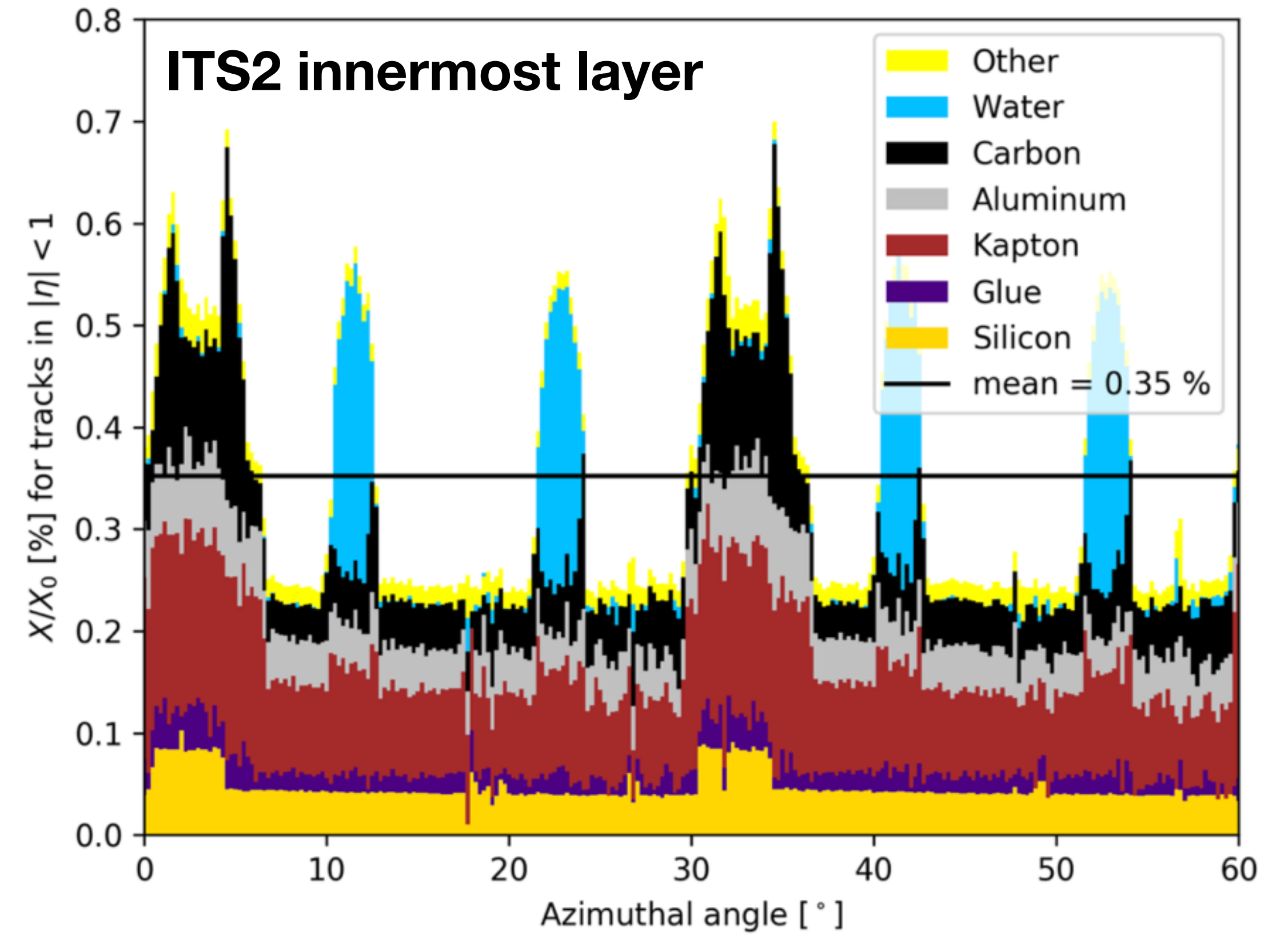
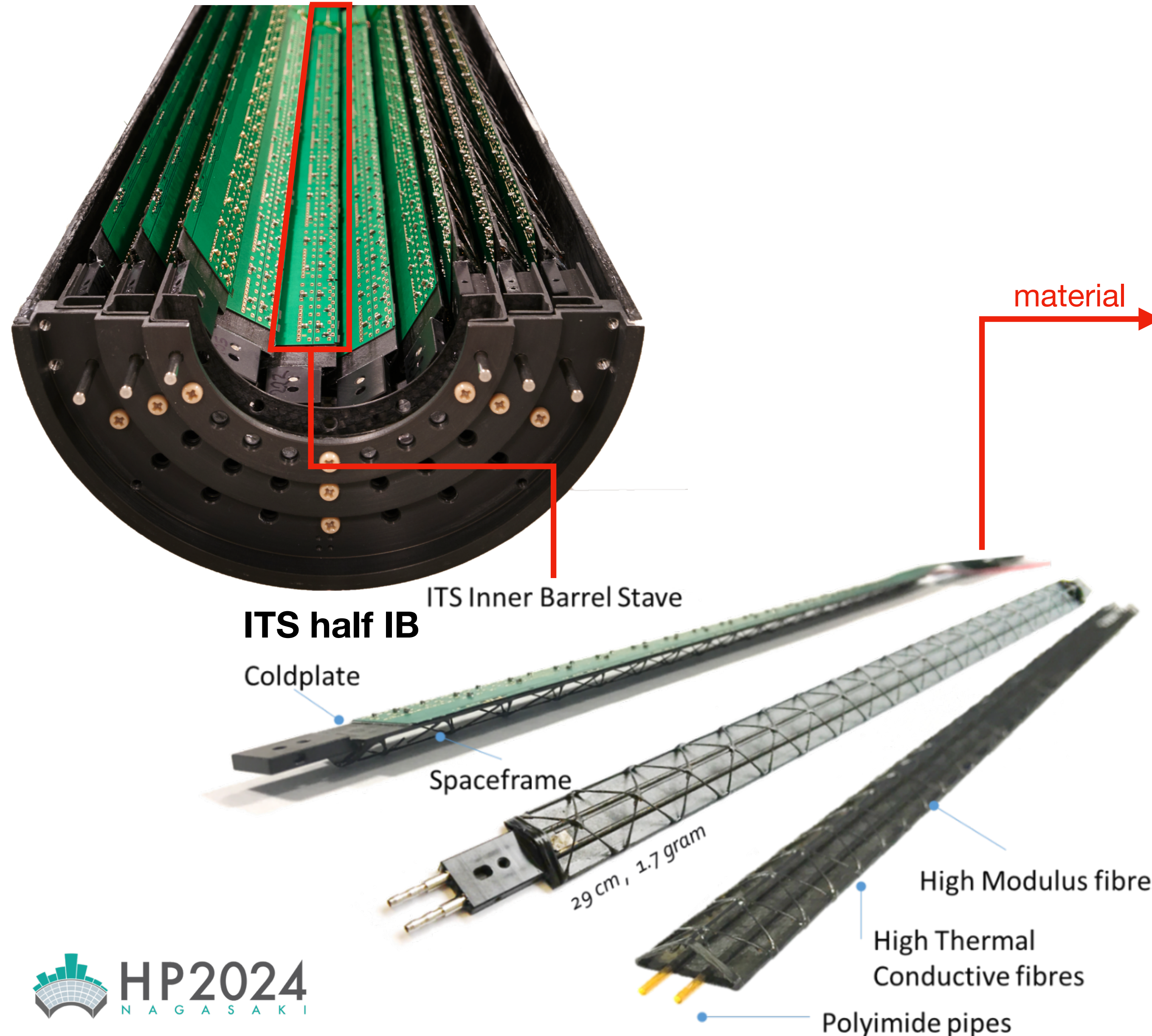
ALICE

Run 3 Pb-Pb
 $\sqrt{s_{NN}} = 5.36$ TeV

27 September 2023, 04:50

What can we achieve?

Observation on the current ITS

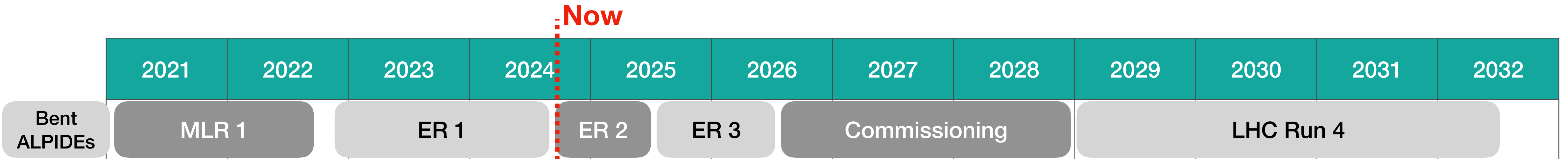


- **ITS2 IB one layer material budget**

- **Silicon** makes only ~15% of the material.
- Irregularities: support structures, cooling, and overlaps

ITS3 upgrade project

Milestones of prototype sensor submission



- **Tower Partners Semiconductor (TPSCo) 65 nm CMOS Imaging Technology:**

- Smaller transistors: higher integration density
- Lower power consumption
- Larger wafers 300 mm

- **MLR 1 tape out (2020-12):**

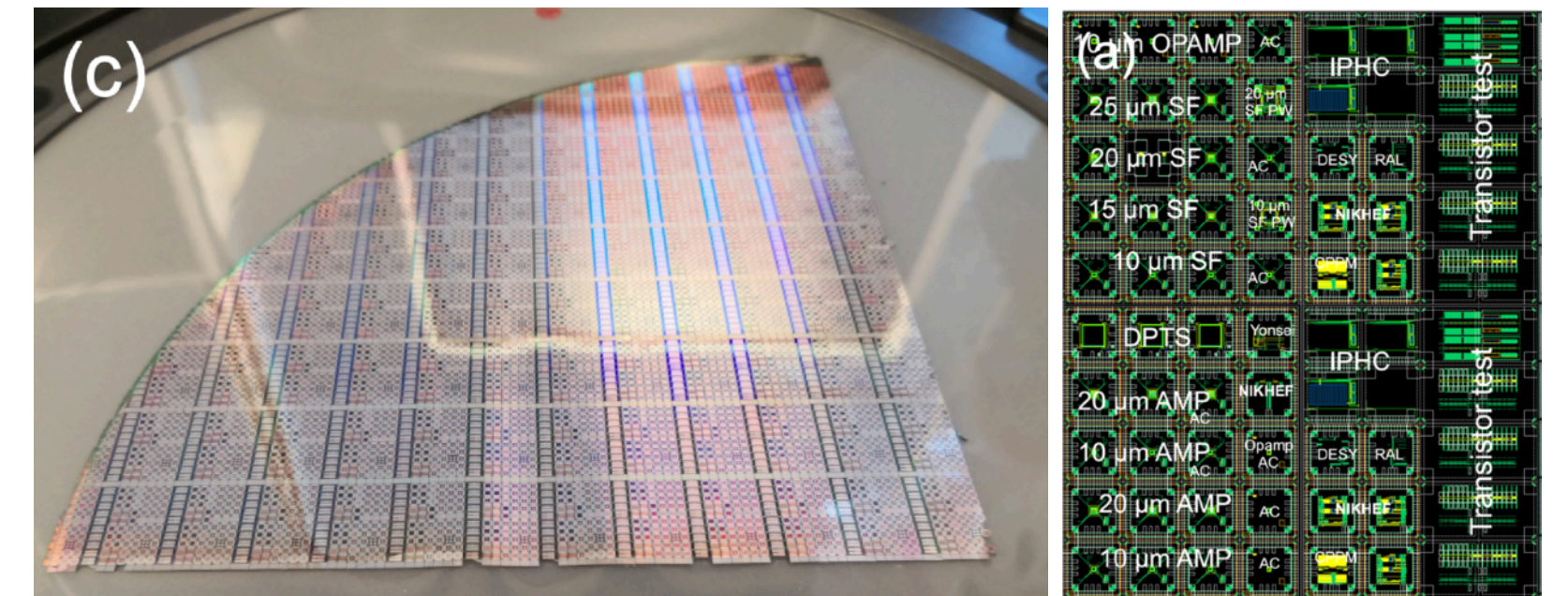
Qualify the 65 nm process MAPS with 3 prototypes: APTS, CE65, DPTS

- **ER1 tape out (2022-11):**

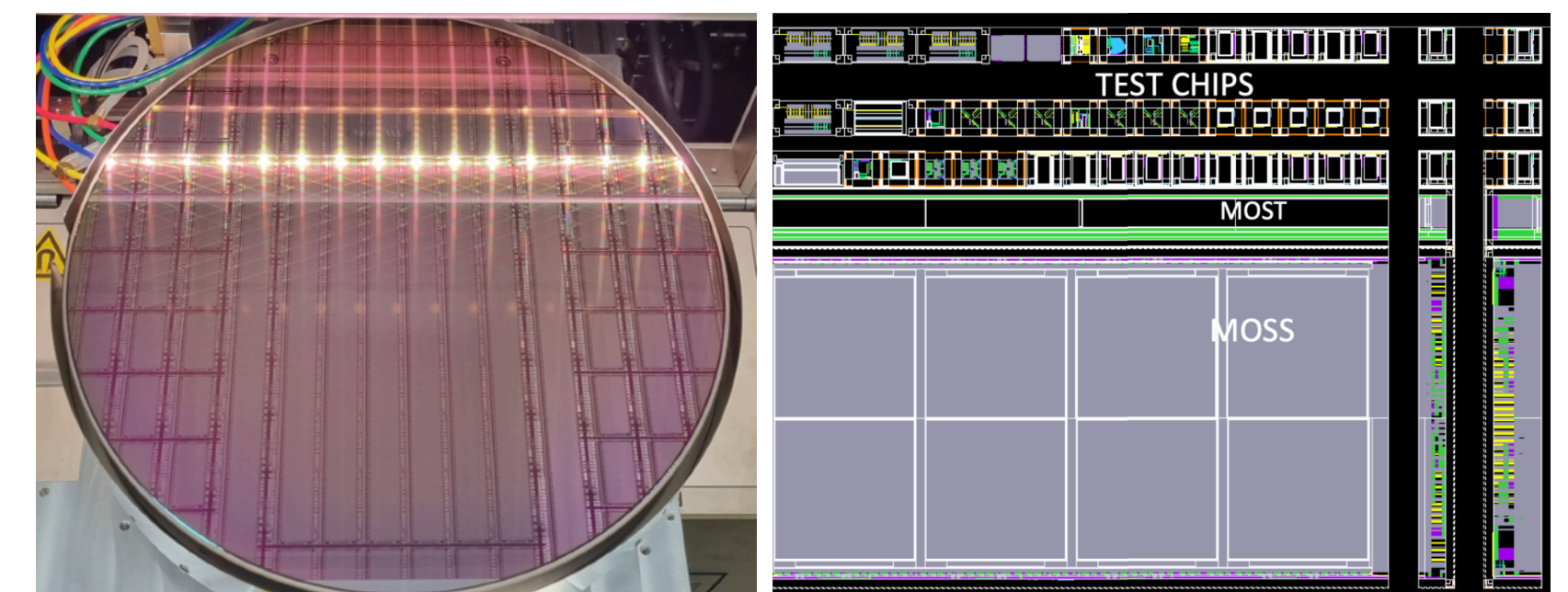
Stitching 1D (+ assess yields by the foundry) with 2 large sensors: MOSS, MOST

- **ER2 tape out (2024-fall):** ITS3 full-size prototype with full functionalities (power, readout, etc)

- **ER3 tape out (2025-middle):** ITS3 sensor production



MLR1 wafer (1/4) and layout



ER1 wafer and layout

ITS design and R&D

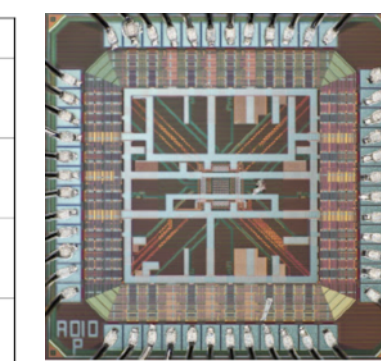
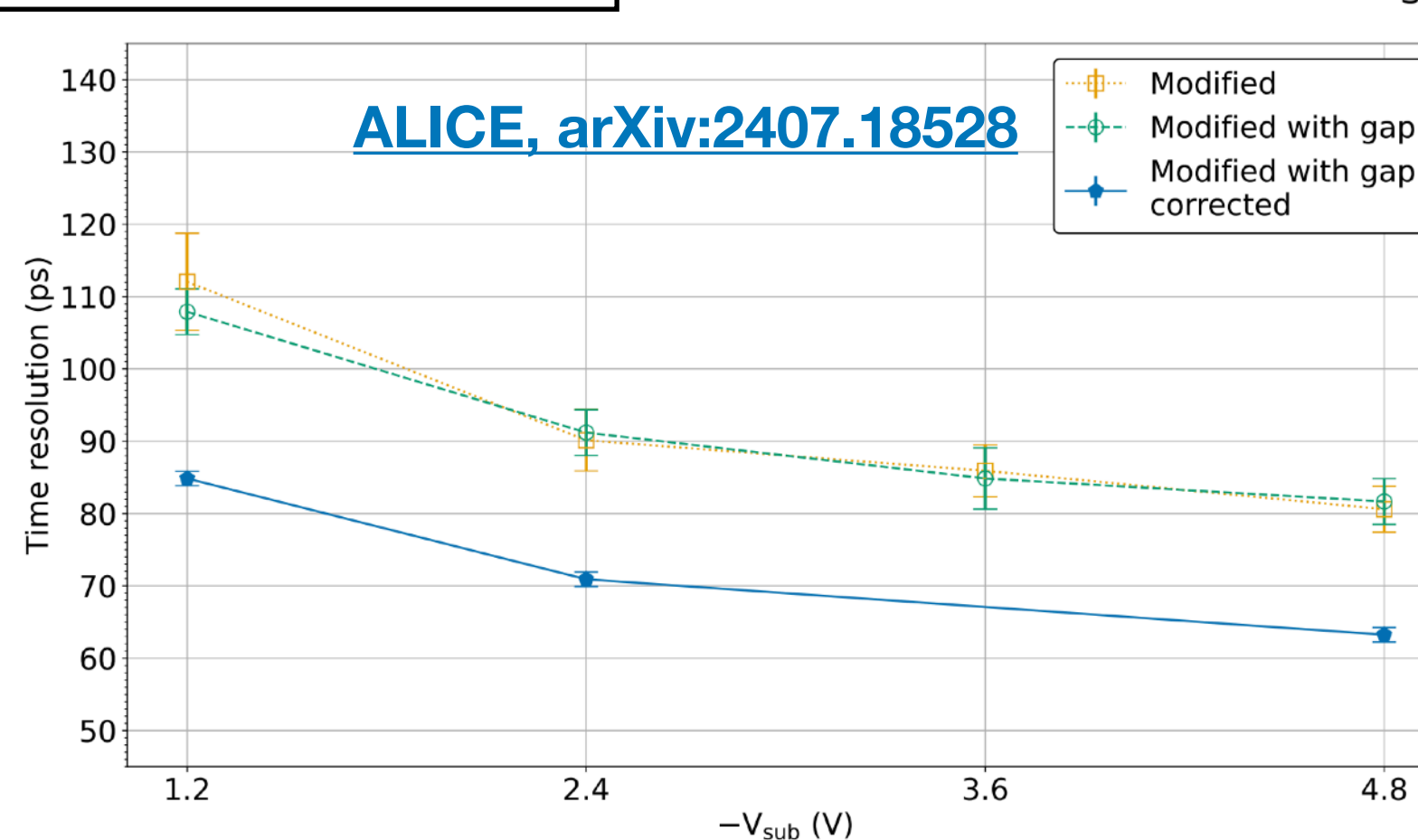
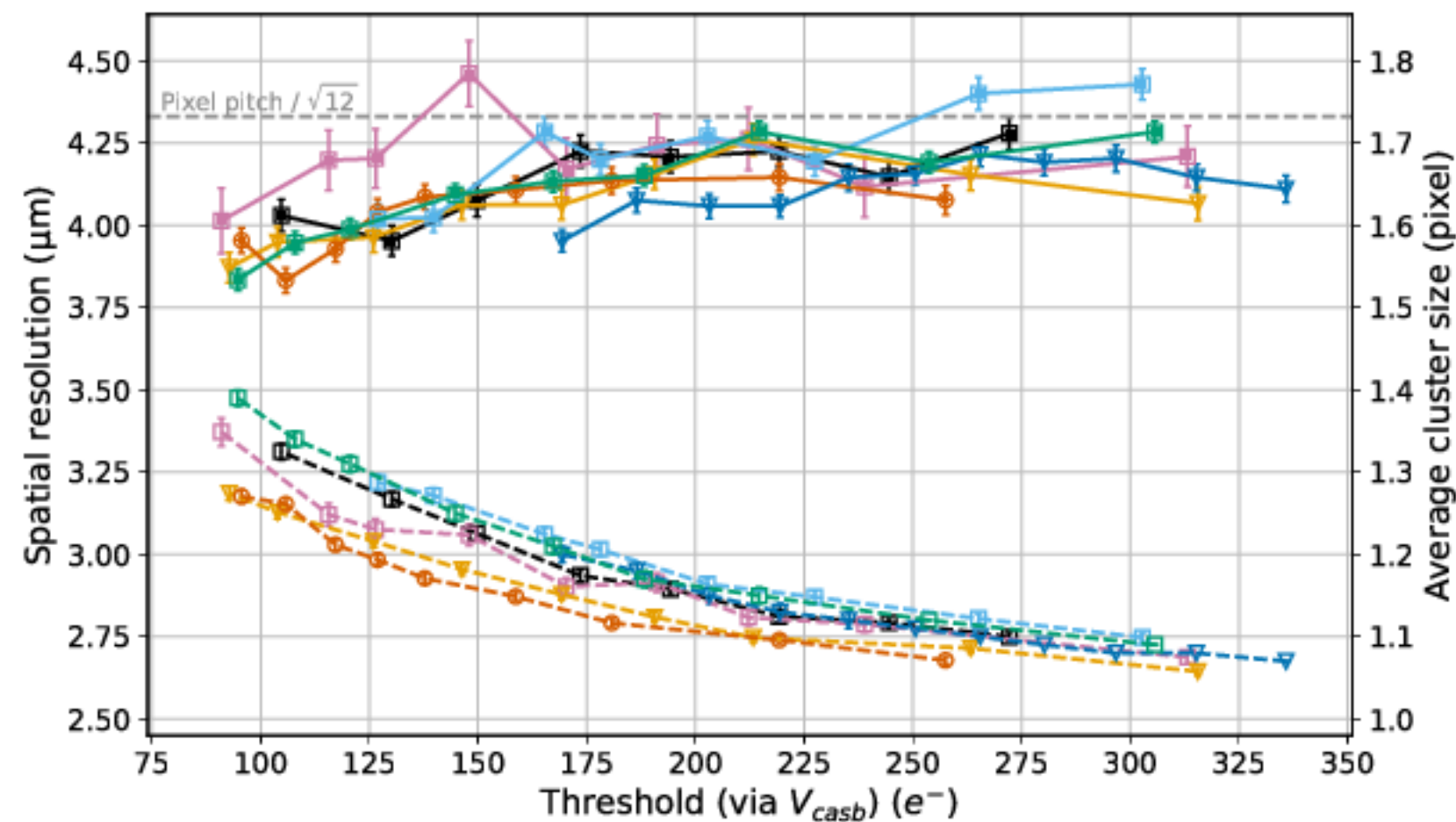
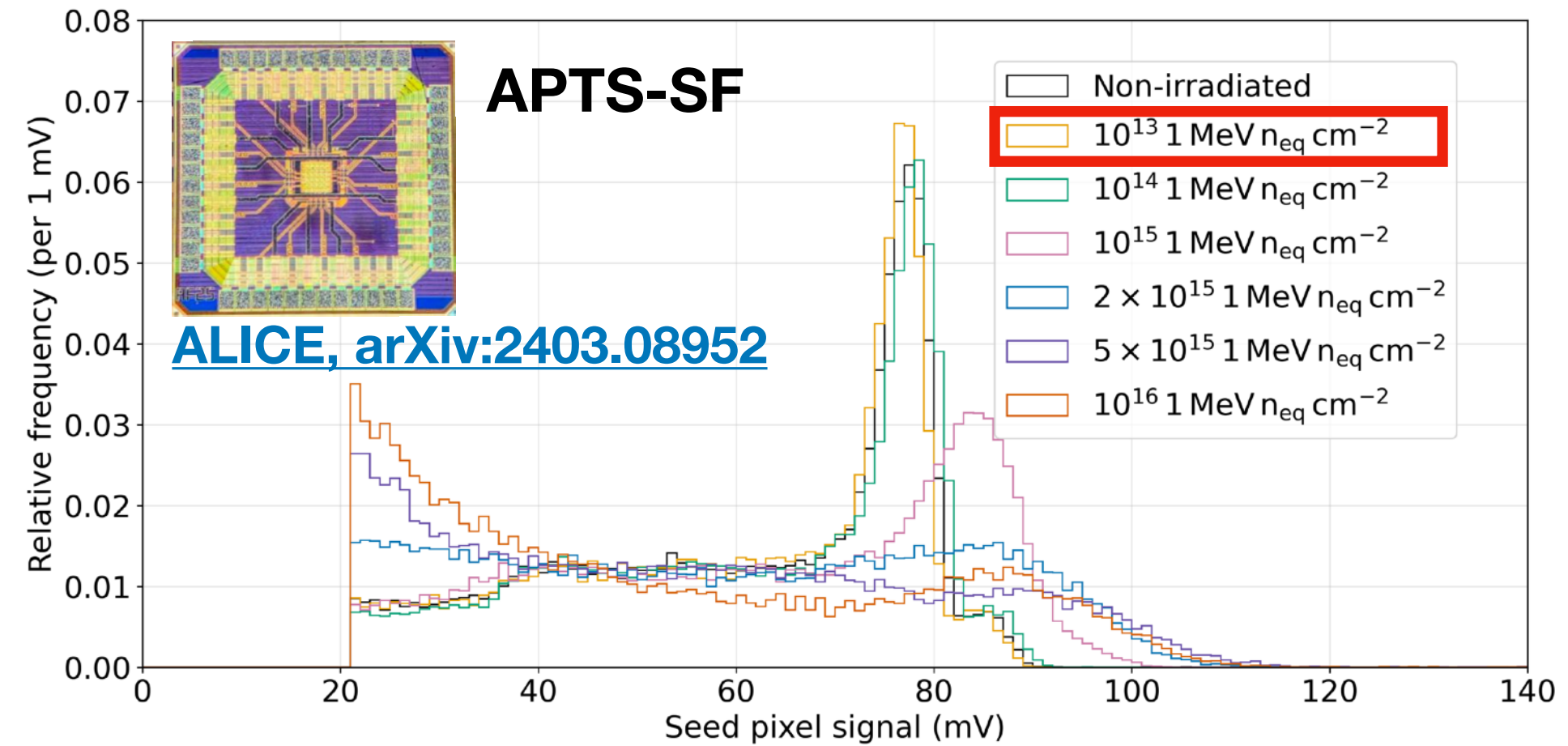
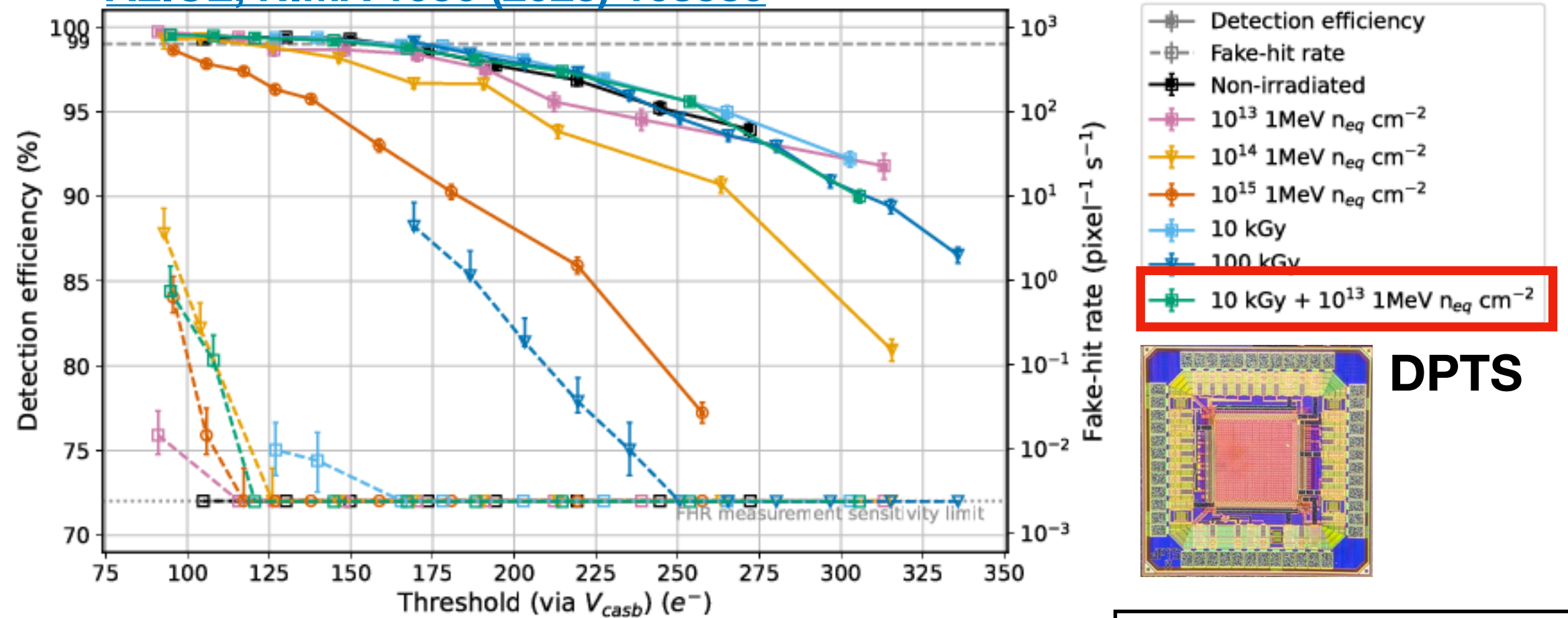
Qualification of 65nm CMOS: MLR1



- Concentrated effort **ALICE ITS3** together with **CERN EP R&D**
- **Prototype sensors: APTS, CE65, DPTS**

Irradiation ITS3 requirements

ALICE, NIMA 1056 (2023) 168589



- **DPTS:**
 - Efficiency (>99%) and spatial resolution (< 5μm) matches **ITS3 requirements**
 - matrix power consumption 40mW/cm²
- **APTS:**
 - **SF:** Charge collection not deteriorated by irradiation
 - **OA:** Sensor time resolution ≤ 70 ps