

### Daiki Hayakawa (Chiba University) on behalf of the FASER collaboration









### Introduction

**Energetic light particles are** produced in the far-forward direction ν<sub>e</sub> , ν<sub>μ</sub> , ν<sub>τ</sub> , π, Κ, D, ...



There is a rich and unexplored physics program in the far forward direction!



### The existing collider detectors (e.g. ATLAS) were designed to find <u>strongly interacting heavy particles</u> SUSY, top, Higgs, ...









- Large Hadron Collider (LHC): 27 km ring collider, 13.6 TeV proton-proton collisions
- Energetic particles ( $\pi$ , K, D, etc) produced in the far-forward direction of the collisions
- **FASER**(ForwArd Search ExpeRiment) is a new experiment at the LHC to search for long-lived BSM particles (dark photon, axion-like-particles (ALPs)) and study **TeV neutrinos**



### **FASER Detector**



2 tungsten layers (2 X<sub>0</sub>) + 2 graphite layers + 2 scintillators

### arXiv:2207.11427

Scintillators for veto, trigger, and preshower (particle ID)



## **Results from FASER**



A. Ariga, Moriond EW 2024





## **Desired Detection Capabilities**









3 ab-	-1
90 fb	-1
$\delta_{\gamma\gamma} \ge$	<u>200 µm</u>
$\delta_{\gamma\gamma} \ge$	<u>*</u> 300 µm
$\delta_{\gamma\gamma} \ge$	<u>2</u> 500 μm
$\delta_{\gamma\gamma} \ge$	<u>*</u> 1000 μm

- Resolve diphoton events by upgraded pre-shower calorimeter with high X-Y granularity
  - Improve v BG suppression in the search for ALPs
- The updated detector could also improve the search for dark-photons  $(A' \rightarrow e^+e^-)$  or similar final states



## New Pre-shower Calo metre accommodate





pixel ASICs • total of 432 ASICs, or 11.5M pixels



current preshower detector highlig







### **Detector Module**

6 planes in total (silicon detector + tungsten plate)



Wire bond protection cap

100

75

lity [%]

0

**Module flex Glue interface** Asics

Thermal glue

**Aluminum base** plate

Thermal interface sheet

fithelayout with 12 modules mounted on a cooling plate with an overlap along the des. The cooling lanies of the so period plane, on cooling plate

in an instrumented plane with dimensions and mass. The module consists of l on Figure 13 except the base plate and the thermal interface sheet.



























![](_page_11_Figure_3.jpeg)

![](_page_11_Picture_4.jpeg)

![](_page_12_Picture_0.jpeg)

![](_page_12_Figure_1.jpeg)

![](_page_12_Picture_2.jpeg)

## Simulation: Energy Resolution de GENEVE

![](_page_13_Figure_1.jpeg)

![](_page_13_Picture_2.jpeg)

• For the energy above 100 GeV, which is our primary area of interest, maintaining good energy resolution with preshower (6X<sub>0</sub>) correction

![](_page_13_Picture_4.jpeg)

![](_page_14_Picture_0.jpeg)

## nares-section and CDERGENEV/E

![](_page_14_Figure_2.jpeg)

### $\mathbf{C}_{\text{mem}}$ Pre-amp Discriminator + memory contro

### Monolithic ASIC Specifications

Main specifications		
Pixel Size	65 μm side (hexagonal)	
Pixel dynamic range	0.5 ÷ 65 fC	
Cluster size	O(1000) pixels	
Readout time	< 200 µs	
Power consuption	< 150 mW/cm <sup>2</sup>	
Time resolution	< 300 ps	

Selected technology: SG13G2, by IHP microelectronics.

ASIC design in collaboration between CERN, University of Geneva, and KIT

![](_page_14_Picture_10.jpeg)

![](_page_14_Picture_11.jpeg)

![](_page_14_Figure_12.jpeg)

![](_page_14_Figure_13.jpeg)

![](_page_14_Picture_14.jpeg)

![](_page_15_Picture_0.jpeg)

### More details: <u>C. Magliocca (TREDI2024)</u>

## increasing the size of the preamplifier transistors

![](_page_15_Picture_3.jpeg)

![](_page_15_Figure_4.jpeg)

![](_page_15_Picture_5.jpeg)

400.0

### illustrations of loois – Assembly Stand

![](_page_16_Picture_1.jpeg)

![](_page_16_Picture_2.jpeg)

### Loopback testing board

Module pigtail

# Received post-processed wafers (final chip) in May 2024 Module assembly procedure is finalized Detector assembly and surface commissioning is planned at CERN Experimental Hall North 1 (EHN1)

Figure 21: Left: Front projected CAD view of the preshower detector overlaid with the

### Module assembly tools

![](_page_16_Picture_7.jpeg)

### FPGA BOARD

Function	Status
Power Supplies	<ul> <li>V</li> </ul>
FPGA Programming	<ul> <li></li> </ul>
FPGA Pin Assignment	( 🗸 )
Ethernet	
TLB Signals	<ul> <li></li> </ul>
Adapter Board Connectors	<b>~</b>
ROARDID Rotary Switch	<b>_</b>

### ADAPTER BOARDS

Function	Status
Power Supplies	<b>~</b>
Threshold Voltage Programming	<b>~</b>
Module Connectors	<b>~</b>
Power Supply Connectors	<b>~</b>
MPOD Connector	<b>~</b>
FPGA Board Connector	~
PIM SE Connector	
PIM Diff Connector	
Frame NTC Connector	
Humidity Sensor Connector	

![](_page_16_Picture_12.jpeg)

![](_page_16_Picture_13.jpeg)

![](_page_16_Picture_14.jpeg)

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**FPGA board** 

ASIC 3 Sic

ane layout with 12 modules mound and the composed by six ASICs glued at a second carbon of a module assembly. A module is composed by six ASICs glued to a second by six ASICs glued to a second by six ASICs glued to a second by six and the second by six as a second by second by six as a second by second b

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![](_page_16_Picture_17.jpeg)

![](_page_16_Picture_18.jpeg)

![](_page_16_Picture_19.jpeg)

![](_page_16_Picture_20.jpeg)

![](_page_16_Picture_21.jpeg)

## Summary

- FASER is taking data in the very forward region of the LHC from 2022
- New ALPs limits
  - Observed 1 event in 57.7 fb<sup>-1</sup>, expecting 0.42  $\pm$  0.38 from v CC interactions in pre-shower
- A new pre-shower detector will enable multi-γ tagging and resolve very collimated photon pairs
- Pre-production ASIC extensively tested
- Received post-processed wafers
- Targeting installation in December 2024

![](_page_17_Picture_10.jpeg)

## Collaboration

![](_page_18_Picture_1.jpeg)

![](_page_18_Picture_2.jpeg)

![](_page_18_Picture_3.jpeg)

![](_page_18_Picture_4.jpeg)

![](_page_18_Picture_5.jpeg)

![](_page_18_Picture_6.jpeg)

![](_page_18_Picture_7.jpeg)

![](_page_18_Picture_8.jpeg)

![](_page_18_Picture_9.jpeg)

agreement with CERN

![](_page_18_Picture_11.jpeg)

![](_page_18_Picture_12.jpeg)

![](_page_18_Picture_13.jpeg)

![](_page_18_Picture_14.jpeg)

![](_page_18_Picture_15.jpeg)

![](_page_18_Picture_16.jpeg)

Tsinghua University

![](_page_18_Picture_17.jpeg)

![](_page_18_Picture_18.jpeg)

![](_page_18_Picture_19.jpeg)

The University of Manchester

![](_page_18_Picture_21.jpeg)

![](_page_19_Picture_0.jpeg)

![](_page_19_Picture_2.jpeg)

### September 2022: CERN SPS Test Beam (20-150 GeV e-)

![](_page_20_Figure_1.jpeg)

**Stefano Zambito** | *Université de Genève* 

![](_page_20_Picture_3.jpeg)

![](_page_20_Picture_11.jpeg)

## **Forward Physics Facility (FPF)**

- FPF is a proposal to create a new facility ~650 m away on the LOS for HL-LHC era • At the moment 5 proposed experiments to be situated in the FPF

![](_page_21_Figure_3.jpeg)

### FPF White Paper (2022/3) http://arxiv.org/abs/2203.05090

![](_page_21_Picture_5.jpeg)

![](_page_21_Picture_6.jpeg)

## **Neutrino Background**

![](_page_22_Figure_1.jpeg)

- Evaluated with MC Simulations and validated in
- Expecting 0.42  $\pm$  0.38 from v CC interactions in

![](_page_22_Picture_6.jpeg)

![](_page_22_Picture_7.jpeg)

![](_page_23_Figure_0.jpeg)

m<sub>a</sub> [GeV]

![](_page_23_Picture_2.jpeg)

## Event Display of "ALPtrino"

![](_page_24_Figure_1.jpeg)

## **Dark Photon**

![](_page_25_Figure_1.jpeg)

![](_page_25_Figure_2.jpeg)

### Physics Letters B 848 (2024) 138378

 $A' \rightarrow e+e-$ 

![](_page_25_Figure_6.jpeg)

![](_page_25_Picture_7.jpeg)

![](_page_25_Picture_8.jpeg)

![](_page_26_Picture_0.jpeg)

### Modular Architecture

![](_page_26_Picture_2.jpeg)

- Chip size: 2.2 x 1.5 cm<sup>2</sup> with ulletmatrix of 208x128 pixels (26'624 pixels in total)
- 13 Supercolumns (SC) ullet
- Each Supercolumn has 8 • **Superpixels** (SP) (16x16 pixels)
- and 1 **Digital Line** (40 µm)  $\bullet$
- **Periphery** (I/O and arbitrary logic) with dead area
  - 720 µm on the readout side
  - 270 µm for the guard ring

![](_page_26_Picture_10.jpeg)

### 20.02.2024

Chiara Magliocca | TREDI 2024

![](_page_26_Picture_15.jpeg)

![](_page_26_Picture_20.jpeg)

11

![](_page_27_Picture_0.jpeg)

### **Pixel Circuitry**

![](_page_27_Figure_6.jpeg)

![](_page_27_Picture_7.jpeg)

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![](_page_27_Figure_11.jpeg)

![](_page_27_Picture_12.jpeg)

![](_page_28_Picture_0.jpeg)

ulletconsidering the response of each pixel

![](_page_28_Figure_2.jpeg)

### 20.02.2024

Goal of the charge calibration: from the digitized data information, reconstruct the charge the particle deposited in each pixel,

![](_page_28_Picture_8.jpeg)

### **Monolithic Pixel ASIC: Sensor**

- VDD 000 000 - VDD 000 - VDD 000 → VDD 000 -• VDD 000 - VDD 000 → VDD 110 - VDD
- High resistivity substrate as active 2. volume. Depletion: 50 µm

CMOS die

μm

thinned to 130

1.

Electronics inside the guard-ring, 3. isolated from substrate using deep nwell.

Digital electronics can be placed in pixel or in a 7. separate deep-nwell to improve noise robustness. >95% fill factor.

![](_page_29_Picture_6.jpeg)

Analogue electronics in pixel.

Pixel and electronic deep nwells are kept at positive low voltage.

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### **Super-pixel Architecture**

![](_page_30_Figure_1.jpeg)

![](_page_30_Picture_2.jpeg)

![](_page_30_Picture_3.jpeg)

Charge needs to be measured for each pixel: acts as an imaging device.

Data is stored on the capacitor in each pixel and

converted on the fly with a **flash ADC** at the output of a 256-to-1 MUX.

The capacitor is charged with a **constant load current** during the TOT.

The same ADC will poll all pixels in a Super Pixel (SP) and convert them as needed.

![](_page_30_Figure_9.jpeg)

![](_page_30_Picture_11.jpeg)

### **Super-column Architecture**

- MUX, handles readout and communication with the periphery.
- SC are read out only if they register a hit. ullet
- SC level **frame-based** solution for readout logic in the periphery.

![](_page_31_Figure_4.jpeg)

• Super-column (SC) logic: mask the pixels, generates the test-pulse (TP), drives the analog

![](_page_31_Figure_7.jpeg)

### **ASIC Structure and Readout**

![](_page_32_Figure_1.jpeg)

- A copy of the signal exit **IMMEDIATELY** the pixel through the FASTOR
- Each FASTOR send a signal to the perifery to start the READOUT
- To be sure we collected the charge entirely, the **perifery waits a bit before starting the READOUT**
- Readout time max 200 µs
- If in a super-pixel zero FASTOR are active, zero bit are sent to the periphery (optimization)

![](_page_32_Picture_8.jpeg)