

HL-LHC Upgrades For the ATLAS Liquid Argon Calorimeter

Lauren Larson The University of Texas at Austin

On behalf of the ATLAS LAr Calorimeter project

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High Luminosity LHC (HL-LHC)





- The HL-LHC with have an integrated luminosity 10 times greater than the current LHC
- The increased luminosity makes it harder to trigger on signal events
- Larger backgrounds from in-time and out-oftime pileup events



LAr Upgrade Motivation



- LAr Calorimeter is a CRITICAL sub-detector for most HL-LHC physics signatures
- LAr Calorimeter itself remains unchanged for HL-LHC
 - Liquid argon stability shown in ATLAS and previous experiments
- The calorimeter electronics will be upgraded
 - In order to be compatible with the upgraded trigger and DAQ systems that are being designed for the higher luminosity
- To meet the needs of the HL-LHC LAr will undergo several upgrades
 - Already commissioned, improved Digital Trigger system, providing finer granularity to the trigger system
 - For the HL-LHC, new radiation hard readout electronics, providing precision readout of all calorimeter cells at 40 MHz



HL-LHC LAr Readout Electronics





HL-LHC:

- Upgrade electronics currently in preparation, to be installed for use in Run 4
- Cover full range of energy expected in the HL-LHC, from ~ 50 MeV – 3 TeV
- Linearity of 0.1%
- Low electric noise, below intrinsic calorimeter resolution
- 11-bit precision at high energy
- All data sent off detector
 - ~180 Gbps per Front-End-Board
 - ~275 Tbps for the full calorimeter

Phase-I:

- Updated L1 Trigger to have finer granularity
- Already Commissioned used for Run 3

HL-LHC LAr Readout Electronics





On Detector Electronics

ATLAS DRIVER BUCK

On Detector Electronics





- sample and digitize the signal
- send the signal off through optical fibers



ALFE2 – Pre-Amplifier and Shaper



Initial analogue processing of the signal

- Custom ASIC designed in 130 nm CMOS
 - Amplification of signal, and bipolar CR-(RC)² shaping over high and low gain scales
 - 4 input channels and 9 output channels: 4 high gain and 4 low gains + 1 sum over the 4 channels sent to the hardware trigger
 - Input impedance and dynamic range programmability



Testing Results:

Exceeds specifications

- Non-linearity < 0.1%
- Noise ~150 nA, below specification of 350 nA for 10 mA channels
- Radiation testing showed good performance after 12 kGy dose, this is 8x higher than expected at the HL-LHC

Current Status:

- Production wafers are ready (need ~80k ASICs)
- Begun quality control testing and integration



COLUTA- Analogue to Digital Converter



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- **Digitizes the PreAmp/Shaper output** at bunch crossing rate of 40 MHz with a 14-bit dynamic range and > 11-bit precision
- 15-bit, 40 MHz ADC
 - Custom ADC ASIC designed in 65 nm CMOS
 - 8 channels matches ALFE output, 4 channels x 2 gains
 - 3-bit Multiplying DAC (MDAC) + 12-bit Successive Approximation Register (SAR)
 - Digital Data Processing Unit (DDPU) applies calibrations and transmits data (15 bits of ADC + 1 overflow) at 640 Mbps
 - Fully compatible with PA/S,
 - eLink interface to IpGBT (optical transmission off-detector)

Testing Results:

Exceeds specifications

- ENOB > 12
- Radiation Tested TID up to 1 MRad, SEU performance excellent

Current Status:

- Production wafers are ready (need ~80k ASICs)
- Begun quality control testing and integration





FEB2 Development



 $\sqrt{\sigma_i^2} = 89.93 \pm 0.91$

The Front End Boards (FEB2s) receive signals from calorimeter cells and perform analogue processing

- The FEB2 will be on the detector, must be entirely radiation hard, composed of two custom ASICs and optical readouts, all actively cooled
- Signals are digitized, serialized and transmitted off-detector via IpGBT protocol
 - 1524 FEB2s with up to 128 channels each
 - 32 ALFE Preamp/shapers, 32 COLUTA ADCs, and 22 IpGBT serializers
 - First full-size prototype (with all 128 channels populated) is ready, and is currently being tested
 - In particular, tests for radiation-hard powering solutions are in progress
 - Tested various solutions for on-board stepping down 48 V power supply to the voltages needed by the ASICs with the help of mezzanines



Run 513, pedestal, hi Gain, Channels 0-127

RMS = 94.33



Calibration Board







Sends a known LAr-like signal to the electrodes to calibrate the read-out electronics

- Full 16-bit dynamic range
- 122 boards installed in the front ends crates, 150 to be fabricated and assembled
- Composed of two custom ASICs
 - CLAROC
 - creates pulse using high frequency (HF) switches, based on 180 nm HV-CMOS
 - LADOC
 - 16-bit DAC, used to send commands to the HF switches, based on 130 nm CMOS
 - Both ASICs are conducting final pre-production tests to validate production routine (QC testing)
- Both ASICs exceed linearity requirements
- Construction of the **CABANE**, a full-scale test board, has been completed and will be followed by future iterations

Off-Detector Electronics

ATLAS DRYDSTAT BI

LAr Timing System (LATS)





- The LAr timing system (LATS) handles Trigger, Timing and Control (TTC) distribution, configuration, and monitoring of the FEB2 and Calibration boards, relying on IpGBT protocol
- 30 LATOURNETT ATCA Blades
 - Each equipped with 1 central + 12 array Cyclone 10 GX FPGAs
 - Each can control up to 72 on-detector boards

- Completed test board design and prepared test bench
- First full prototype cabled, and passed initial electrical tests
- Proposed architecture for integration with ATLAS TTC and DAQ systems
- First integration tests with FEB2 and Calibration board ongoing
- Software and firmware development ongoing



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LAr Signal Processor (LASP)



The LAr signal processor (LASP) applies digital filtering to waveforms from the FEB2, calculates energy and time, and transmits to DAQ systems

- Composed of the LASP ATCA board (main blade) and the Smart Rear Transition Module (sRTM)
- Main Blade
 - Receives data from up to 6 FEB2s (768 channels) using IpGBT protocol at 10.24 Gbps
 - Computes energy and time in real time
 - Sends output to the trigger system at 25 Gbps
 - Data is buffered at least 10μ s until a trigger decision is reached
 - Implemented using two Intel Agilex FPGAs per blade
- sRTM
 - Used for data transmission with TTC and DCS integration

Development

- Prototype LASP + sRTM in development
- A first set of test boards are produced, and are continuously running in test bench
- Regular monitoring of temperature, voltage and current in place
- Validated power, I2C sensors, and FPGA configuration
- Work ongoing on the firmware, including transitioning from the Stratix FPGA to the Agilex FPGAs, and aiming to optimize FPGA resource usage and power consumption
- Long series of tests in stand-alone and within the full system are foreseen



LASP Prototype Design 13



LASP- FPGA and Machine Learning



- Current signal processing uses Optimal Filtering (OF), modern machine learning techniques may allow us to improve energy and timing calculations in a high pileup environment
- Convolutional and Recurrent Neural Networks (CNN and RNN) are being investigated and show good performance



- Understanding trade-off between performance and optimizing FPGA resource usage and power consumption
- Firmware prototype implementations are available for both CNNs and RNNs and fit on one FPGA

Integration at CERN





Currently, primary integration tests of FEB2 and LASP + SRTM are underway at CERN

- Constructed a small scale readout chain for integration testing
 - 32 channel on and off detector setup with DAQ and TTC from current ATLAS systems
- **Software** effort for online and offline software including reconstruction, monitoring, and analysis is underway

Integration at BNL

- Use BNL's high-fidelity reproduction of the mechanical and electrical properties of the LAr calorimeter
 - Detector cables/feedthrough
 - Power supplies
 - •Front-End crates with baseplane
 - •Water cooling system
- Measure coherent noise in a realistic setup
 Half-crate test: using 14 FEB2 (half a crate), simultaneously readout
 - Integrate FEB2, calibration board and off-detector LASP readout system
 - Testbed for firmware development







Summary



- Upgrading the LAr calorimeter electronics system is vital to the success of ATLAS in the HL-LHC
- The radiation-hard custom ASICs used on the detector exceed specification requirements and are in production
- Final designs for the off-detector boards and firmware are underway
- Integration setups are being constructed for testing the full calibration to readout chain
- **On schedule** for installation into ATLAS cavern beginning in **2027**
 - Designed to run through 2041





ATLAS ORYDSTAT BIOCAP #

Front End Board 2 (FEB2)





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ATLAS Experiment

- ATLAS is an mutli-purpose detector
 - Designed to measure a wide range of particles
 - Formed of concentric layers of different subdetectors, each with a unique goal









Liquid Argon Calorimeter (LAr)



- Sampling calorimeter with liquid argon as the active medium, and lead, copper, and tungsten as the passive material
- Measures energy, position, and timing of electromatic showers and hadronic jets
- Accordion geometry allows for full azimuthal coverage
- **182,468 cells** are read off at a rate of **40 MHz** (bunch crossing rate) and sent off the detector or analysis







- Calorimeter Electronics will be upgraded, but the calorimeter itself will not
- Cryostat will not be open, performance continues to exceed expectations

Radiation Testing ASICs





- All on-detector ASICs have been tested for radiation hardness
- Custom boards were designed to isolate the ASIC being tested

- COLUTA was tested at Massachusetts General hospital in Boston
 - SEE σ = 3.7 x10-10 cm2/bit
 - Expected 6140 SEE/channel over the lifetime of the HL-LHC
- ALFE was tested at BNL and Fermilab Test Beam Facility Irradiation Testing Area
 - SEE $\sigma < 1.1x10-15$ cm2/bit
 - Expected error rate for the full LAr Calorimeter in HL-LHC = 61 SEE bit errors/day.