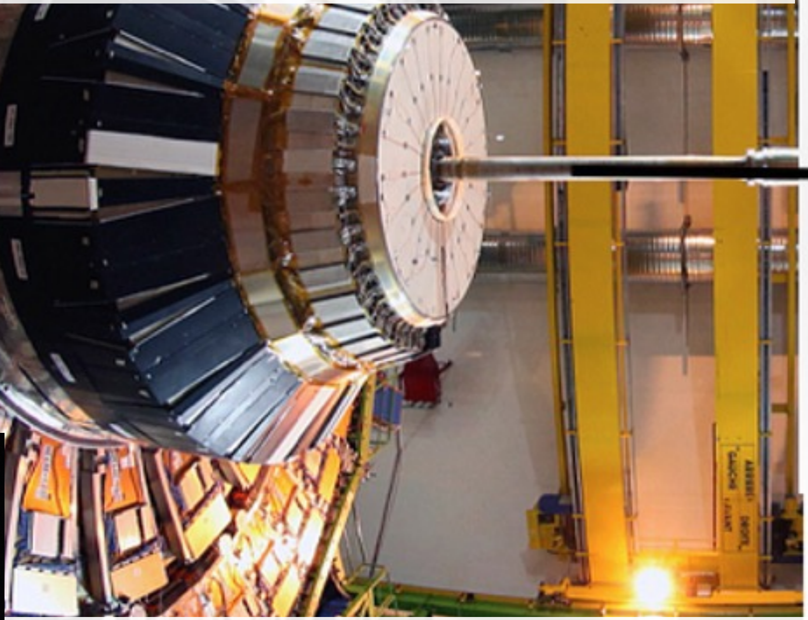
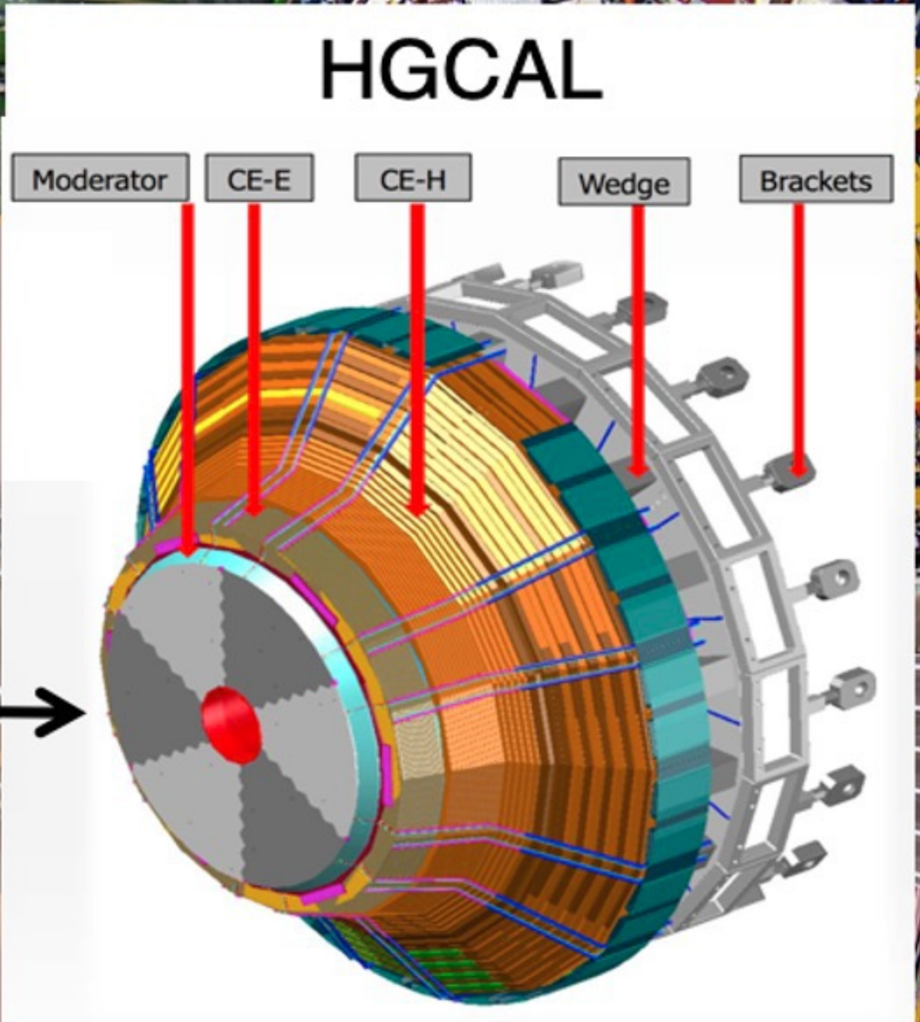
Overview of the front-end electronics of CMS HGCAL

Including readout and powering





Total eclipse
Credit: Danny Noonan , April 2024

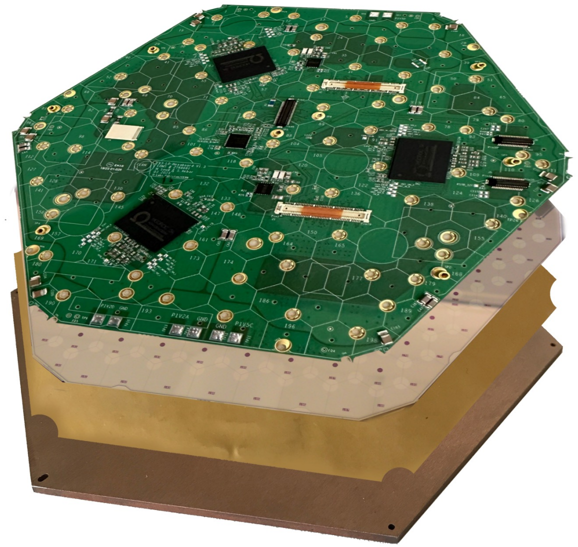
Aidan Grummer, On behalf of the CMS Collaboration
Fermilab

2024, May 24

Introduction: HGCal front-end

- This presentation provides an overview of the HGCal frontend
  - Digitizing signal with HGCal Readout Chip (HGCROC)
  - Data concentration with the E-link Concentrators (ECON)
  - Data transmission:
    - Low power gigabit transceiver (lpGBT)
    - Electrical to optical conversion (VTRX+)
- Powering and services plans will also be discussed

Silicon Module



SiPM and Scintillator Tile Module

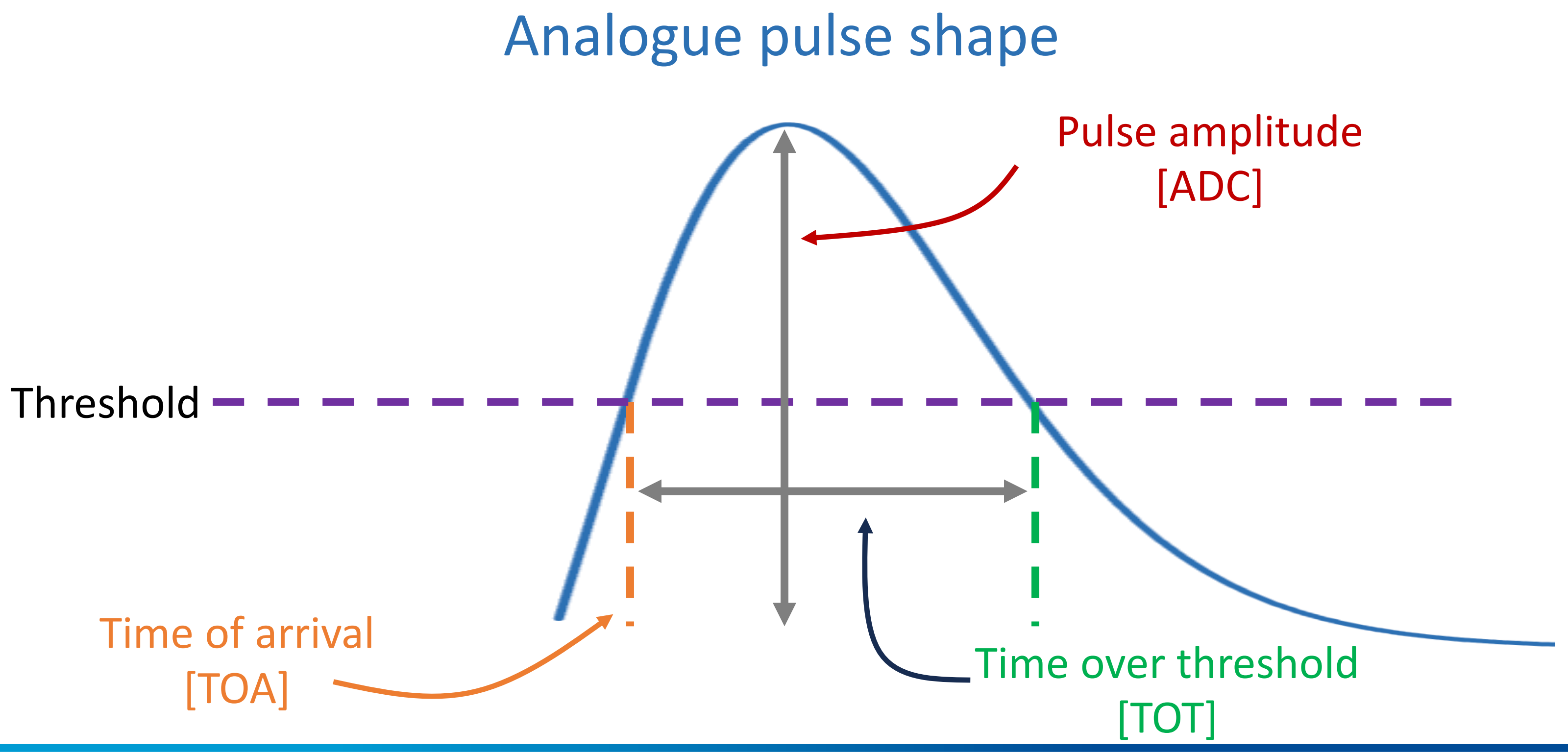
See Thomas French’s talk for a full HGCal overview: https://indico.cern.ch/event/1339557/contributions/5919422/

Motivation

- Fundamental information needed for the calorimeter:
- Measure charge over a large dynamic range: 0.2 fC — 10 pC
    1. Single minimum ionizing particle (MIP) - for calibration
    2. High energy jet measurements
- Measure time
    - Mitigate high pileup conditions in HL-LHC
- Measurements needed for over 6 million channels

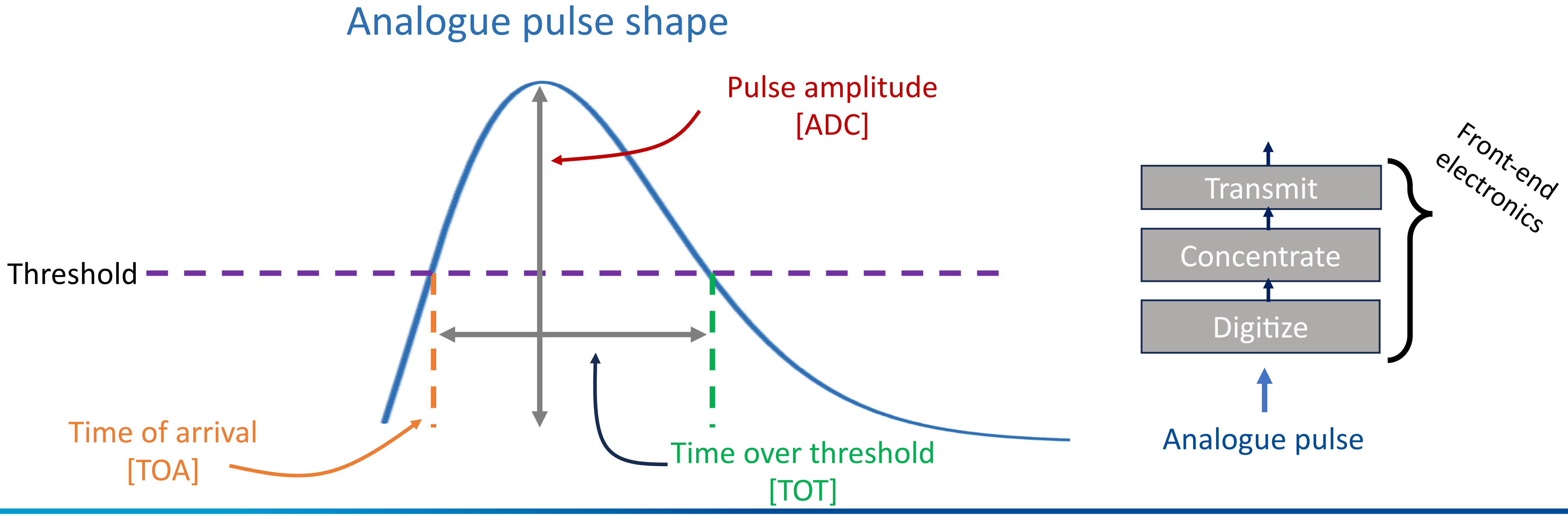
Motivation

- To measure charge
  - Read out ADC for small charge deposits (small pulses)
  - TOT used for large charge deposits (large pulses)
- Time of arrival of a signal (TOA) also measured



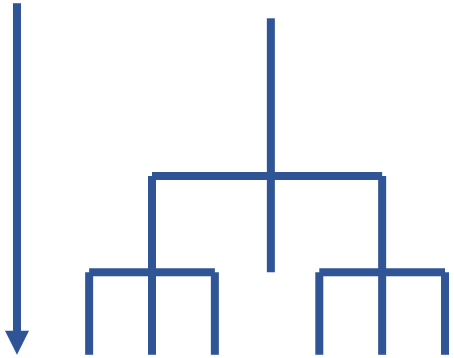
Motivation

- Purpose:
  - Digitize, concentrate, and transmit data



Motivation

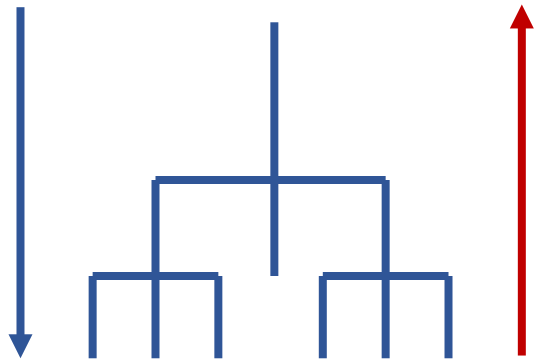
- Purpose:
  - Digitize, concentrate, and transmit data
  - Distribute clock and control signals



Motivation

- Purpose:
  - Digitize, concentrate, and transmit data
  - Distribute clock and control signals
  - Provide detector monitoring:
    - temperature, currents, voltages, etc.





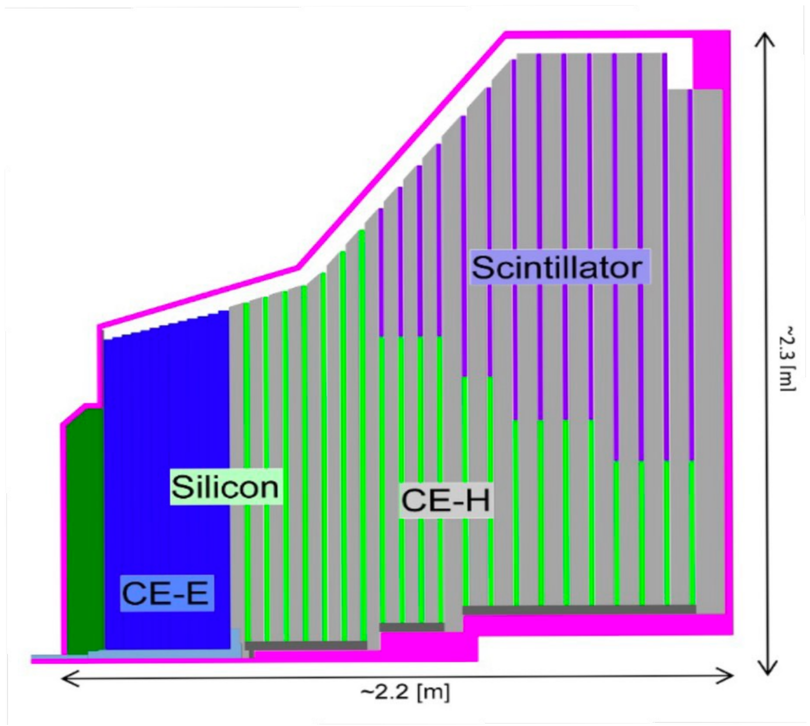
Motivation and Requirements

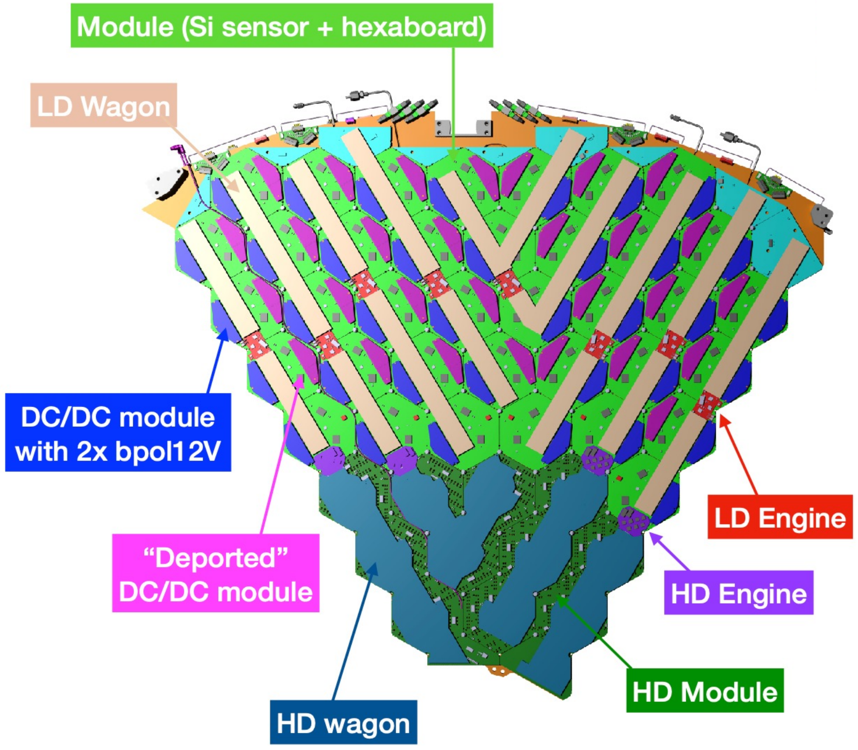
- Purpose:
  - Digitize, concentrate, and transmit data
  - Distribute clock and control signals
  - Provide detector monitoring:
- Constraints:

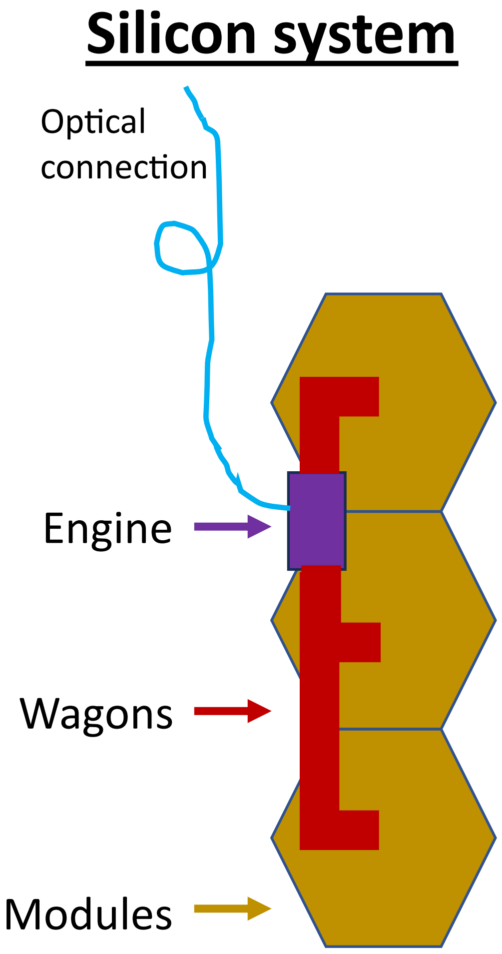
Parameter	Specification
Total ionizing dose	200 Mrad
Tolerance to single event effects (SEE) (average detector fluence)	Hadron fluence (E $>$ 20 MeV): 1×10^{14} cm^{-2}
Charge measurements with large dynamic range	0.2 fC — 10 pC
Time resolution	25 ps
Fit in limited physical space	$\sim$5 mm gap
Low power consumption (including digitization and concentration on DAQ and trigger paths)	$\leq$ 20 mW/ch
Allow transfer of large data volumes required for good trigger and physics performance.	Trigger path: $\sim$60 Tb/s DAQ path: $\sim$40 Tb/s

Complex geometry

- Almost every layer of the calorimeter has a different size
  - Introduces complications in geometry of modules and connectors
- Large variety in connector shapes required
- Grouping modules allows for a uniform scheme to readout data



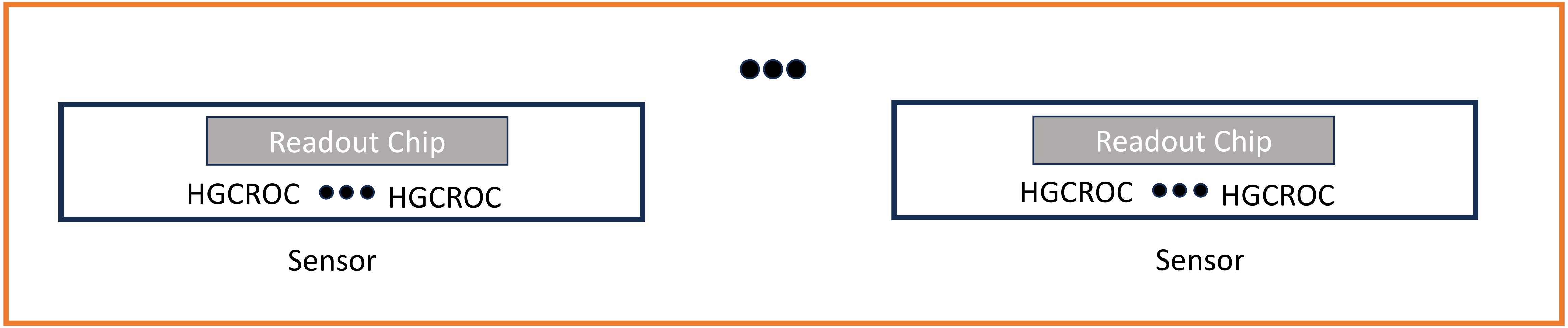




Frontend readout scheme

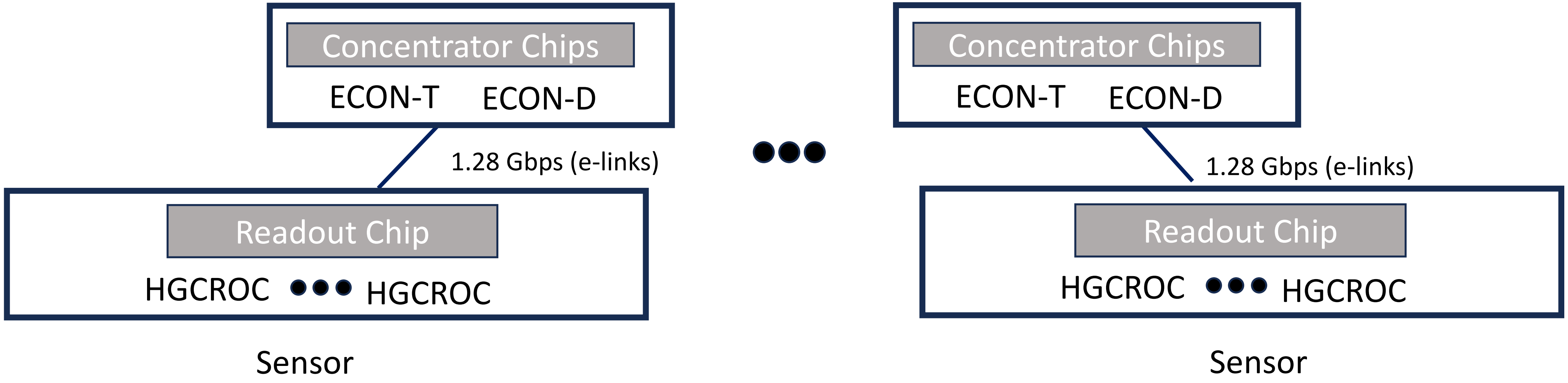
- Sensor data is digitized

Group of modules



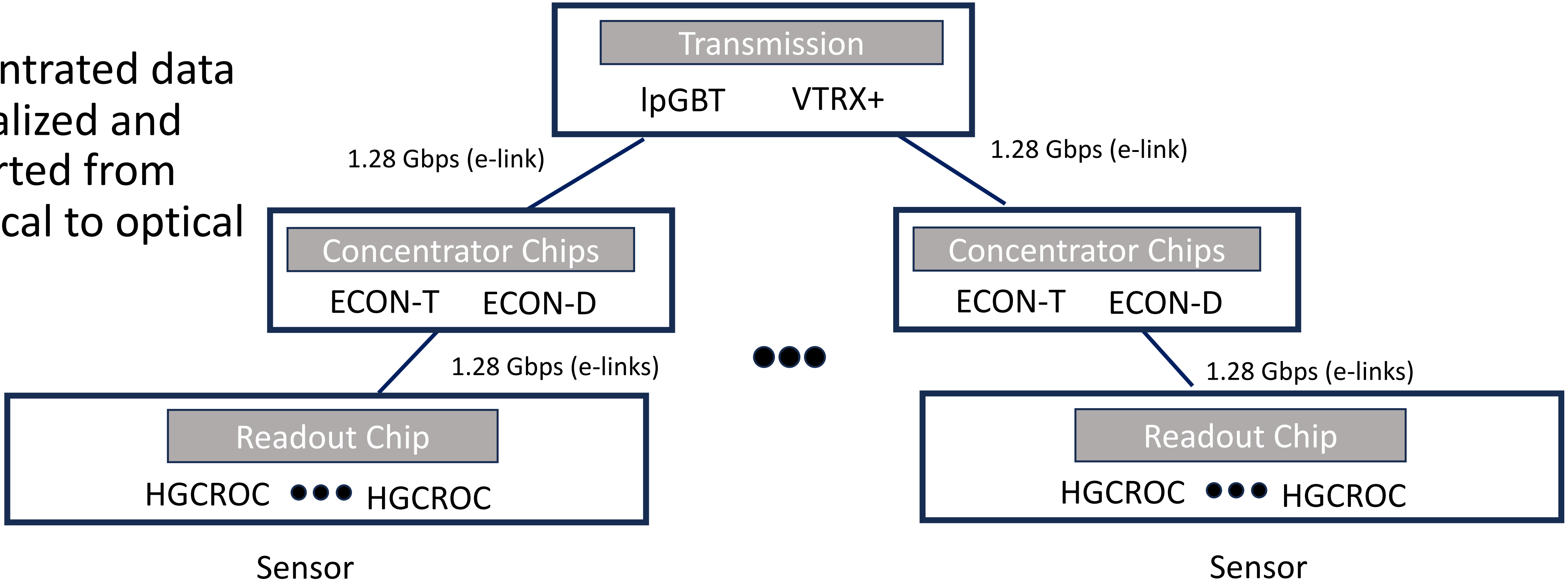
Frontend readout scheme

- Digitized data is concentrated



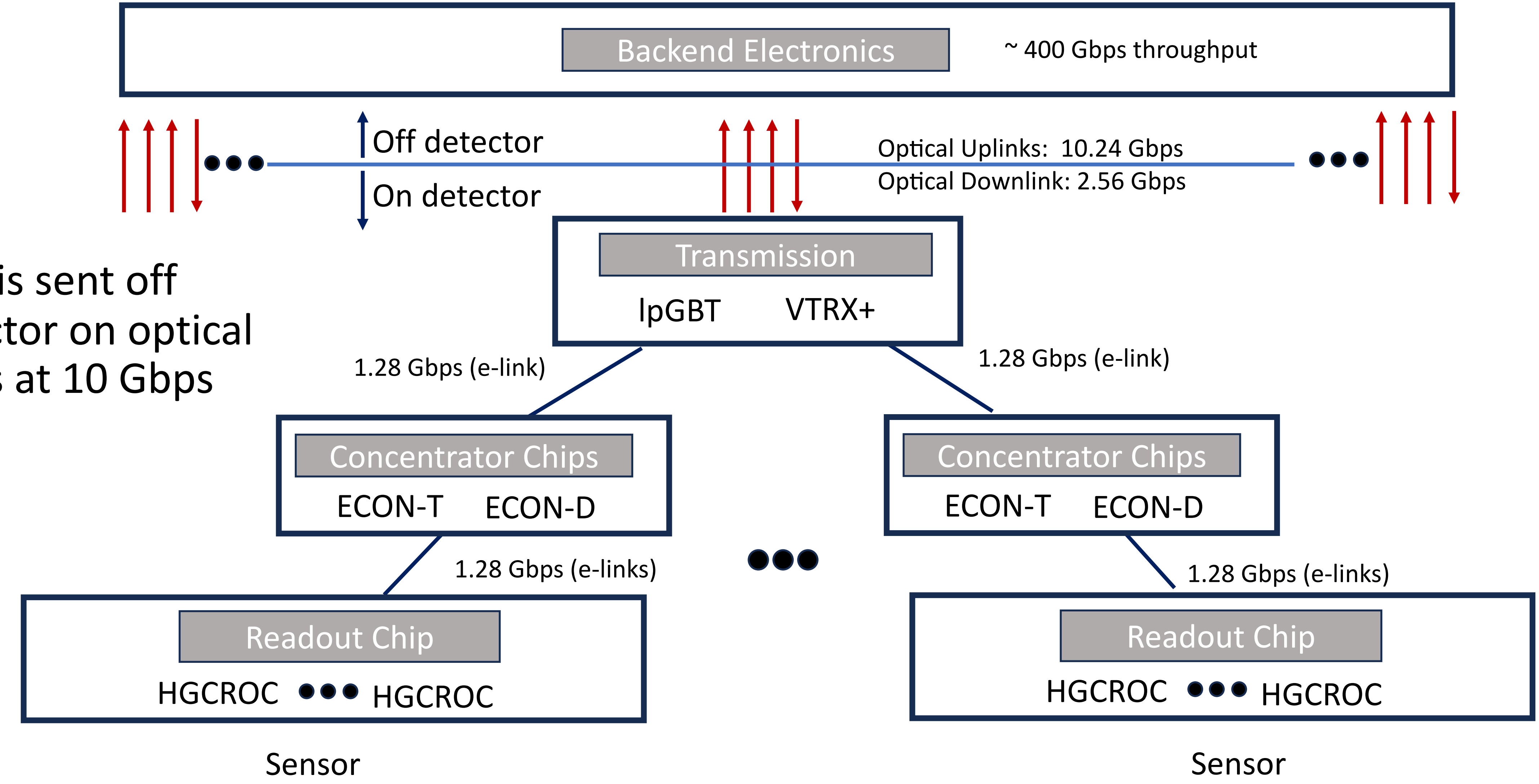
Frontend readout scheme

- Concentrated data is serialized and converted from electrical to optical

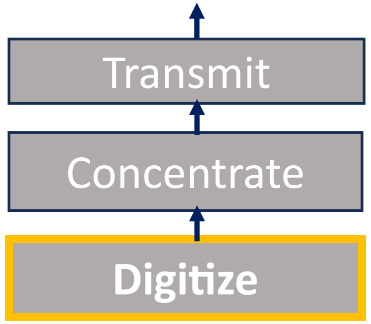


Frontend readout scheme

- Data is sent off detector on optical fibers at 10 Gbps



Readout chip: HGCROC

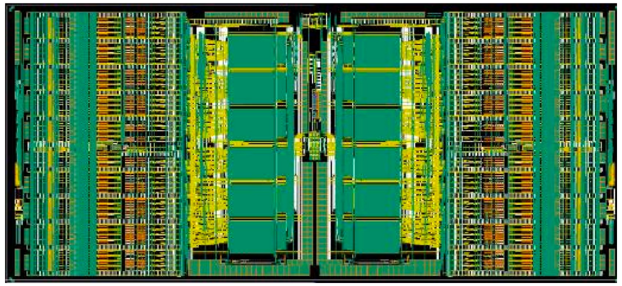


- HGCROC measures up to 72 readout channels on a module
  - As well as 4 common mode channels to mitigate noise and 2 calibration channels

- Trigger path
  - Sum of 4 (9) channels, linearization, 7-bit floating point output
  - 4 Trigger 1.28 Gbps output links

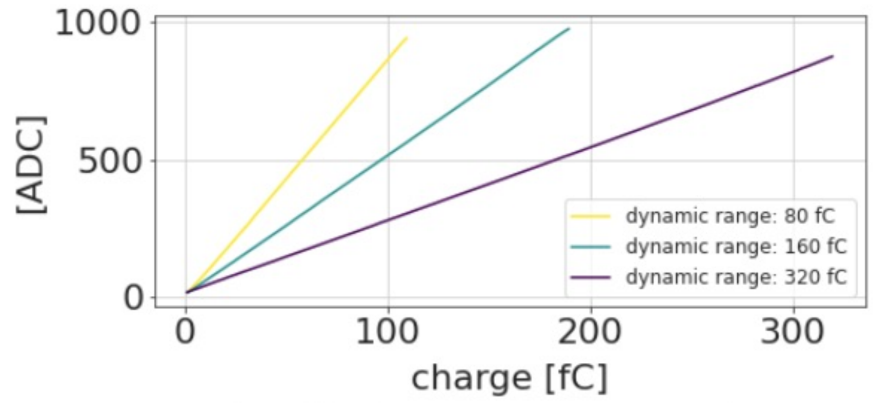
- DAQ path
  - 512 depth DRAM, circular buffer, storing full event info (ADC, TOT and TOA) for 12.5µs
  - 2 DAQ 1.28 Gbps output links

- Control:
  - I2C protocol for slow control
  - 320 MHz clock and fast commands

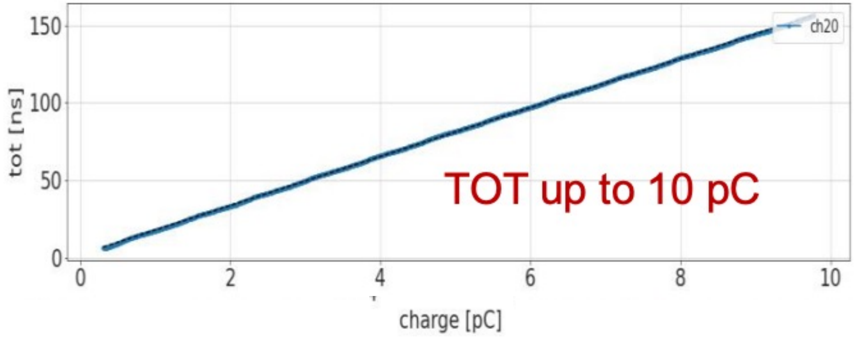


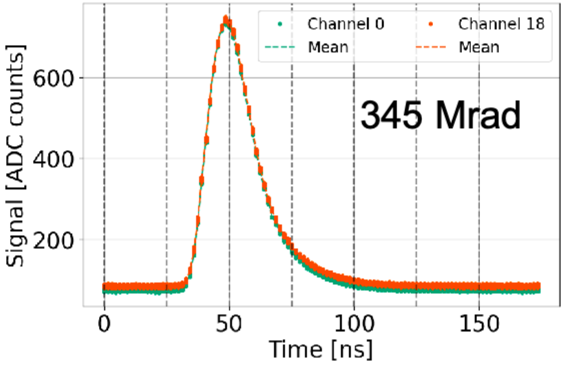
Readout chip: HGCROC

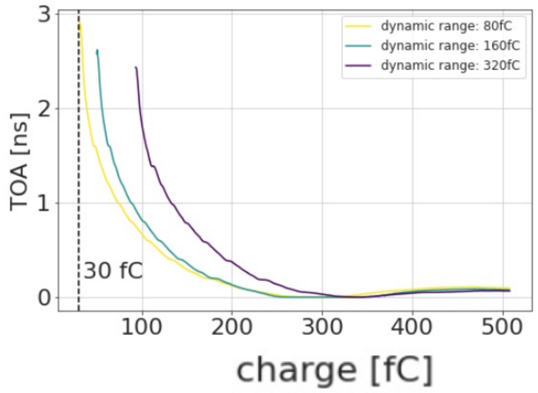
- Characterization well advanced, no showstoppers.
  - ADC range
    - Linearity in +/- 0.5 %
  - TOT range
    - Linearity in +/- 0.5 %
    - Jitter around 25 ps
    - TOT 12-to-10 compression visible on the jitter
  - TOA: 2.5 ns time walk
- Radiation campaigns, module and system tests continuing
  - TID results: at 5°C, up to 350 Mrad, chip behavior very stable, almost no change on ADC, TDC, PLL
- Pre-production HGCROC chips received at end of February 2024



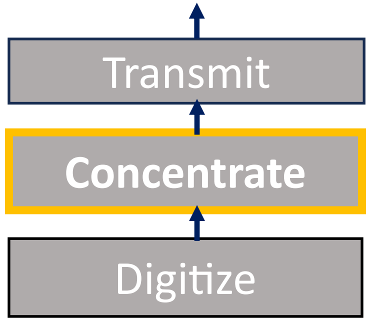
TOT linearity and Jitter (w/ 47pF sensor capitance)







Data concentration: ECON chips



- ECONs concentrate data to reduce number of links to backend
- Monitor synchronization of the ROC to ECON chain, report to backend

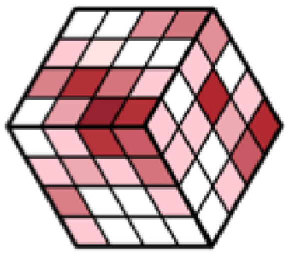
Trigger path (ECON-T)

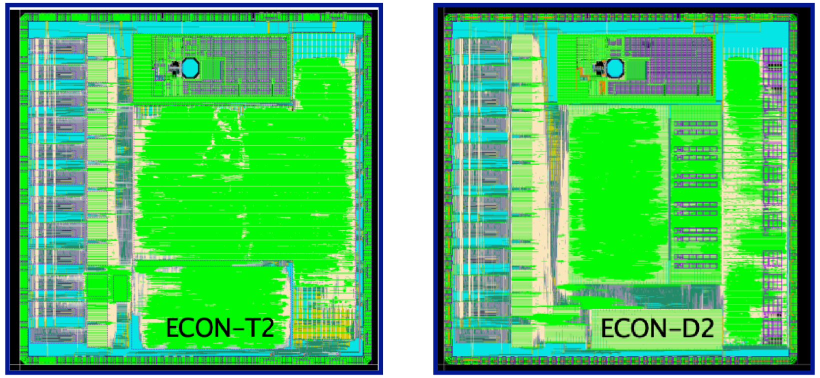
- Select or compress HGCROC trigger data for transmission off detector at 40 MHz
- Four algorithms:
  - Threshold-sum
  - Best-Choice
  - Super trigger cell
  - Auto-encoder (“AI on Chip”)

DAQ path (ECON-D)

- Performs digital processing of sensor data for events passing L1 trigger at 750 kHz
  - Applies zero-suppression
  - Aligns channels from multiple HGCROCs

Starting from 48 Trigger Cells (TC)

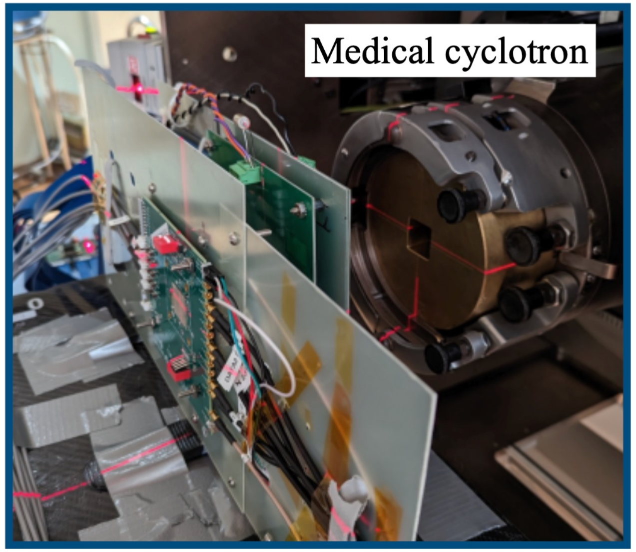




5.315×5.315 mm^2

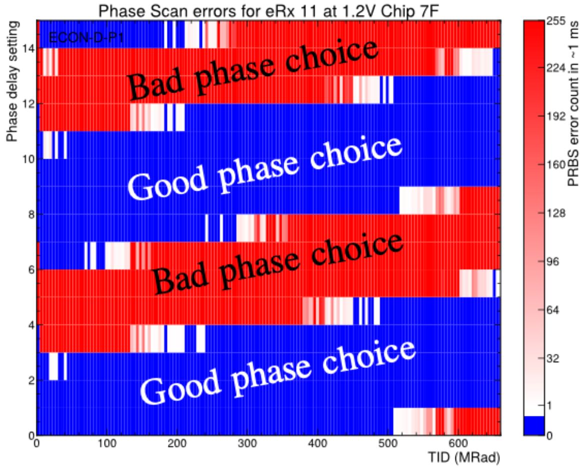
Data concentration: ECON chips

- Radiation campaigns show excellent performance against radiation effects
  - No single event upsets in I2C registers
    - Set upper limit on cross section of errors requiring reset
  - Good behavior up to 660 Mrad, 1.2V
    - test facility: CERN ObeliX X-ray
    - Evidence of small error rate at >450 Mrad for ECON-D-P1, 1.08 V (HGCal requirement: 200 Mrad)

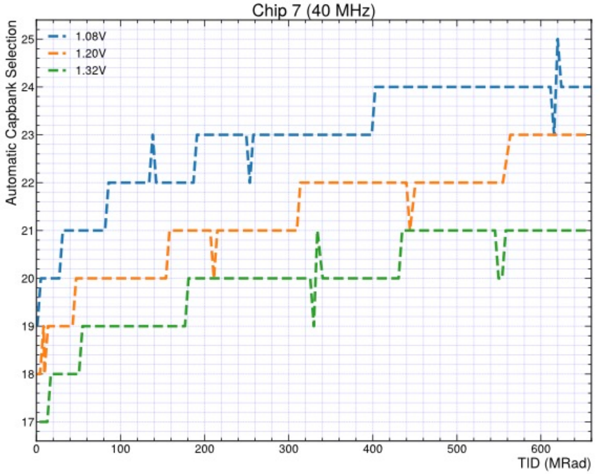


- ECON engineering run is complete
  - Will receive 24k ECONs in 1-2 weeks.
    - about half of the total number needed for the detector
  - Characterization and testing will happen this summer.
  - Will produce and test all ECONs by early 2025.

Evidence of shift of good phase window at high TID, as expected

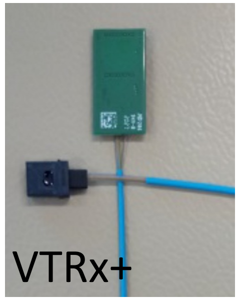


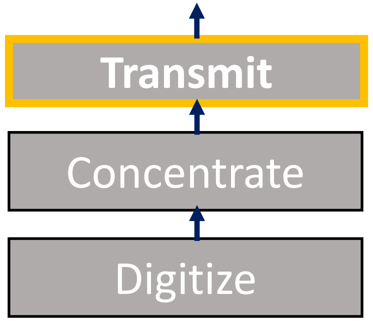
Automatic Capacitance selection for PLL as a function of TID, as expected



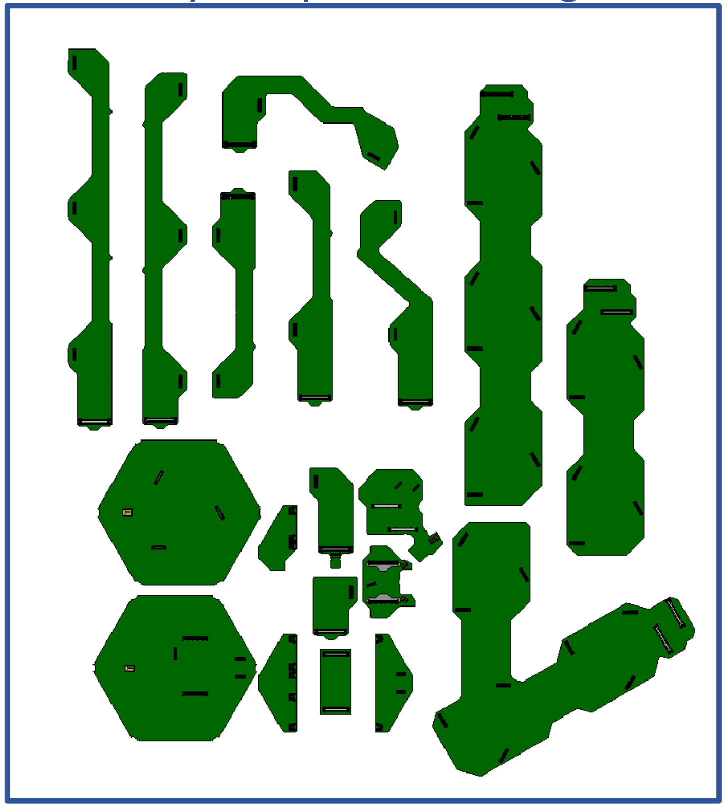
Data transmission: Engines

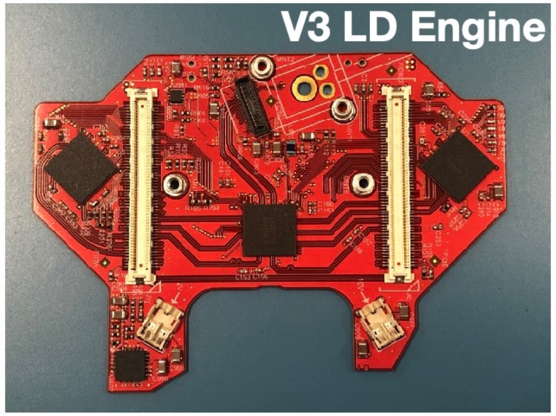
- Serialize data from the up to 7 concentrator chips and send data optically off detector
  - CERN ASICs: lpGBT and VTRx+
  - Uplinks at 10.24 Gbps
  - Low density engines supports up to 6 full LD silicon modules
  - High density engines support up to 3 full HD silicon modules
- Wagons: passive boards that connect engines to modules
  - Large boards that come in many variants (>50) accommodate

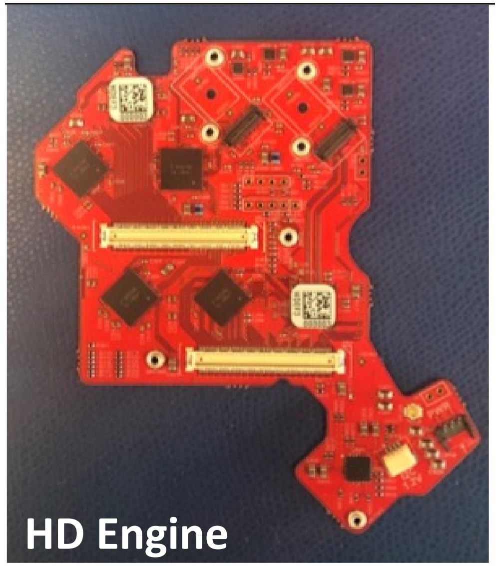




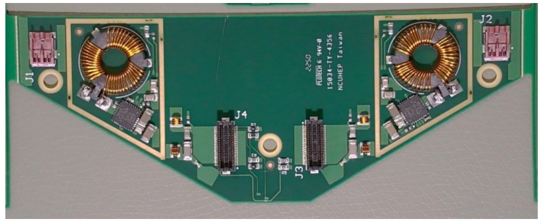
Many complex PCB designs

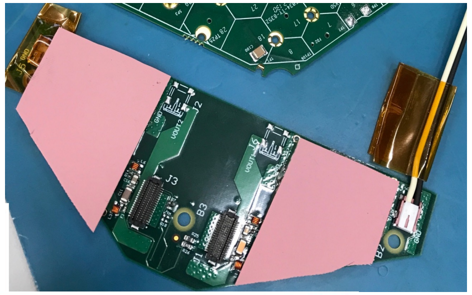


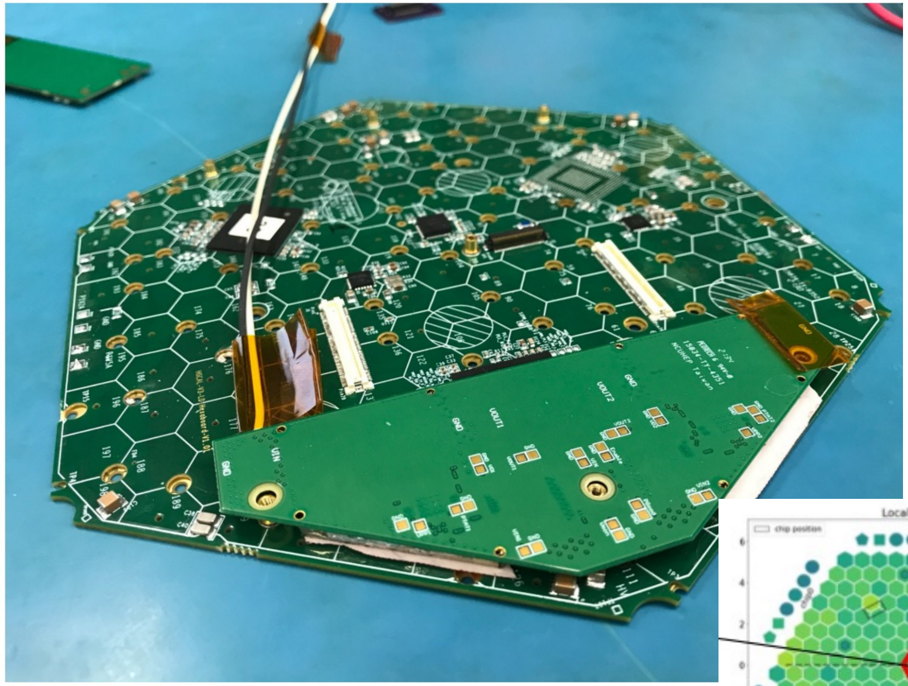


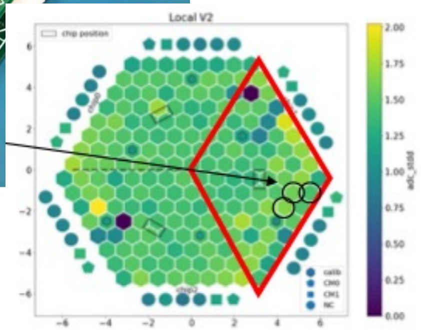


Frontend powering: DC to DC converters





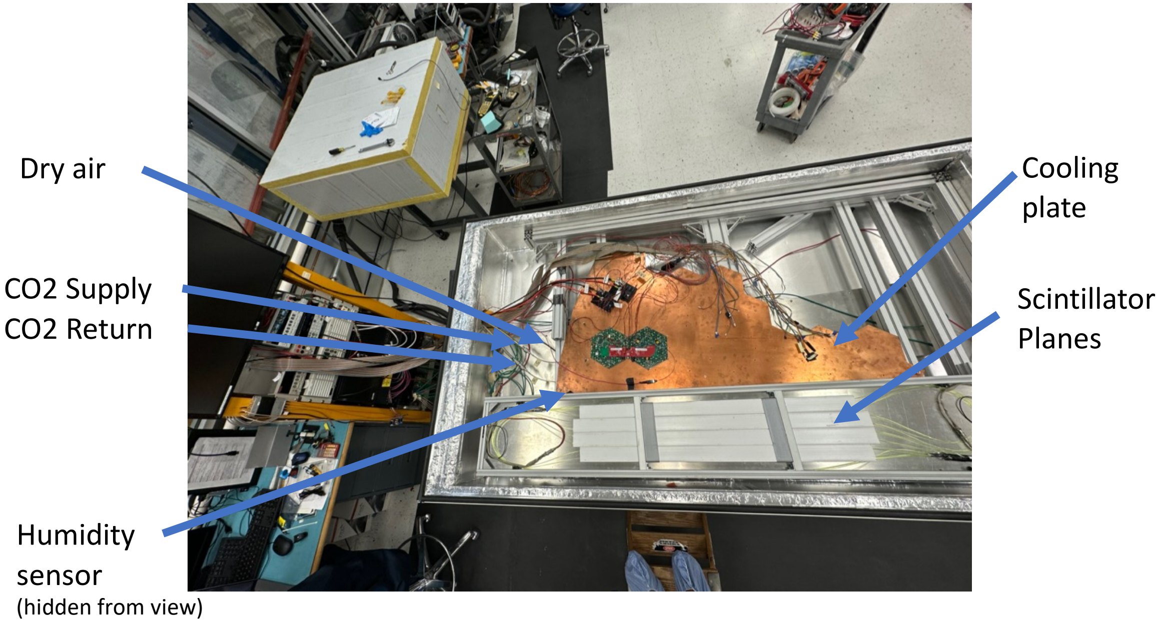


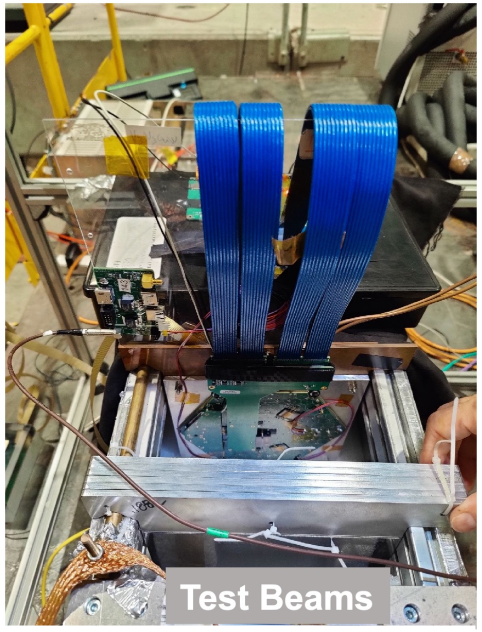


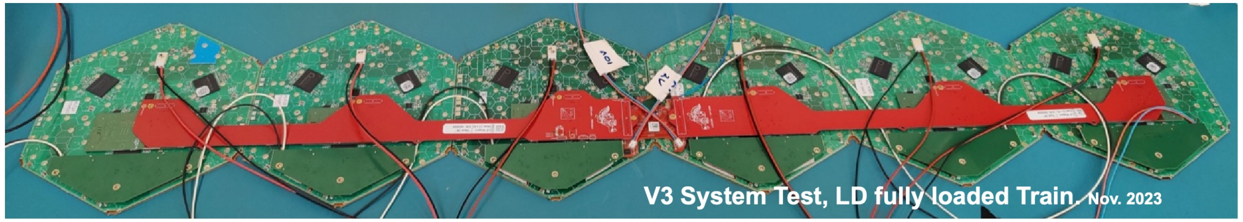
- A single low voltage power level will be provided to the detector
- Custom DC-to-DC converters are used step the voltage level down to appropriate levels for the modules
    - Custom Coils
    - Custom Shields to avoid introducing noise
- BusBars will be used to distribute power
    - Heavy-copper flex PCB
    - Tight coupling between supply and returns
    - Intrinsically radiation tolerant (polyimide-based insulation)

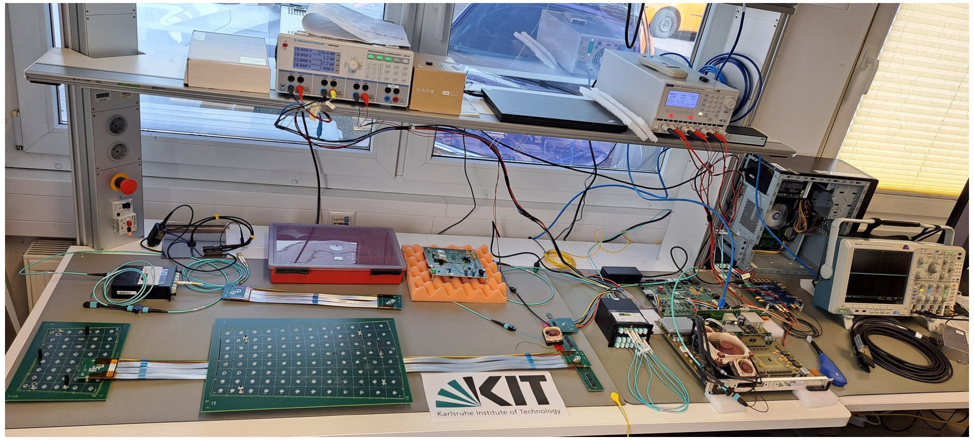
A suite of test systems

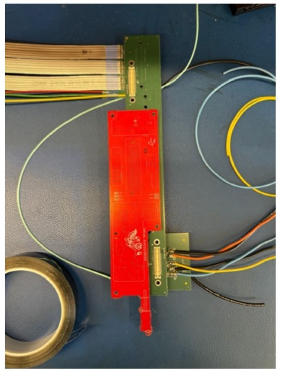
- A rigorous set of test systems and facilities are setup at sites around the world
  - Must ensure robust performance of the entire HGCAL system from prototypes through pre-production and full production











Conclusion

- No show-stoppers found in any part of the system
  - Challenging custom ASICs
  - Extreme radiation tolerance constraints
- Looking forward to a productive year!
  - HGCROC preproduction chips becoming available now (up to 5% of detector)
    - HGCROC production chips expected by end of year
  - ECON engineering run chips arrive this month
    - Will produce and test all ECONs by early 2025.
  - More test beams: systems (in magnetic field) and ASICs
  - Aiming at Cassette Pre-Production at end of year
- Stavros' talk on backend developments and Andre's talk on reconstruction efforts!
  - https://indico.cern.ch/event/1339557/contributions/5917852/
  - https://indico.cern.ch/event/1339557/contributions/5917850/

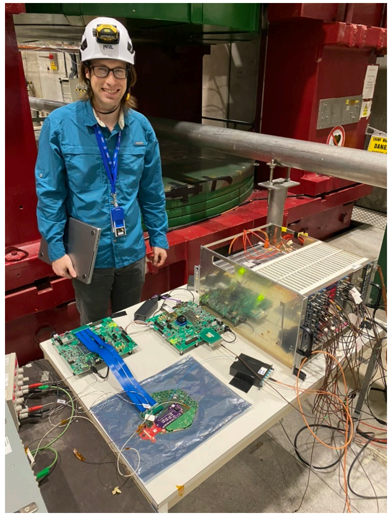
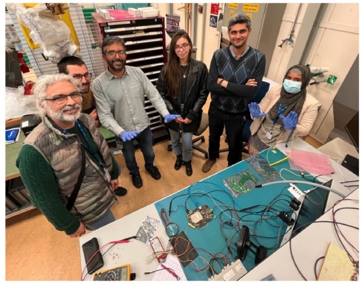
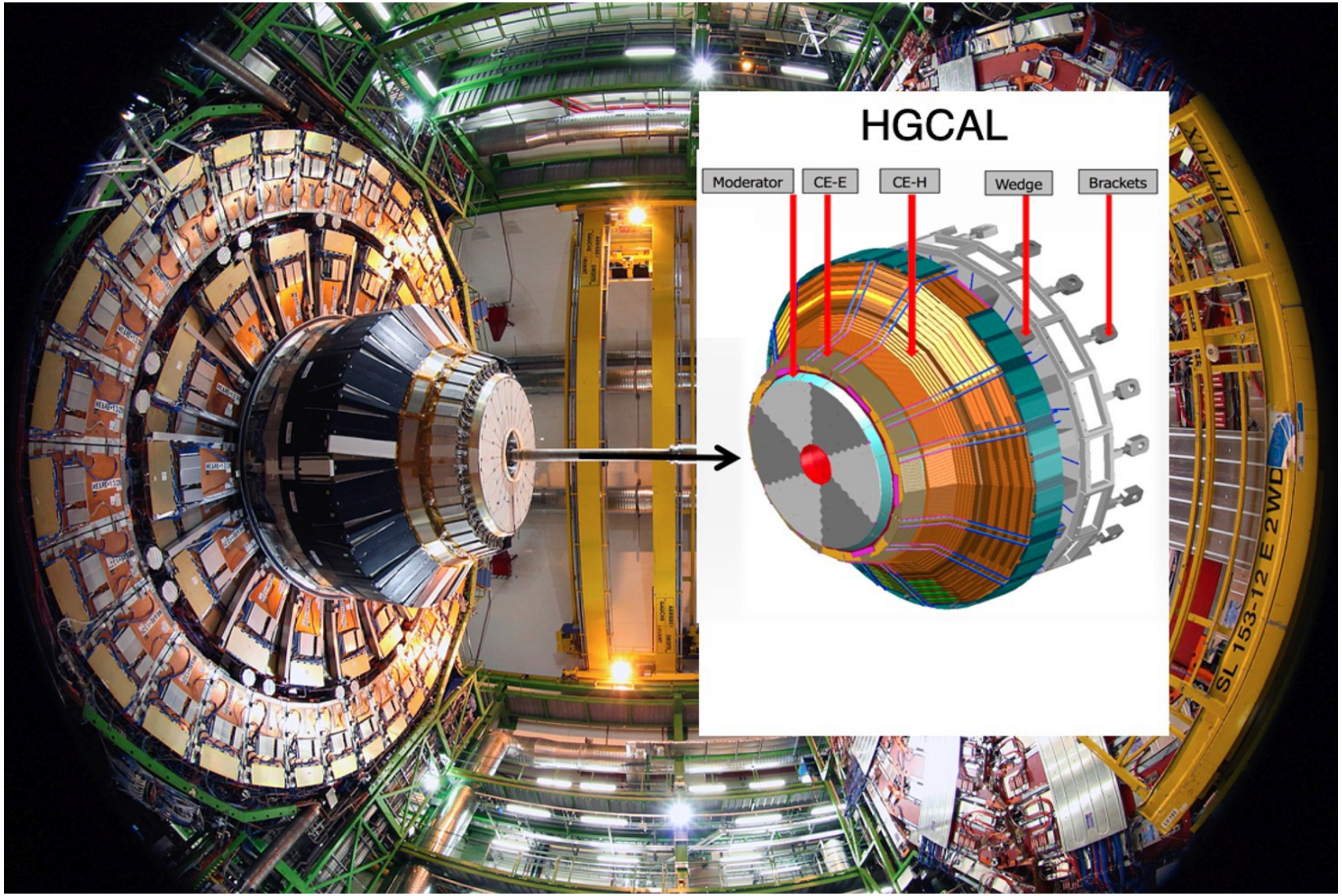


Photo credit: Ryan Postel
Fermilab Communication Office



Additional Slides

HGCal Upgrade



- HGCAL will replace the operating endcap calorimeters
  - “upgrade is an understatement”

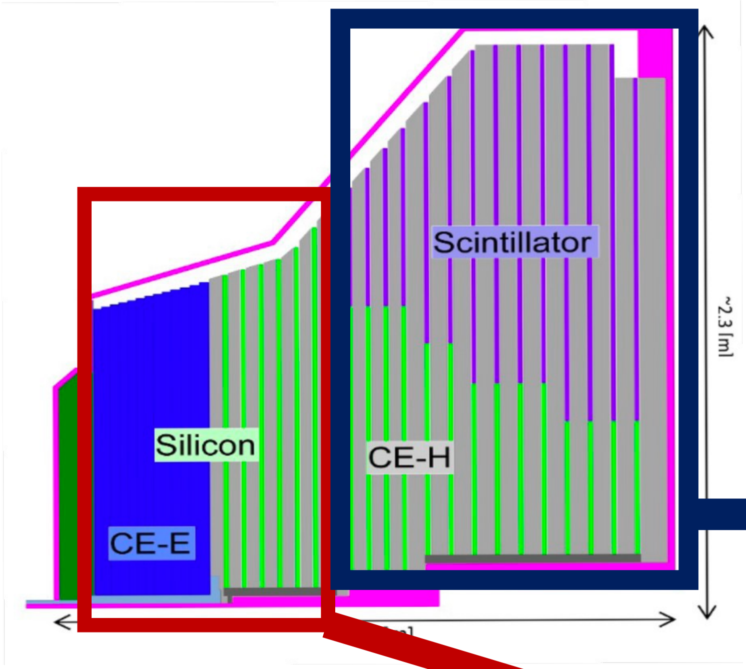
Total eclipse, April 2024
Photo credit: Danny Noonan

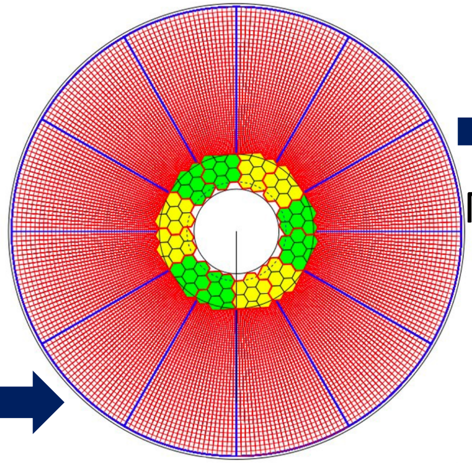
See Thomas French’s talk for a full HGCal overview.

Cassettes

Full detector overview in Thomas French's talk

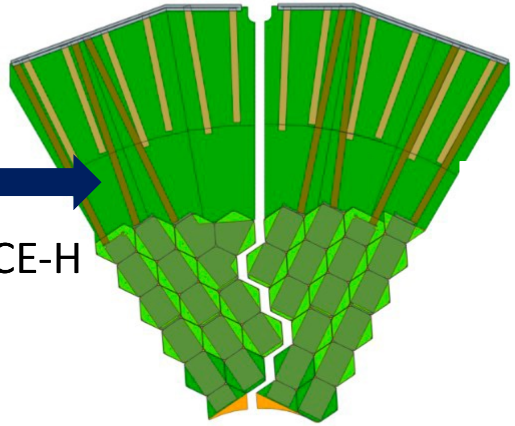
- Cassettes are collections of trains mounted on copper cooling plates
- Silicon only trains in electromagnetic section
- Mixed (silicon and scintillator) trains in hadronic section

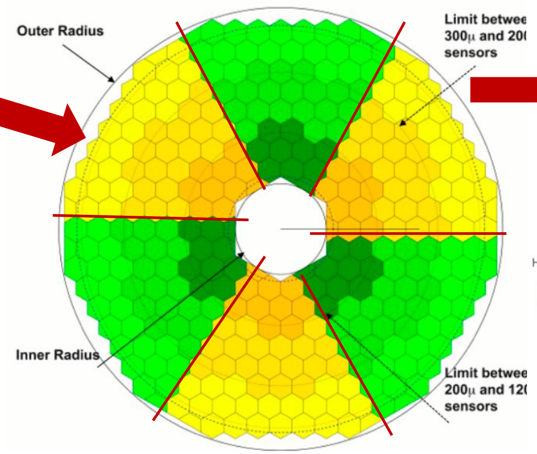




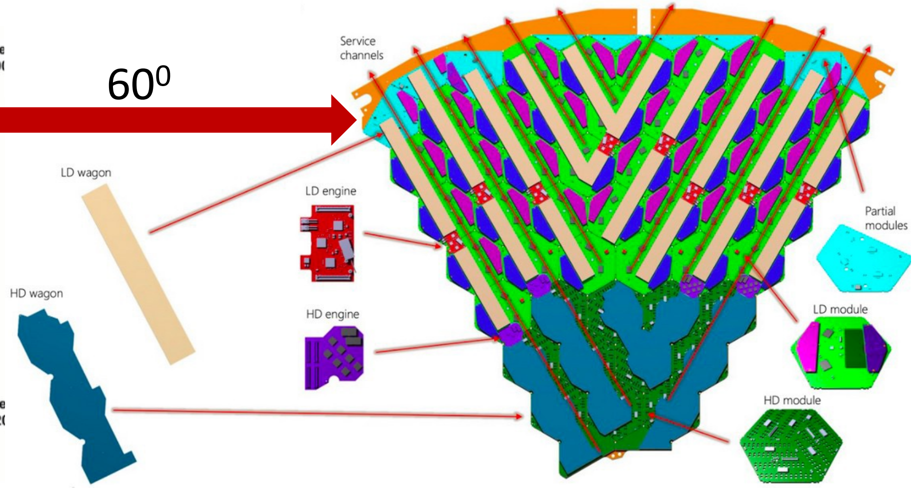
30^0

Mixed CE-H

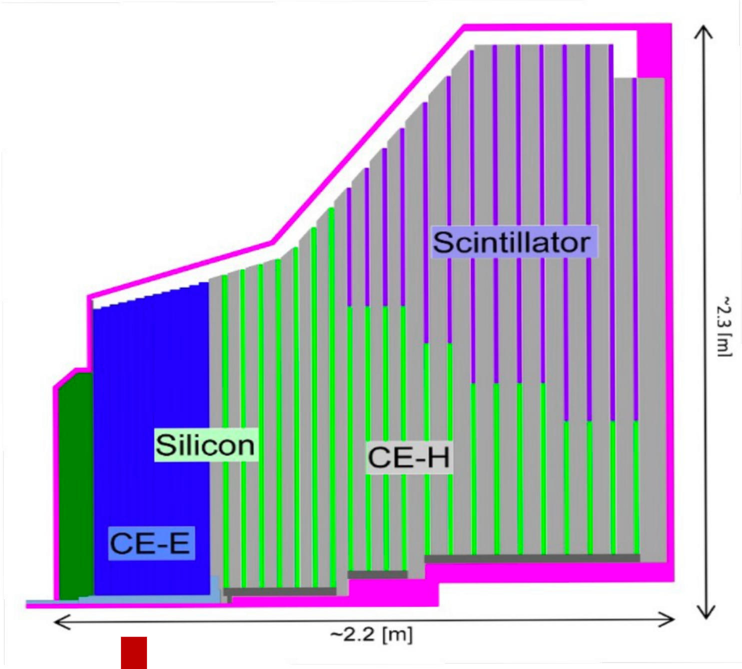




60^0



Silicon Systems



Radiation level comparable to pixel tracker

Module

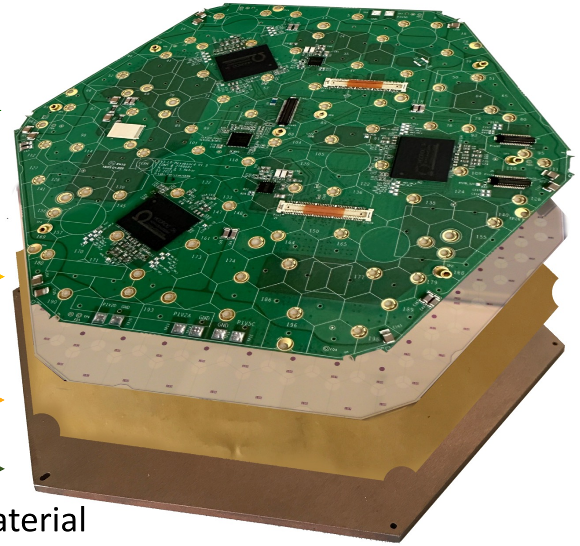
Hexaboard PCB
Hosting the readout chips

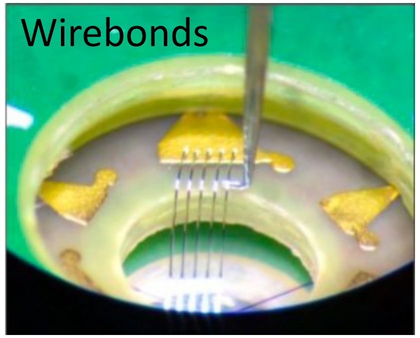
Silicon Sensor

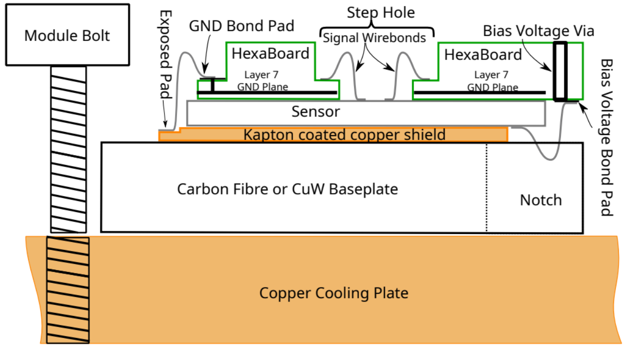
Metalized Kapton Sheet

CuW BasePlate*
Rigidity, contributes to the absorber material

*Carbon fiber baseplate in the hadronic sector







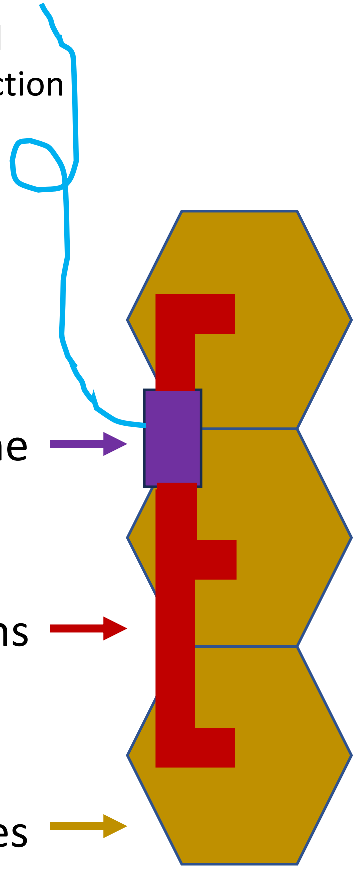
Train

Optical connection

Engine

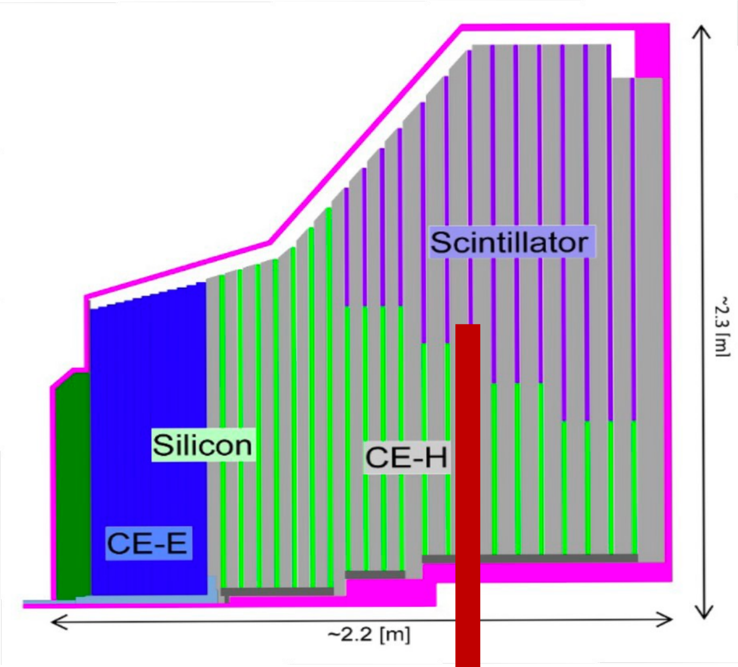
Wagons

Modules



* Powering scheme not shown

Scintillator Systems



Lower radiation level than silicon sector

Module

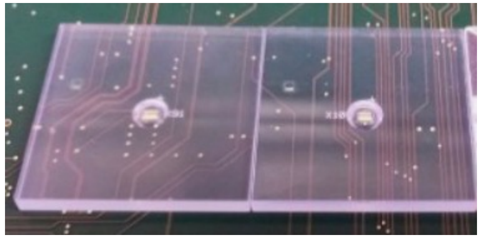
Cell sizes from 4 to 30 cm^2

Tileboard PCB
Hosting the readout chips

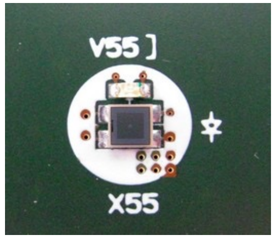
Wrapped Scintillating Tile
Reflective foil

Silicon Photo Multiplier (SiPM)
Calibration with LED

Scintillator

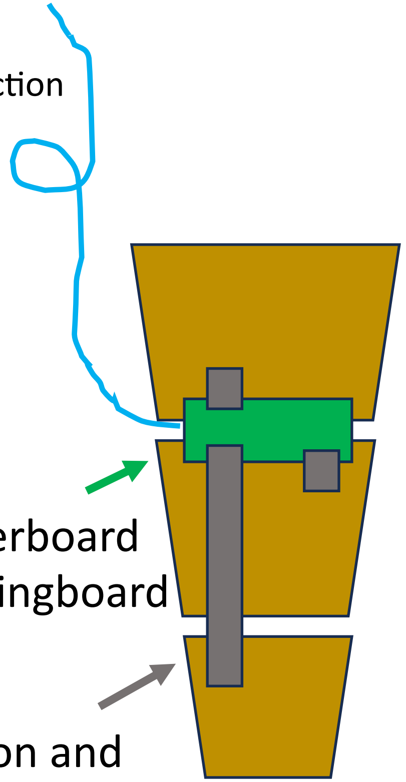


SiPM



Train

Optical connection

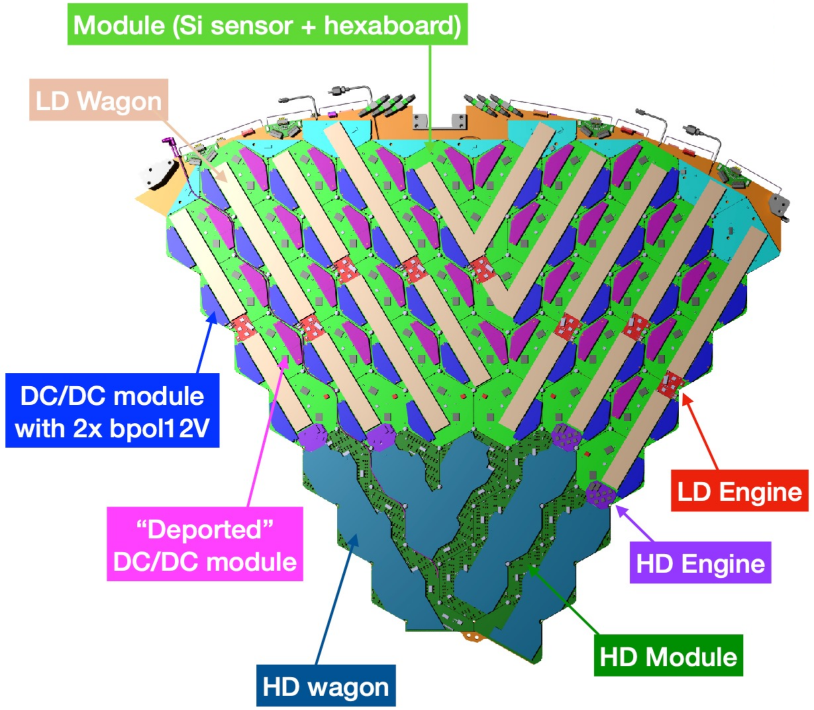


Motherboard and wingboard

Ribbon and flex cables

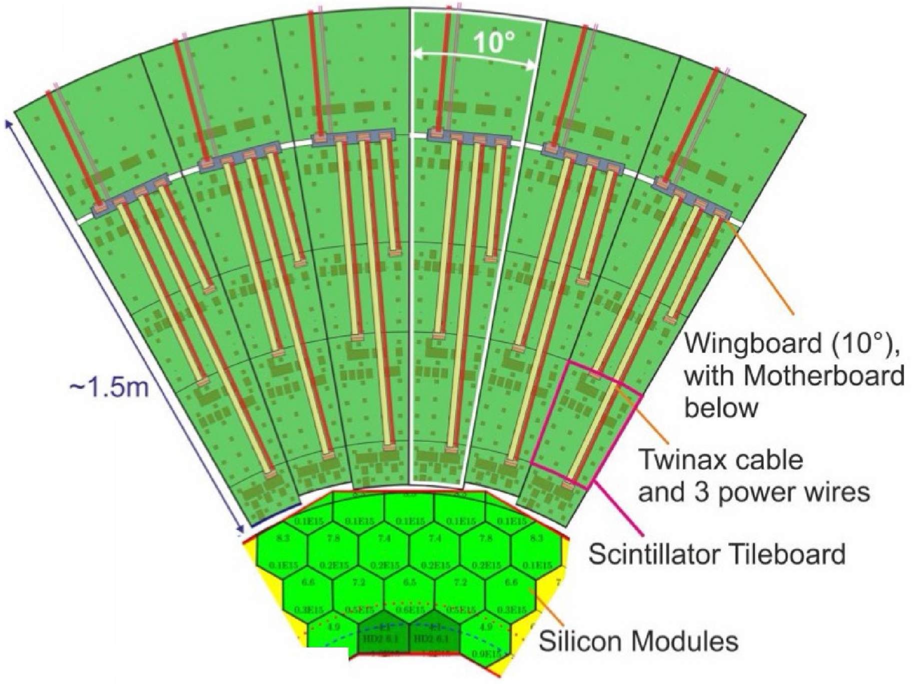
Modular implementation

- Cassettes are collections of trains mounted on copper cooling plates
- Silicon only trains in electromagnetic section
- Mixed (silicon and scintillator) trains in hadronic section
- Each layer is different!
  - Occupancies vary greatly within and between layers

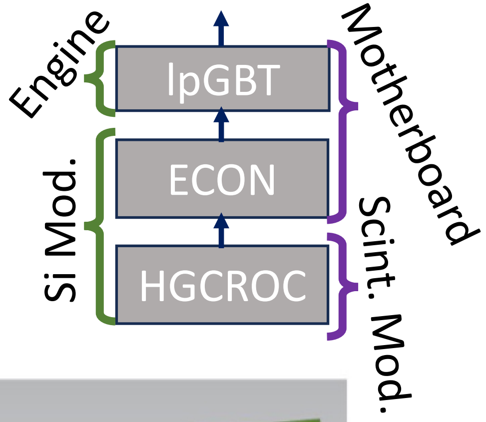


Low density region
- Si sensor 200 or 300 μm thickness
- 192 channels (3 HGCROC) per 8" hexagonal module

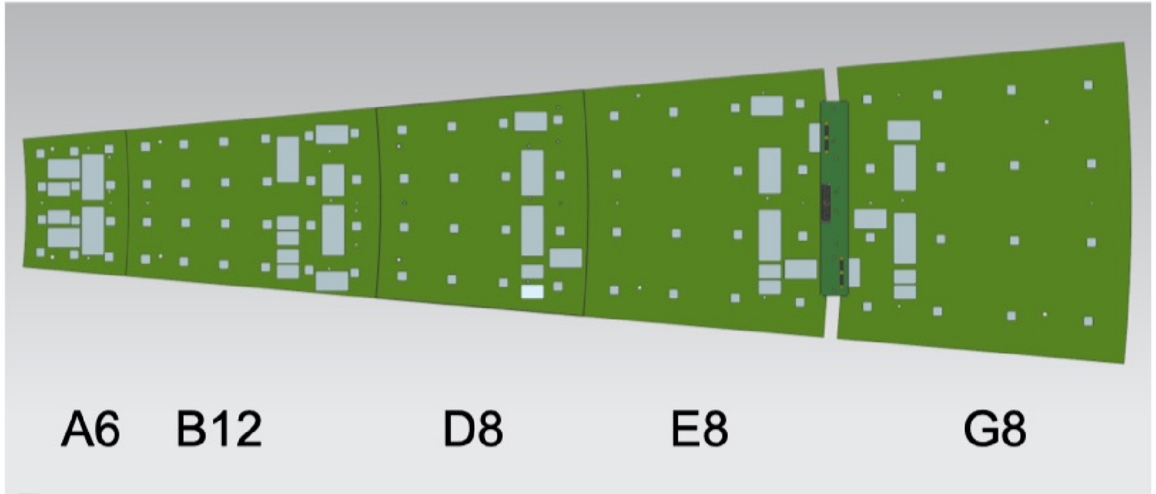
High density region
- Si sensor 120 μm active thickness
- 432 channels (6 HGCROC) per 8" hexagonal module

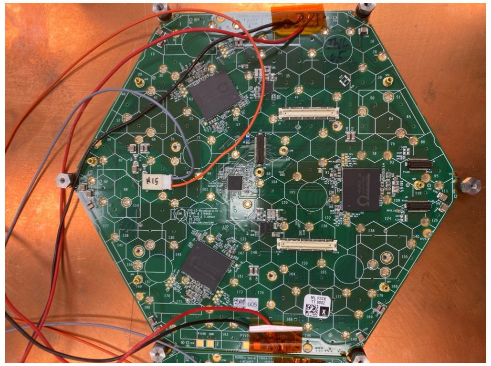


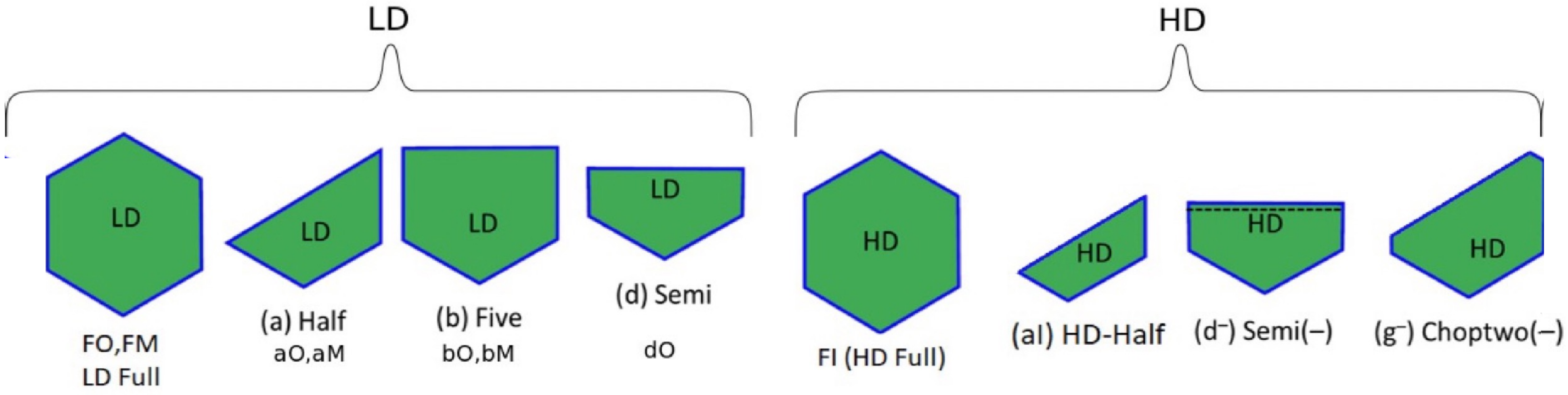
Hexaboards and tileboards



- Many varieties of boards:
  - 3 (6) HGCROCs per LD (HD) hexaboard
  - 1 or 2 HGCROCs per tileboard
- Partial hexagon modules used for the outer edges of the detector layers
  - Require dedicated hexaboards



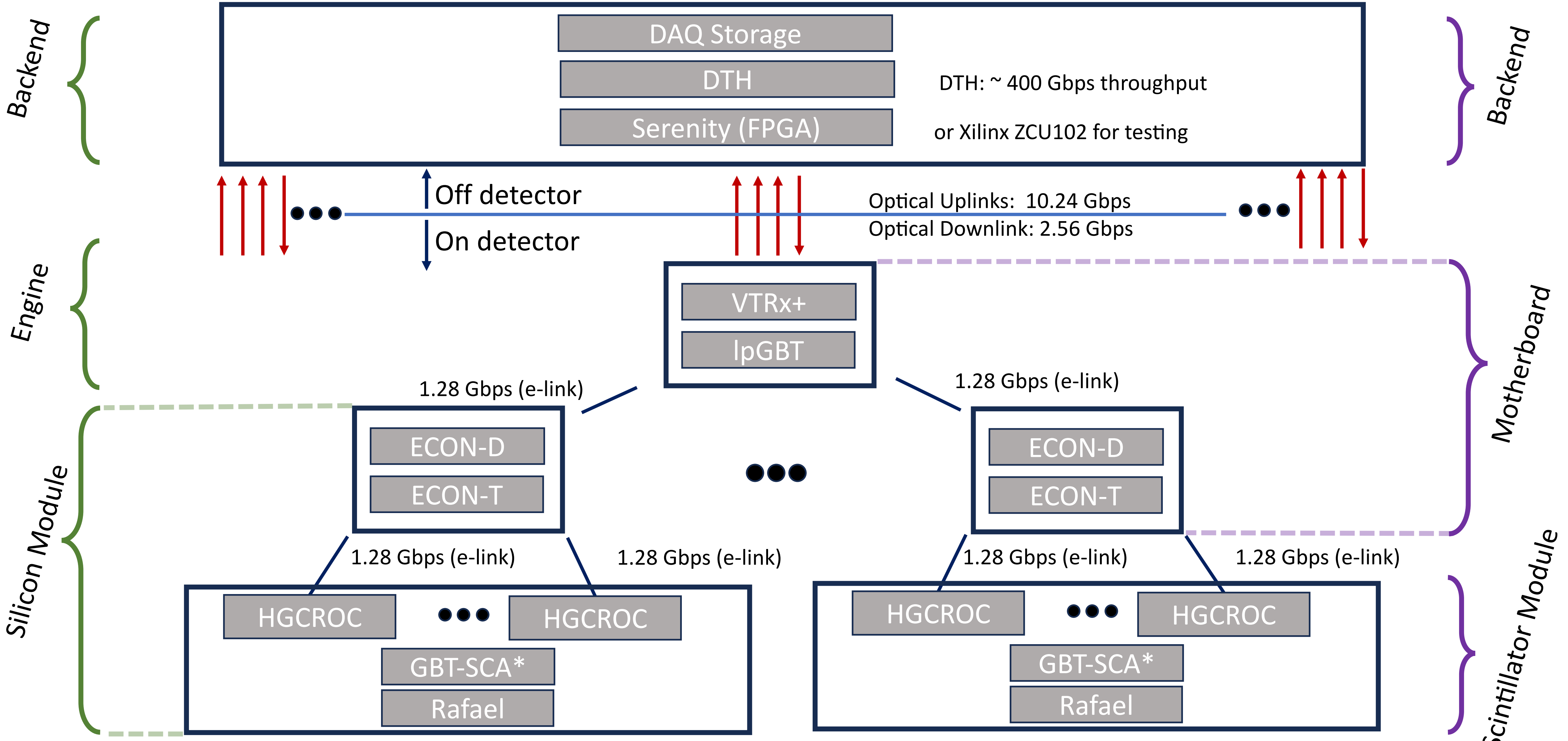




Frontend electronics designed around Custom ASICs

- HGCROC: frontend readout chip, receives and digitizes signals from the sensors (providing ADC, TOT, TDC)
- ECON-T: frontend concentrator chip for trigger path, concentrates trigger channel data via one of 4 trigger algorithms
- ECON-D: frontend concentrator chip for DAQ path, performs channel alignment and zero suppression after L1Accept
- Rafael chip for clock and fast control fanout
- CERN GBT-SCA for slow control signals in the scintillator section
- CERN lpGBT, and VTRx+ for sending and receiving data, clock, and control signals via optical link

Frontend ASICs Overview

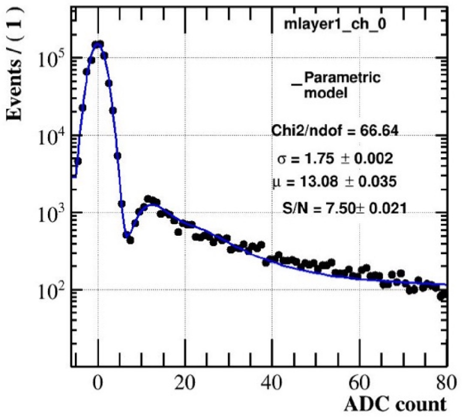


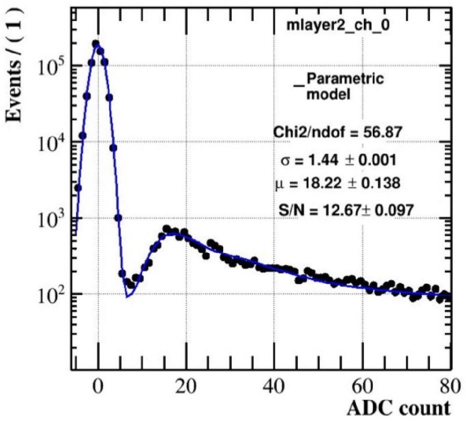
* For scintillator systems only

Silicon modules in test beams 2023

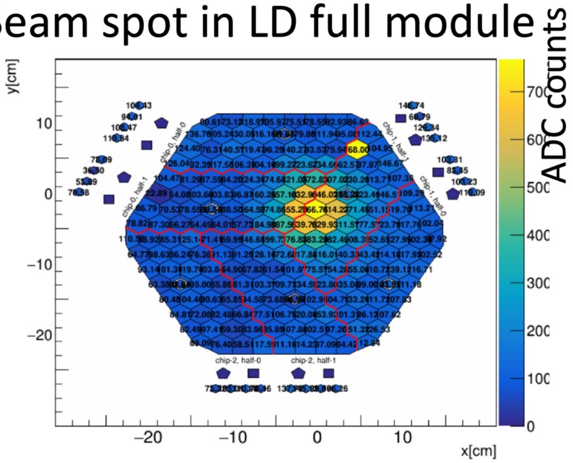
- Multiple successful test beam campaigns for system validation performed with single modules (LD, HD, and partials) and with the full electronic chain (including all ASICs in LD system)

Example of ADC distribution for one channel per layer



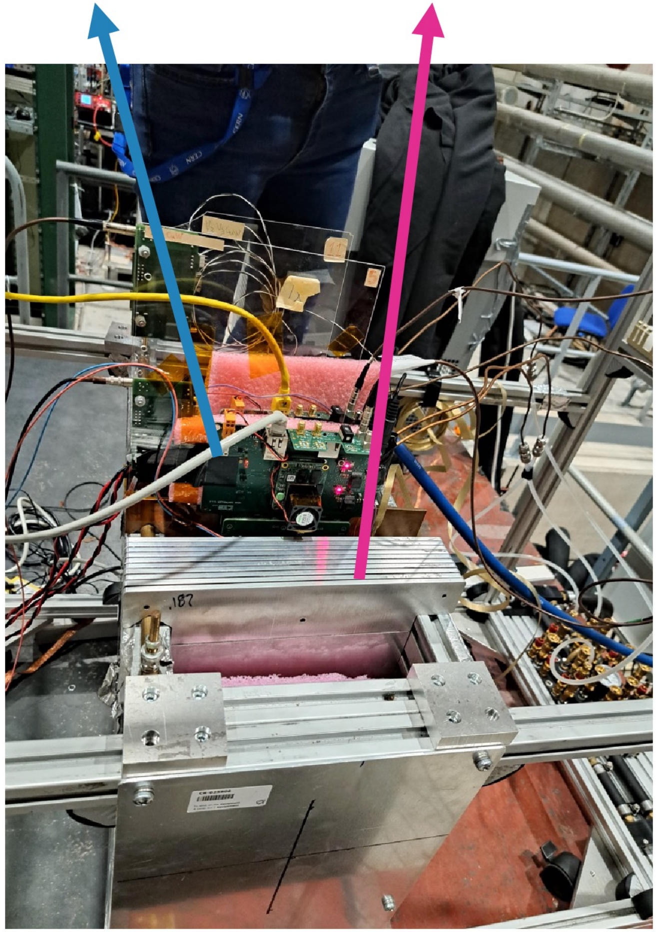


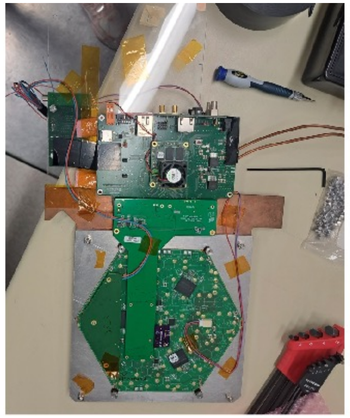
Beam spot in LD full module



modules

absorber

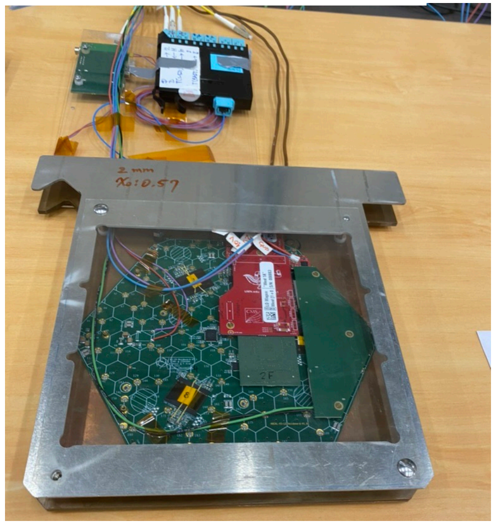




LD full (200 μm)

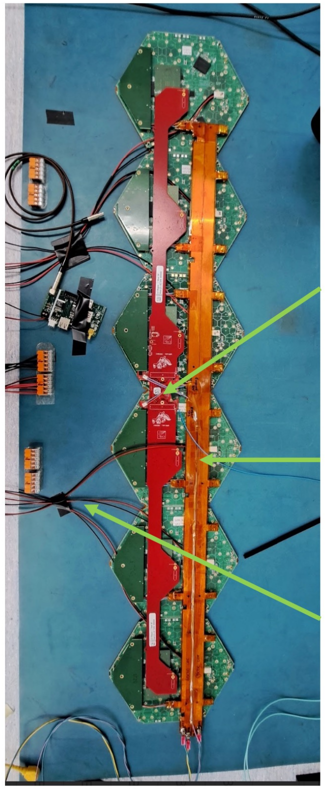
LD right (300 μm)

HD full (120 μm)



Frontend services: BusBars

- On detector powering using BusBars to replace wires
  - Concept now adopted as baseline
  - Heavy-copper flex PCB (two layers 200um copper)
    - Total thickness ~800um
- Advantages:
  - Copper thickness meets DC resistance requirements
  - Tight coupling between supply and returns
  - Integration greatly facilitated
  - Can take the full short-circuit current (no need for fuses at PP0)
  - Intrinsically radiation tolerant (polyimide-based insulation)



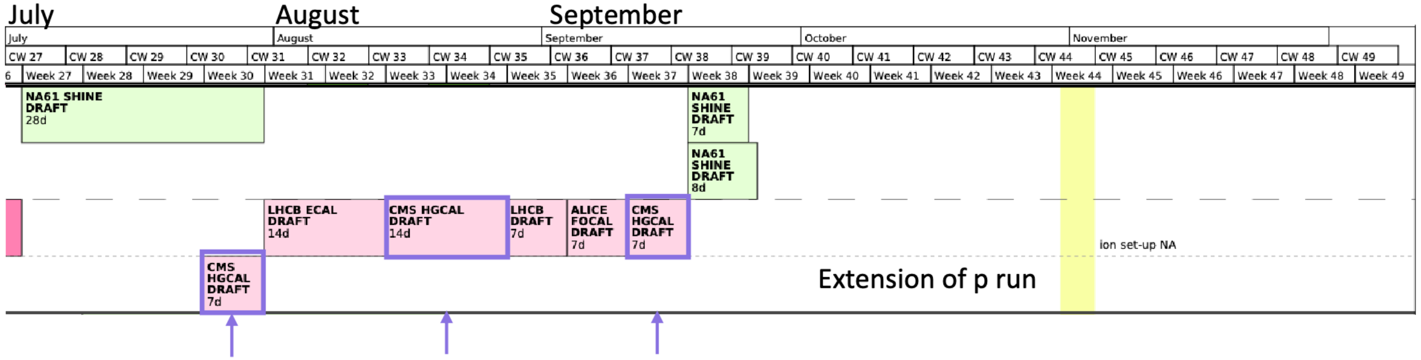
1 engine with 3+3 LD full modules

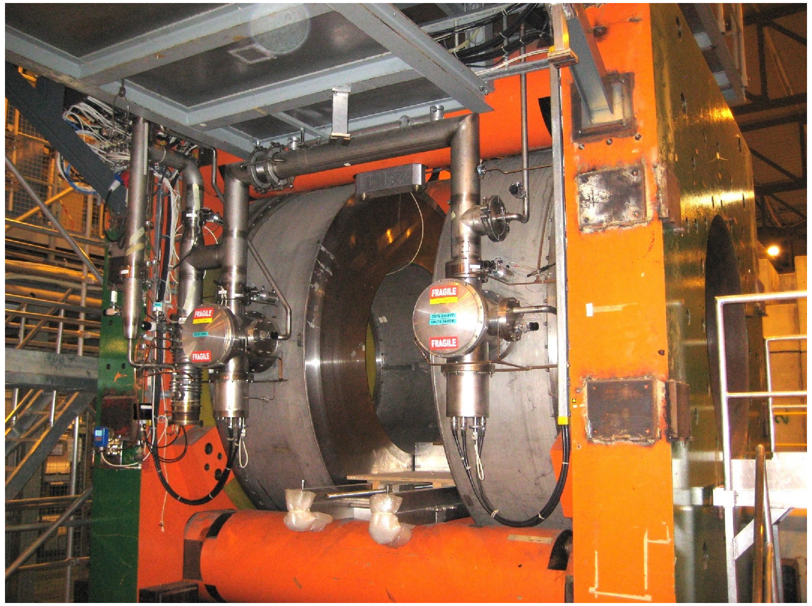
Busbar powering the engine and DCDCs

Bias voltage distribution

Test beams 2024

- Draft schedule for 2024
  - 3(+1) weeks of test beam at the SPS H2 beam in Summer 2024
  - 1 week as a secondary user: setup and prepare for TB data taking
  - Beam: can select particle type (electrons, pions, muons) and beam energy (20-300 GeV)
- Main goal: Test train in magnetic field (up to 3T)
  - Plan to use 1-2 layers with LD modules, 1 layer with HD modules, 1-2 layers with SiPM-on-tile
  - Expect nominal operation without issues as in CMS





Possible configuration
- “T” shaped wagon
- compact system