LHCb Upgrade II Tracking Workshop

UT design and simulation

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2024-03-07

A new UT in UII

Simulation performed with UT in UII condition

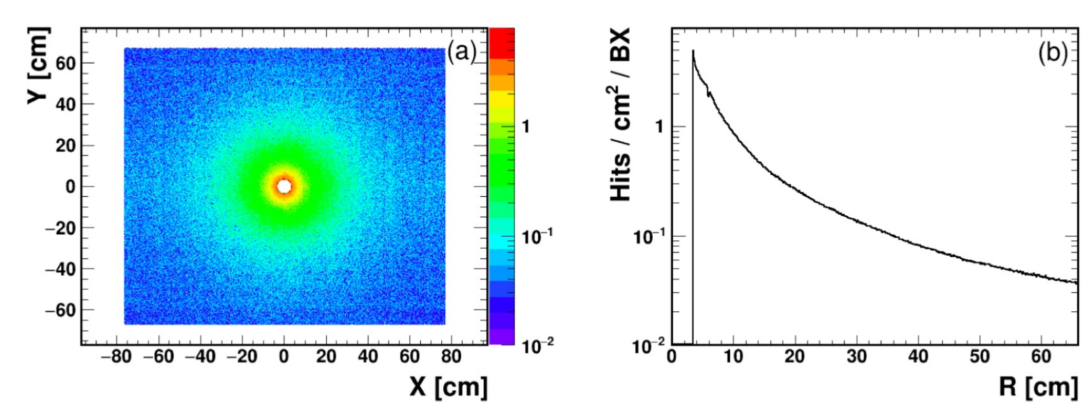
- Max hit density ~ 6 hits/cm^2/BX for beam-beam crossings in pp
- For Pb-Pb ~ 3 hits/cm^2/BX, but multiplicity is higher

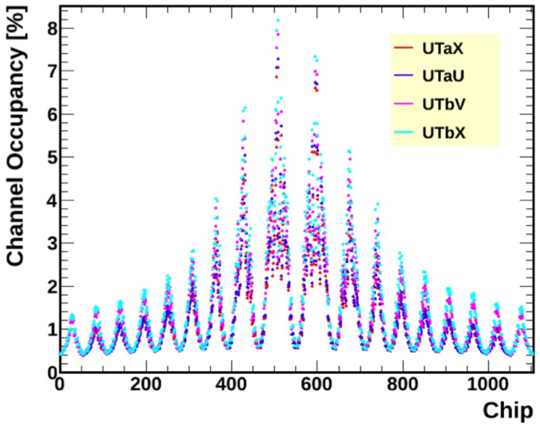
Current UT cannot work safely after x 7.5 increase in luminosity

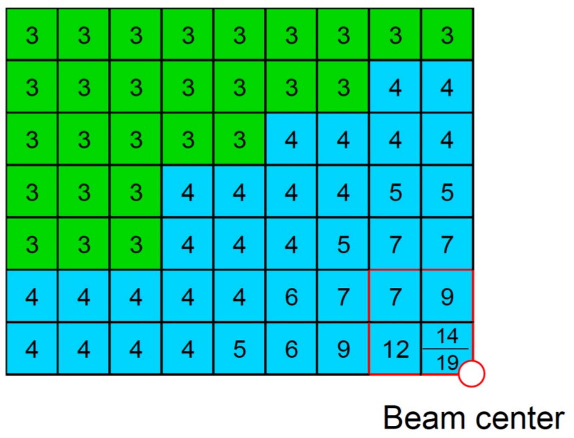
- Max occupancy ~ 10%
- Data rate much more than current UT can handle
- Max fluence of ~ 3 x 10^{15} n_{eq}/cm^2 may be too high for current sensor

UT in UII: A MAPS-based pixel detector

- High Voltage CMOS or CMOS with Small electrode

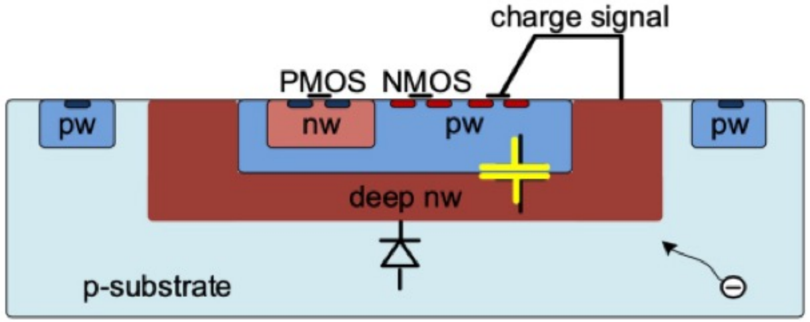




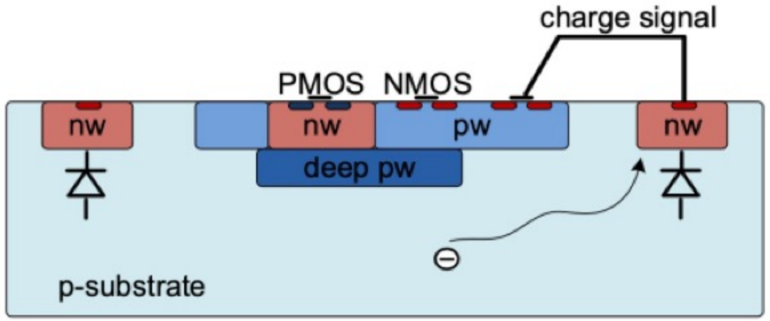


Technical options

High Voltage CMOS



CMOS with small electrode



Two scenarios: HV CMOS or CMOS with small electrode. Each choice has its pros and cons

Will not touch details for chips design, but remind the change of the Chip/pixel size and also the position resolution

Characteristics	CMOS with small electrode	HV-CMOS
Chip size	3.5 x 3.5 cm^2	2.0 x 2.0 cm^2
Pixel size	30 x 30 μm^2	50 x 150 μm^2
Chip thickness	~ 100 um	
Position resolution	5 - 10 μm	15, 40 μm
Time resolution	$\mathcal{O}(1)$ ns	
Power consumption	100 – 300 mW/cm^2	
Radiation dose	3 x 10^{15} n_{eq}/cm^2, or 240 Mrad TID	
Data rate per chip	Up to 30 Gb/s	Up to 9 Gb/s

Outline

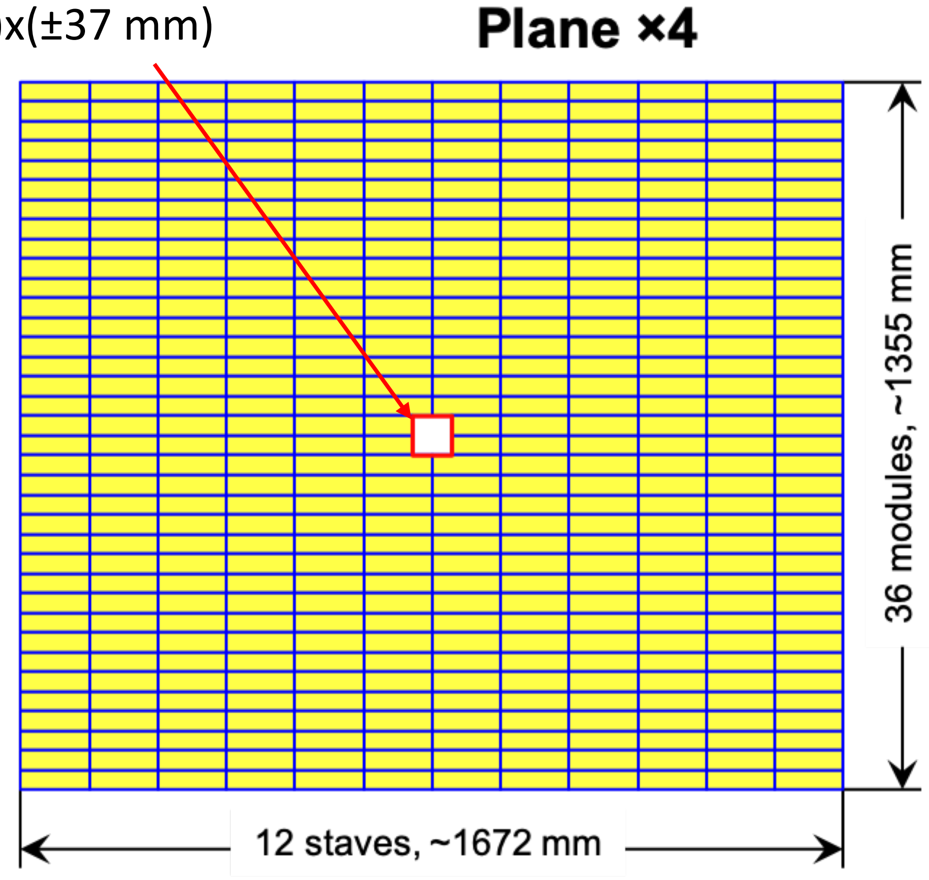
U2UT design
- Detector
- Possible scenarios for scoping document

U2UT detector simulation
- Detector description
- Run 5 events simulating
- Software development in LHCb frame work

UT Geometric configuration

For HV-CMOS design

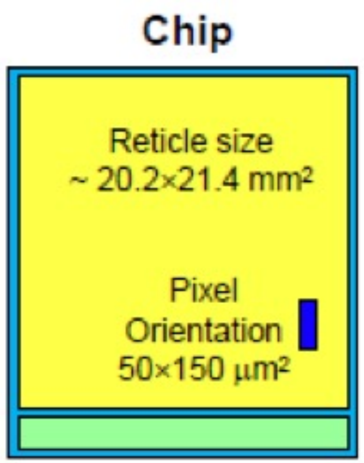
Beam hole inefficient area
(±39 mm)x(±37 mm)



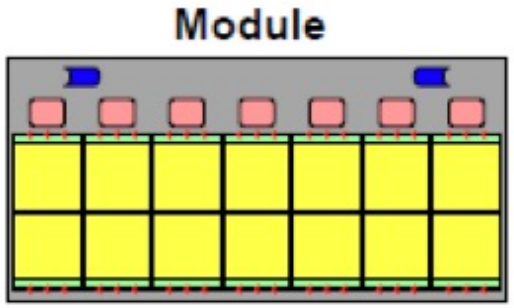
- UT has 4 detector planes (layers), at Z position similar to the current one
- 12 staves for each plane, covers ~ 1672 mm in X direction, with 2mm overlap
- A stave has 36 modules, covers ~1355 mm in Y direction
- A module has 7x2 sensor chip. In the outer regions of each plan dual-modules are used for efficient lbGBT
- The central 4x4 chips are removed for beam pipe, covers (±39 mm)x(±37 mm)
- In total: 4 layers, 48 staves, 1728 modules, 24 128 chips

U2UT Layout

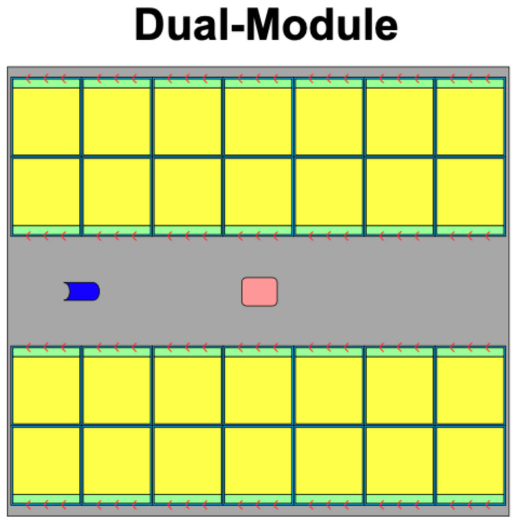
For HV-CMOS design

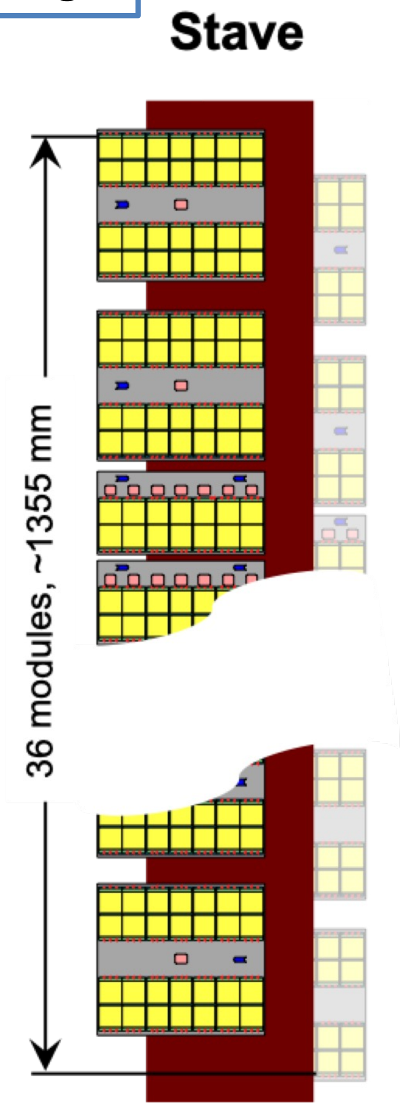


- Reticle size ~ 20.2 x 21.4 mm^2
- Guard ring = 80 µm
  Tolerances ~ 20-40 µm
- Pixel = 50 x 150 µm
  Matrix = 400 x 128
- Periphery ~ 2 mm



Inefficiency ~ 2x100 µm





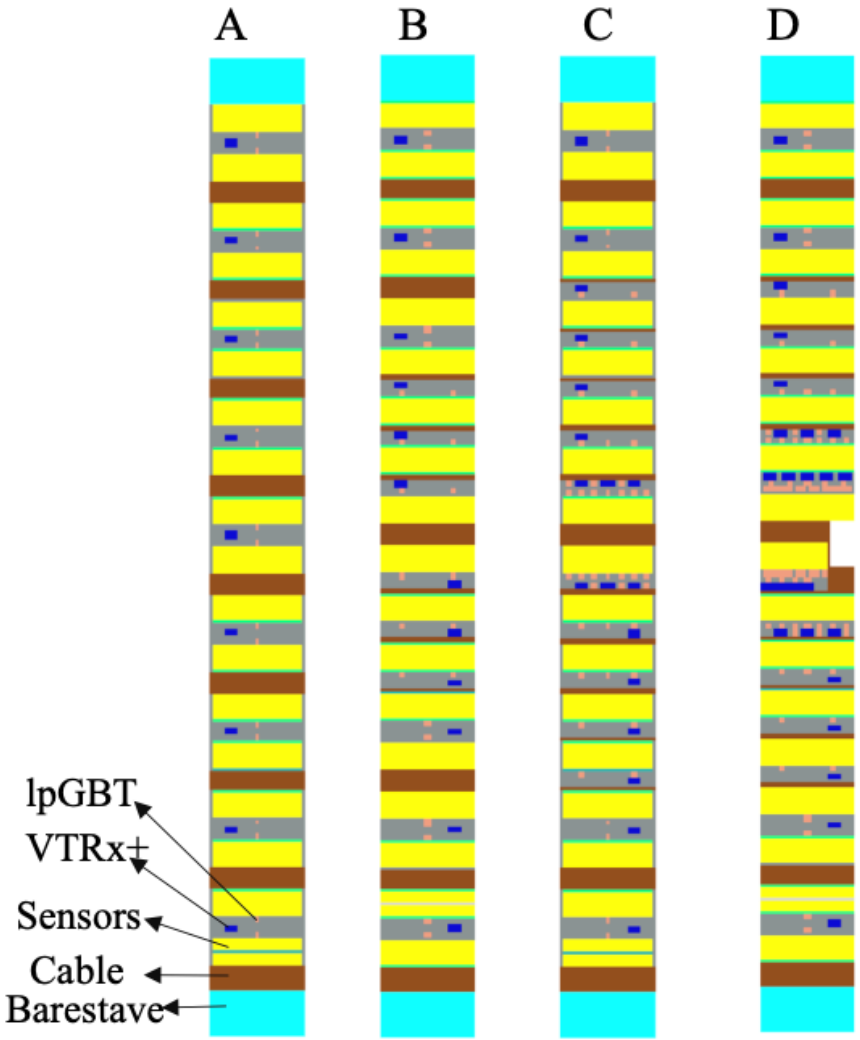
Data read out by lpGBTs, each supports 7/14/28 links of 1.28/0.64/0.32 Gbps bandwidth

- A module has 7x2 chips
- Dual-module for outer region with lower data rate

36 modules are mounted on both sides of a stave with 1mm overlaps, coverage ~ 1355 mm

4-type staves & 5-type modules

For HV-CMOS design

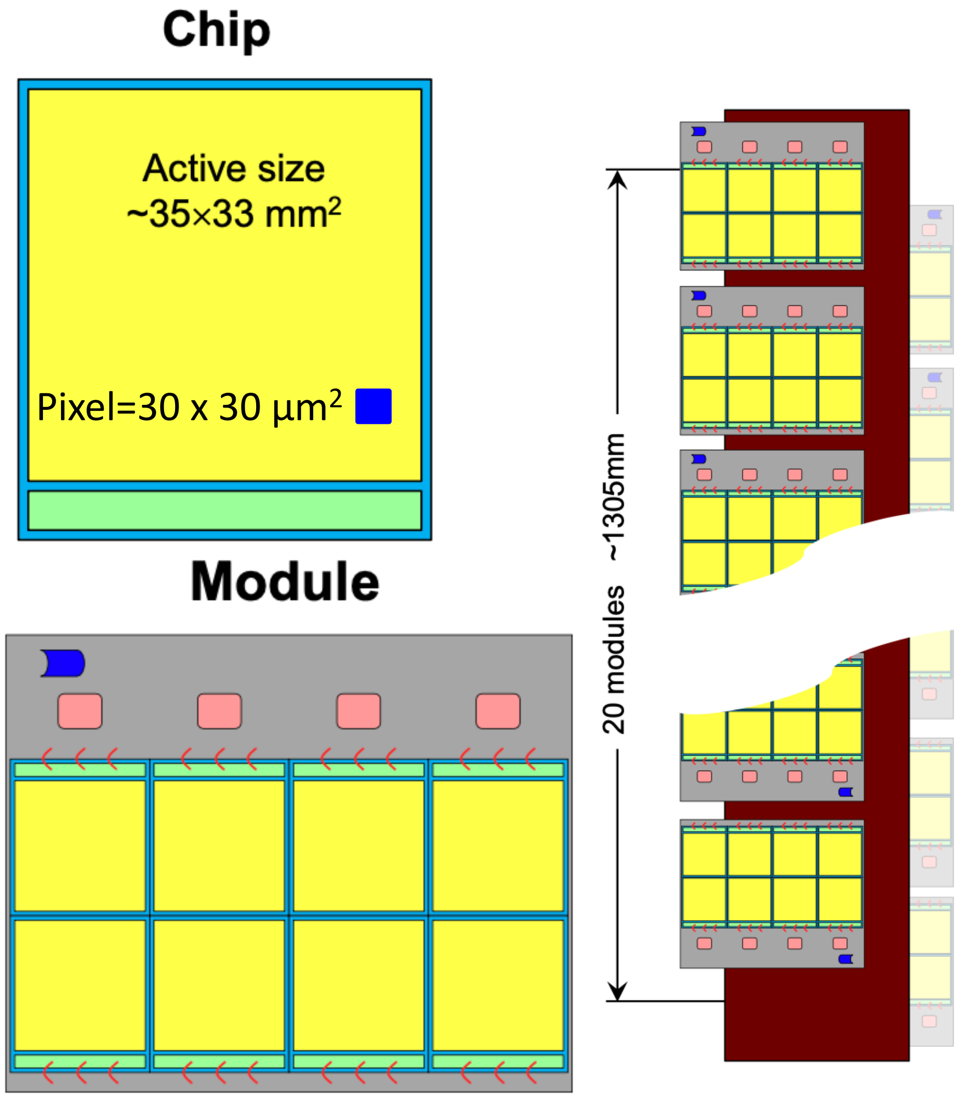


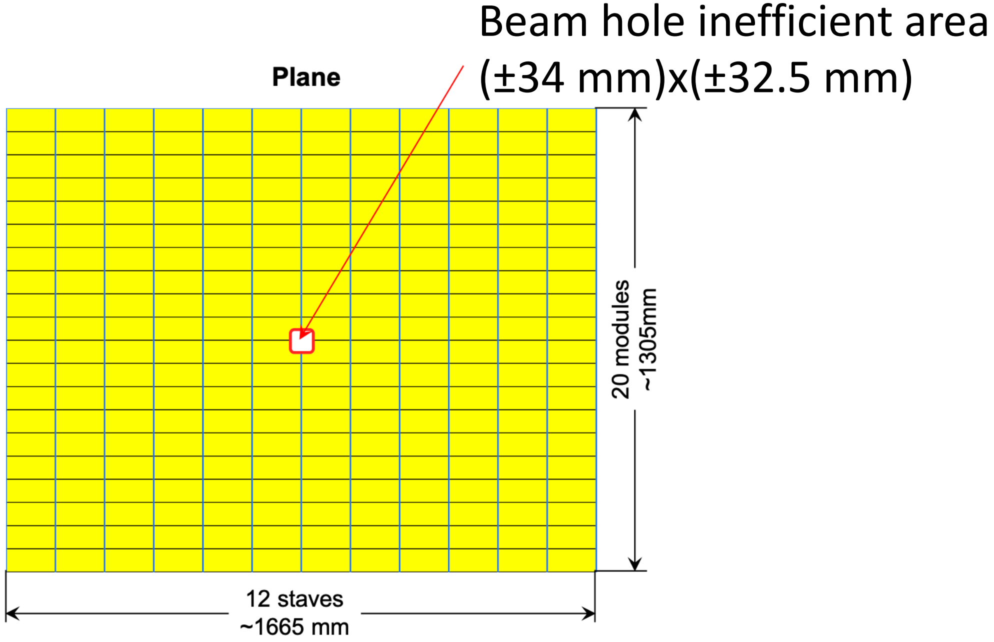
Ring	5	4	3	2	1
e-links / chip	1	1	1	1-3	2-7
Gbps / e-link	0.32	0.64	1.28	1.28	1.28
lpGBT / module	0.5	1	2	7	14/10
Num of modules	1312	240	80	64	32
Num of lpGPTs	656	240	160	448	384

- According to data rate, 5-type modules designed
- UT plan consists of type A, B, C and D staves

Small-electrode sensor design

For small electrode design





A second MAPS technique option: CMOS with small electrode

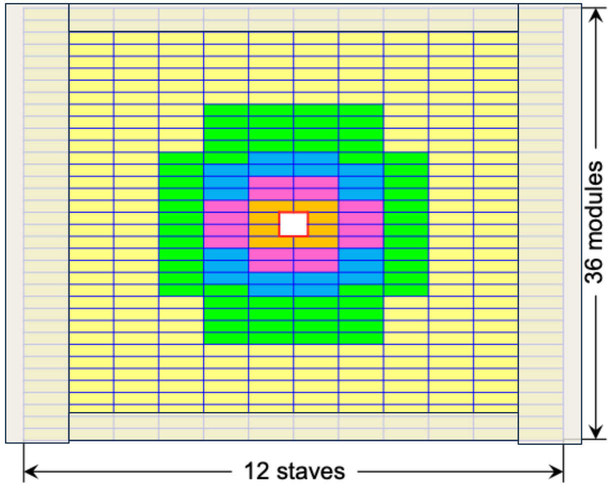
- Pixel size 30 x 30 μm^2; Active size by chip 35 x 33 mm^2
- Each stave consists of 20 modules, same width but shorter length as the one for HV CMOS

Other possible scenarios of U2UT

Details for the performance based on these designs can be found in Benjamin and Carlos talks

Reduce coverage: 12->10 staves x (36 -> 32) modules (10-stave structure)

- ➢ Reduce 26% detection area

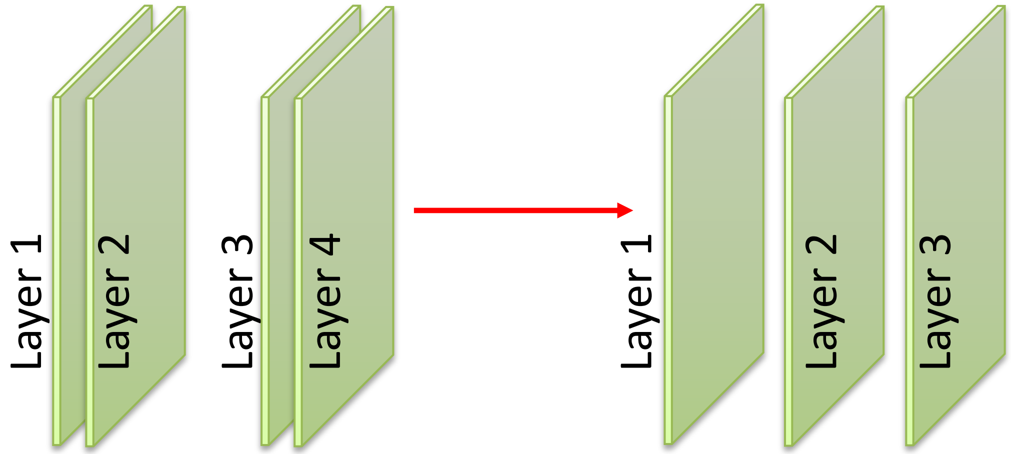


3-layer detector

- ➢ # of Si chips reduced to 75% ➔ cost reduce to 80%
- ➢ Efficiency reduced by ~%, but $\mathcal{P}_{\text{Ghost}}$ increased huge

Reduce the peak luminosity (1.5->1.0)x10^{34} cm^{-2}s^{-1}

- ➢ Designs of chips & modules are less difficult



U2UT design

- Detector
- Possible scenarios for scoping document

U2UT detector simulation

- Detector description
- Run 5 events simulating
- Software development in LHCb frame work

Detector modelling in the software

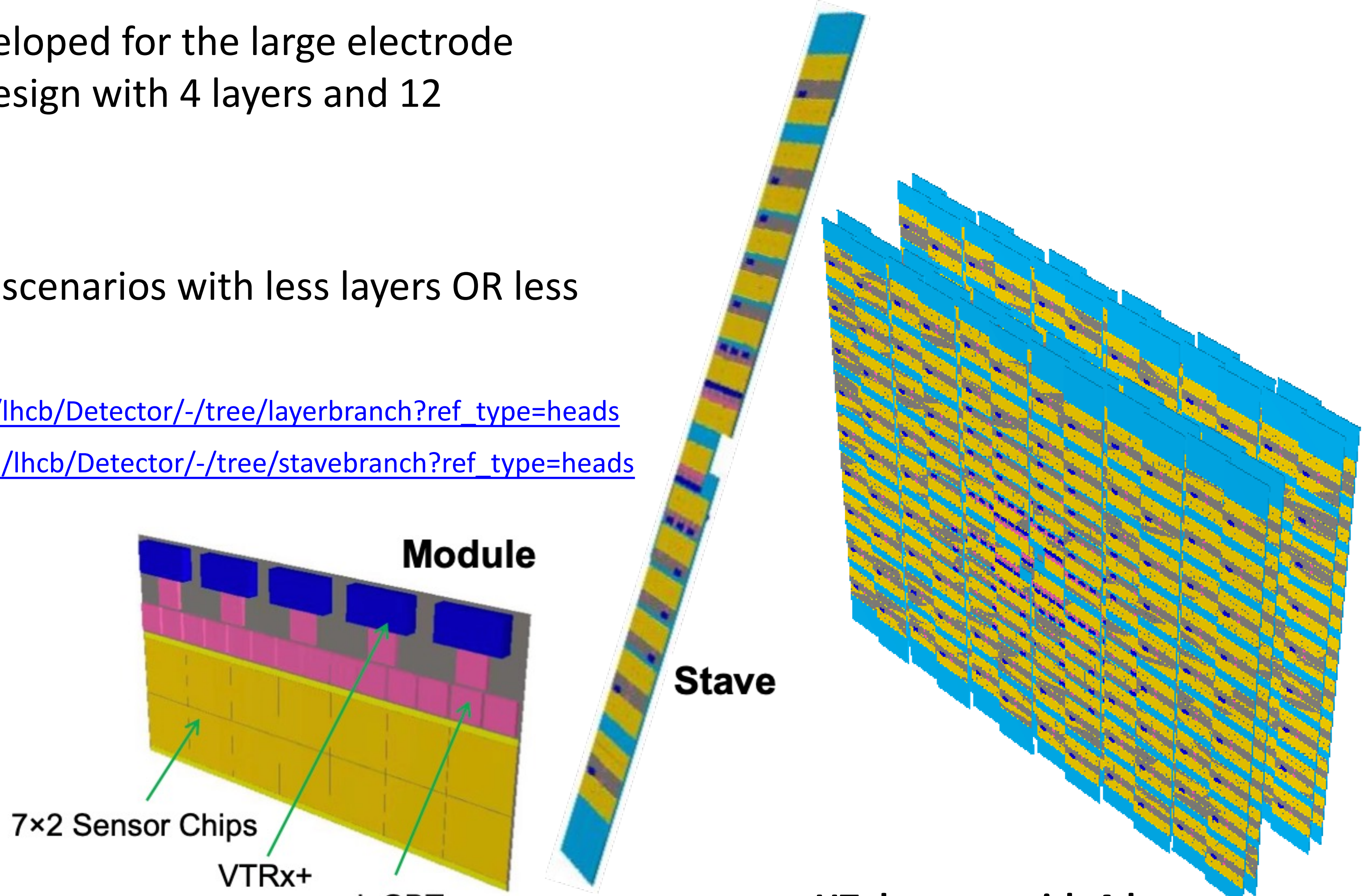
Detector description has been developed for the large electrode solution (HV-CMOS). The default design with 4 layers and 12 stave/layer applied

- MR into LHCb $Detector ready

For scoping document studies, the scenarios with less layers OR less staves also ready at

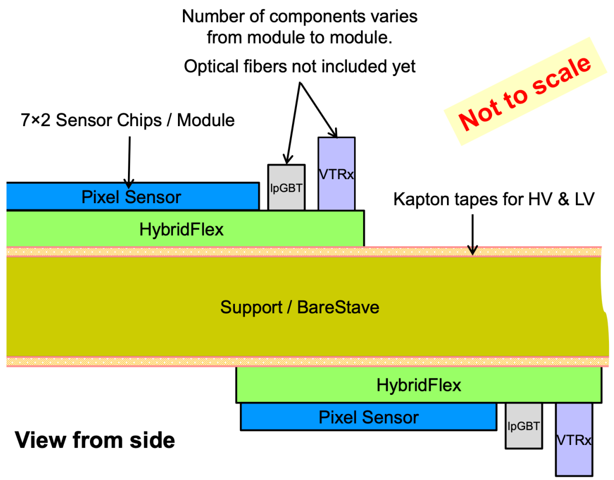
- 3-layers design: https://gitlab.cern.ch/lhcb/Detector/-/tree/layerbranch?ref_type=heads
- 10-stave design: https://gitlab.cern.ch/lhcb/Detector/-/tree/stavebranch?ref_type=heads

For the small electrode solution, development ongoing



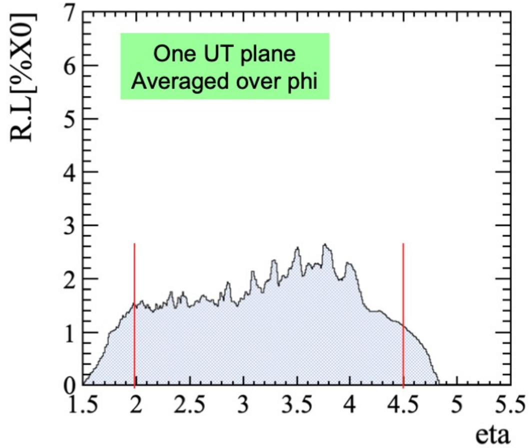
UT detector with 4-layer structure

Radiation length



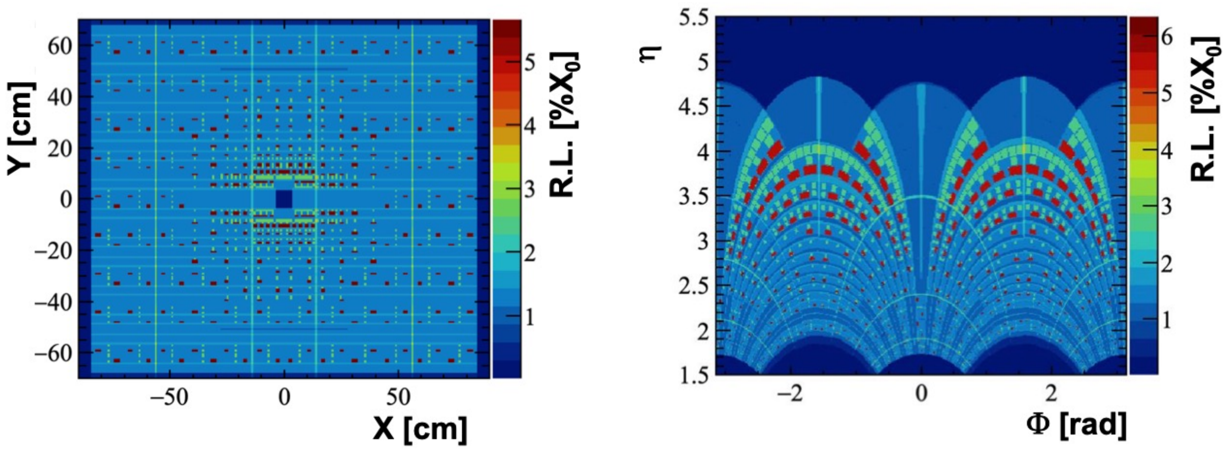
Not the final version, only for software development

- VTRx+ and lpGBT composite to be optimized with better information
- Some electronic components not included yet
- HybridFlex need a thinner design



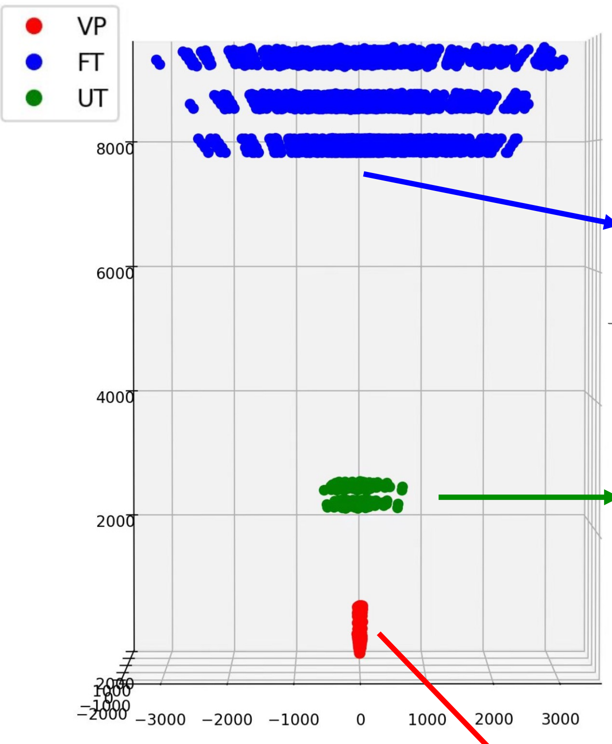
Similar level as current UT

(Preliminary)	Thickness [mm]	W x L [mm]	RL ($2<\eta<4.5$) [% X_0]
Pixel Sensor	0.200	20.2 x 21.4	0.24
lpGBT	1.250	9 x 9	0.25
VTRx+	4.000	10 x 20	0.27
HybridFlex	0.300	142 x 75	0.42
Kapton Tape	0.100	142 x full	0.14
BareStave	4.000	142 x full	0.21
One plane	**-**	**1.54**	**1.54**

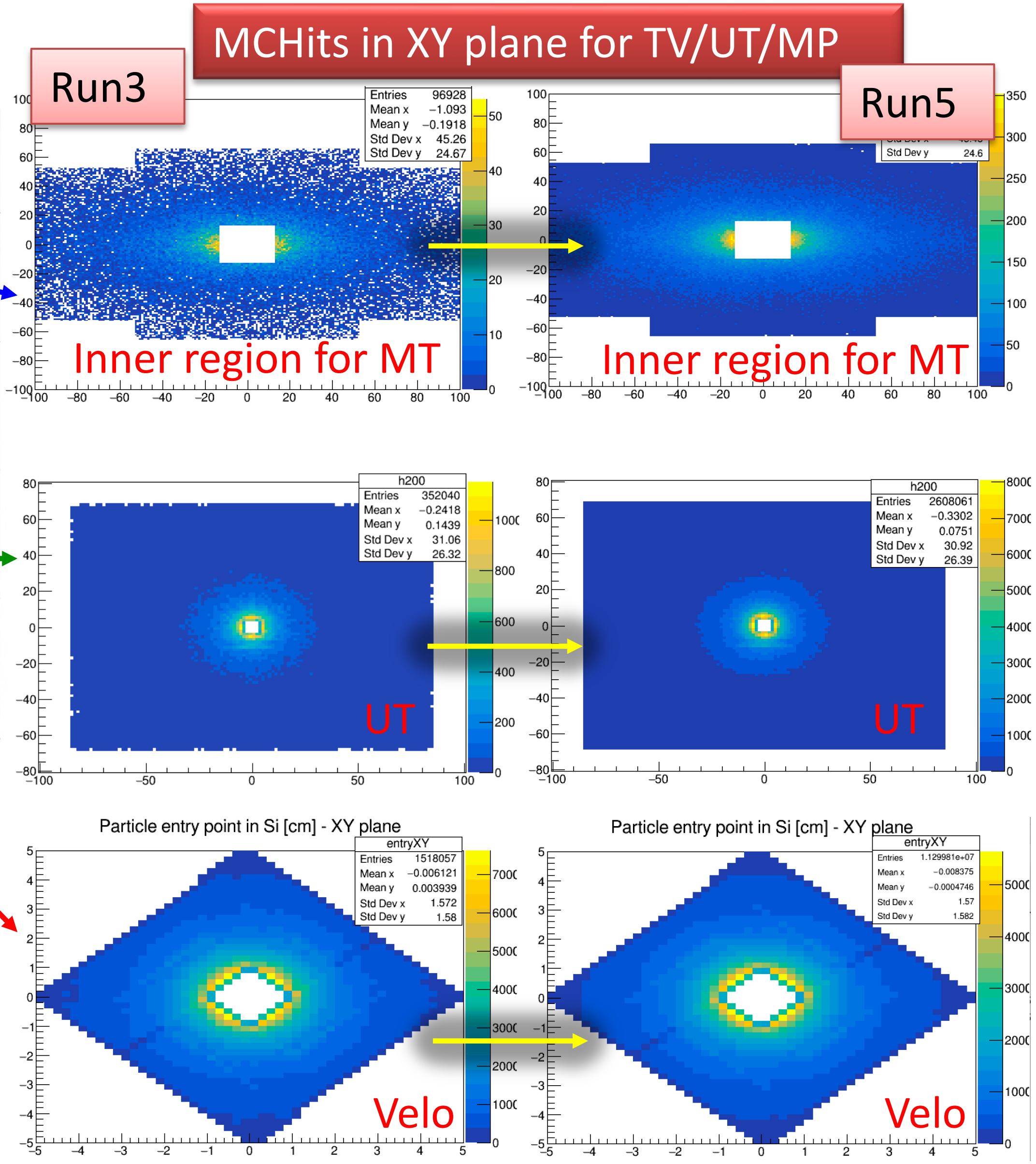


Gauss outputs for U2UT default design

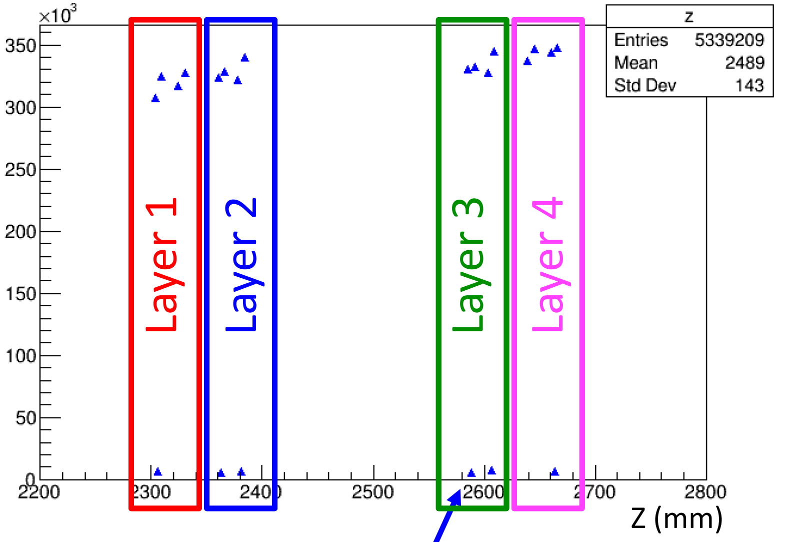
U2UT added into LHCb trackers and Gauss works for it



MCHits in XZ plane for 1 evt @ run5 condition



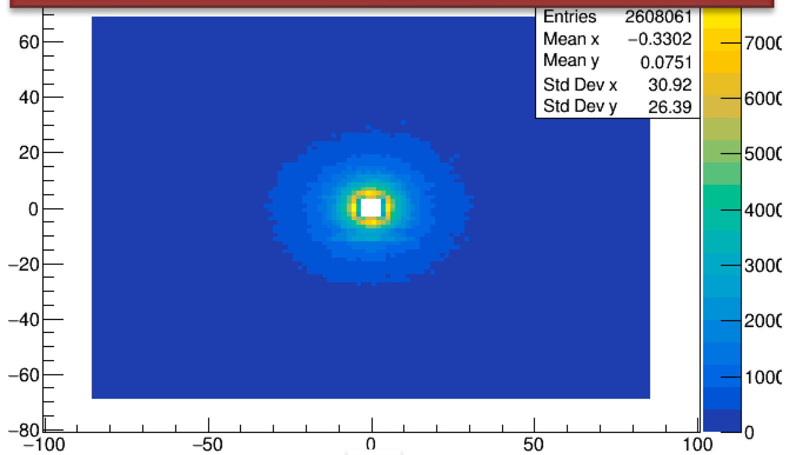
MCHits in Z direction in UT region

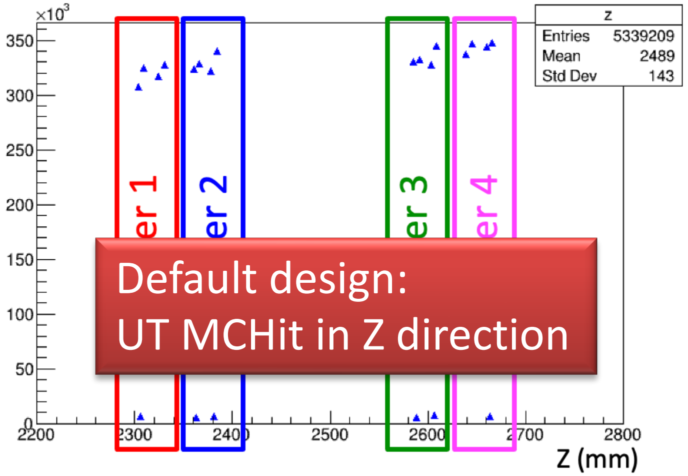


Hits due to overlap btw chips

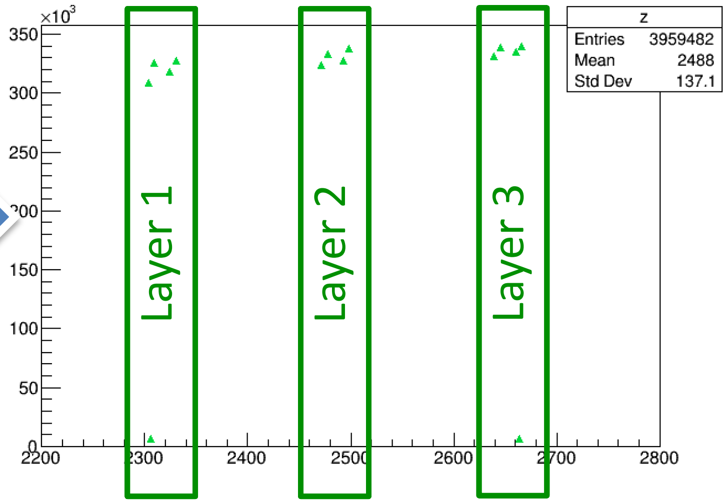
Gauss outputs for other scenarios

Default design: UT MCHit in XY plane

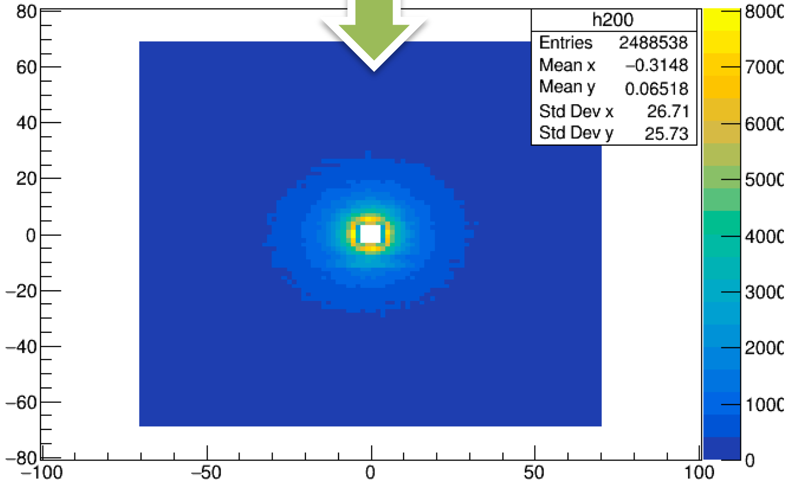




Default design:
UT MCHit in Z direction



3-layer design:
UT MCHit in Z direction



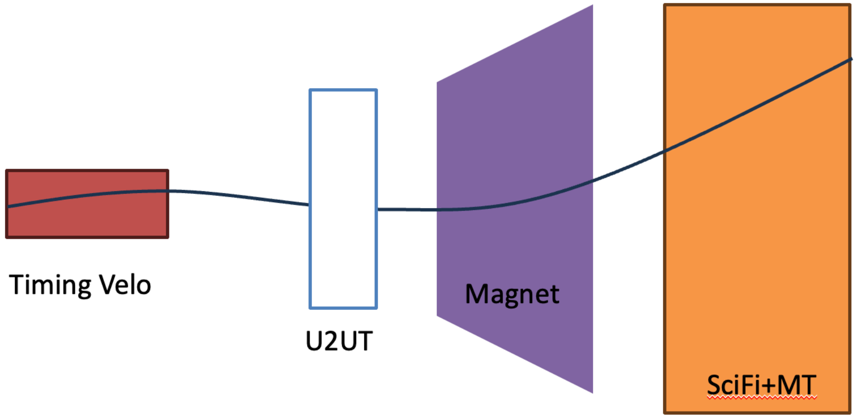
10-stave design: UT MCHit in XY plane

Two scenarios consider now, works well and ready for tracking studies

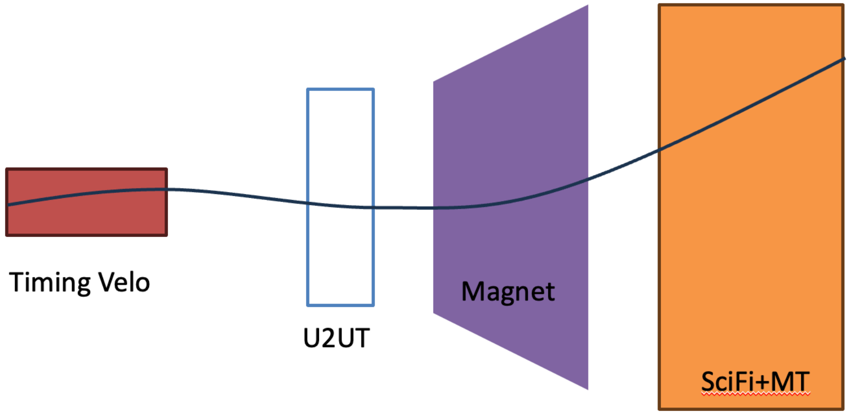
- ➢ The Gauss job runs with
  Gauss/test_run5_mj
  LHCb/run5_withUP
  Detector/layerbranch OR Detector/stavebranch

More possibility under development

UT in long track system



VELO-SciFi tracks w/o UT



VELO-SciFi tracks w/ UT tracks

Long tracks reconstructed w/ or w/o UT, by fitting in both XZ and YZ plane

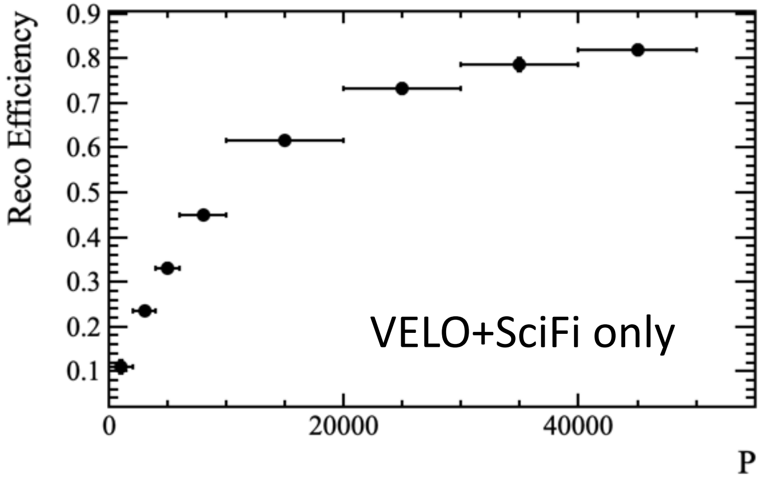
- In XZ plane, a 4th-order polynomial used for Magnet effects
- In YZ plane, a linear func. used

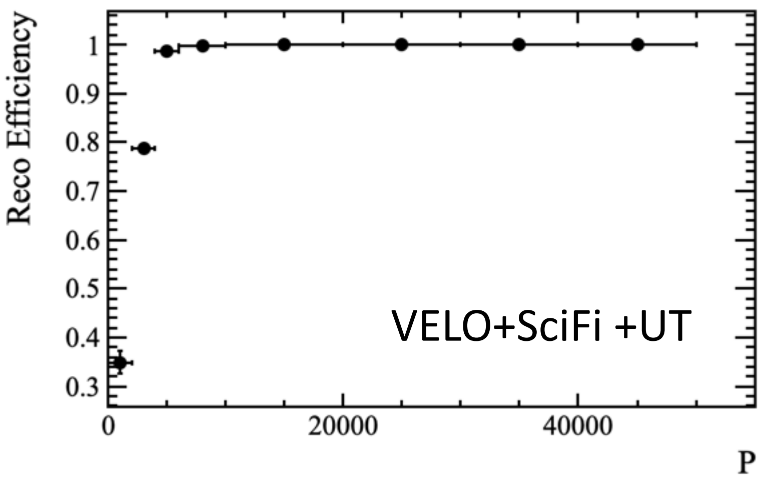
For a quick test, we only select Kaon tracks, and run3 condition

VELO+SciFi only : the total efficiency is 50.18+/-0.41 %
and the “ghost rate” is 34.24+/-0.12 %

Drop of the efficiency due to a rough x^2/ndof cut

VELO+SciFi +UT : the total efficiency is 94.36+/-0.19 %
and the “ghost rate” is 4.54+/-0.01 %

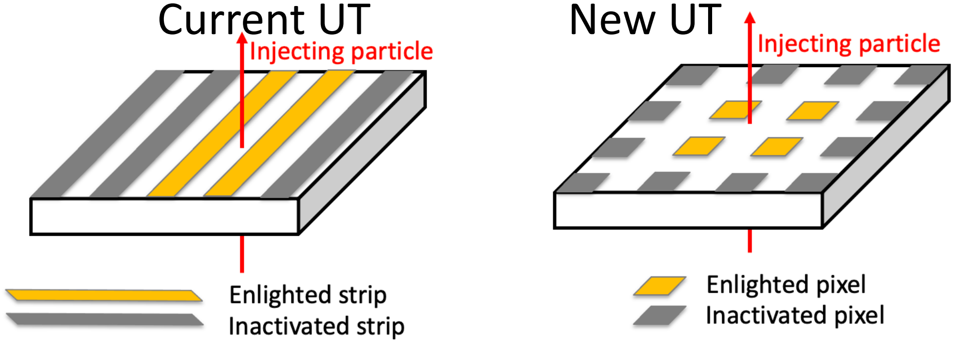




More details can be found in Benjamin and Carlos talks

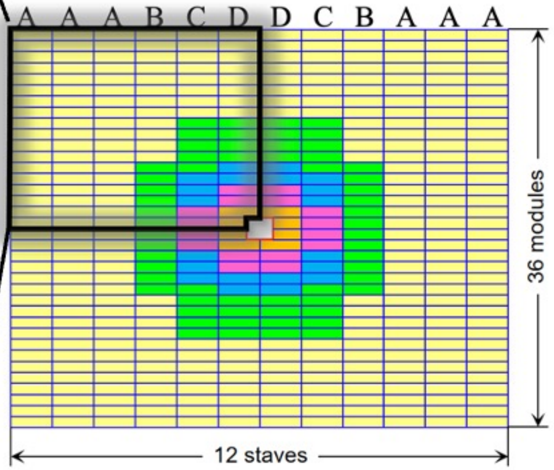
Development in LHCb framework

For UT detector, the simulation for digitization is done
- Based on large electrode tech., HV-CMOS
- New algorithms for pixels instead of strips
- FE simulation parameters copy from current UT

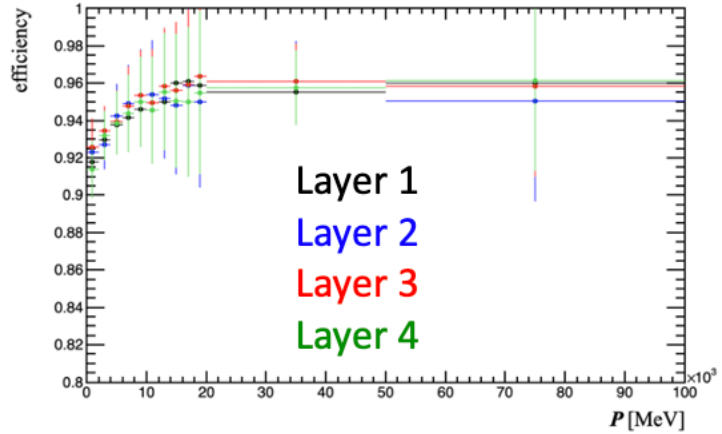


Averaged pixel occupancy (‰) on most busy chips of the modules

0.003	0.004	0.003	0.004	0.005	0.005
0.003	0.004	0.004	0.004	0.007	0.004
0.003	0.004	0.004	0.005	0.004	0.005
0.003	0.003	0.004	0.008	0.006	0.006
0.003	0.004	0.009	0.006	0.006	0.006
0.006	0.008	0.006	0.008	0.007	0.010
0.004	0.005	0.007	0.005	0.006	0.007
0.004	0.005	0.006	0.008	0.009	0.009
0.004	0.005	0.006	0.009	0.010	0.015
0.005	0.005	0.009	0.009	0.011	0.013
0.006	0.008	0.006	0.008	0.013	0.017
0.005	0.006	0.007	0.011	0.020	0.019
0.004	0.006	0.009	0.012	0.020	0.025
0.006	0.006	0.010	0.013	0.024	0.032
0.004	0.006	0.009	0.015	0.031	0.057
0.005	0.006	0.009	0.017	0.034	0.088
0.006	0.011	0.009	0.018	0.049	0.256
0.009	0.008	0.016	0.021	0.047	0.225



Particles response efficiency as a function of particle momentum per layer



- Hottest pixel occupancy estimated based on 1.2K miniBias MC events, where VELO and FT are current ones
- Consistent with estimation in FTDR

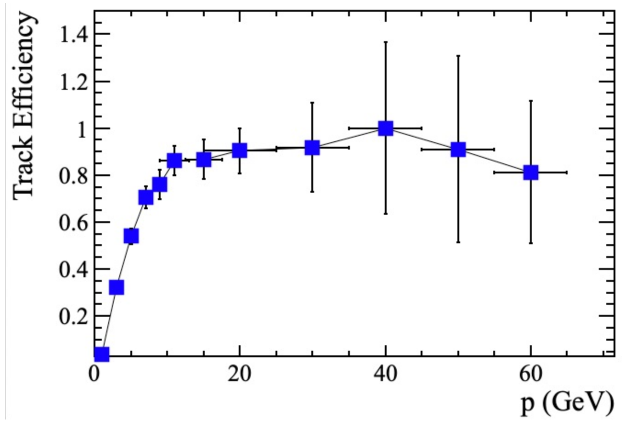
Tracking in LHCb framework

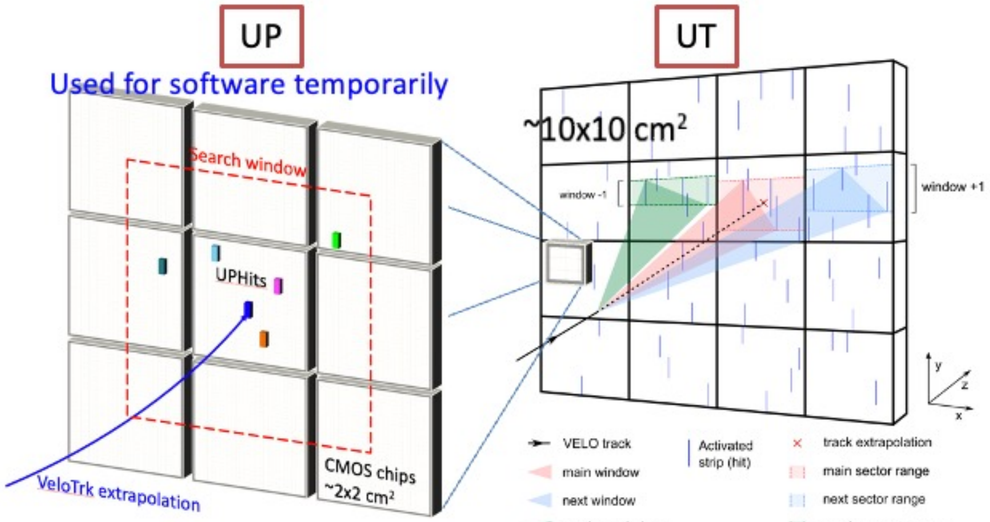
Development of U2UT detector in LHCb tracking system ongoing

- Two methods: (1) UpstreamTrack; (2) StandaloneTrack

For UpstreamTrack: algorithm similar as current UT, but much small search window in UT thanks to the better special resolution in both X and Y

- Inputs can be smeared MCHits OR UTHits decoded from RawBank






```
UpstreamTrackChecker_9ecba7fd          INFO Results
UpstreamTrackChecker_9ecba7fd          INFO **** Upstream                                      2589 tracks including          34 ghosts [ 1.31 %], Event average  1.01 % ****
UpstreamTrackChecker_9ecba7fd          INFO   01_velo                                     :    2426 from     7790 [ 31.14 %]     12 clones [ 0.49 %], purity: 99.92 %, hitEff: 98.83 %
UpstreamTrackChecker_9ecba7fd          INFO   02_velo+UT                                  :    2426 from     7084 [ 34.25 %]     12 clones [ 0.49 %], purity: 99.92 %, hitEff: 98.83 %
UpstreamTrackChecker_9ecba7fd          INFO   03_velo+UT_P>5GeV                           :    1895 from     2631 [ 72.03 %]      8 clones [ 0.42 %], purity: 99.91 %, hitEff: 99.02 %
UpstreamTrackChecker_9ecba7fd          INFO   04_velo+notLong                             :     403 from     3543 [ 11.37 %]      2 clones [ 0.49 %], purity: 99.86 %, hitEff: 98.97 %
UpstreamTrackChecker_9ecba7fd          INFO   05_velo+UT+notLong                          :     403 from     2839 [ 14.20 %]      2 clones [ 0.49 %], purity: 99.86 %, hitEff: 98.97 %
UpstreamTrackChecker_9ecba7fd          INFO   06_velo+UT+notLong_P>5GeV                   :     245 from      359 [ 68.25 %]      1 clones [ 0.41 %], purity: 99.86 %, hitEff: 99.36 %
UpstreamTrackChecker_9ecba7fd          INFO   07_long                                     :    2023 from     4247 [ 47.63 %]     10 clones [ 0.49 %], purity: 99.93 %, hitEff: 98.80 %
UpstreamTrackChecker_9ecba7fd          INFO   07_long_strange                             :      71 from      245 [ 28.98 %]      1 clones [ 1.39 %], purity: 99.80 %, hitEff: 98.68 %
UpstreamTrackChecker_9ecba7fd          INFO   08_long_P>5GeV                              :    1650 from     2273 [ 72.59 %]      7 clones [ 0.42 %], purity: 99.92 %, hitEff: 98.97 %
UpstreamTrackChecker_9ecba7fd          INFO   08_long_strange_P>5GeV                      :      58 from       88 [ 65.91 %]      0 clones [ 0.00 %], purity: 99.75 %, hitEff: 98.71 %
UpstreamTrackChecker_9ecba7fd          INFO   09_long_fromB                               :       3 from        4 [ 75.00 %]      0 clones [ 0.00 %], purity:100.00 %, hitEff:100.00 %
UpstreamTrackChecker_9ecba7fd          INFO   09_long_fromD                               :      32 from       54 [ 59.26 %]      0 clones [ 0.00 %], purity:100.00 %, hitEff: 99.22 %
UpstreamTrackChecker_9ecba7fd          INFO   10_long_fromB_P>5GeV                        :       3 from        3 [100.00 %]      0 clones [ 0.00 %], purity:100.00 %, hitEff:100.00 %
UpstreamTrackChecker_9ecba7fd          INFO   10_long_fromD_P>5GeV                        :      24 from       29 [ 82.76 %]      0 clones [ 0.00 %], purity:100.00 %, hitEff: 98.96 %
UpstreamTrackChecker_9ecba7fd          INFO   11_long_electrons                           :      19 from       93 [ 20.43 %]      0 clones [ 0.00 %], purity:100.00 %, hitEff: 98.95 %
UpstreamTrackChecker_9ecba7fd          INFO   14_long_fromB_P>3GeV_Pt>0.5GeV              :       2 from        2 [100.00 %]      0 clones [ 0.00 %], purity:100.00 %, hitEff:100.00 %
UpstreamTrackChecker_9ecba7fd          INFO   14_long_fromD_P>3GeV_Pt>0.5GeV              :      27 from       30 [ 90.00 %]      0 clones [ 0.00 %], purity:100.00 %, hitEff: 99.07 %
UpstreamTrackChecker_9ecba7fd          INFO   14_long_strange_P>3GeV_Pt>0.5GeV            :      46 from       59 [ 77.97 %]      0 clones [ 0.00 %], purity: 99.69 %, hitEff: 98.91 %
UpstreamTrackChecker_9ecba7fd          INFO   15_UT_long_fromB_P>3GeV_Pt>0.5GeV           :       2 from        2 [100.00 %]      0 clones [ 0.00 %], purity:100.00 %, hitEff:100.00 %
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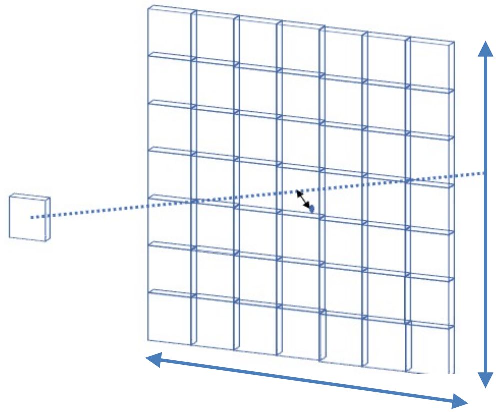
UT standalone track in LHCb framework

More details can be found in Benjamin and Carlos talks

UT standalone track in LHCb framework developing

- Loop over "1st-layer" hits and those in the searching window on downstream layers
- Pickup the "good" tracks with MIN chisq from two linear fits in both XZ and YZ planes



7 x 7 chips as searching window

- Smeared MCHits as input

The interface to LHCb tracking system under developed

UT standalone track at Run5

Evt number	1	10
UTHits Related MCParticle	1731	15766
3-hit real track can reco	632	6113
3-hit reconstructed right unique track	604	5824
Track efficiency	604/632~95%	5824/6113~95%
Clone track of 3-hit track	37	393
Ghost track of 3-hit track	105	926
Ghost rate	105/632~16%	926/6113~15%
4-hit real track can reco	605	5895
4-hit reconstructed right unique track	536	5081
Track efficiency	536/605~88%	5081/5895~86%
Clone track of 4-hit track	51	544
Ghost track of 4-hit track	5	46
Ghost rate	5/605~0.8%	46/5895~0.7%

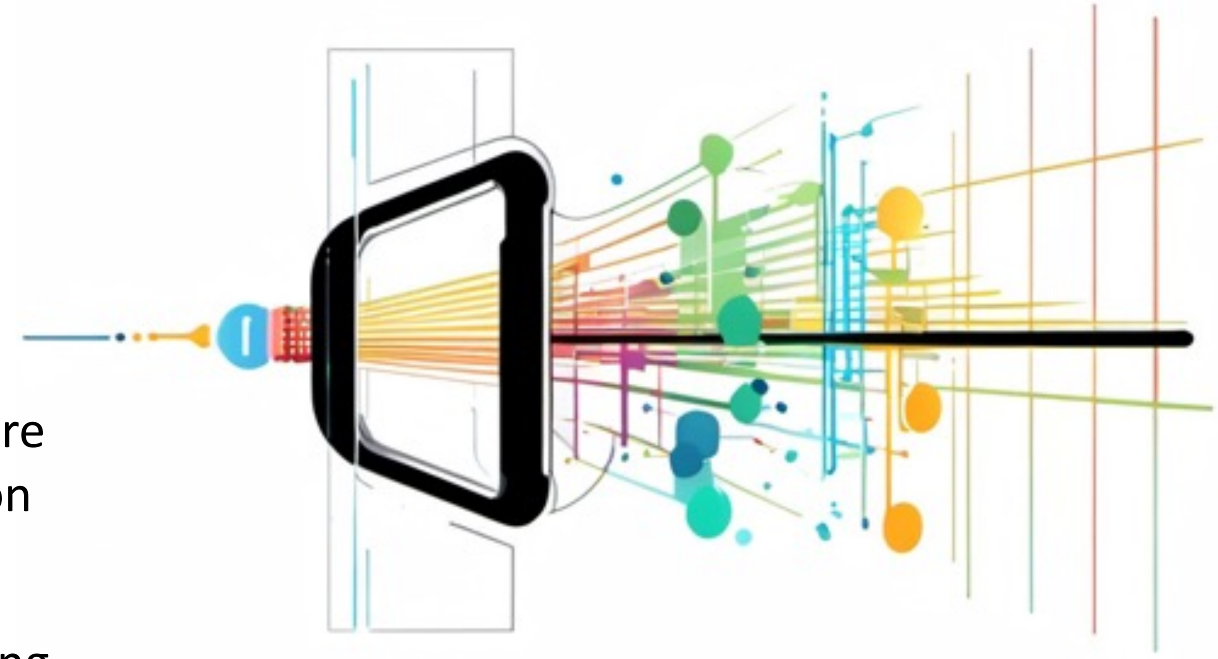
Conclusion

U2UT detector design in FTDR
- HV-CMOS: Large-electrode chip, pixel size 50 x 150 µm
- CMOS with small electrode: pixel size 30 x 30 µm

For scoping document
- 4-layer vs 3-layer design
- Less modules/staves used in U2UT detector
- Reduce peak luminosity

U2UT geometry description added into LHCb framework
- Including: Default HV-CMOS; 3-layer; 10-stave structure
- CMOS with small electrode scenario will be ready soon

Simulation studies on U2UT
- Based on LHCb framework, digitization is done; tracking reconstruction codes to be ready soon
- More performance results can be found in Benjamin and Carlo’s talk



Thanks