Contribution ID: **77** Type: **Talk 22min**

Test and characterization of multi layer ion traps on fused silica

Tuesday 9 July 2024 11:23 (22 minutes)

Quantum computing has emerged as a promising frontier with the potential to revolutionize computation by effectively tackling classically intractable problems. Among the various platforms for realizing a universal quantum computer, trapped ions have demonstrated their capabilities, allowing for quantum gate operations on quantum bits (qubits) by manipulating single or multiple ions. This approach offers notable advantages such as low error rates and long storage times [1]. However, the pursuit of a universal quantum computer inherently demands the scaling up of qubit numbers, which presents a significant engineering challenge. One such challenge is the construction of ion traps capable of storing many ions while keeping the qubit-to-qubit connectivity sufficiently high.

To tackle this scalability problem, our primary focus is on an industrially microfabricated surface ion trap designed to accommodate larger numbers of ions arranged in a two-dimensional grid [2]. Furthermore, we have developed an electrical wafer test as an example of how increasingly complex ion traps can be tested before their integration into a setup.

We use a surface ion trap with the capacity to confine 18 ions within two adjacent 1D crystals. The trap comprises three aluminum layers separated by silicon oxide, constructed on a fused silica substrate manufactured at the industrial fabrication site of Infineon Villach. Additionally, the ion trap incorporates an integrated resistance-based temperature sensor with sensitivity of 2.5 Ohm/K @ 10K to monitor the ion trap during operation. Furthermore, a comprehensive room temperature electrical wafer test concept comprising 540 measurements per chip was developed. This verifies the functionality of the trap before insertion in the setup. Heating rates below 10ph/s at an axial frequency of 1.2MHz on different trapping sites were measured to benchmark the trap in a cryogenic environment. The presentation will cover the trap concept, the electrical wafer test procedure, the characterization of the temperature sensor, and the results achieved with the ion trap in a cryogenic setup.

[1] C. Bruzewicz, Trapped-ion quantum computing: Progress and challenges, arXiv:1904.04178

[2] P. Holz, Two-dimensional linear trap array for quantum information processing, arXiv:2003.08085

Author: DIETL, Matthias

Co-authors: ZESAR, Alexander (Infineon Technologies Austria AG, Universität Graz); RÖSSLER, Clemens (Infineon Technologies Austria AG); ANMASSER, Fabian; VALENTINI, Marco (Universität Innsbruck); VAN MOURIK, Martin (University of Innsbruck); HOLZ, Philip (Alpine Quantum Technologies GmbH); SCHINDLER, Philipp (University of Innsbruck); BLATT, Rainer (Universität Innsbruck, Institut für Quantenoptik und Quanteninformation); AUCHTER, Silke (Infineon Technologies Austria AG)

Presenter: DIETL, Matthias

Session Classification: Quantum Technologies

Track Classification: Quantum Technologies