

# Industrially fabricated ion trap chips for double-well coupling experiments

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# Introduction

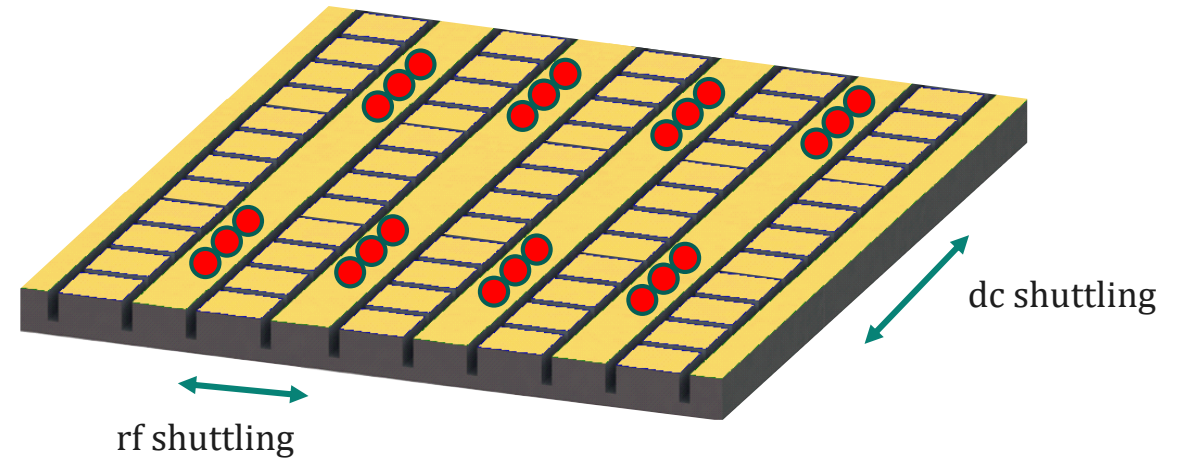
- Ion trap chips for quantum processors
- **Goals:** Scalable architecture, industrial fabrication

- Scalable architecture: axial and radial coupling → **double-well coupling**

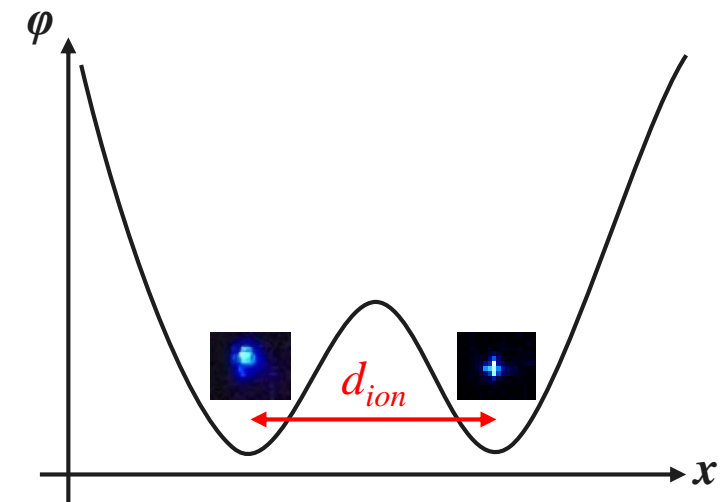
- Coupling strength:  $\Omega_C \sim \frac{1}{\omega d_{ion}^3}$

- $d_{ion} = 100 \mu m \rightarrow \Omega_C = 0,09 \times 2\pi \text{ kHz @ 1 MHz axial}$

- $d_{ion} = 30 \mu m \rightarrow \Omega_C = 3.3 \times 2\pi \text{ kHz @ 1 MHz axial}$



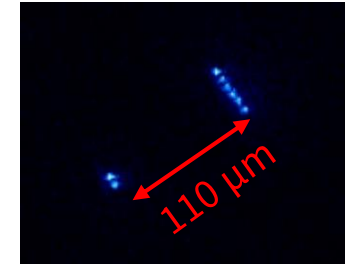
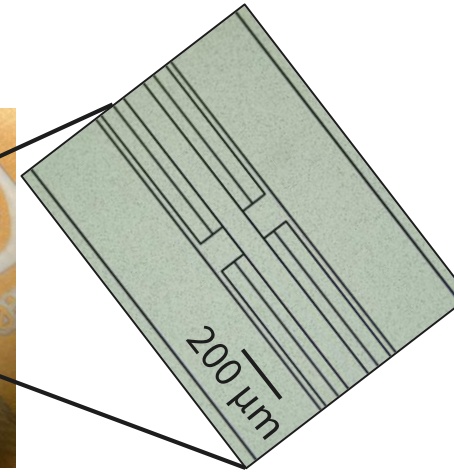
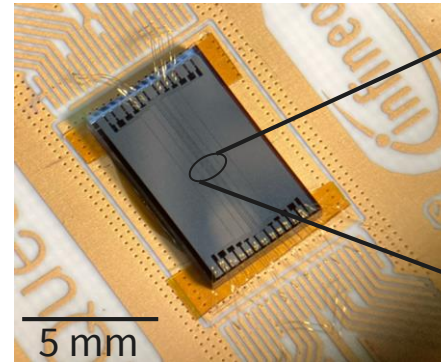
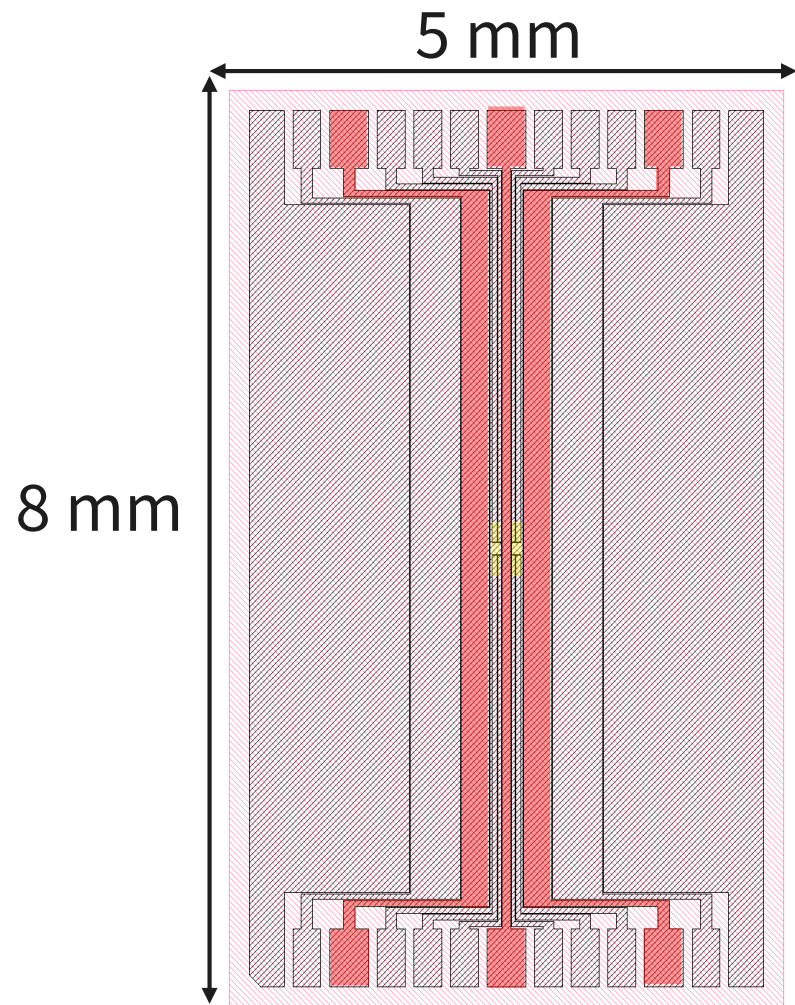
P. Holz, S. Auchter *et al.*, Adv. Quant. Technol. **3** (2020)



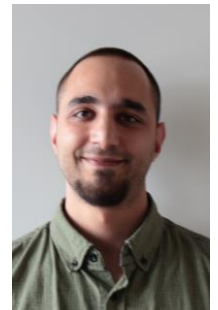


# Tested devices

# Quattro stagioni trap (4S)

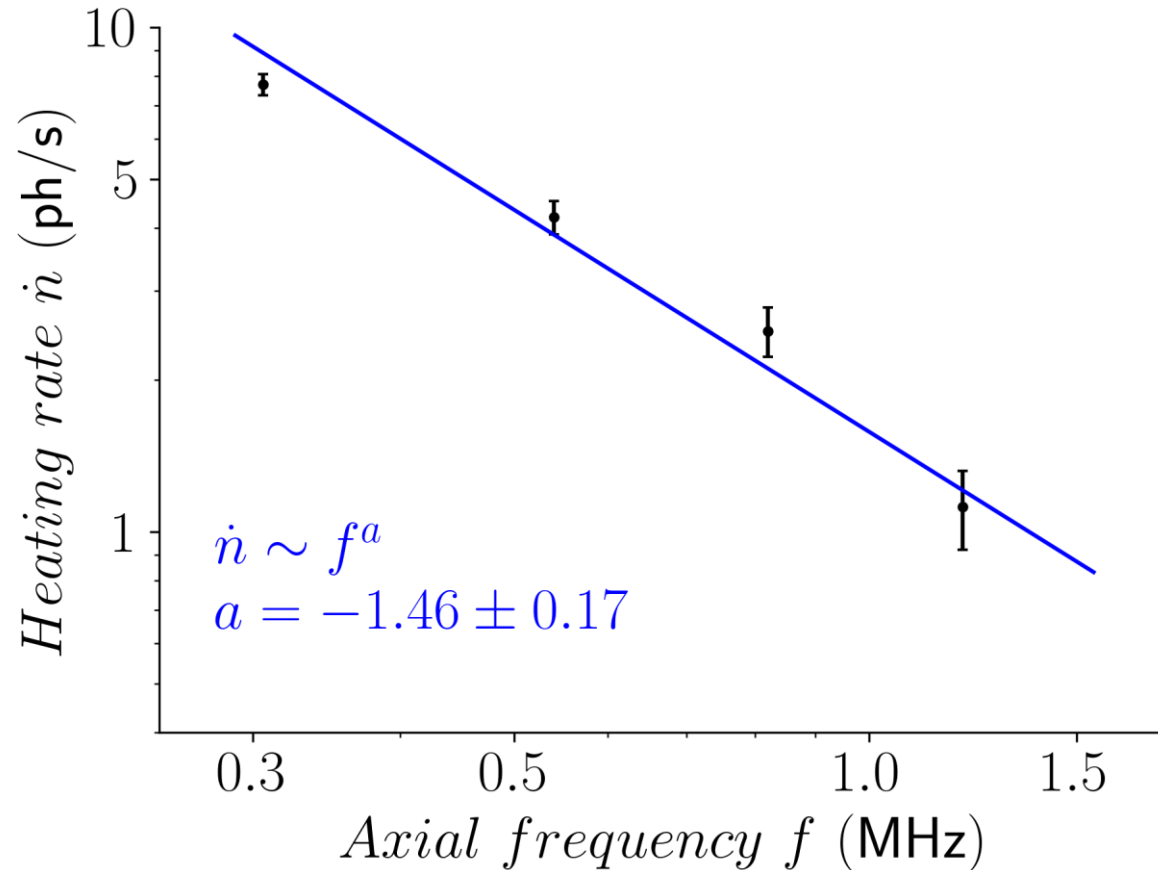


- rf shuttling experiments
- 2 trapping sites
- Single metal layer trap
- Fused Silica and Sapphire substrate
- 110  $\mu\text{m}$  ion-ion distance
- 130  $\mu\text{m}$  ion-surface distance



Marco Valentini

# Quattro stagioni trap (4S) - results



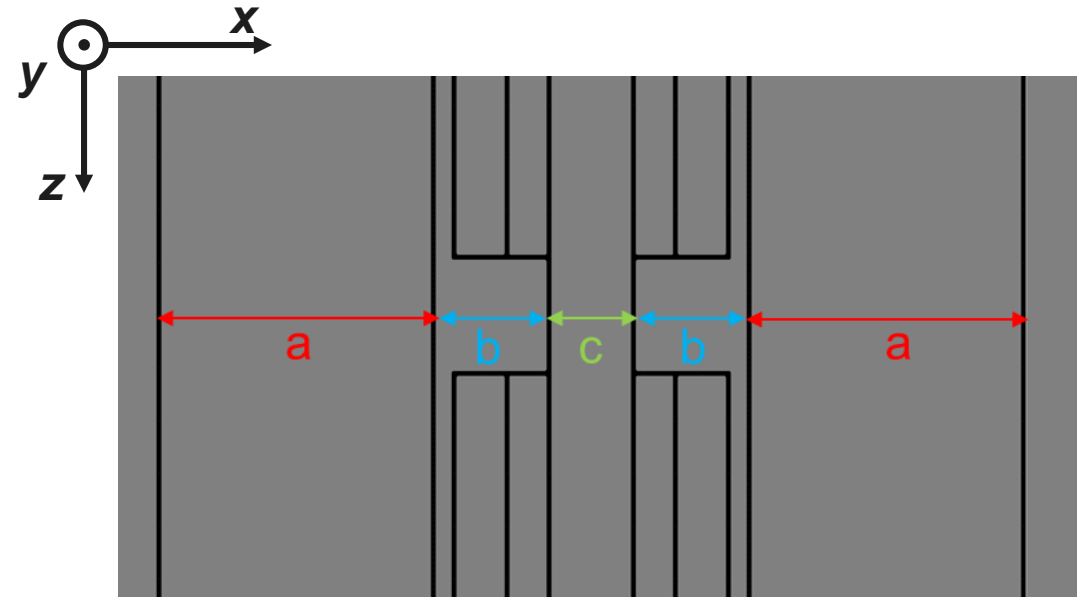
- Reliably traps ions
- Heating rate of  $1.1 \pm 0.2$  ph/s @ 1.2 MHz axial  
→ suitable for experiments
- rf shuttling experiments

## Due stagioni trap (2S) - idea

- Lower ion-ion distance  $\rightarrow$  higher coupling rate
- Vary electrode size ratios with trade-off between ion height, trap efficiency  $\kappa$  and potential depth.

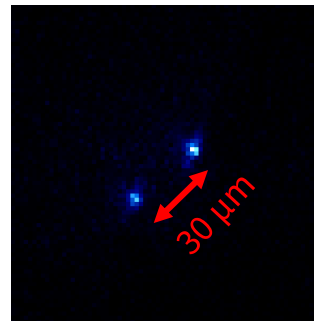
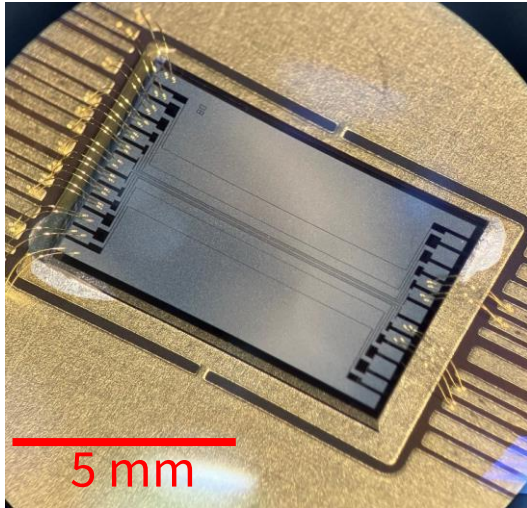
$$\varphi(x, y, t) = \frac{\kappa U_{\text{RF}}}{2y_0^2} (x^2 - y^2) \cos(\Omega_{\text{RF}} t)$$

- Optimize trap efficiency  $\kappa(a, b, c)$  for given  $(d_{\text{ion}}, y_0)$
- Analytic simulations  $\rightarrow$  check by FEM



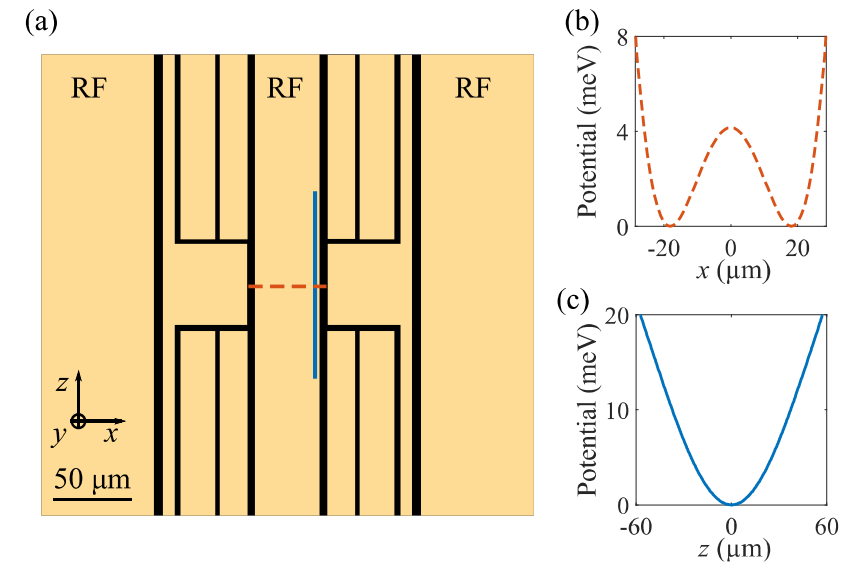
Trap:	a ( $\mu\text{m}$ )	b ( $\mu\text{m}$ )	c ( $\mu\text{m}$ )	$\kappa$ (%)
4S	255	115	75	17.6
2S/80	214	63	42	10.0

# Due stagioni trap (2S) – heating rates



- 30  $\mu\text{m}$  ion-ion distance, 80  $\mu\text{m}$  ion height
- Fused Silica substrate, Aluminum electrodes

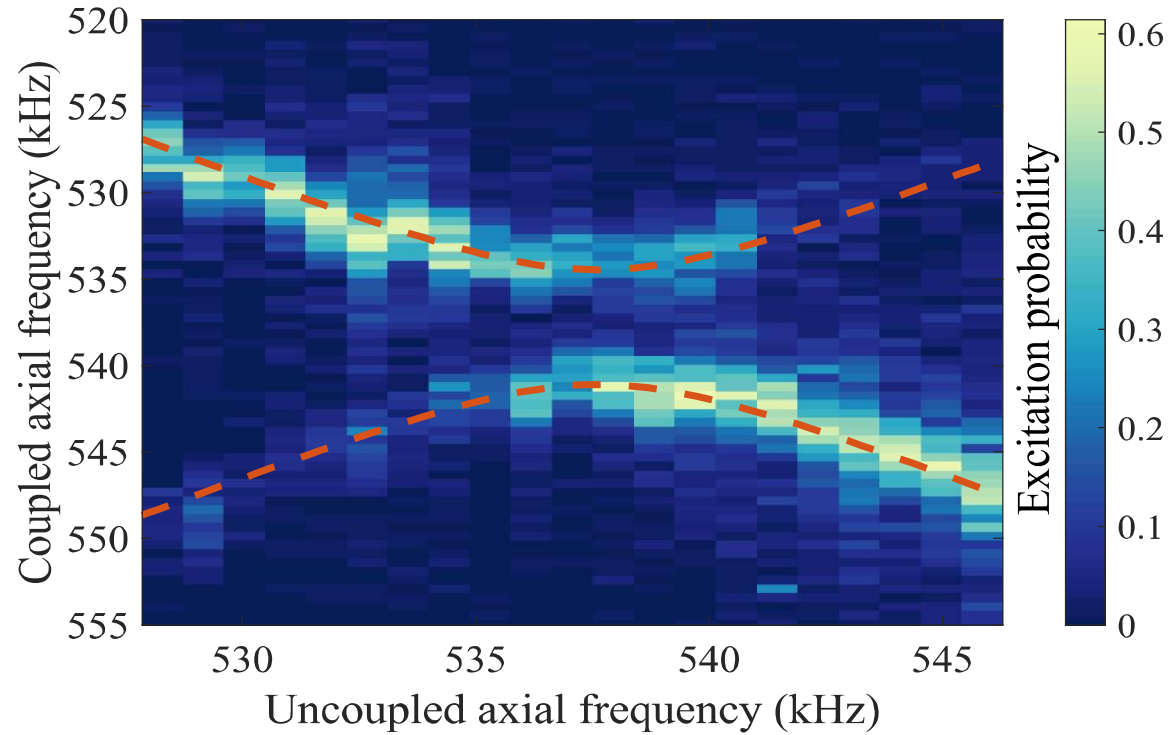
Trap site:	Axial frequency (MHz)	Heating rate (phonons/s)
left	0.5	~20
	1	~5
right	0.5	~20



- Lower ion height than 4S, but still low heating rates

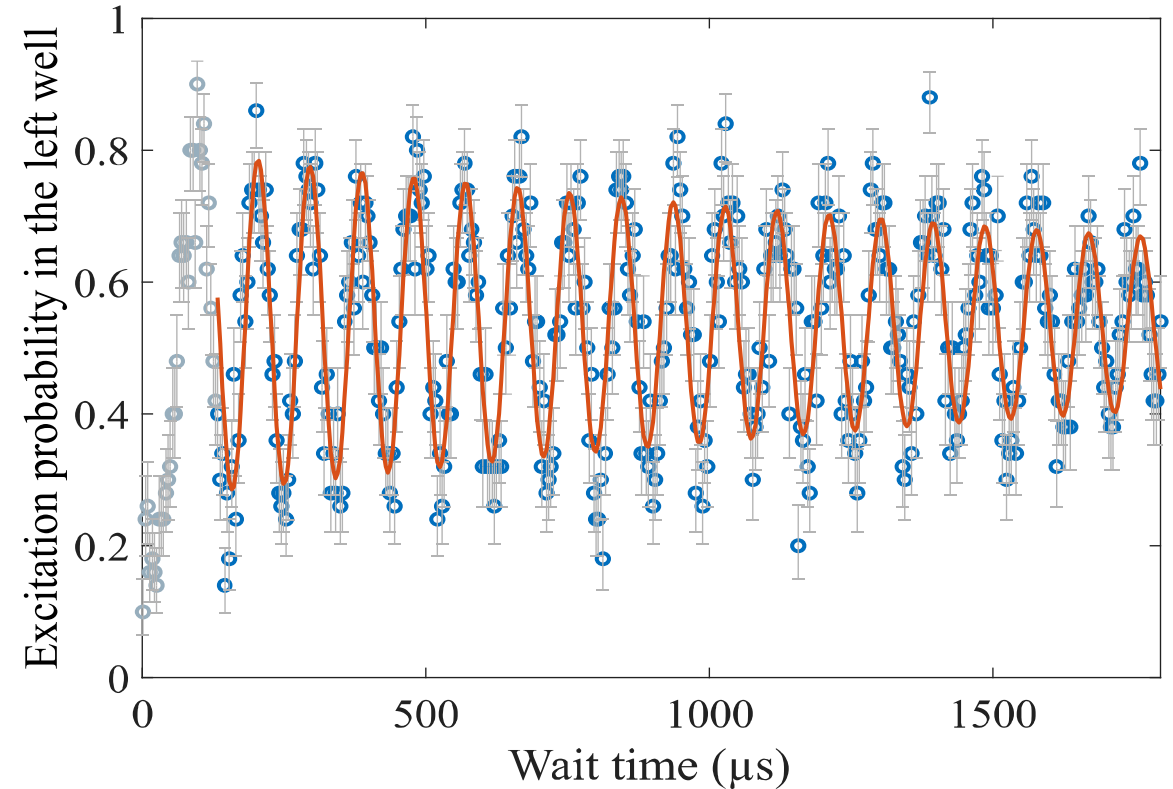
arXiv:2406.02406

# Due stagioni trap (2S) – radial coupling



- Radial coupling rate: ~ 6.5 kHz @ 500 kHz axial (2 ions per well)
- Enables radial coupling experiments and gates

M. Valentini, M. van Mourik *et al.*, arXiv:2406.02406



Marco Valentini



Martin van Mourik

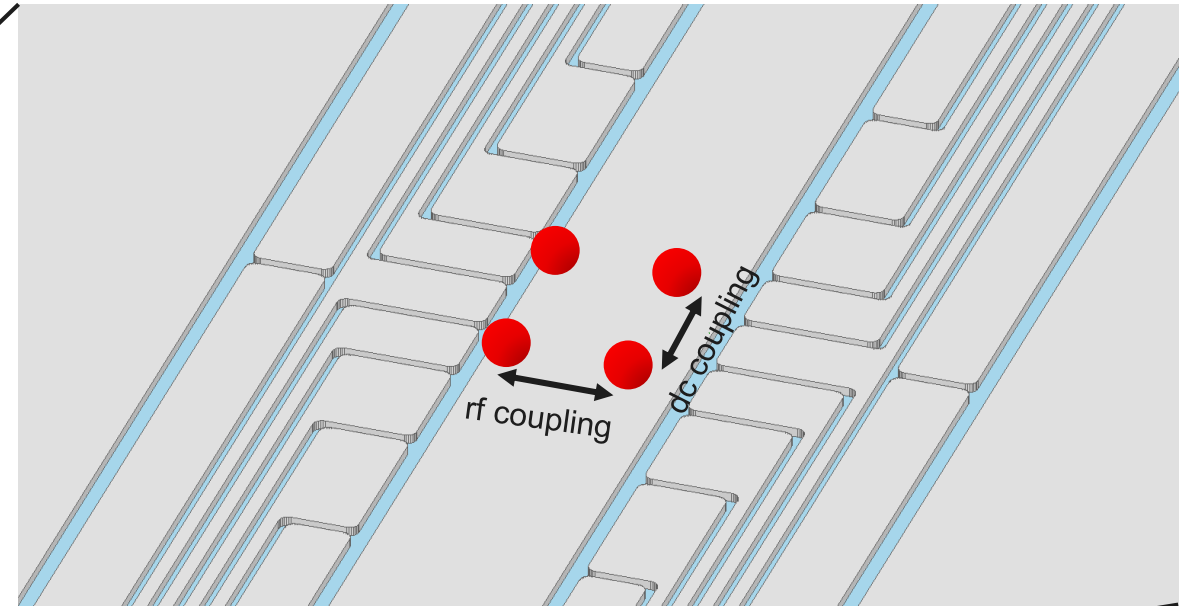
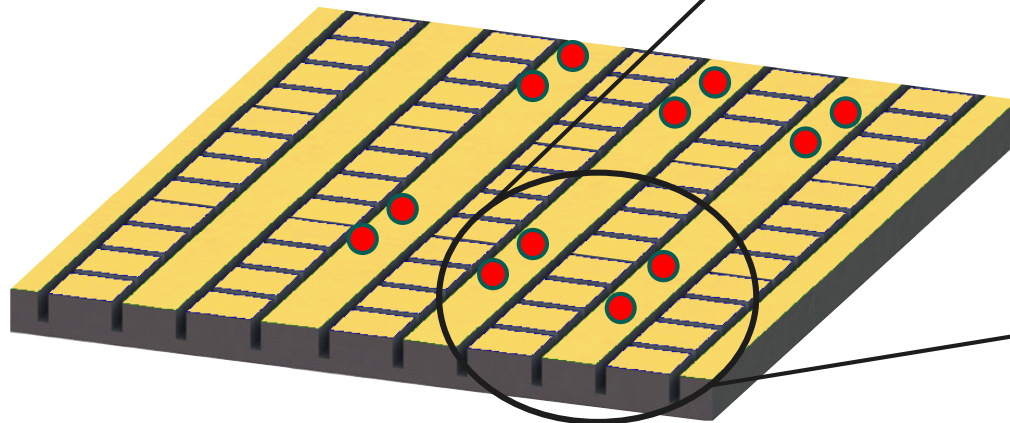




# New devices

## 2S<sup>2</sup> trap - idea

- Radial and axial coupling on one trap
- Smallest version: 4 ions in 4 wells
- Rf electrodes: 2S trap
- New set of dc electrodes for axial double-well potential



## 2S<sup>2</sup> trap - design

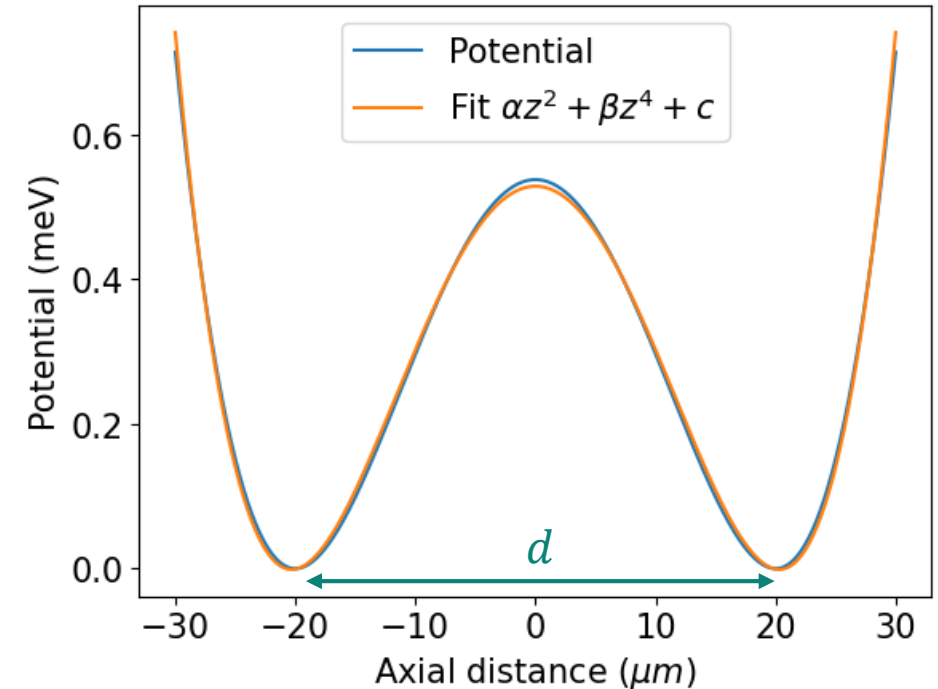
- Design: Choose dc electrode layout and electrode sizes
- Goal: minimize shim voltages @  $d_{ion} = 40 \mu m$

- Axial double-well (symmetric):

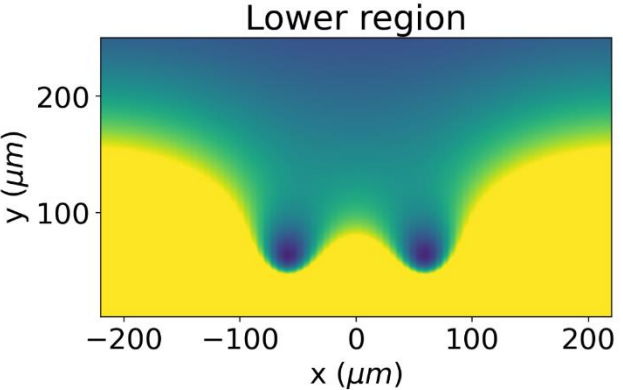
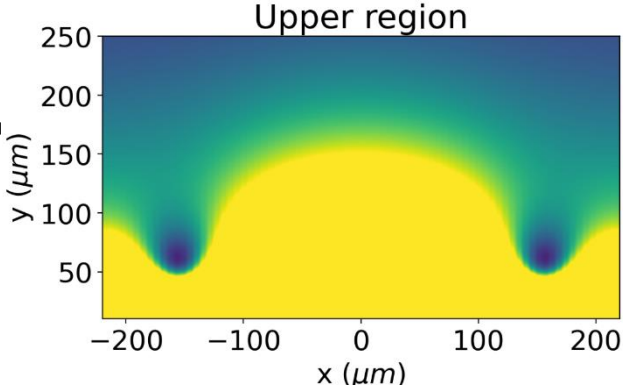
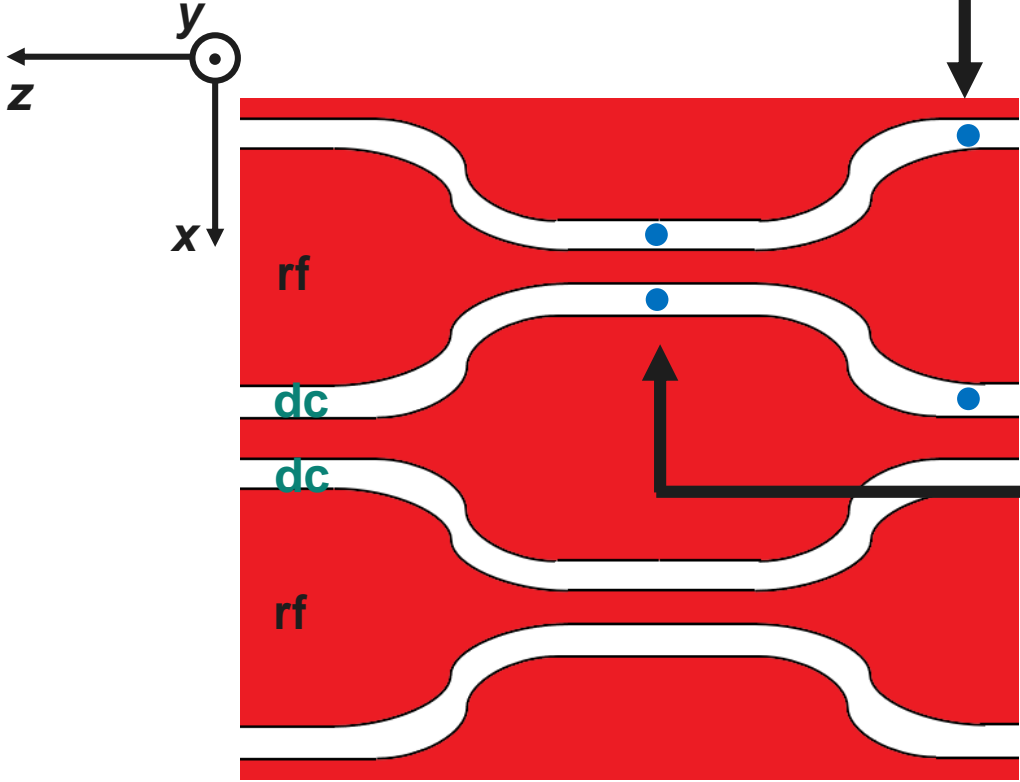
$$\varphi(z) = -\alpha z^2 + \beta z^4 + h = \frac{1}{32} m \omega_0^2 d^2 + \frac{m \omega_0^2}{2d^2} \left( z^4 - d^2 \frac{z^2}{2} \right)$$

Well-to-well distance  
axial frequency

- Axial vs radial double-well
- Fabrication: single metal-layer on Fused Silica



# Outlook: Meander trap

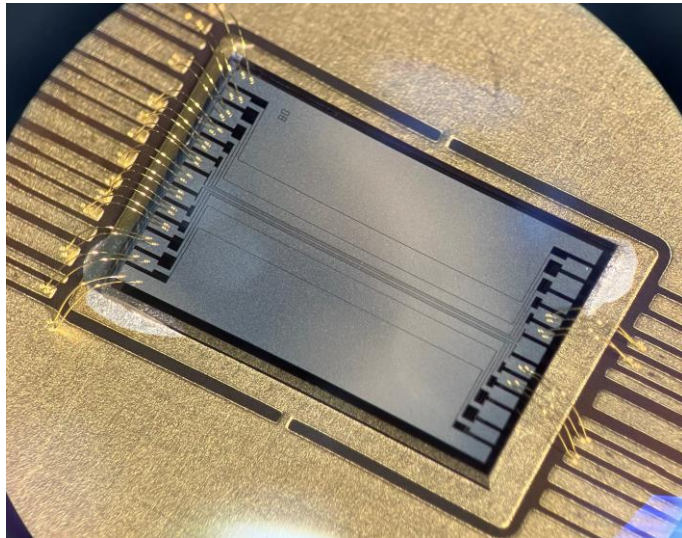


- Ion trap chip with axial dc and radial shuttling
- „Meander zones“: tune radial distance via dc shuttling

- Fabrication:
  - Multi-layer stack (complex electrode layouts)
  - Dielectric substrate (heating rates)
- Simulation:
  - Analytic model (fast)
  - Check with FEM

## Summary

- Double-well coupling on dedicated industrially fabricated ion trap chips
- Scaling: Quantum Spring Array (QSA)



- **Posters:**
- Entanglement on the 2S trap: **Marco Valentini**
- Rydberg chip traps: **Simon Schey**
- Optical integration into glass traps: **Jakob Wahl**
- 3D ion traps: **Max Glantschnig**

- **Paper:**

M. Valentini, M. van Mourik, F. Butt, J. Wahl, M. Dietl, M. Pfeifer, F. Anmasser, Y. Colombe, C. Rössler, P. Holz, R. Blatt, M. Müller, T. Monz, P. Schindler:

*Demonstration of two-dimensional connectivity for a scalable error-corrected ion-trap quantum processor architecture,*  
[arXiv:2406.02406](https://arxiv.org/abs/2406.02406) (2024)

