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Industrially fabricated ion trap chips for radial coupling experiments

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We present and discuss industrially fabricated ion trap chips [1, 2] on the dielectric substrates Fused Silica and Sapphire.

Surface ion trap chips offer a promising platform for the scaling of ion trap quantum computers. We investigate shuttling in the radial direction as element of a scalable architecture [1]. For this, we present chips that are designed to trap ions in two-well potentials in the large separation and in the radial coupling regimes. The chips presented are capable of trapping ions or ion chains in separate rf potential wells. The design parameters of a surface ion trap in the radial coupling regime with fixed ion height and ion-ion distance are investigated. Based on this, we present improved trap designs. We discuss the simulation, design and fabrication challenges involved in creating such chips. The traps are or will be fabricated on single- and multi-layer stacks. The fabrication on multi-layer stacks enables a more complex electrode geometry and therefore more complex scalable ion trap layouts.

The ion traps are fabricated on the dielectric substrates Fused Silica and Sapphire, which are ultra-wide-bandgap materials and therefore promise excellent resilience against UV light and low rf losses. The status of industrial microfabrication on these materials is discussed, with a focus on the challenges of fabrication on different substrate materials and the fabrication of multi-layer stacks.

[1] Ph. Holz, S. Auchter et al., Adv. Quantum Technol. 3, 2000031 (2020)
[2] S. Auchter, C. Axline et al., Quantum Sci. Technol. 7, 035015 (2022)

Author: PFEIFER, Michael (University of Innsbruck, Infineon Technologies Austria AG)

Co-authors: SCHEY, Simon (Stockholm University and Infineon Technologies Austria AG); DIETL, Matthias (Infineon Technologies Austria AG, University of Innsbruck); ANMASSER, Fabian (Infineon Technologies Austria AG, University of Innsbruck); WAHL, Jakob (Infineon Technologies Austria AG, University of Innsbruck); GLANTSCHNIG, Max (Infineon Technologies Austria AG, Physikalisch-Technische Bundesanstalt Braunschweig); AUCHTER, Silke (Infineon Technologies Austria AG); HANKE, Kilian (ETH Zurich, Infineon Technologies Austria); VALENTINI, Marco (University of Innsbruck); VAN MOURIK, Martin (University of Innsbruck); HOLZ, Philip (Alpine Quantum Technologies GmbH); MONZ, Thomas (University of Innsbruck, Alpine Quantum Technologies GmbH); RÖSSLER, Clemens (Infineon Technologies Austria AG); ROOS, Christian (University of Innsbruck); COLOMBE, Yves (Infineon Technologies Austria AG); SCHINDLER, Philipp (University of Innsbruck)

Presenter: PFEIFER, Michael (University of Innsbruck, Infineon Technologies Austria AG)

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