Scintillating fiber-based Ion Beam Profile Monitor for HIT

HighRR Seminar Mar.20.2024

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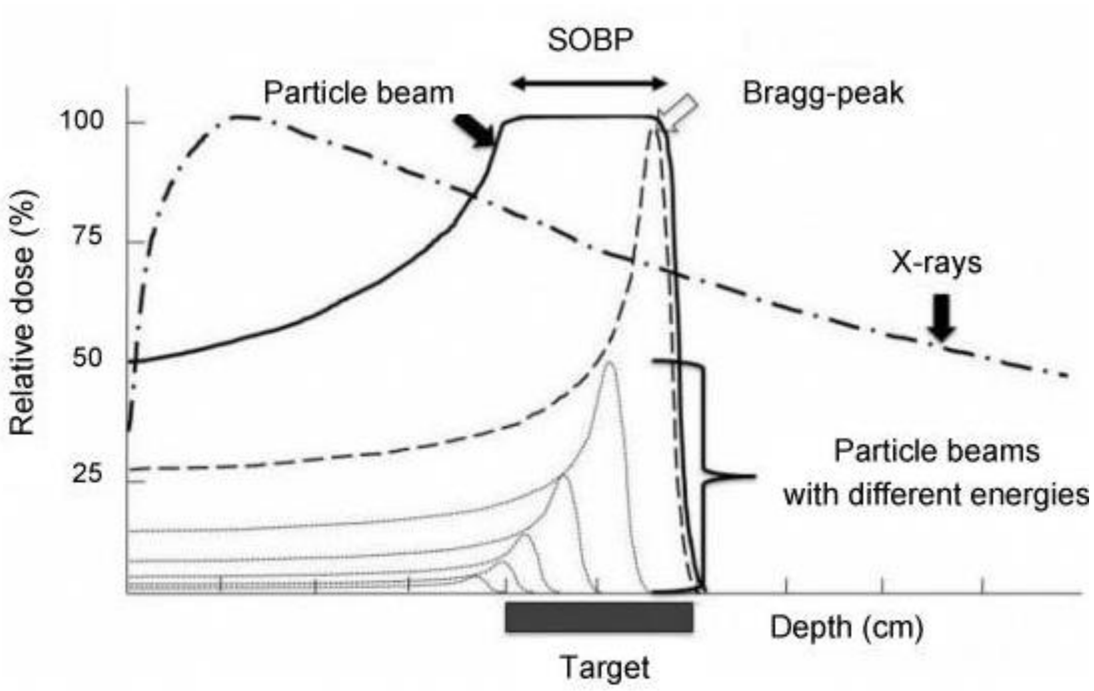
Outline

- Introduction
- Detector Setup
- Algorithm for reconstruction
- Real-time reconstruction on FPGAs
- Measurement and performance
- Summary and outlook

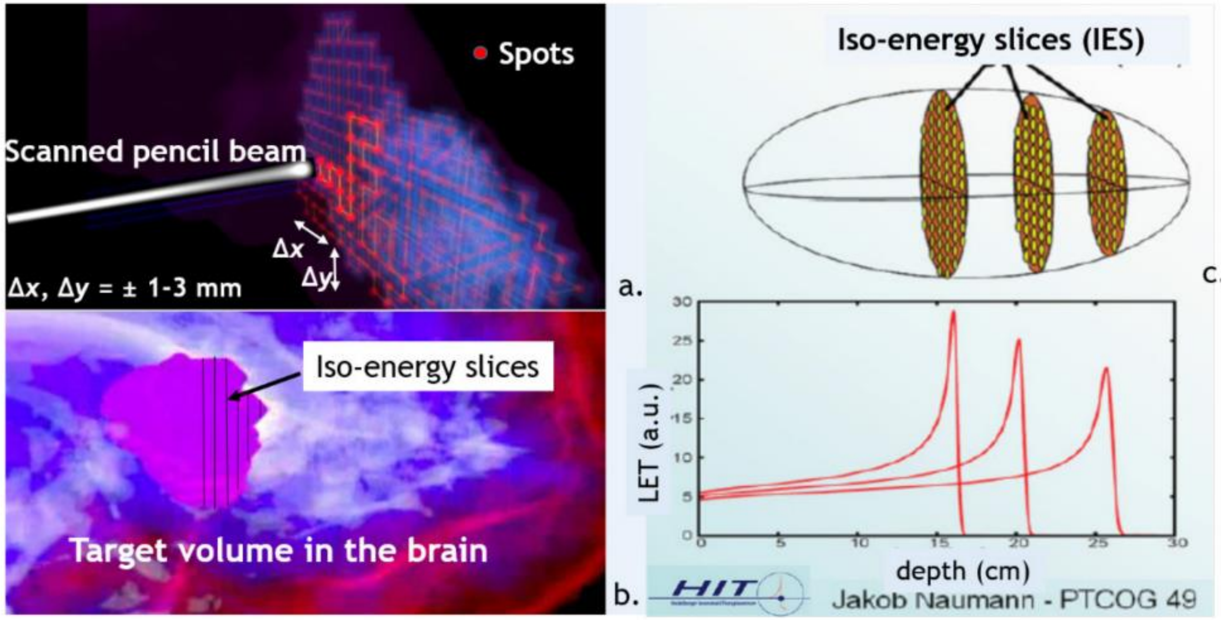
Introduction

Ion Therapy

Purpose of radiotherapy: deliver the prescribed amount of **dose** to a tumor at the same time as sparing the surrounding tissues
Ion therapy unique: Bragg-peak
Dose delivery method: **pencil beam** scanning
Pencil beam scanning: **scan spot by spot**, tuning the energy of beam to reach different depths



Relative dose with photon therapy and ion therapy. In ion therapy, an extended Bragg peak (spread-out Bragg peak; SOBP) is formed to fit this Bragg peak to the size of the cancer

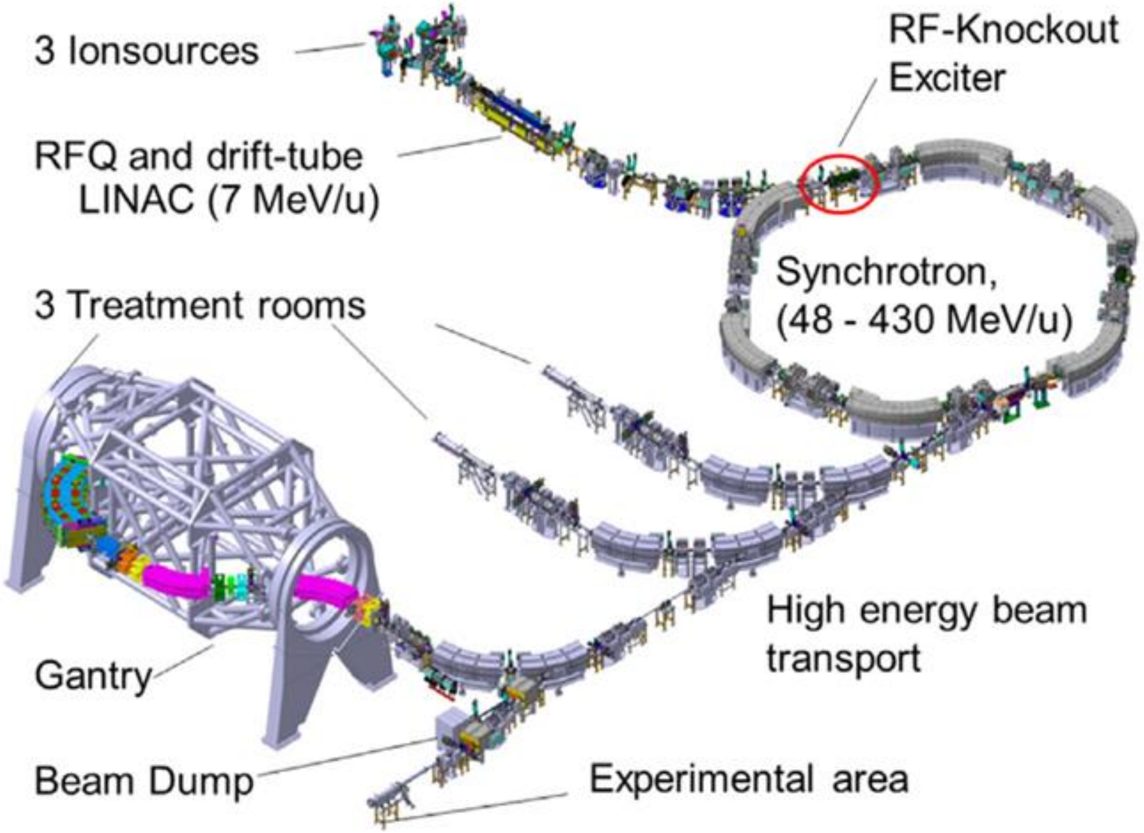


Example of spot distribution for pencil beam scanning (a) for a simulated target volume in the brain (b). (c) Iso-energy slices treated with different Bragg peaks

Matsumoto Y, Fukumitsu N, Ishikawa H, Nakai K, Sakurai H. A Critical Review of Radiation Therapy: From Particle Beam Therapy (Proton, Carbon, and BNCT) to Beyond. J Pers Med. 2021 Aug 23;11(8):825. doi: 10.3390/jpm11080825. PMID: 34442469; PMCID: PMC8399040.

Heidelberg Ion Therapy Center

The location of HIT, red star is where we are right now.

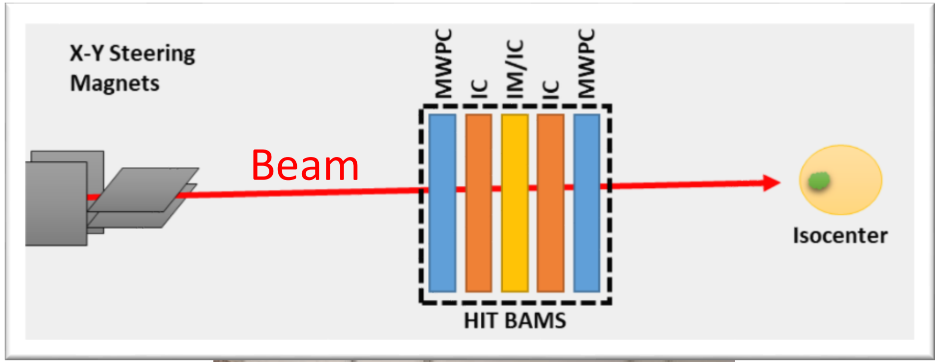


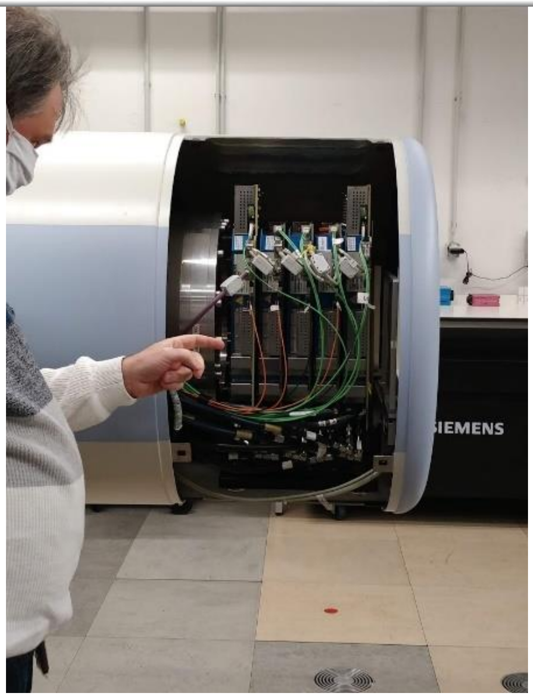
HIT accelerator

HIT is a large medical accelerator facility for ion therapy. It produce proton/helium/carbon/oxygen pencil beam with different intensity/energy/focus.

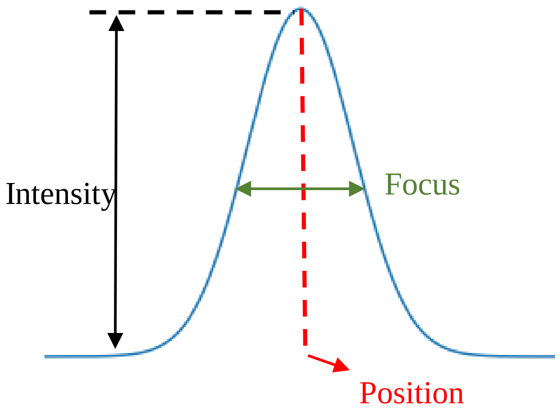
Figure from: David Ondreka, Udo Weinrich, The Heidelberg ion therapy (HIT) acceleratorcoming into operation, in: Proceedings of EPAC08, Genoa, Italy, 2008.

Heidelberg Ion Therapy Center & Beam Accelerator Monitoring System





One beam nozzle. It's at end of the beamline, with BAMs inside the nozzle.



Sketch for beam profile.

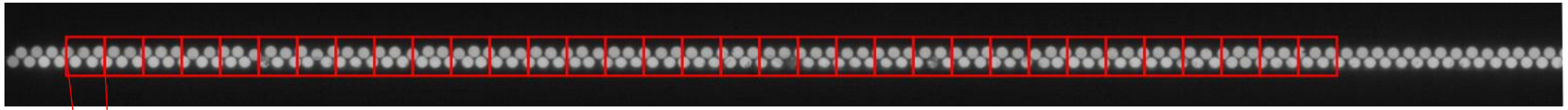
The position, focus and intensity of pencil beam is monitored by BAMs
New beam profile monitor (BPM) is needed to replace aged MWPCs.

Requirement for new BPM

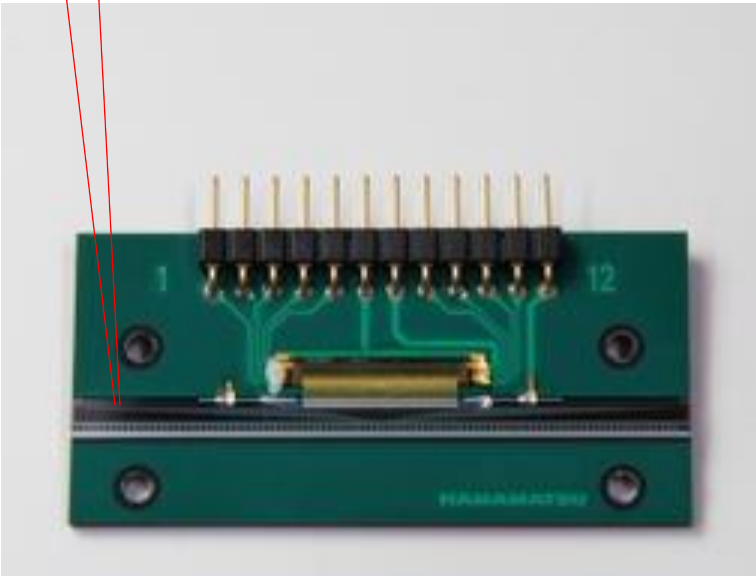
Requirement	Value
Beam Spot Size (FWHM)	1 - 33 mm
Active area	20 cm * 20 cm
Beam Position Resolution	< 0.2 mm @ 4-8 kHz
Beam Focus Resolution	< 0.4 mm @ 4-8 kHz
Material in Active Area	< 0.35 mm Water Equiv./ plane (4 planes in total)
In addition	
Work with MRI	less sensitive to magnetic field
Work with Flash	fast, function at high beam intensity

Scintillating fiber-based Beam Profile Monitor Setup

Scintillating Fiber-Based Detector Basic Principle

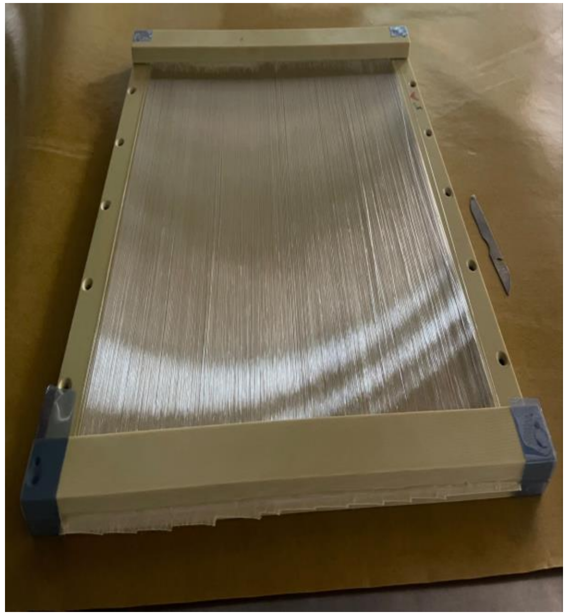


2-layer planes



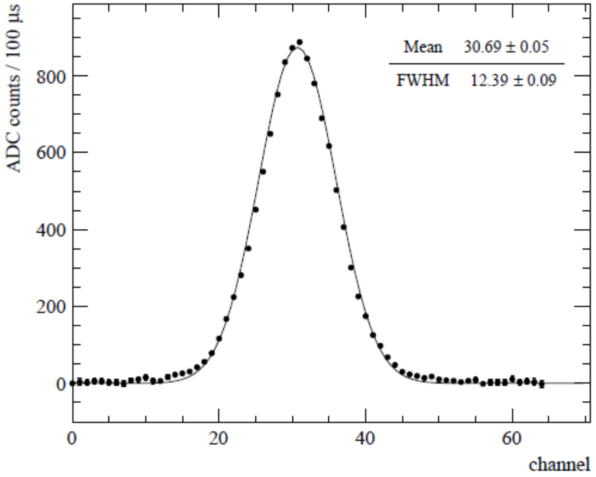
64 channel photodiode array
@ 4 to 10 kHz (0.8mm pitch)

+



0.250mm diameter
scintillating fibres

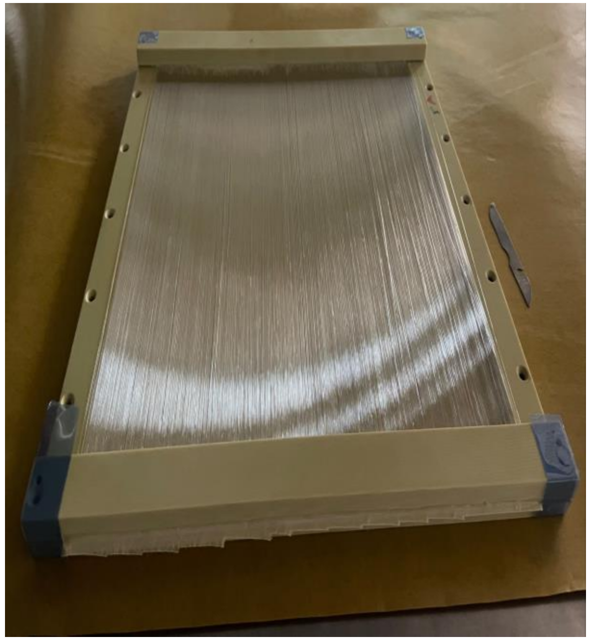
=



Scintillating Fiber + Photodiodes Array = Beam Profiles
One end of the fiber mat coupled to sensor array; the other either in air or with mirror

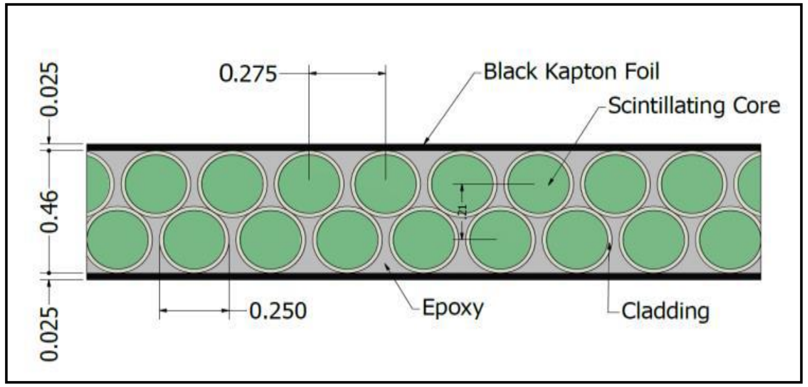
Scintillating Fiber Mat details

5m LHCb Scintillating Fiber Mat

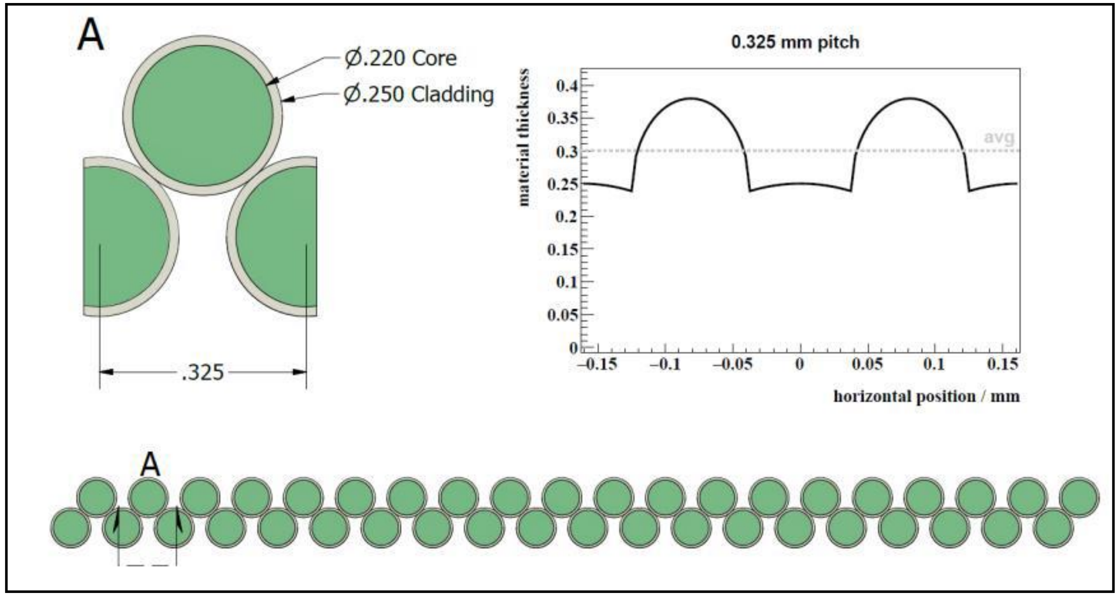


25 cm Scintillating Fiber Board for HIT

LHCb-style contains 50% dead material

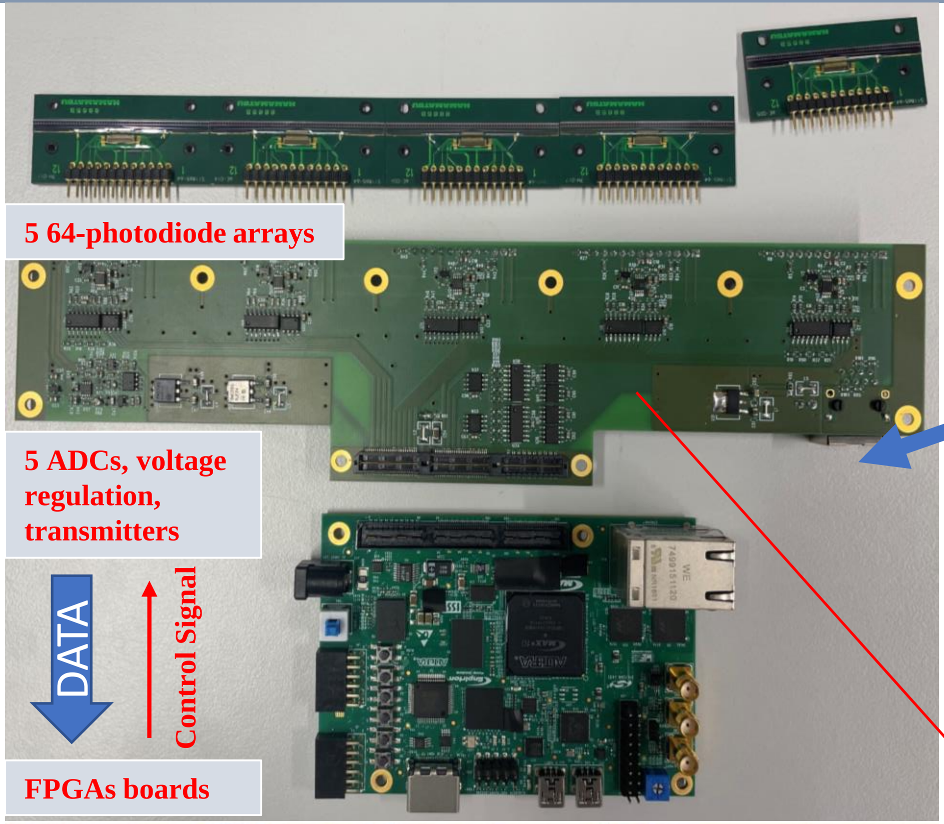


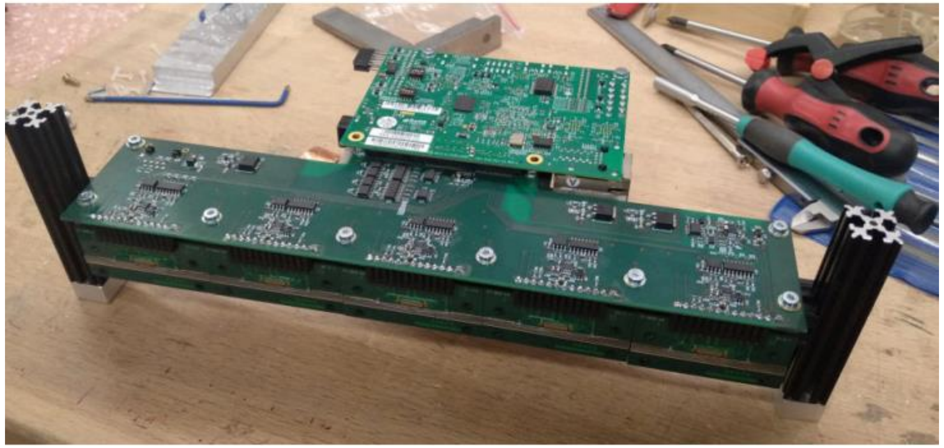
Developed for HIT

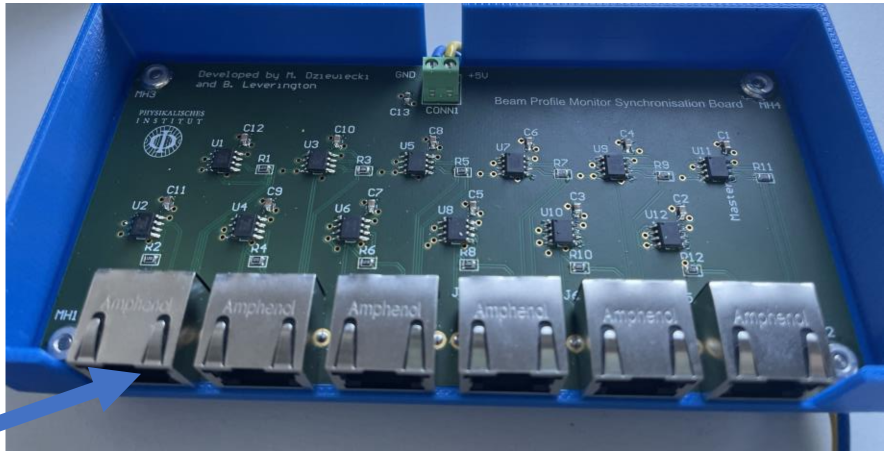


The fibre plane contributes 0.3 mm of plastic per layer to the material budget in the beamline. 2 XY stations are foreseen (total = ~1.2mm of polystyrene)

More hardware Details







Synchronization board

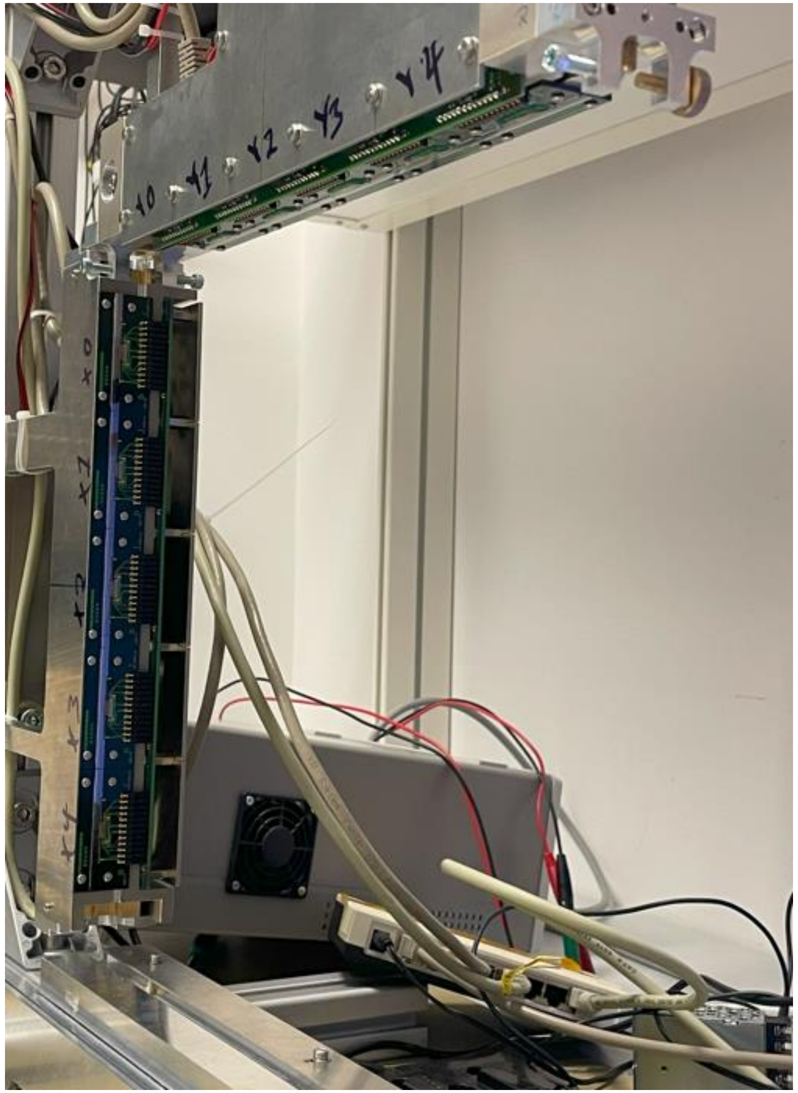
Synchronization board receive the sync signal from master board send to slave board

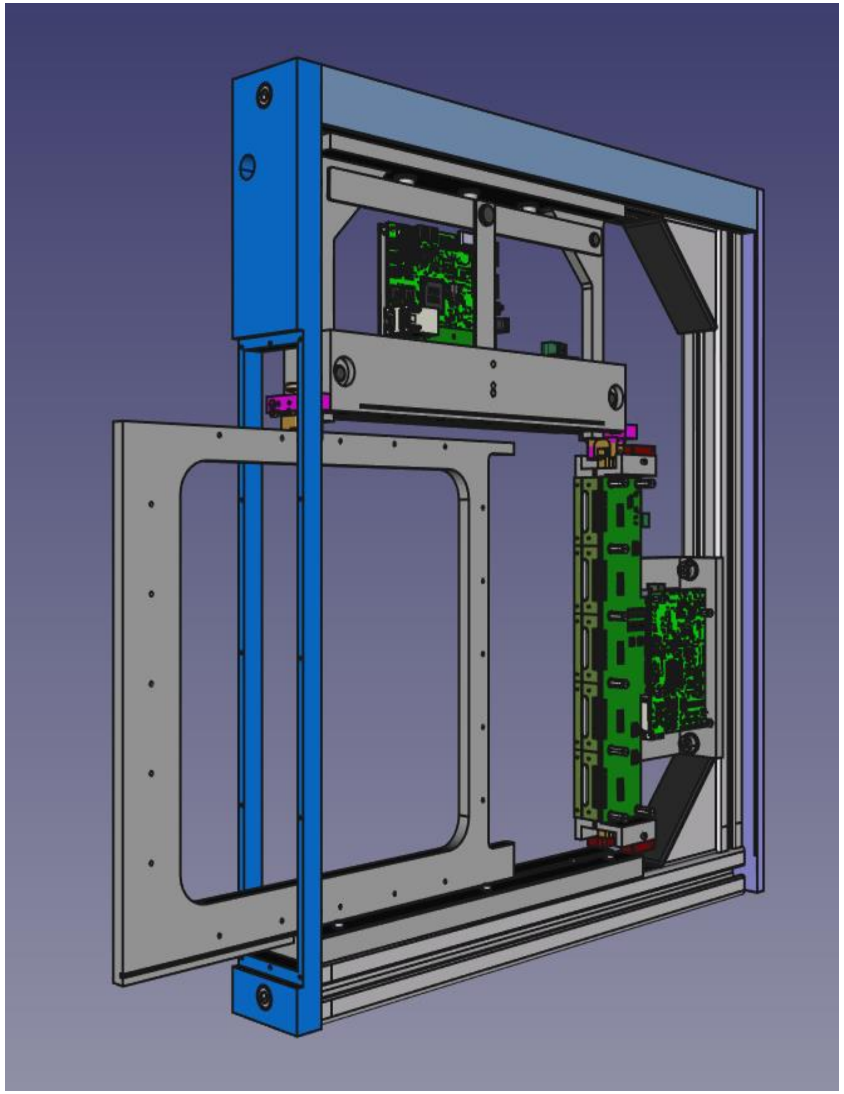
12V Power supply, can support 3 XY stations

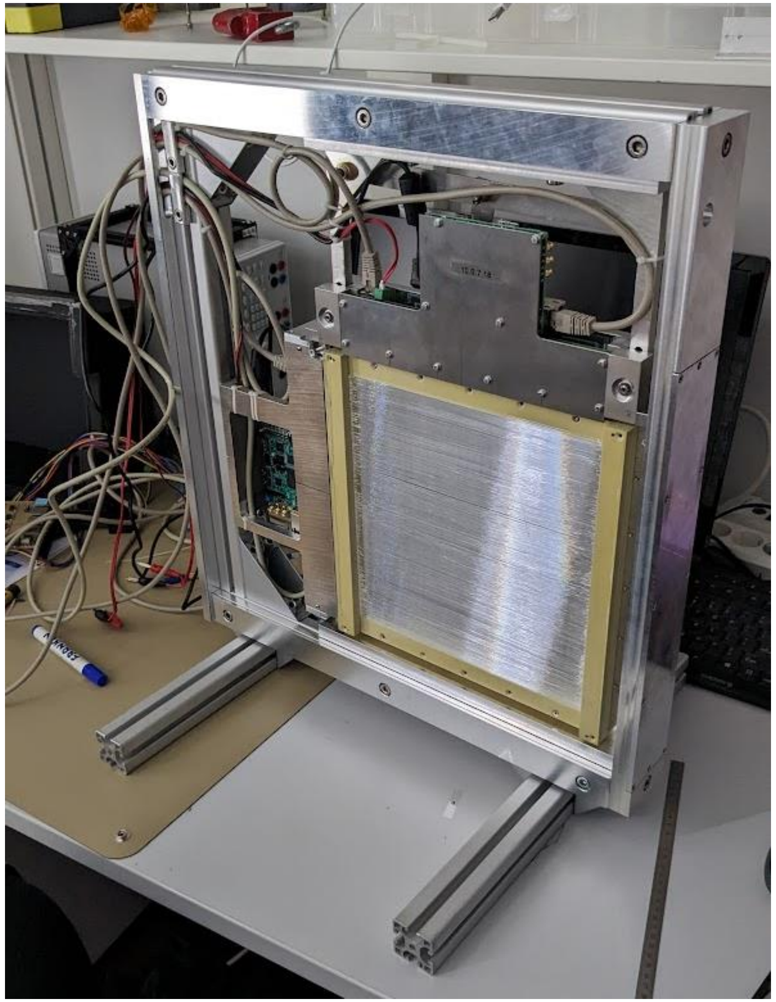
Right now, we only have 2 of these adc boards.

FPGAs control photodiodes arrays and ADC, collect signal from all the channels, reconstruct position and focus, pack data into UDP package, send to ethernet

Latest version

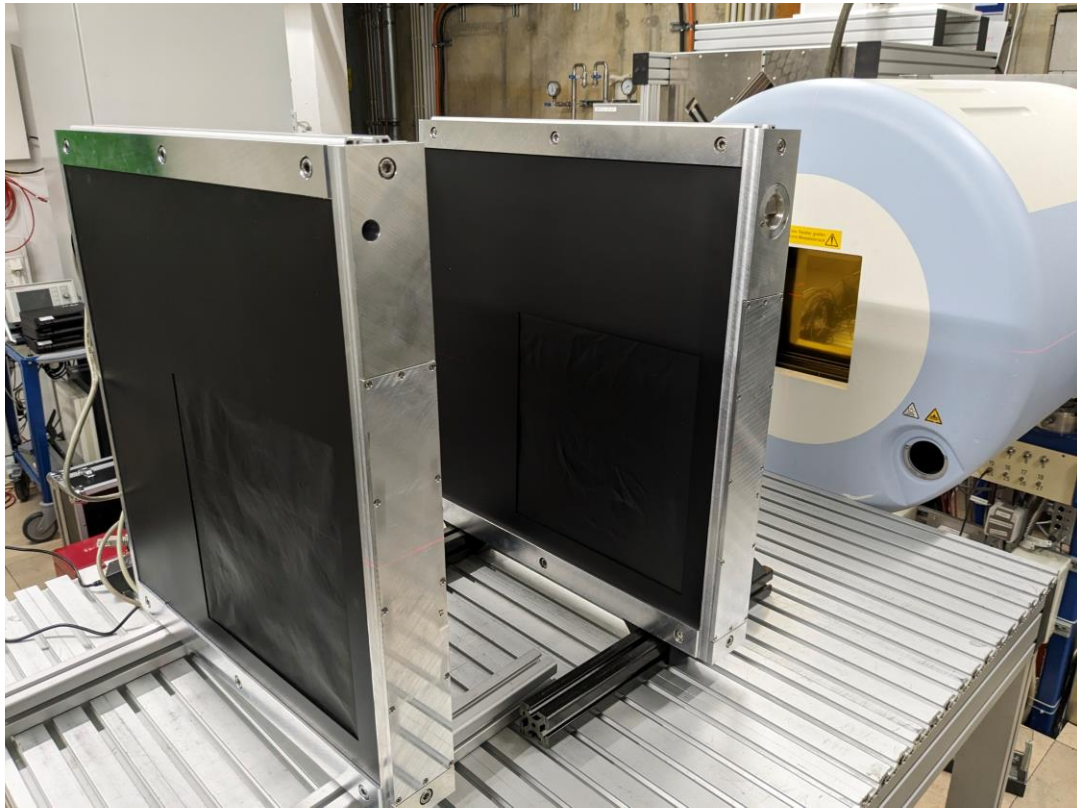






Built 1st XY station for debugging the assembly design. 25*25 cm2; easy replacement of fibers

Detector Setup for test beam on 2024-02-01



On 1st Feb 2024, we tested 2 X stations to compare two layers.
It's the first time that FPGAs reconstructing the position and focus.
We had planned for test 3XY stations, but the new ADC boards failed to receive sync signals.

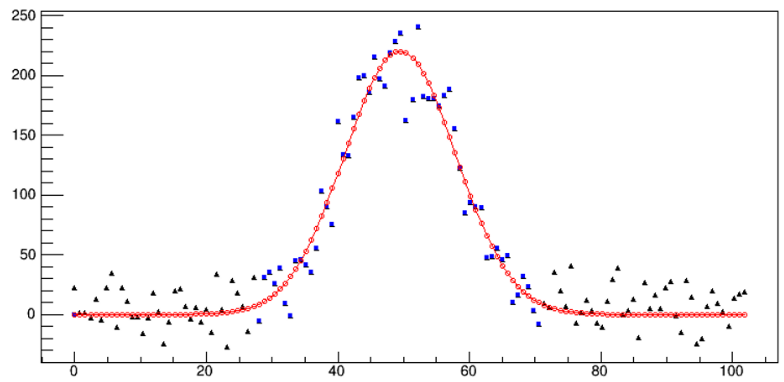
Algorithm for Gaussian-like beam

Algorithm for Gaussian-like beam which can be in principle implemented on FPGAs

Gaussian function, and it’s natural logarithm form:

$$y = Ae^{-\frac{(x-\mu)^2}{2\sigma^2}}$$

$$\ln y = \ln A - \frac{(x-\mu)^2}{2\sigma^2} = \ln A - \frac{x^2}{2\sigma^2} + \frac{x\mu}{\sigma^2} - \frac{\mu^2}{2\sigma^2} = a + bx + cx^2$$



RMS: **Easiest to implement**

use center of gravity to get position;

root mean square for sigma;

maximum signal for amplitude;

FAS (2*2 linear regression):

take the natural logarithm of gaussian to get a linear function;

estimate sigma by the area under gaussian and maximum signal;

calculate the rest 2 parameters (**position** and amplitude) by **least squares** method;

3*3 linear regression:

take the natural logarithm of gaussian to get a linear function;

calculate the 3 parameters (position, sigma, amplitude) by least squares method;

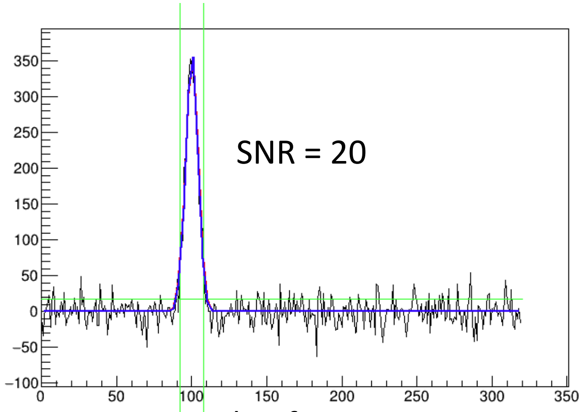
Algorithm Comparison by Toy Monte Carlo

Generate a simple gaussian shape, add noise, run the Linear regression algorithm, or RMS.

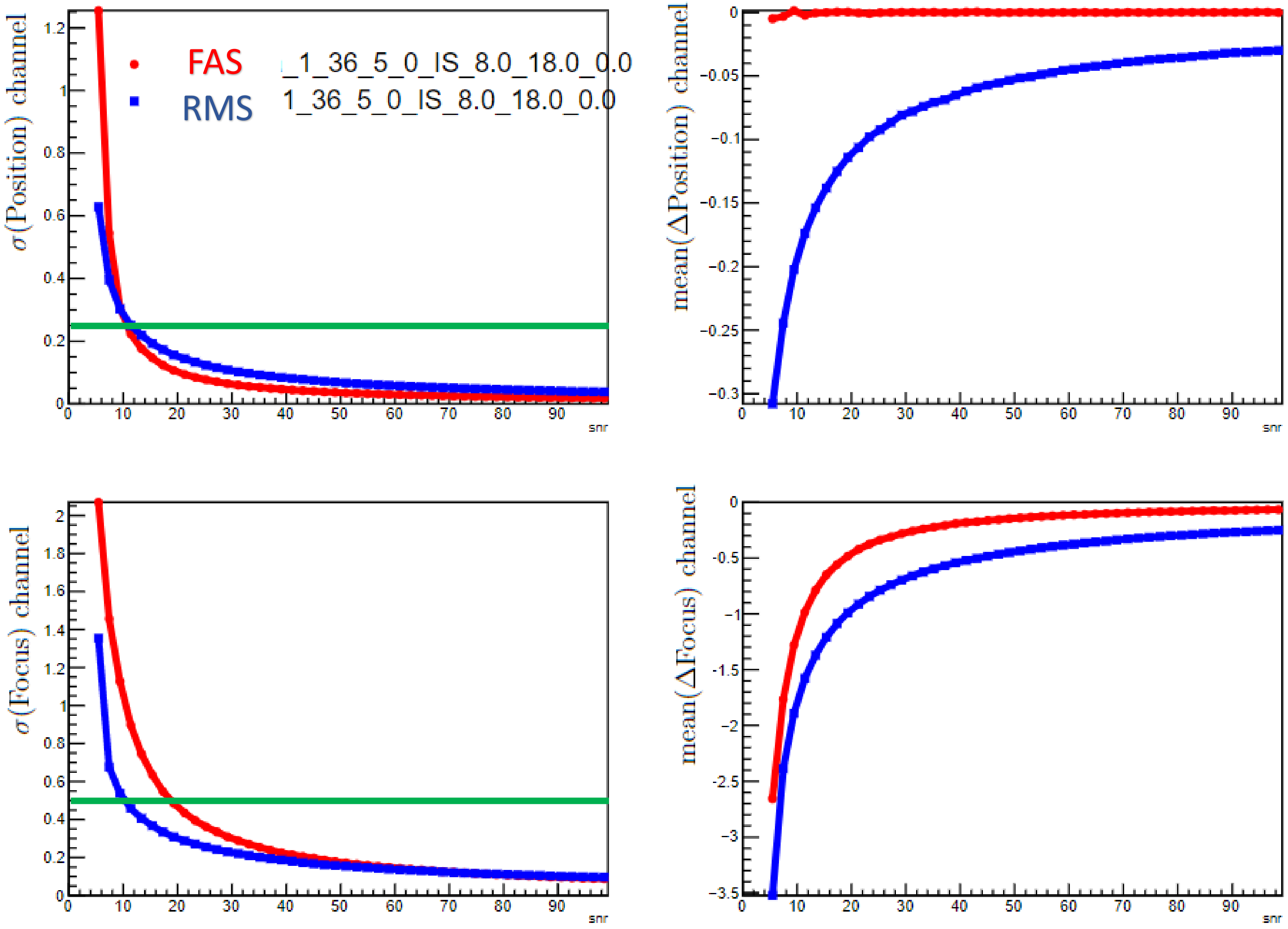
Gets better at higher SNR

Position from least squares no bias

MWPCs use RMS
we'd like to provide improvement with linear regression



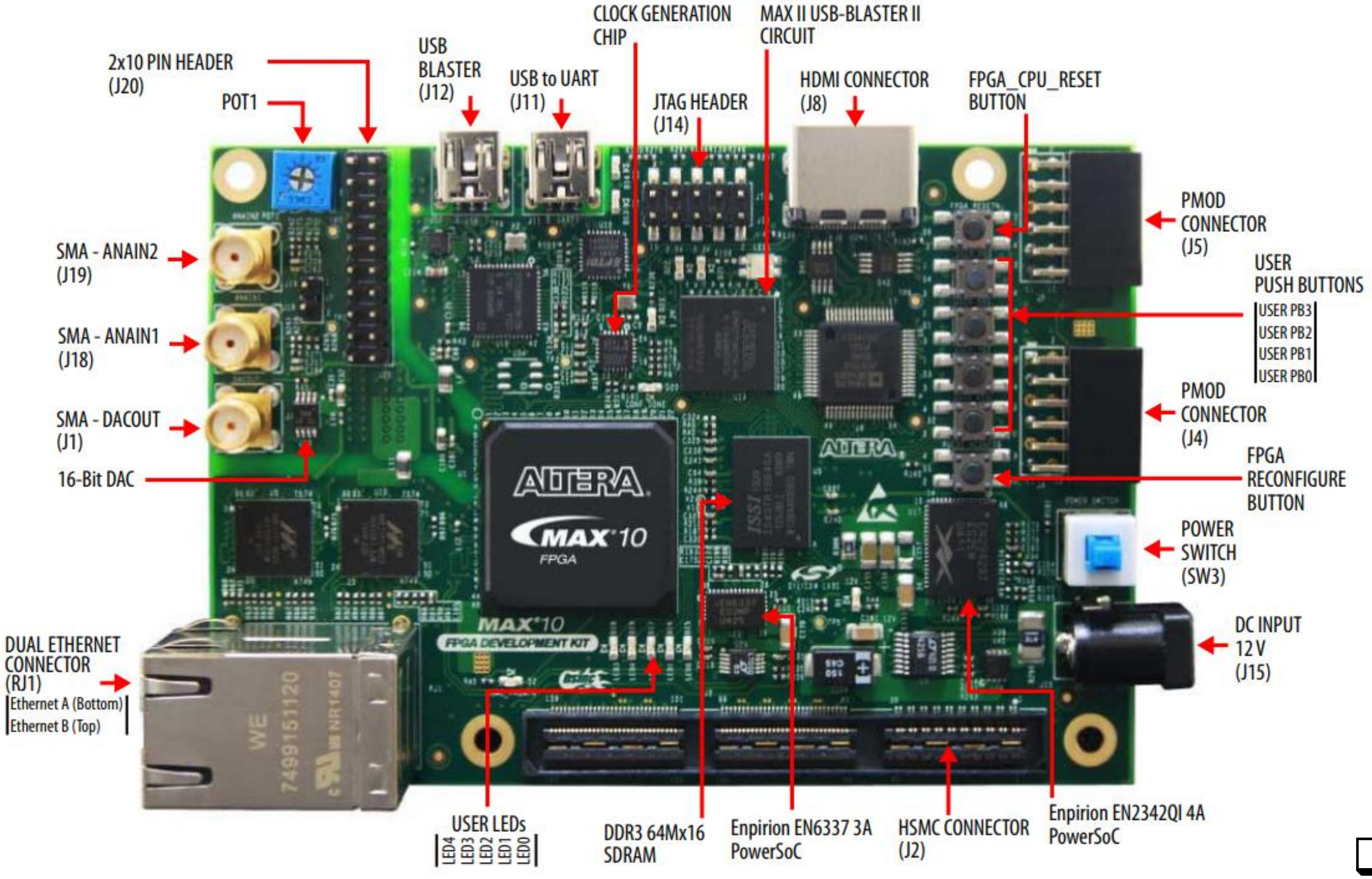
Example of gaussian shape with noise



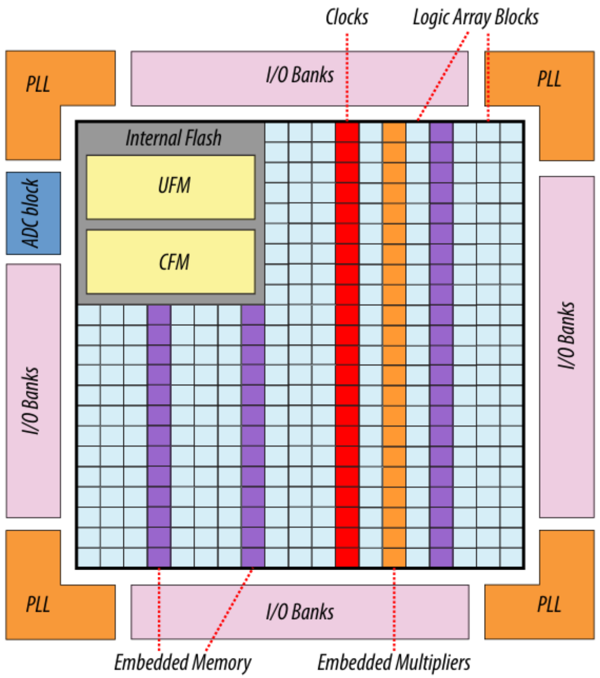
Two candidates algorithm for FPGAs implementation

Real-time reconstruction on FPGAs

MAX10 Development Board



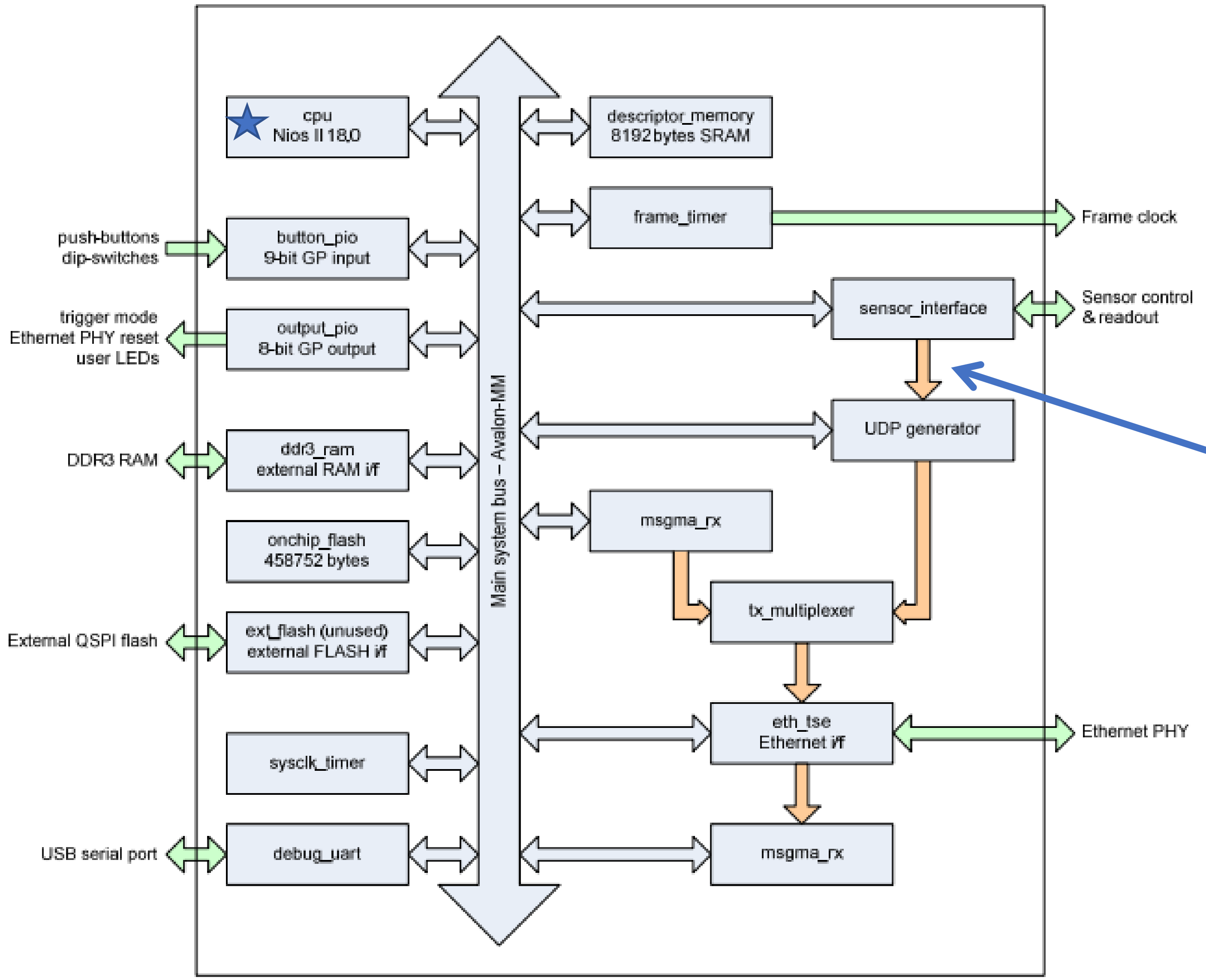
MAX10 Development Board



MAX10 FPGAs

- HSMC Connector: connect with ADC board
- MAX10 FPGAs: CPU, Data Processing
- Ethernet Connector: communication
- DDR3: RAM for Software
- Flash: for store FPGAs image
- Power

Firmware v1.0



Simplified Platform on FPGA boards for HIT Beam Profile Monitor

- The major part of Michael's firmware.
- ★ The niosII sets up TCP/IP socket server, listening the command for configuring sensor interface.
- The sensor interface controls Photodiode arrays and ADC, collects and packs the data, and sends to UDP generator and then directly to Ethernet.
- The reconstruction algorithm is implemented between sensor_interface and UDP_generator.

Resource on Max10	usage
Total logic elements	32,471 / 49,760 (65%)
Total registers	23632
Total pins	156/360 (43%)
Total memory bits	284,392 / 1,677,312 (17%)
Embedded Multiplier 9-bit elements	6 / 288 (2%)
Total PLLs	2 / 4 (50%)

Reconstruction Process

Data in ⇨ Background Subtraction ⇨ Cluster Locating ⇨ Calibration ⇨ RMS/FAS ⇨ Data out

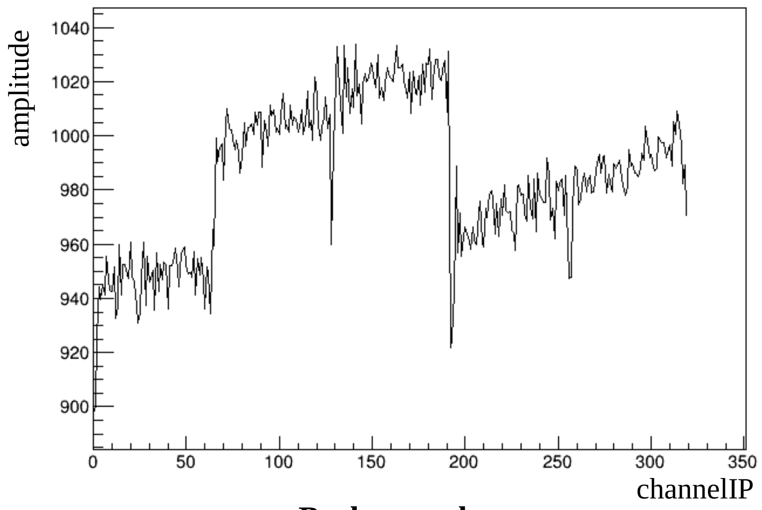
16-bit Signal stream from sensor_interface;

Background Subtraction: calculate the average signal of each channel of the first 8192 frames; and start subtract background from the 8193rd frame;

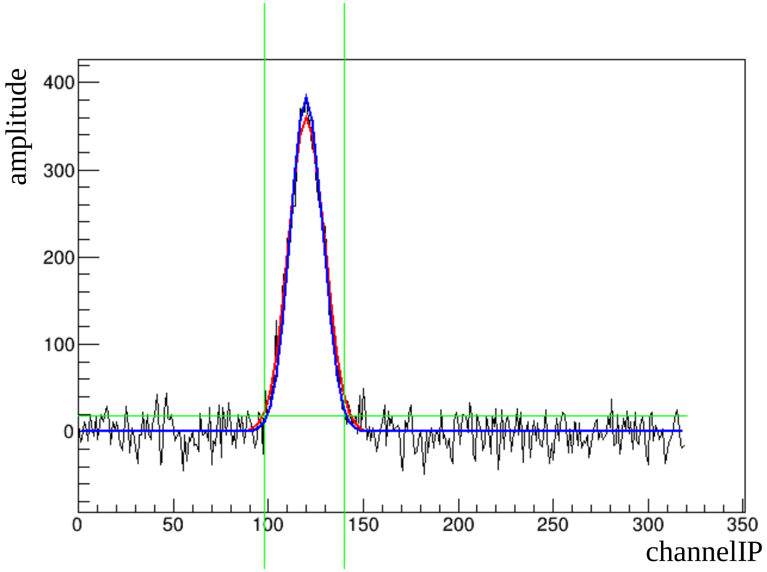
Cluster Locating: two parameters, cluster_size and threshold, find the cluster above threshold with length larger than cluster_size, store the leftmost and rightmost channelIP in registers; output if there is cluster or not.

Calibration: calibrate difference between channels

RMS/FAS: calculate the mean and sigma by the signal inside the cluster;



Background



Example of cluster locating and rms

Basic idea for design on FPGAs & Current Status

Stream in → Background Subtraction → Cluster Locating → RMS → Stream out/with data after bkg_sub

Due to the limited logic resource on Max10, and tolerance in latency:

- Calculation is done one channel by one channel;
- RAMs are used for store the background subtraction and pipeline the signals;
- All the calculations are with fixed point;

The size of each registers is from C++ code simulation.

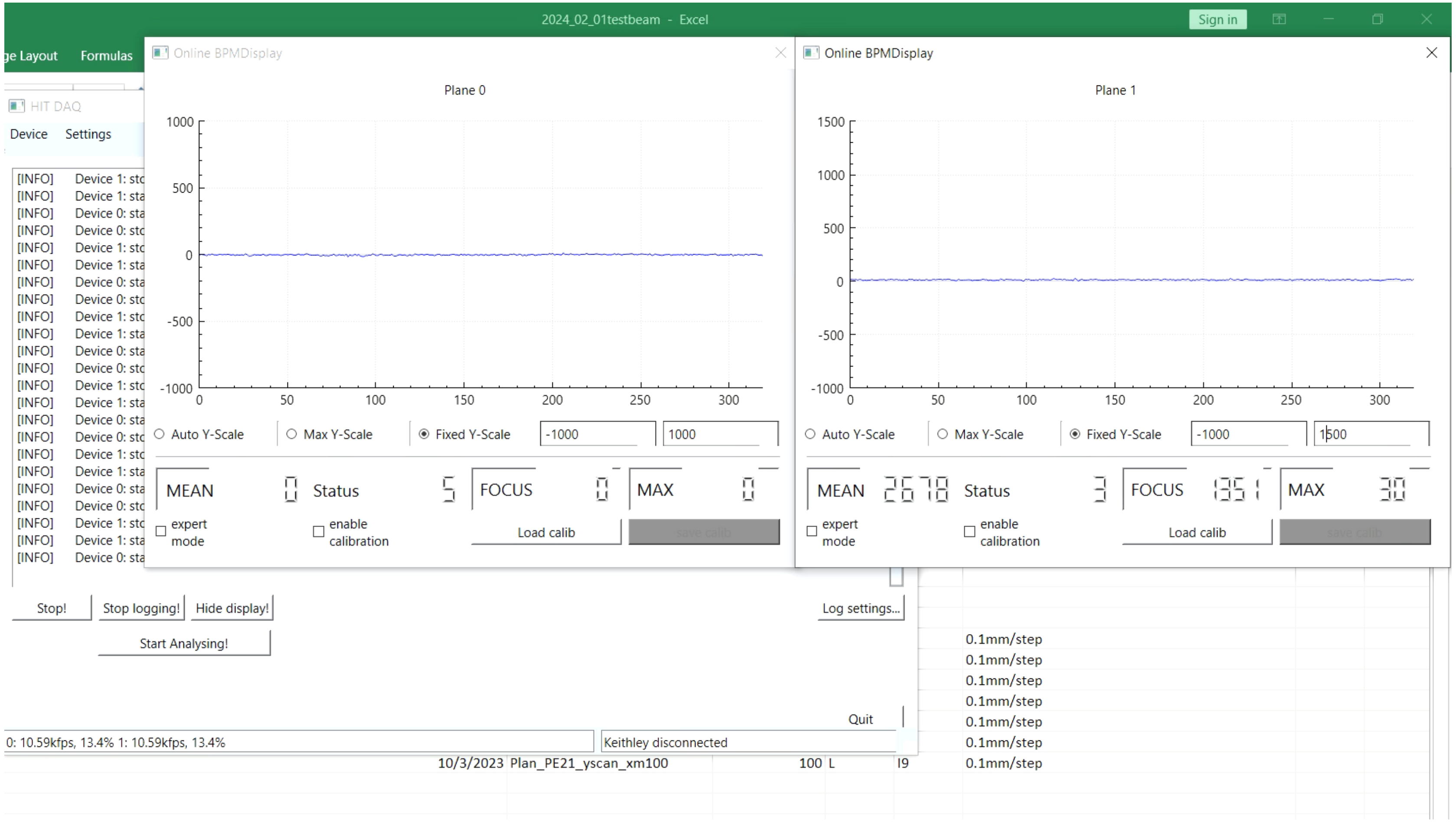
From the end of integration window for photodiodes, until the result stream out, there is about 94 micros latency (about **8 micros** from calculation);

Resource on Max10	usage	
Total logic elements	36,421 / 49,760 (73%)	+8%
Total registers	26547	+2915
Total pins	156/360 (43%)	
Total memory bits	307,750 / 1,677,312 (18%)	+1%
Embedded Multiplier 9-bit elements	14 / 288 (5%)	+3%
Total PLLs	2 / 4 (50%)	

Num	RegisterName	bitsize
0	X.Max	11
1	Y.Max	15
2	Y.Sum	18
3	XY.Max	27
4	XY.Sum	29
5	MeanXleftshift	13
6	DiffxMeanX.Max	13
7	DiffxMeanX2.Max	26
8	DiffxMeanX2Yi.Max	41
9	DiffxMeanX2Yi.Sum	38
10	Sigma2	26
11	Sigma0	11

Registers list for RMS example.(the size on FPGA is larger than the bitsize in the table)

Real time line scan



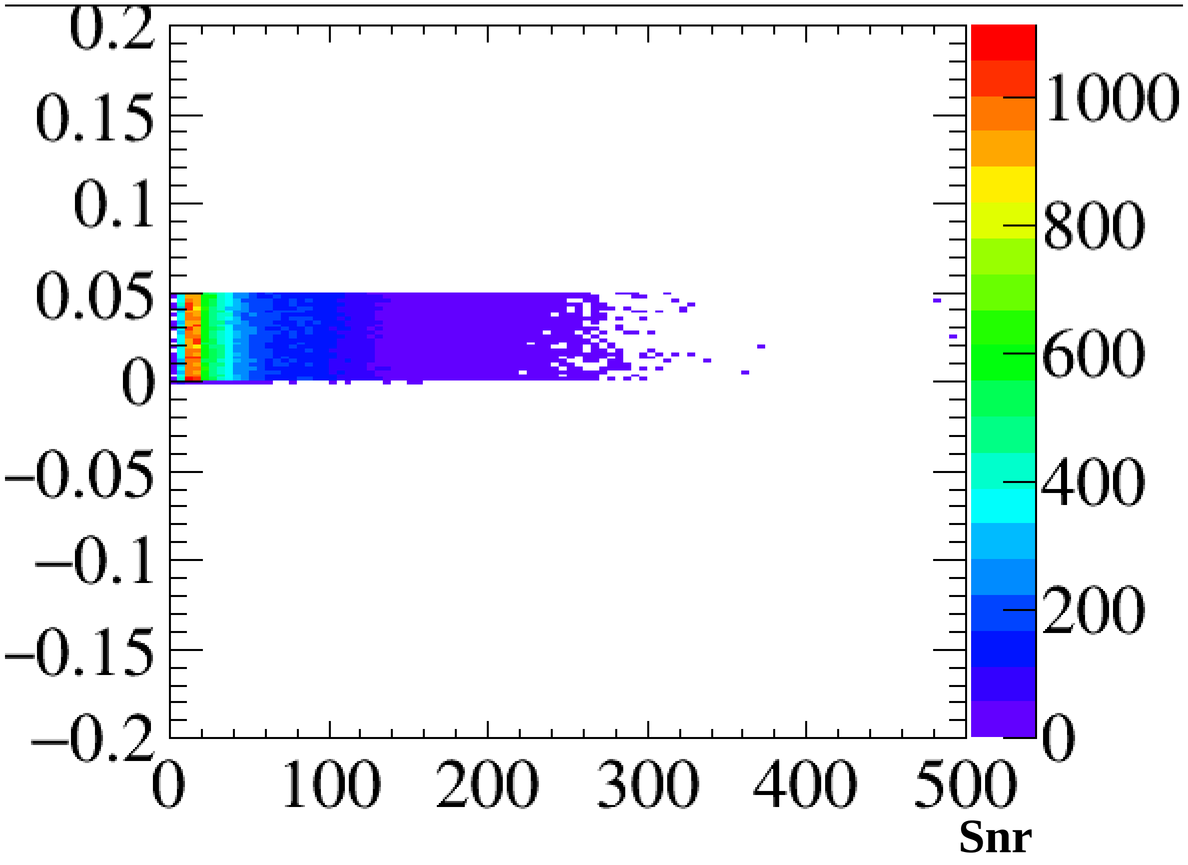
Status 5: no beam; Status 3: there is beam;

Two boards with the same FPGAs setting, including threshold and cluster_size; but board1 is much noisy than board0; The cluster location shows there is cluster for board1 from time to time even there is no beam.

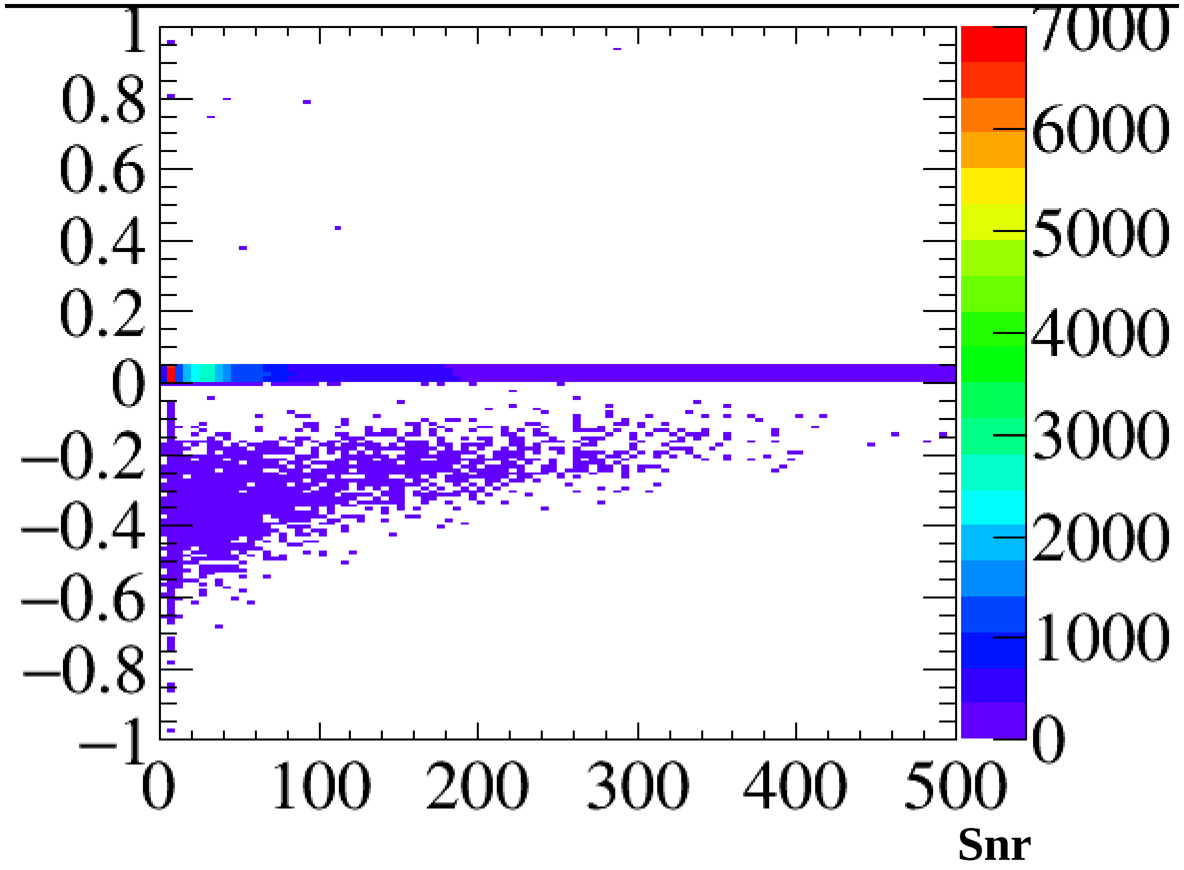
FPGA vs. CPU Position Diff (intensity scan)

Compare the position calculated by FPGAs with CPU; 1 bit is 0.05mm on FPGAs.

Board0: Position Difference(mm) vs. Snr



Board1: Position Difference(mm) vs. Snr



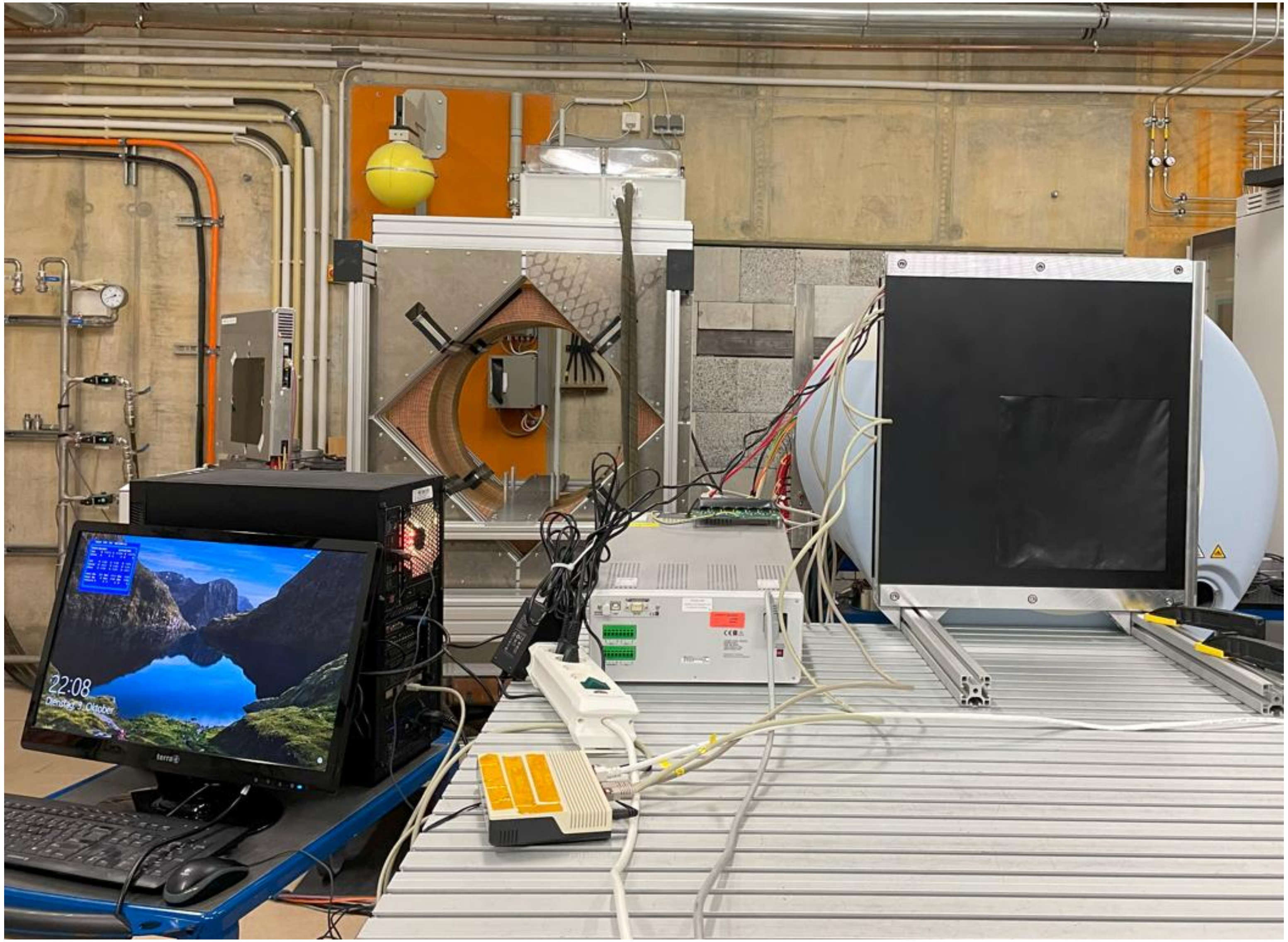
FPGAs for board0 produce the same value as CPU.
Focus diff is similar to this plot.

Measurement and performance

Algorithm for this part, RMS if it's not declared as FAS:

Data after bkg_sub by FGPAs ⇒ Cluster Locating ⇒ Calibration ⇒ RMS/FAS ⇒ results out

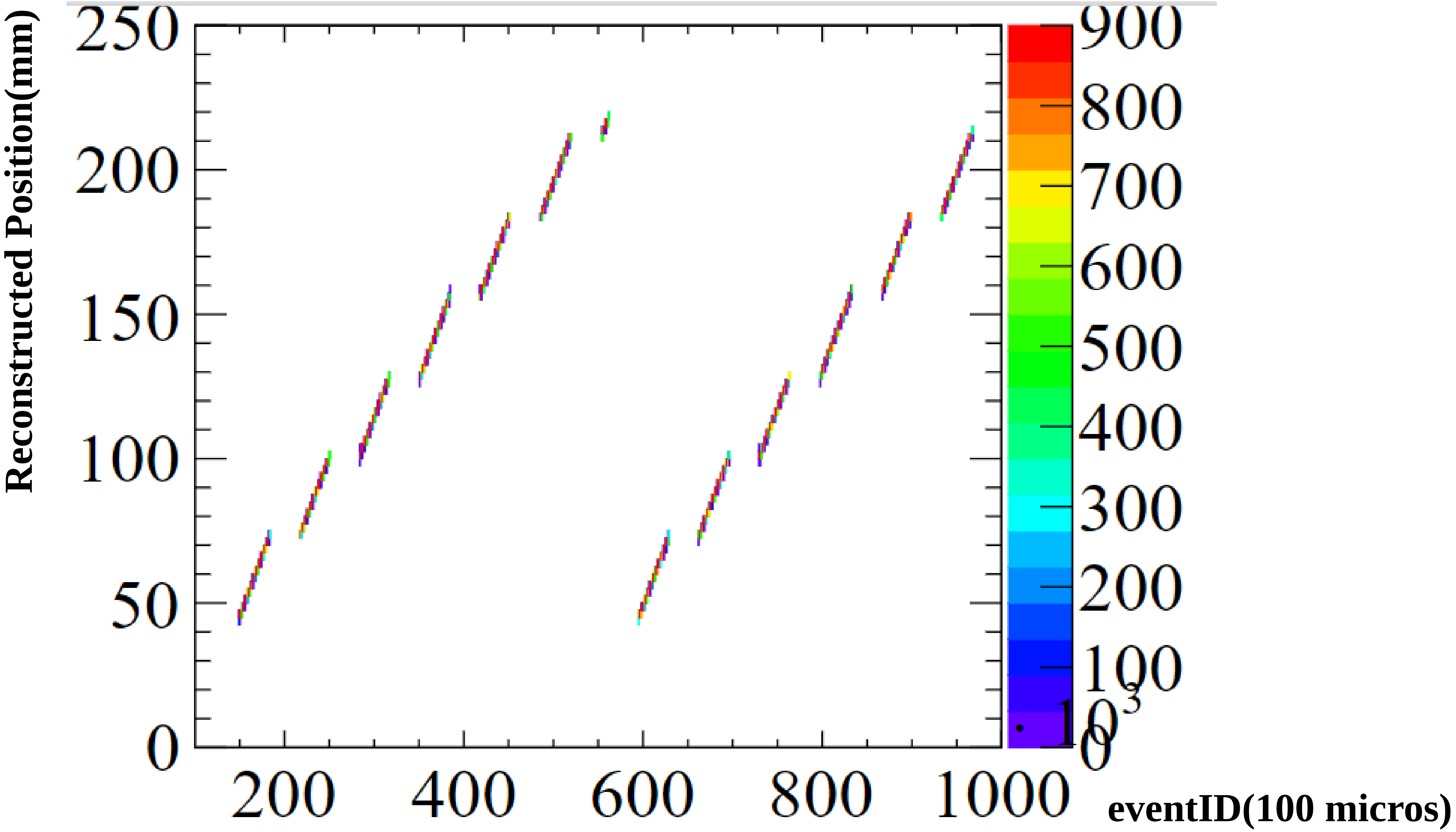
In QA room



To get the beam shape as close to the beam shape at the location of MWPCs as possible=>Detector is very close to beam exit.

Line Scan: Calibration

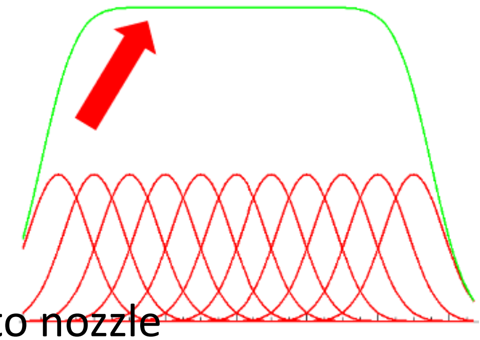
Board0

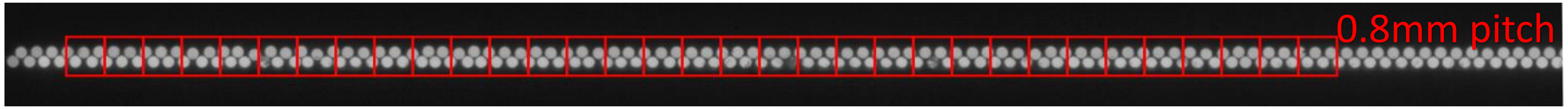


deposit same amount of beam on all the channels with fixed particle type, energy, focus

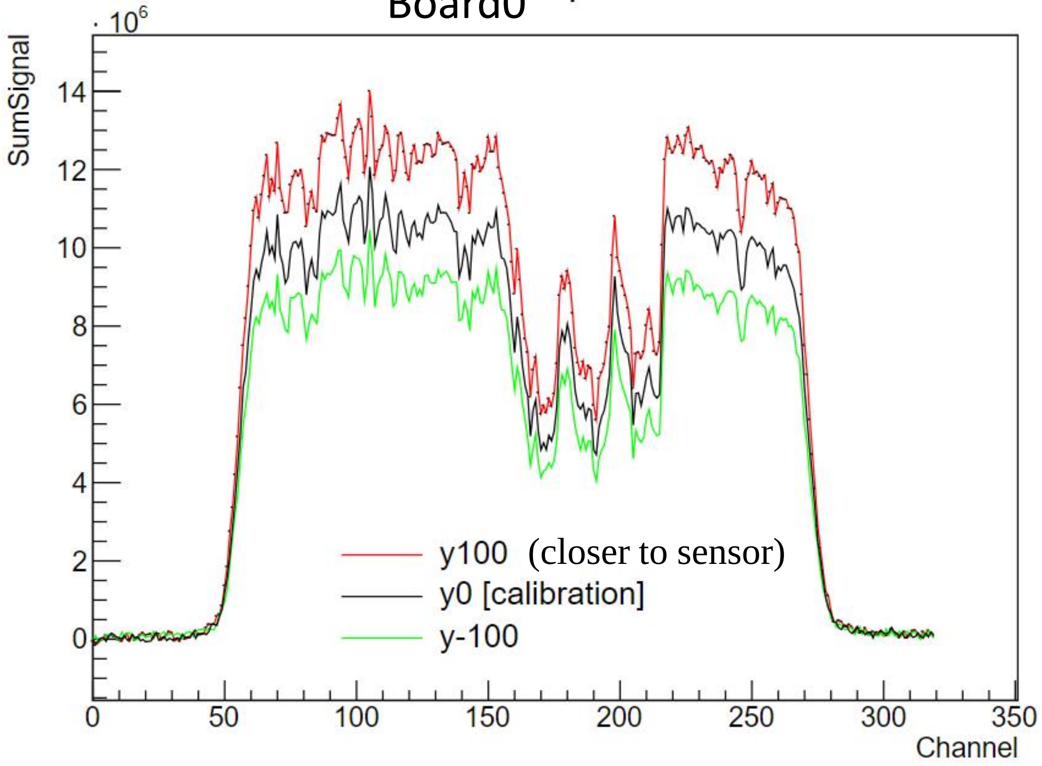
Full range scan

Purpose: Calibration the difference between channels (fibers per diode, optical coupling, ~~radiation damage~~, photosensor)
Method: line scan, beam width: 26-channels, step size: 0.1 mm (0.125 channel)

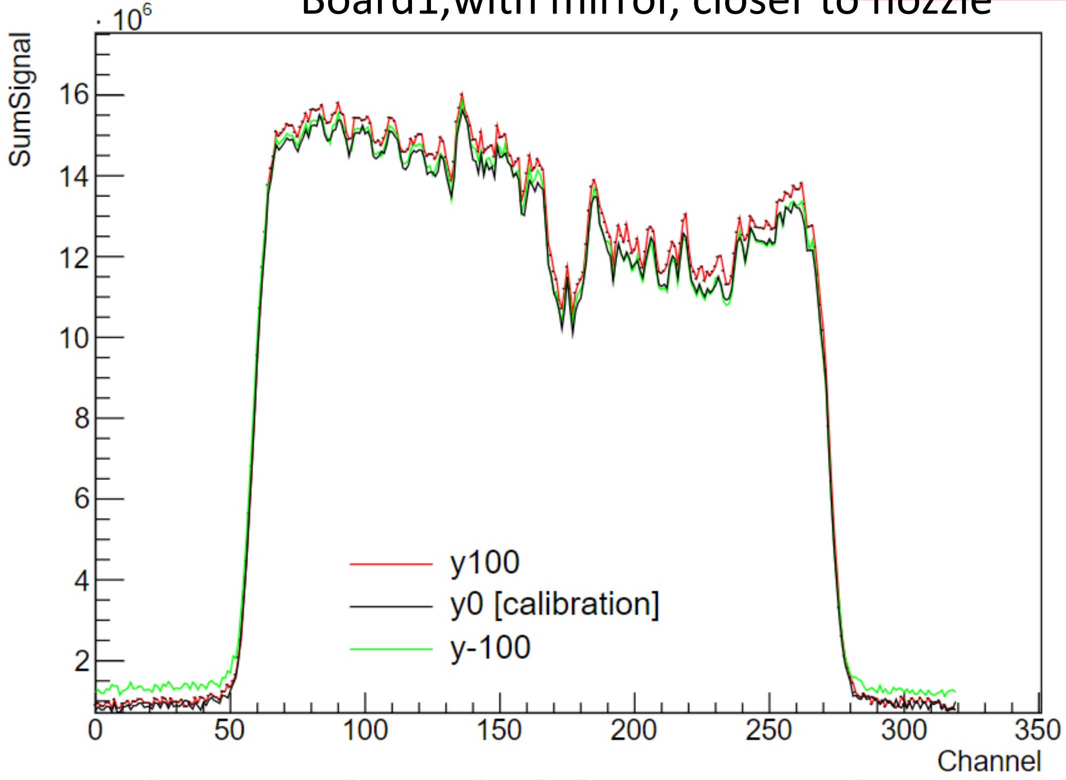




Board0



Board1,with mirror, closer to nozzle

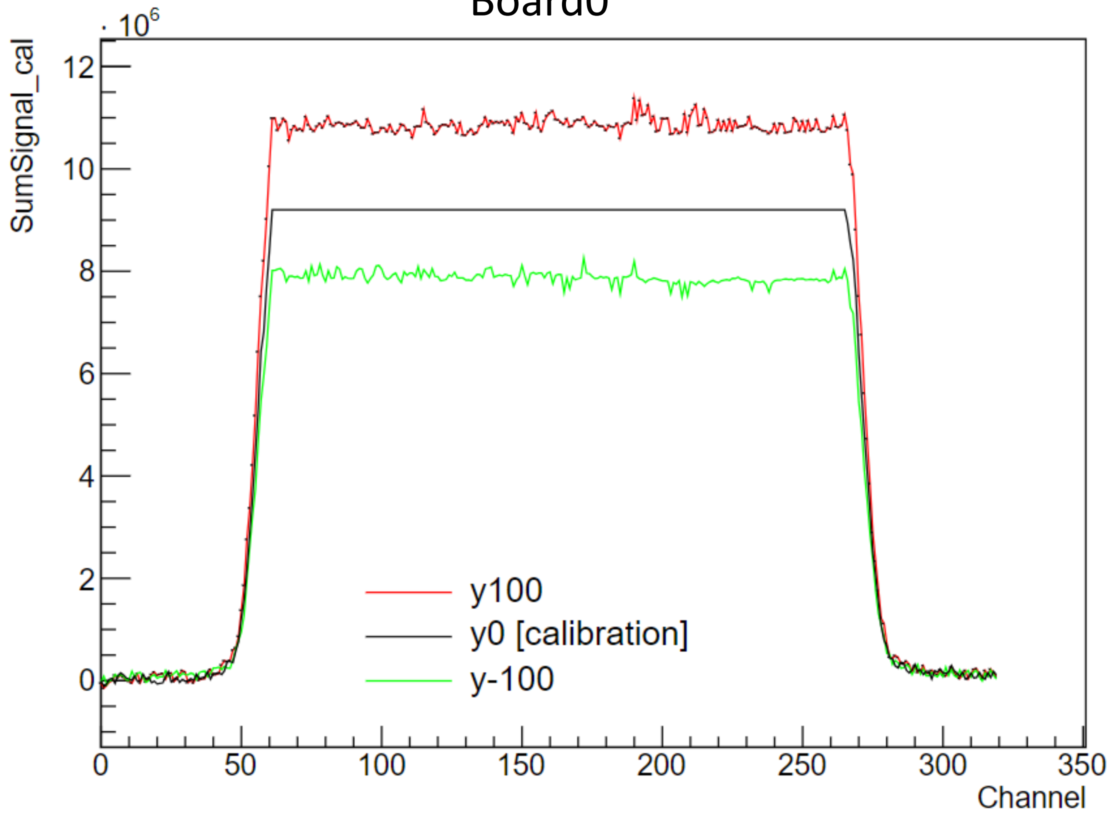


These scans cover the whole pencil beam scan area. About 80 channels did not get any beam.
Mirror improves the amplitude, alleviate the attenuation

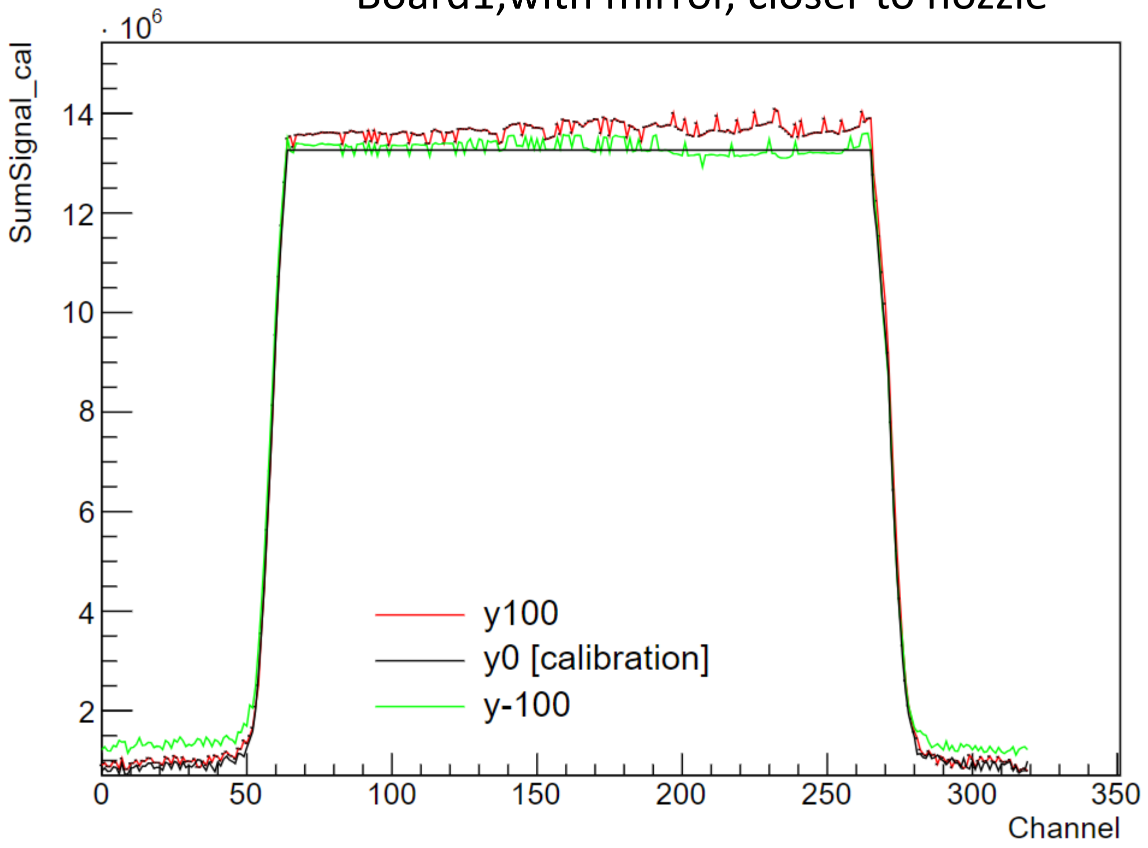
SumSignal_cal

Inverse the sum of signal => calibration factor.
Calibration factor*Signal => calibrated signal.

Board0

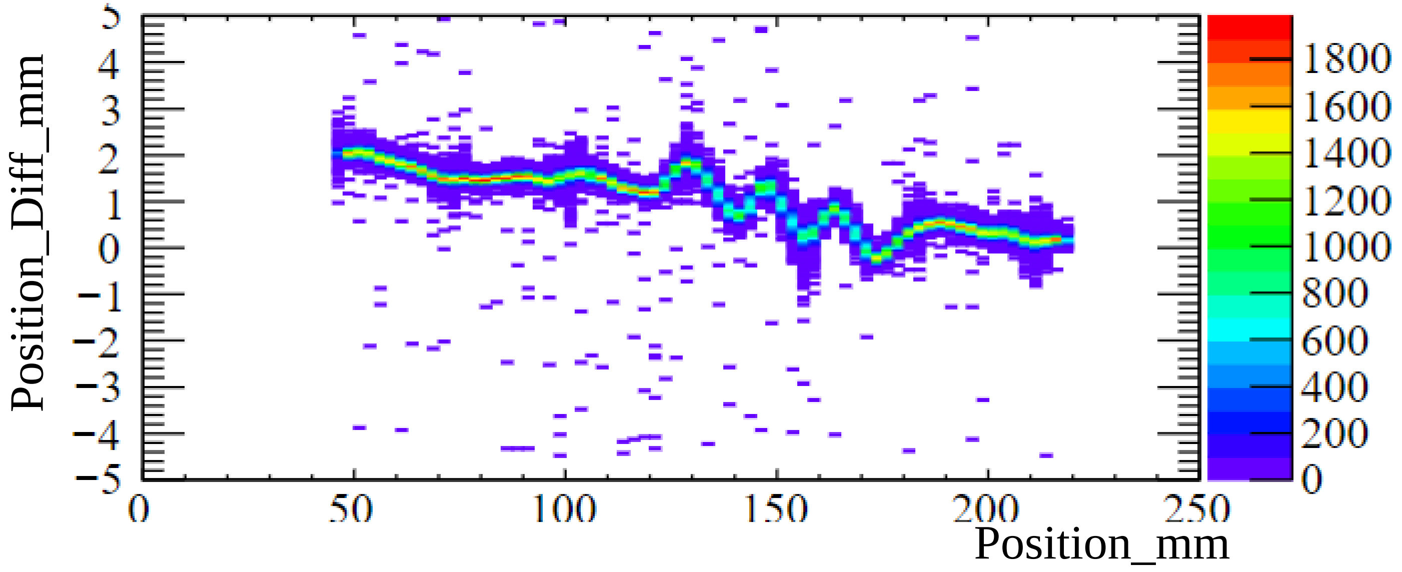


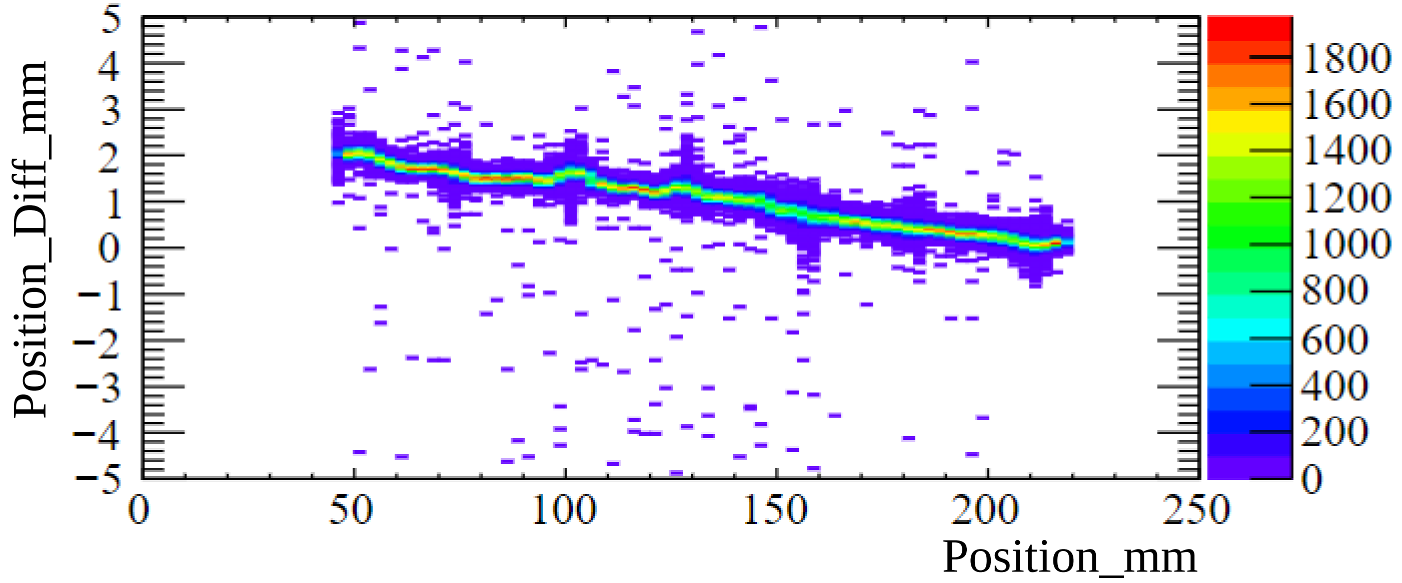
Board1,with mirror, closer to nozzle

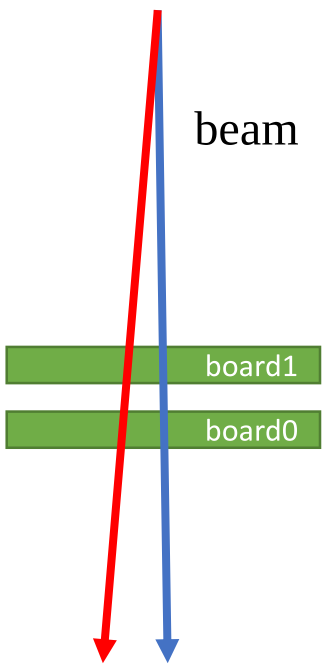


~30% attenuation in 20cm
sum_signal much even after calibration

Position Difference between boards before and after calibration



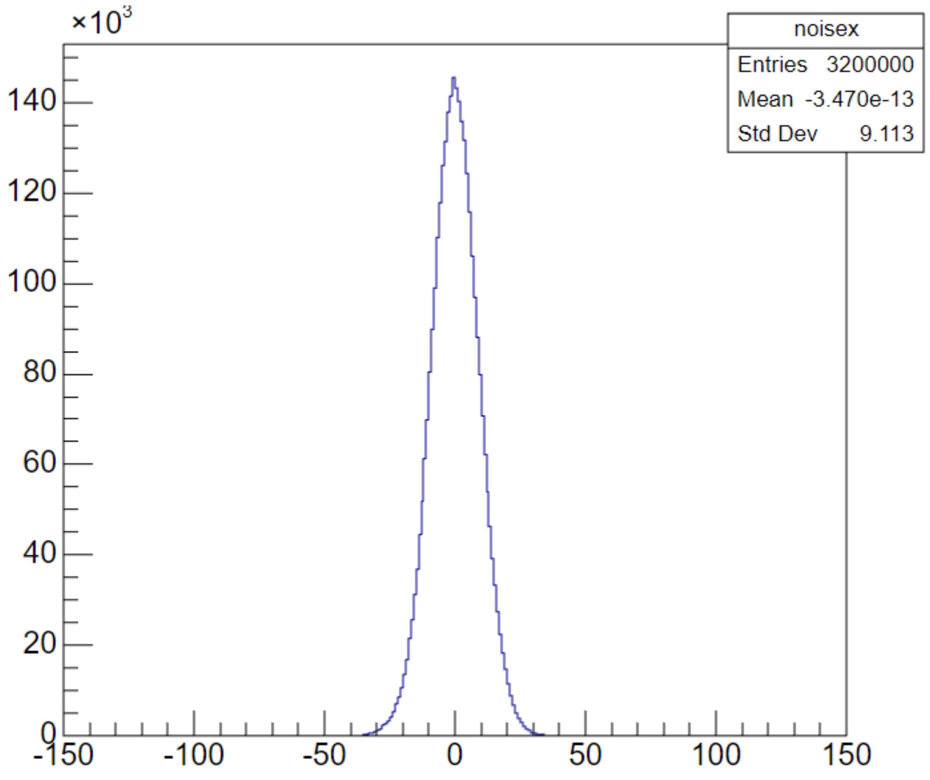




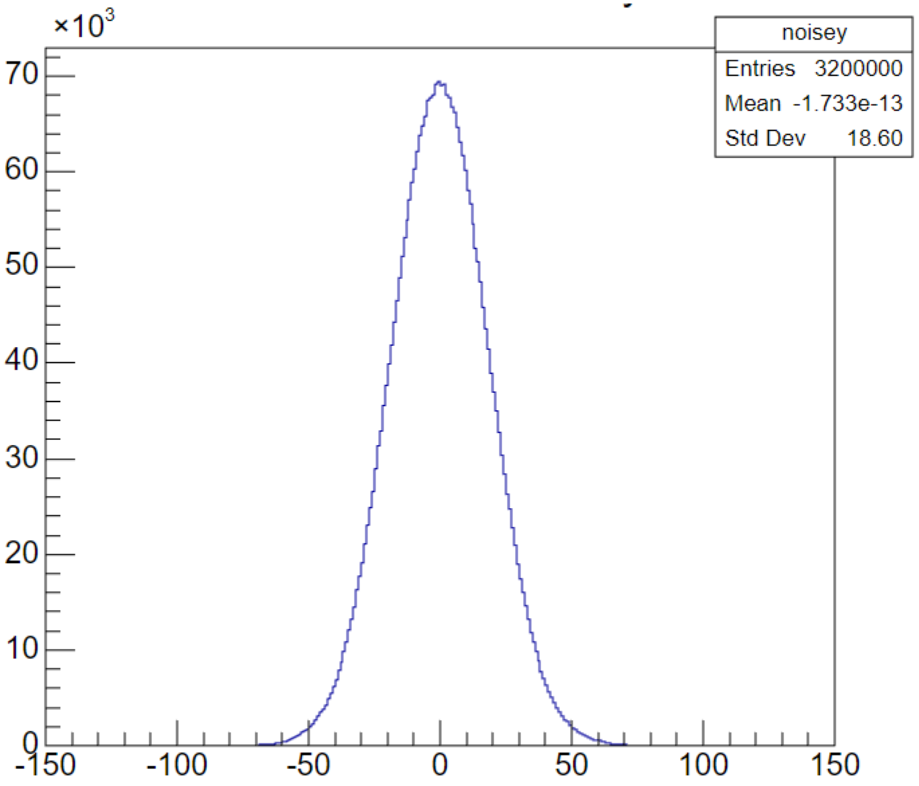
Position difference slope caused by beam angle
Calibration decrease the bias

Beam OFF: Noise

Noise level (Integration time 100 micro seconds)



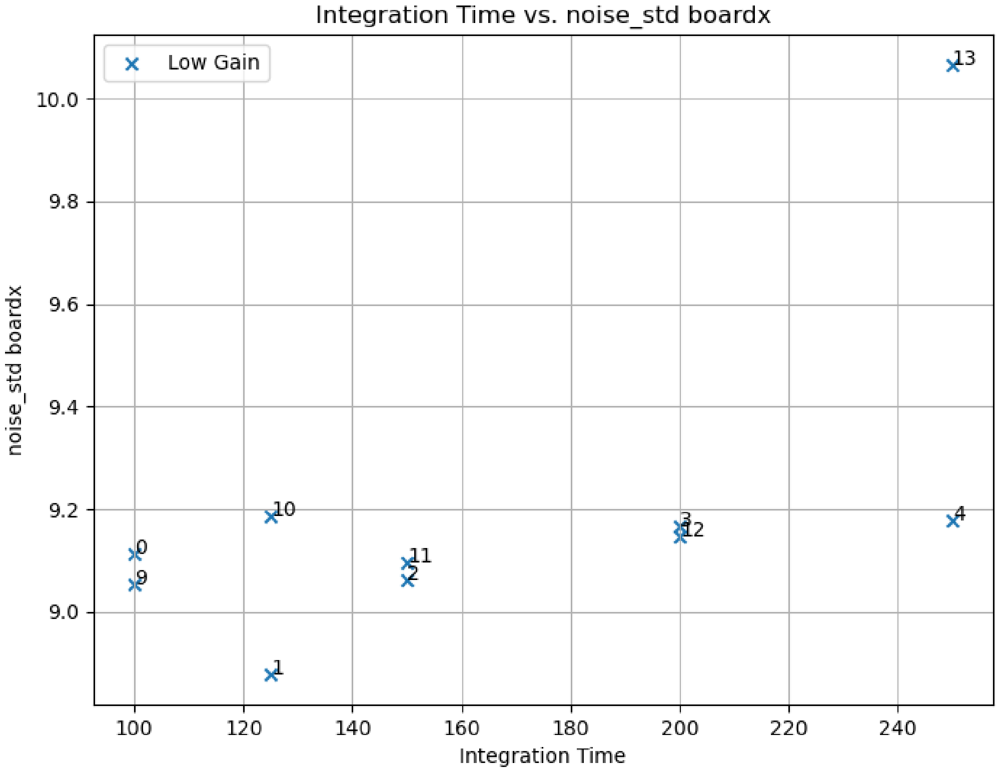
Board0, 9.113



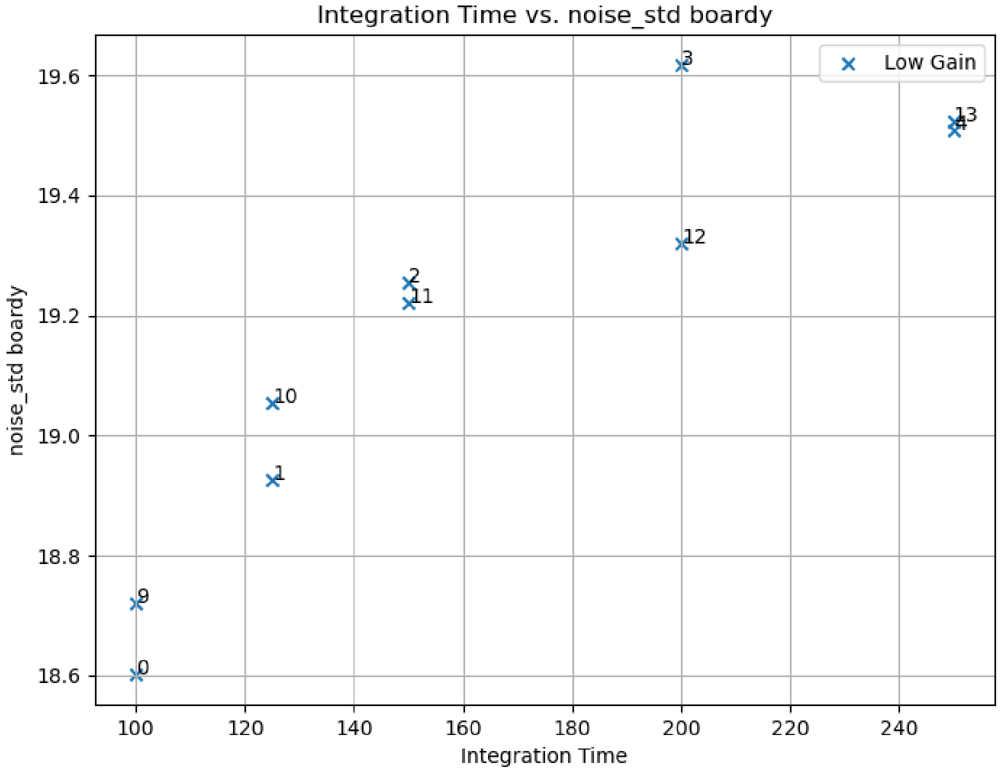
Board1, without noise filter inductance,18.60

histograms for noise for all the channels in 1 s for board0 and board1 after background subtraction.
Board1 is with newly build frontend ADCs board. The noise filter inductance was not there at test beam.

Noise level vs. integration time



Board0

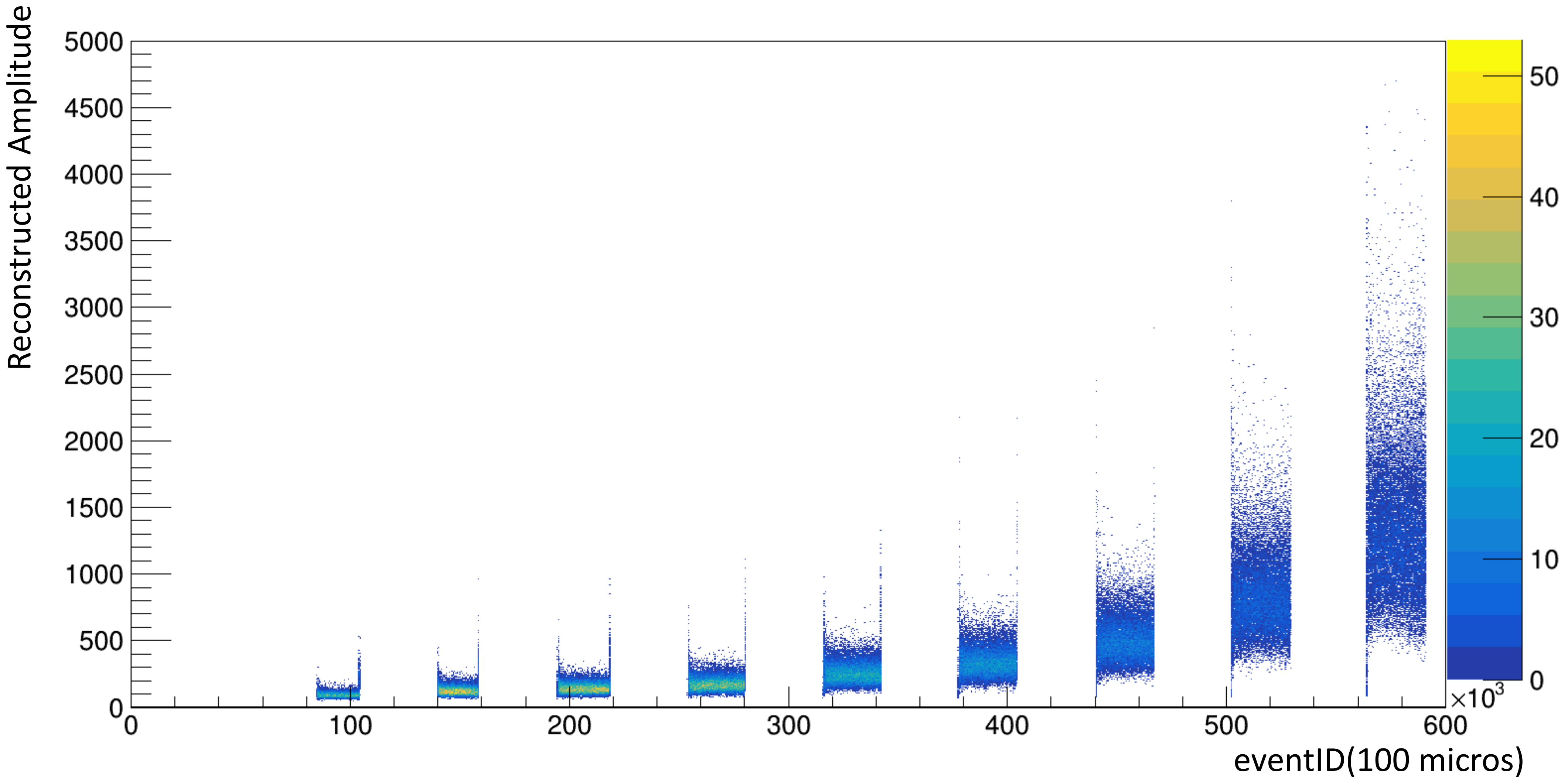


Board1, without noise filter inductance

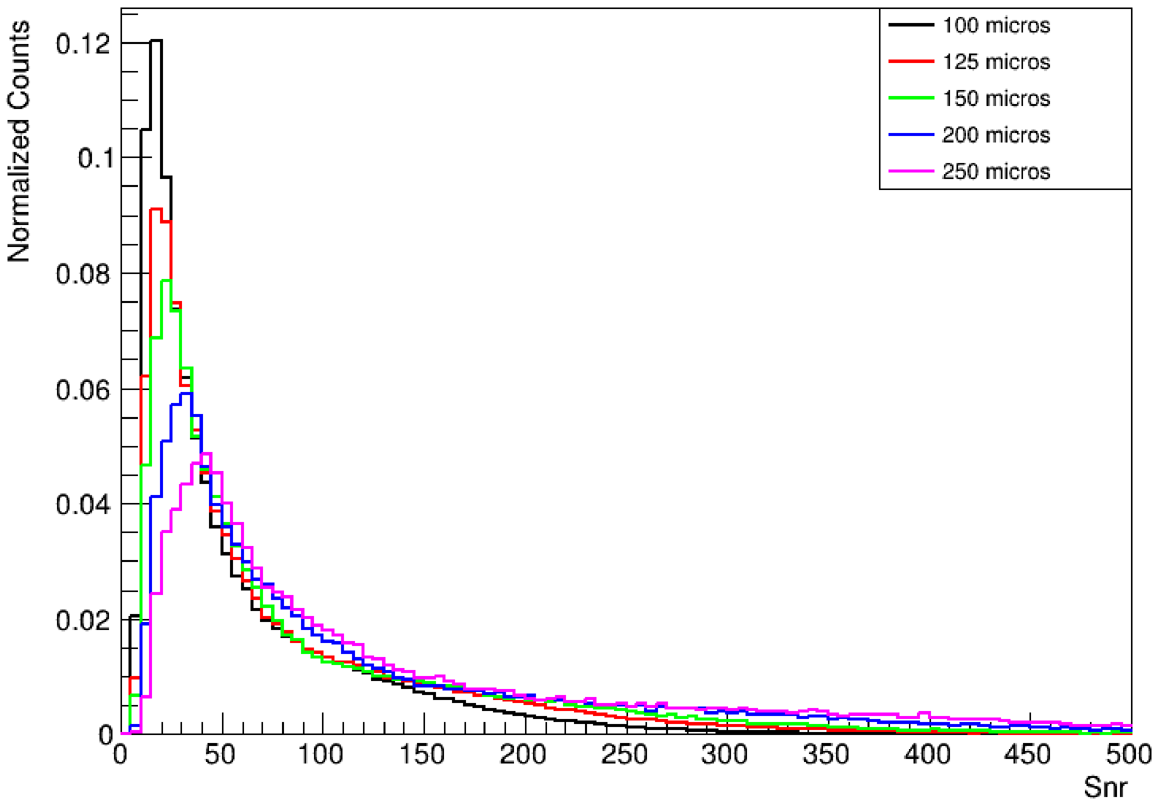
The noise level is basically stable for board0, while it increases with integration time for board1.

Intensity Scan: Snr

Intensity increasing

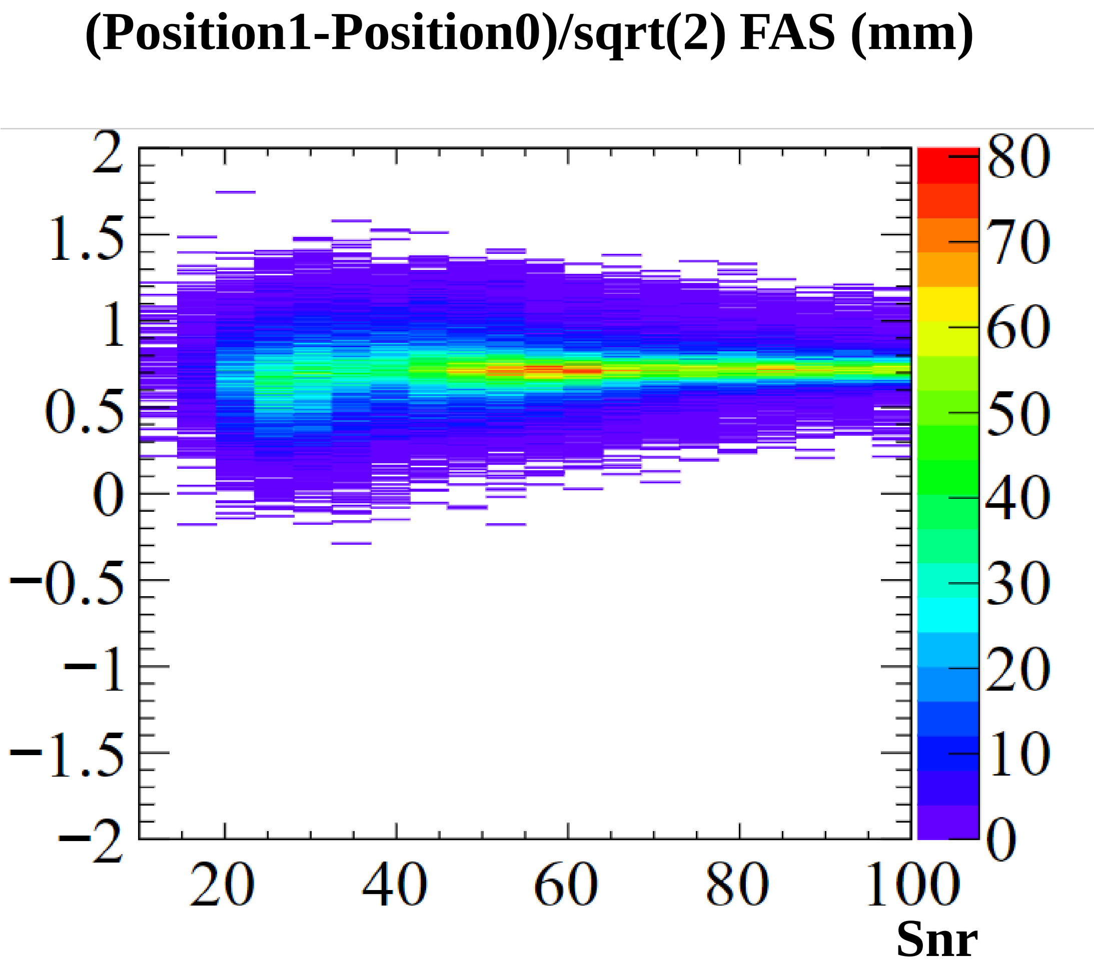


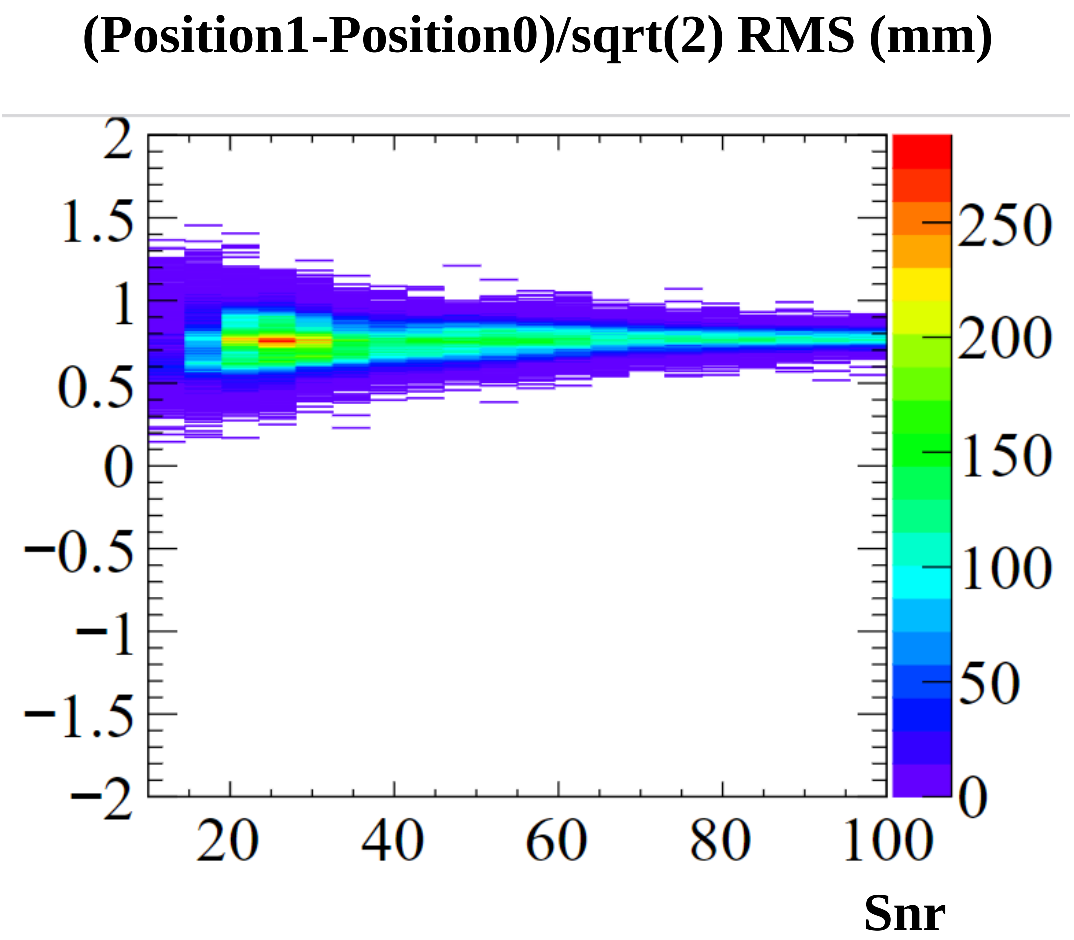
Snr Hist with Integration time



The Snr increase with integration time.
We can increase integration time to get better performance.

Position Difference of two board



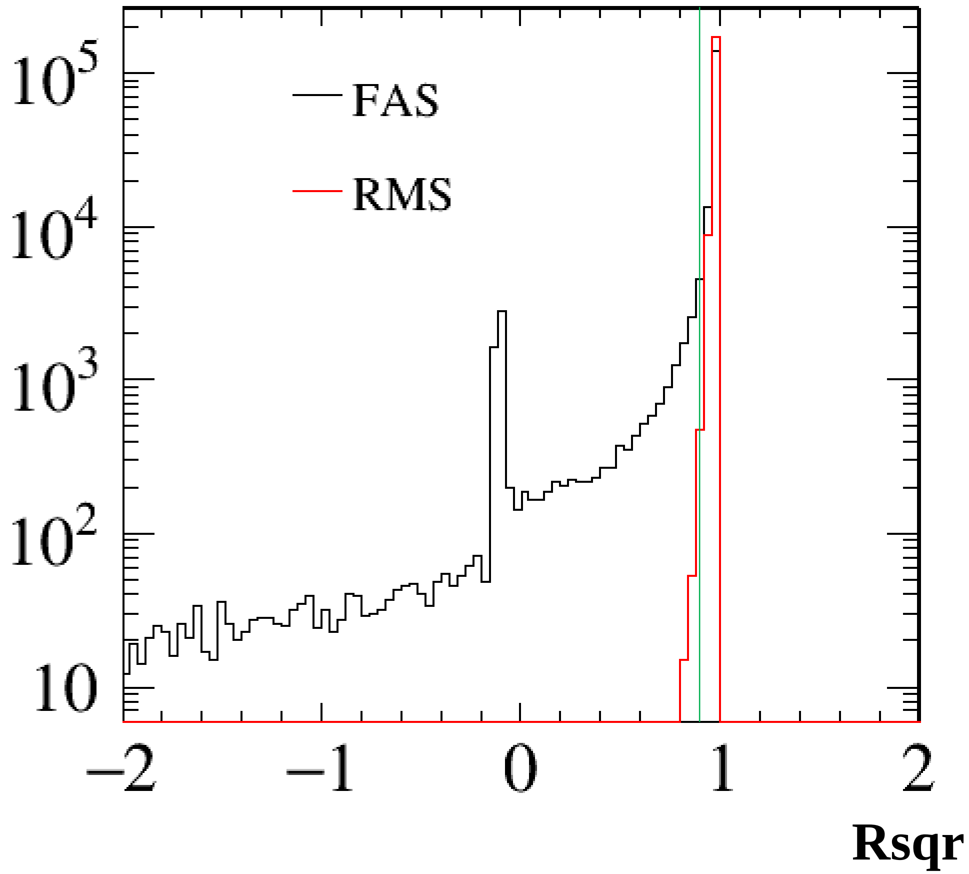


RMS is better than FAS, probably is caused by the unstable baseline of board1. FAS is more sensitive to baseline???
FitsliceY, take the width of the fit as resolution.
With Rsqr>0.9 cut.

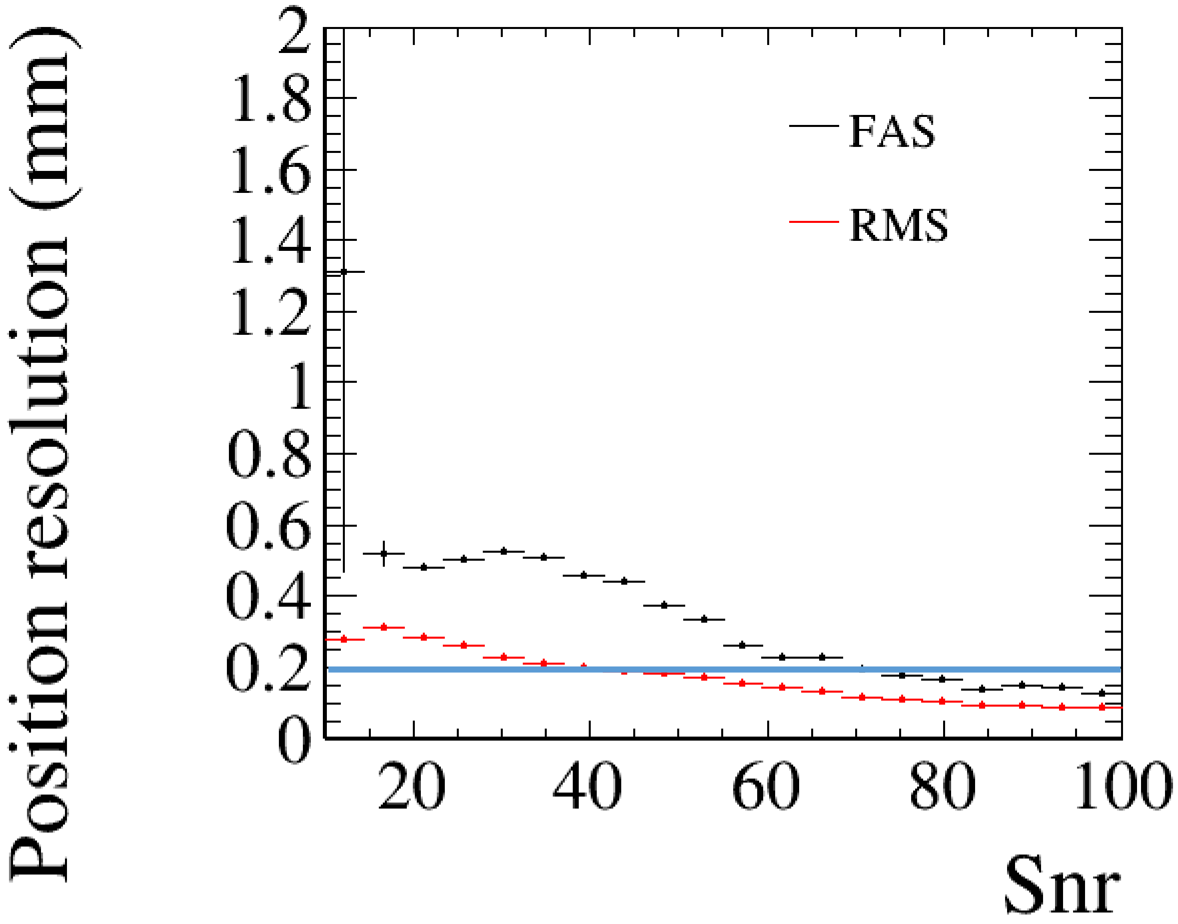
Rsqr Hist for FAS and RMS

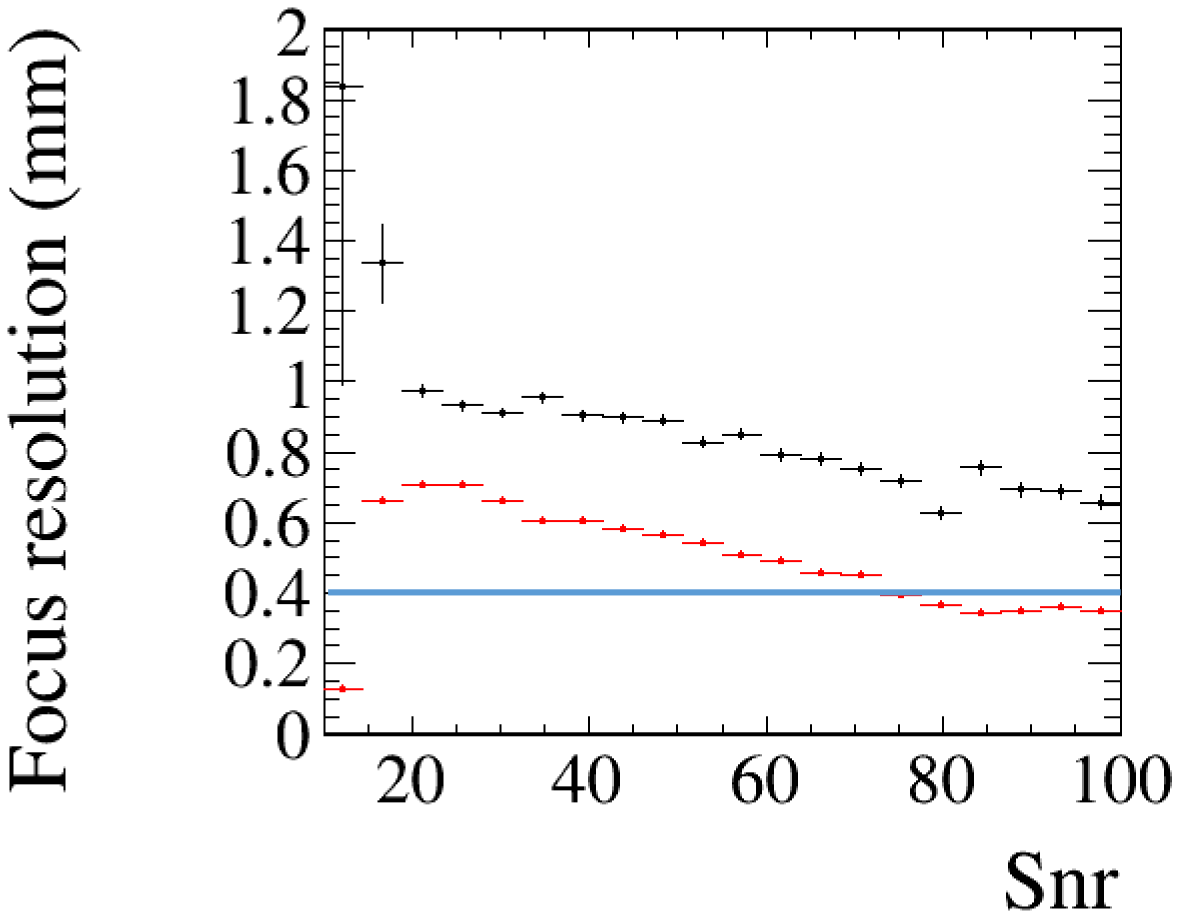
$$Rsqr = 1 - \frac{\sum(y_i - f(x_i))^2}{\sum(y_i - \bar{y})^2}$$

Rsqr, the closer to 1, the better.
RMS is much better than FAS, somehow.



Position and Focus resolution





Resolution getting better with Snr
Not fully understand FAS vs. RMS

Summary

- BPM design basically done
- ADC boards needed to be debug
- RMS with background subtraction and cluster locating implemented on FPGAs
- FPGAs firmware proved by CPU result
- Next step: calibration on FPGAs

Questions to be answer:

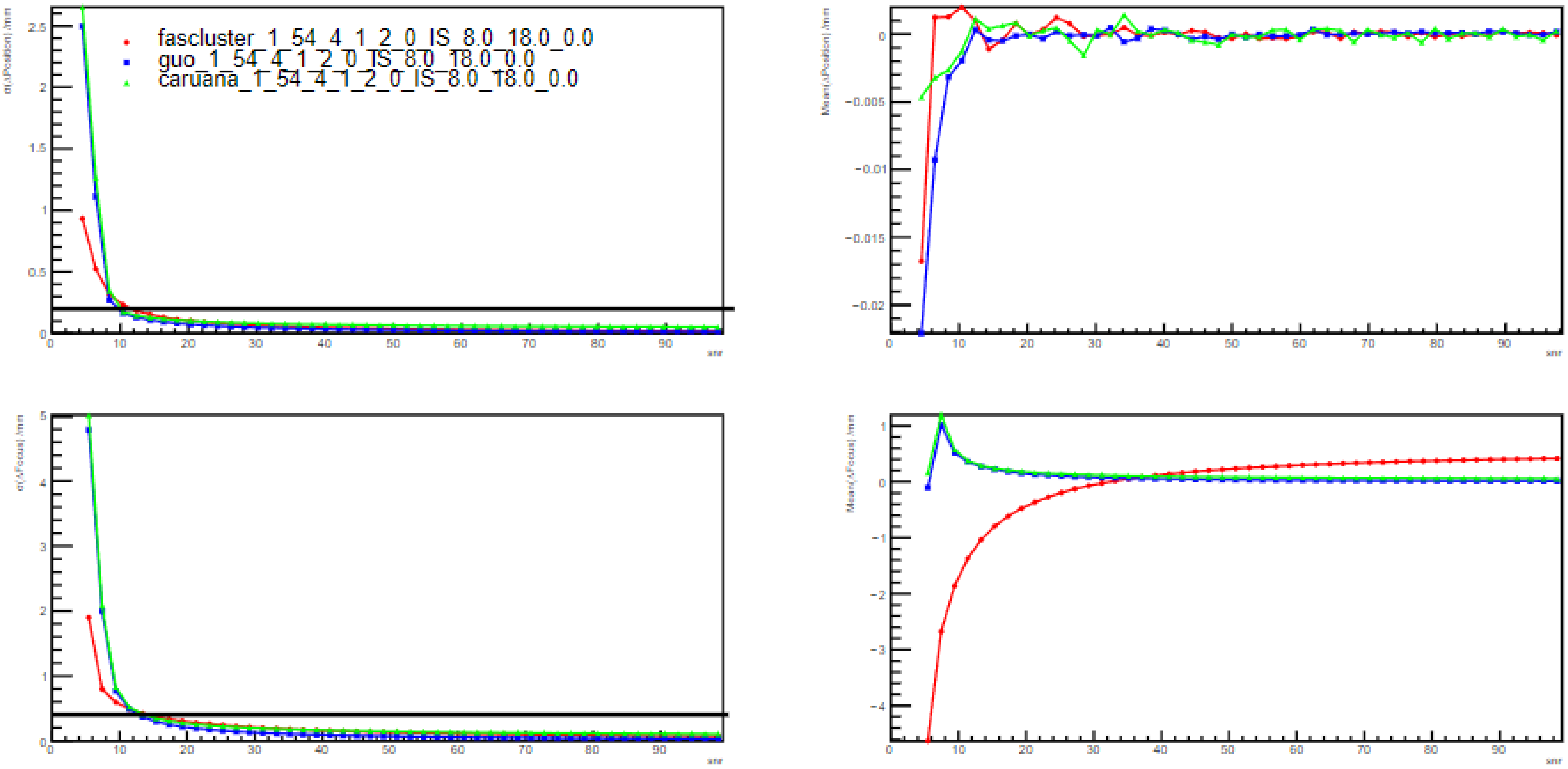
Why RMS better than FAS in newest results?

Questions to audiences:

advice or comment about FPGAs design workflow?

Thank you for you attention

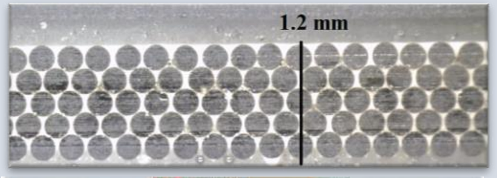
Toy intensity scan

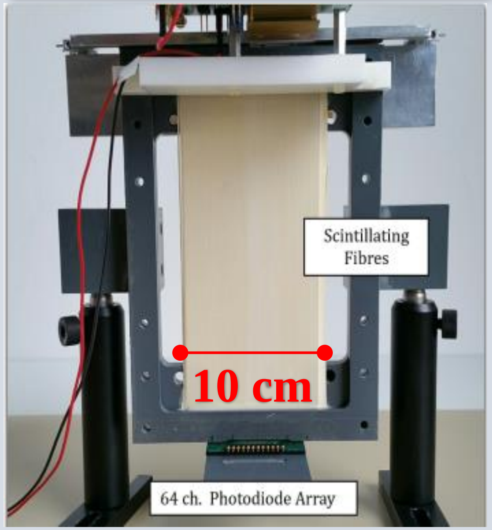


Scintillating Fiber-based Beam Profile Monitor Iteration Overview

2017
Prove of Principle

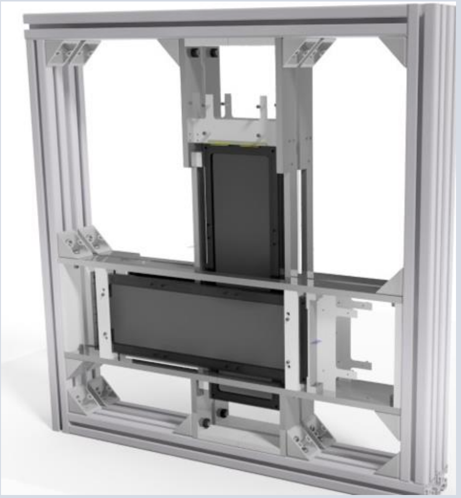
- 10 cm wide
- 1.2 mm thick
- 64 channel Photodiode Chips
- USB 2.0
- 1-3 kHz





2021
Calibration
Resolution study

- First 2-layer mat
- 10 cm wide
- 0.46 mm thick
- 128 channel
- Ethernet RGMII
- 10 kHz

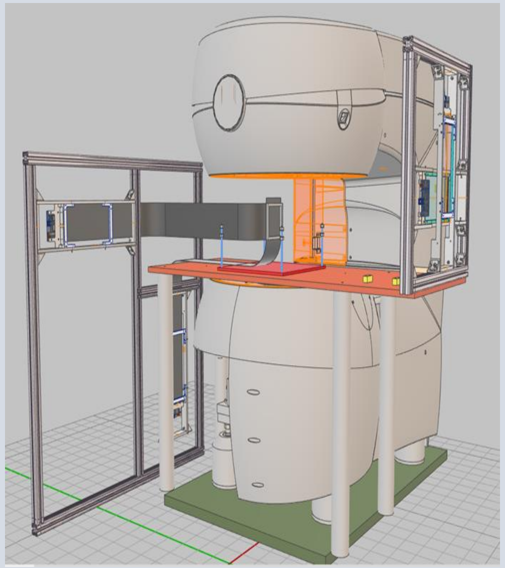


2022
Correlation with MWPCs

- First 2-layer glueless fiber mat
- 10 cm wide
- 128 channel
- 0.3 mm thick

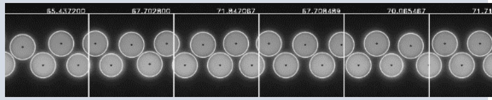
2022
First test under MRI

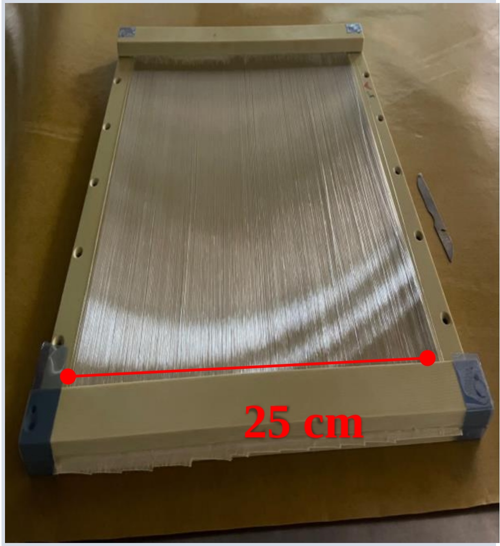
- 10 cm wide
- 2.5 m long



2023 and future
Real-time algorithm implement on FPGAs

- First 25 cm wide
- 0.3 mm thick
- Better lined up
- 320 channel





Compare with MWPCs

- Large active area
- Low cost
- ✓ Good spatial resolution due to high granularity. 0.25 mm
- ✓ Decay time in the order of several nanoseconds
- ✓ Not sensitive to magnetic field
- ✓ Function well at high intensity
- ✓ Without Gas handling requirement
- ✗ Material in active area