

LDO characterization

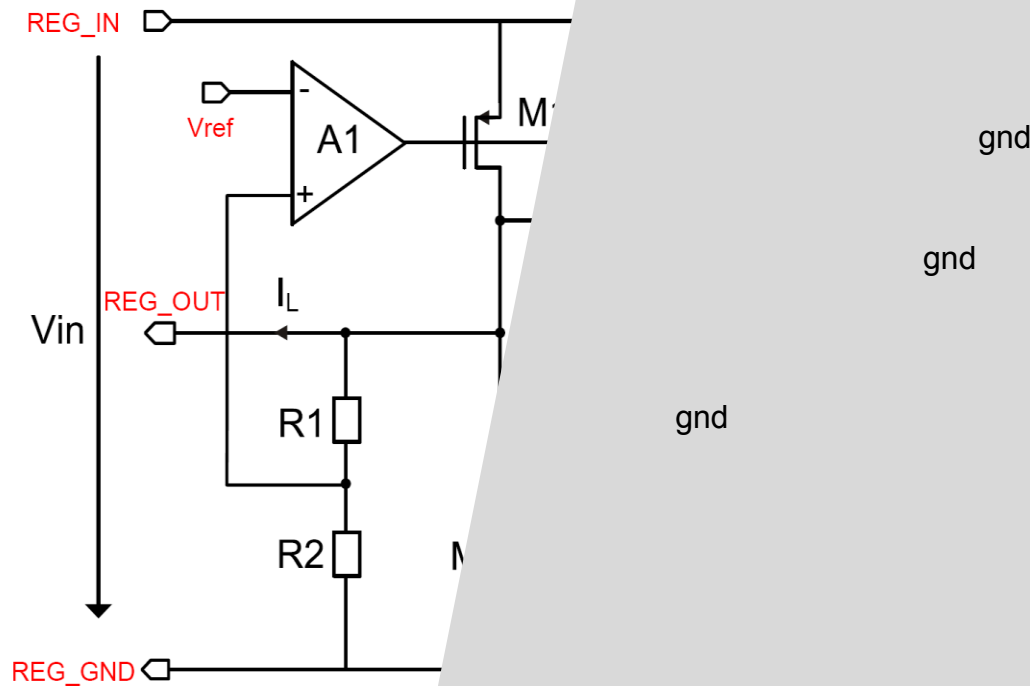
Laura Gonella

Physikalisches Institut Uni Bonn



LDO mode fo the Shunt-LDO regulator

- The Shunt-LDO can be used as a normal LDO by switching off the current regulation path
 - Set Rint, Rext, VDDShunt to gnd
- For the IBL the shunt-LDOs in FE-I4 will be used in LDO mode



Outline

- Single device characterization
 - Quiescent current
 - Line regulation
 - Load regulation
- Regulator safety
 - Overvoltage
 - Short at the output



Quiescent current

- Current flowing through the regulator when it is on but without a load

Vdrop (mV)	Iq (mA) @ 1.2V	Iq (mA) @ 1.5V
100	0.87	1.18
200	1.05	1.26
300	1.17	1.32
400	1.23	1.36
500	1.27	1.42

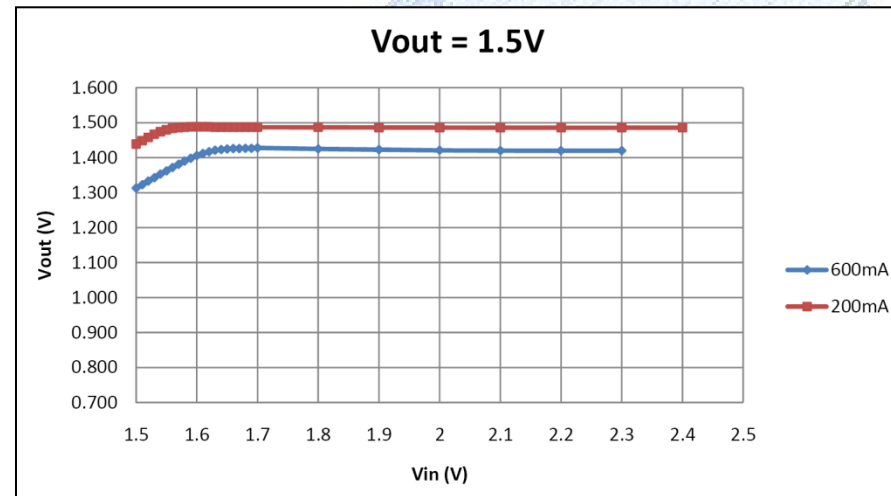
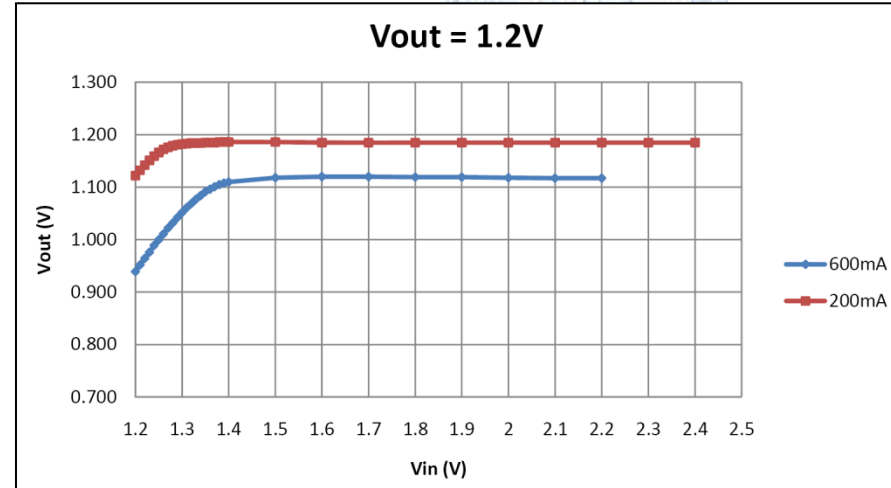
Line regulation: introduction

- Definition
 - Line regulation = $\Delta V_{out}/\Delta V_{in}$
- Specs for an LDO in FE-I4
 - Line regulation = $1/20$
- Measurement
 - Switch on the LDO
 - Set a certain Iload
 - Change the Vin (i.e. change the Vdrop)
 - The slope of $V_{out}=f(V_{in})$ gives the line regulation
 - The Vin and Vout shown in the following plots are measured with a wirebond from the chip pad to a measurement point
 - Avoid IR drop on the Vin line from the power supply to the pad
 - Avoid IR drop on the Vout line from the pad to the DVM

Line regulation

- The line regulation works fine, once regulation is reached
- At high Iload, a Vdrop of 100mV is not enough to have a regulated output
- To have a regulated Vout up to 0.6A, a Vdrop of 200mV has to be used

Iload (mA)	Vout = 1.2V	Vout = 1.5V
200	1/1000	1/400
600	1/200	1/75

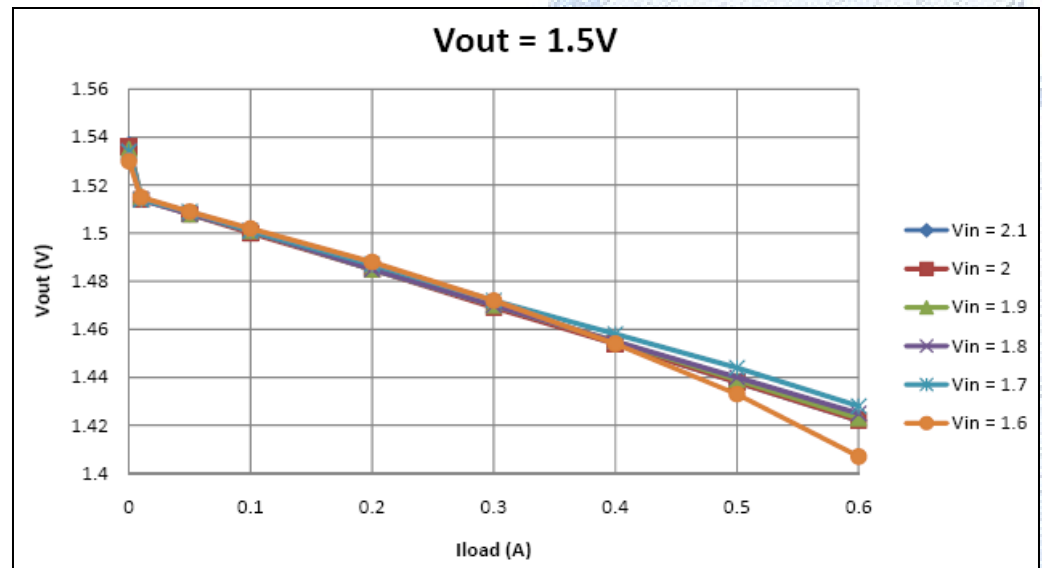
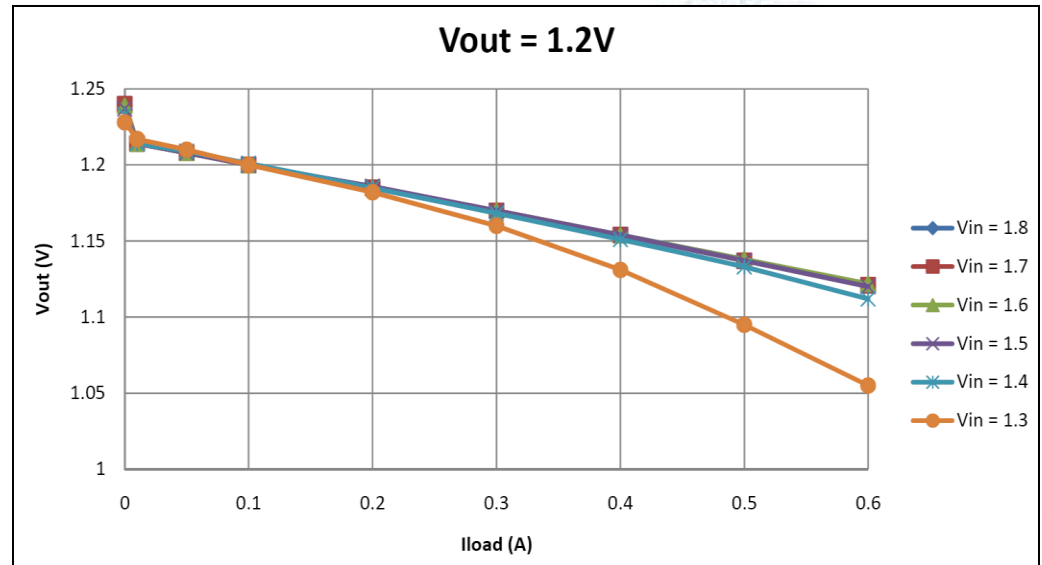


Load regulation: introduction

- Definition
 - Load regulation = $R_{out} = \Delta V_{out} / \Delta I_{load}$
- Specs for an LDO in FE-I4
 - Load regulation = $33m\Omega$
- Measurement
 - Define a certain V_{drop}
 - Increase the load from 0 to (max) 0.6A
 - Measure the V_{out} in this range of I_{load}
 - The slope of $V_{out}=f(I_{load})$ gives the load regulation
 - The measured value of R_{out} includes regulator output resistance and on chip wiring resistance

Load regulation

- For $I_{load} < 10\text{mA}$, the output stage of the amplifier A1 that controls the pass transistor is driven out of saturation which decreases the regulation loop gain. This explains the bad load regulation for $I_{load} < 10\text{mA}$.



Load regulation

- The load regulation is considerably out of specs!

Vdrop (V)	Load regulation @ Vout=1.2V (mΩ)	Load regulation @ Vout=1.5V (mΩ)
0.200	176	147
0.300	160	151
0.400	160	155
0.500	158	156
0.600	158	156

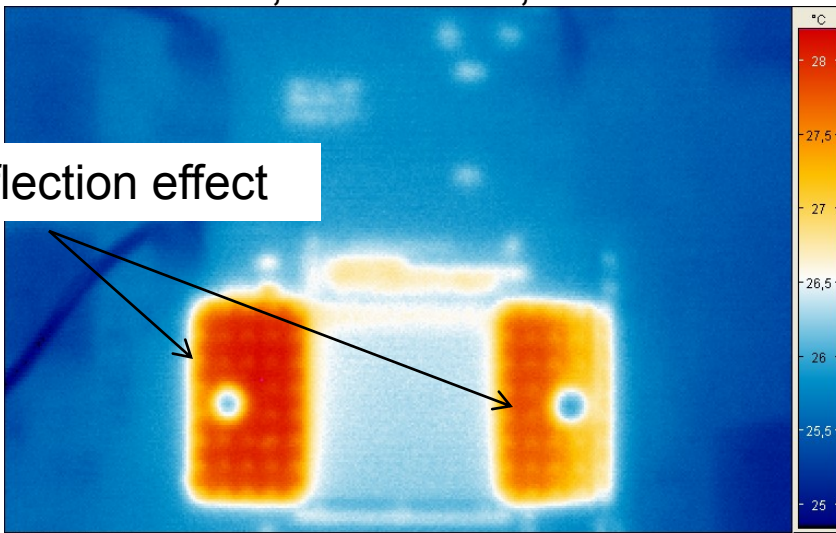
Temperature effects

- Thermo picture of the board during load regulation measurement shows only an increase of about 3°C, but the resolution is not high enough to see if the pass transistor gets warm
- At least no parasitic current paths are seen on the board

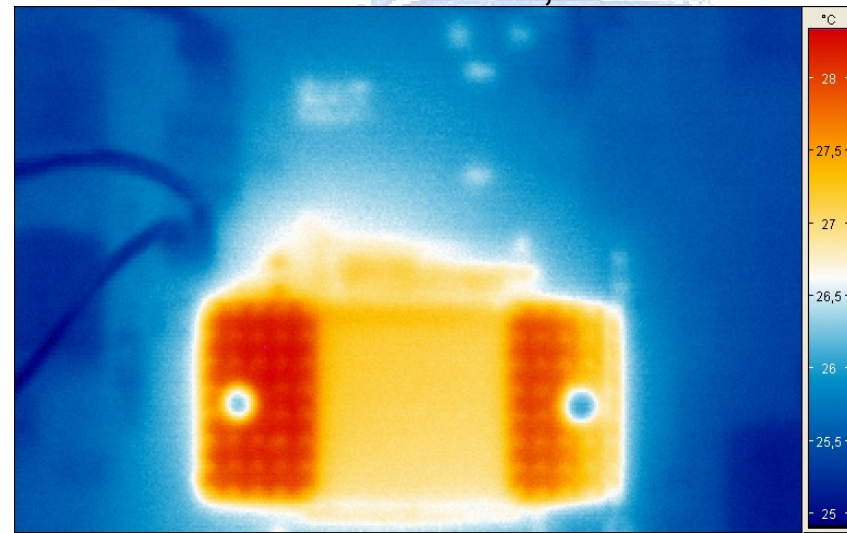
Vout = 1.2V; Vin = 1.8V; Iload = 0.05A

Vout = 1.2V Vin = 1.8V ; Iload = 0.4A

Reflection effect

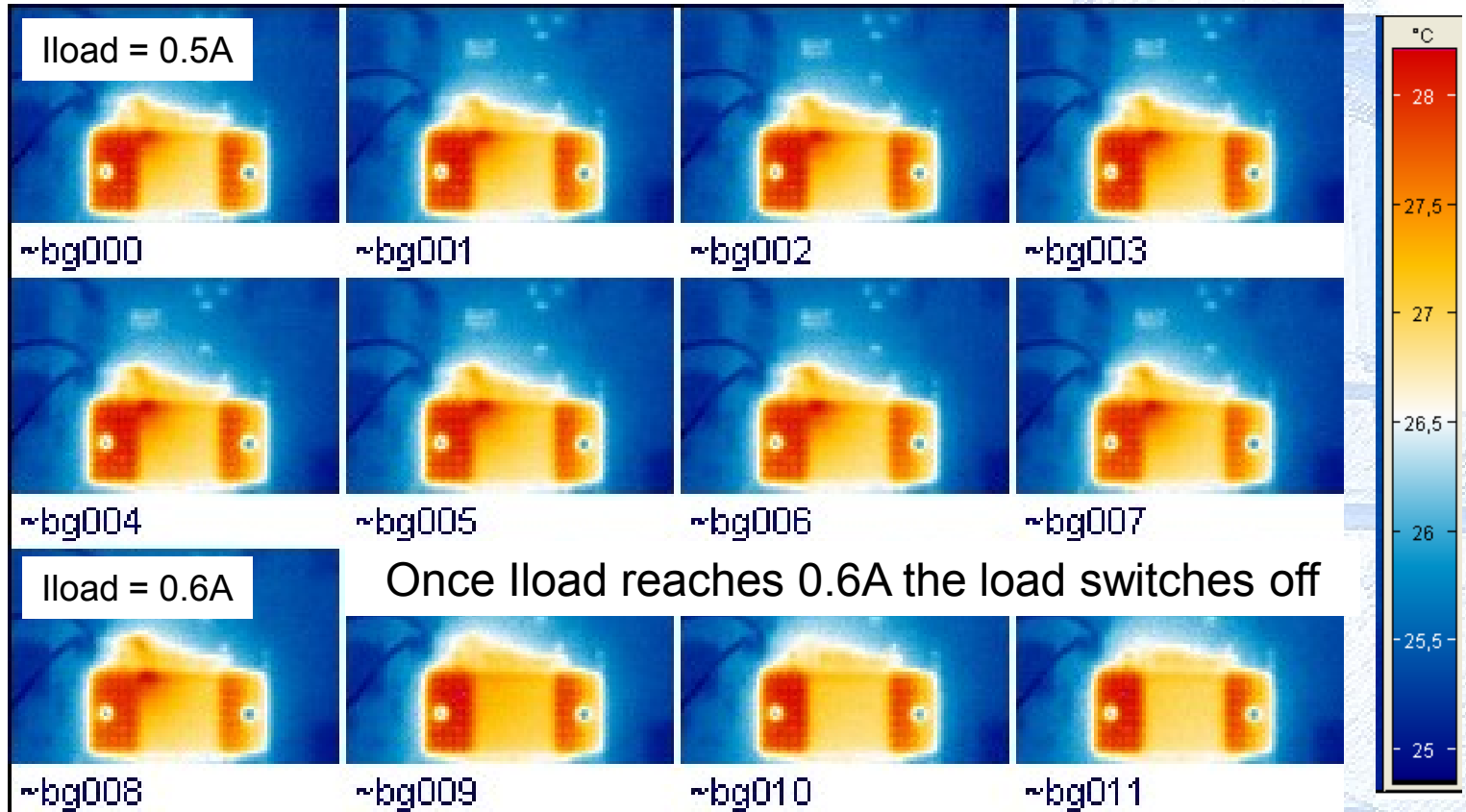


JENOPTIK L.O.S.
FEI-4 Thermobild Shunt LDO-01.ab



JENOPTIK L.O.S.
FEI-4 Thermobild Shunt LDO-02.ab

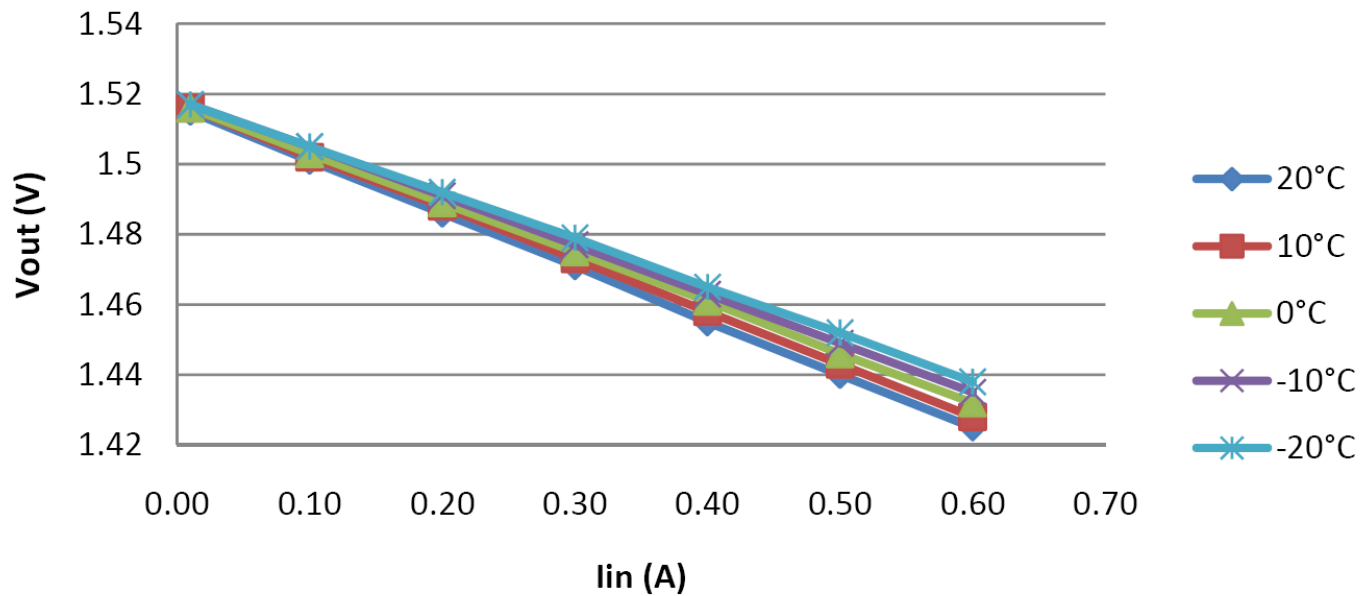
Temperature effects



Measurements in climate chamber

- Going to lower temperature does not improve the load regulation
- The load regulation is stable in a T range from +20°C to -20°C
- $R_{out} @ +20^{\circ}\text{C} = 0.153\text{Ohm}$
- $R_{out} @ -20^{\circ}\text{C} = 0.134\text{Ohm}$

$V_{drop} = 0.400\text{ V}$



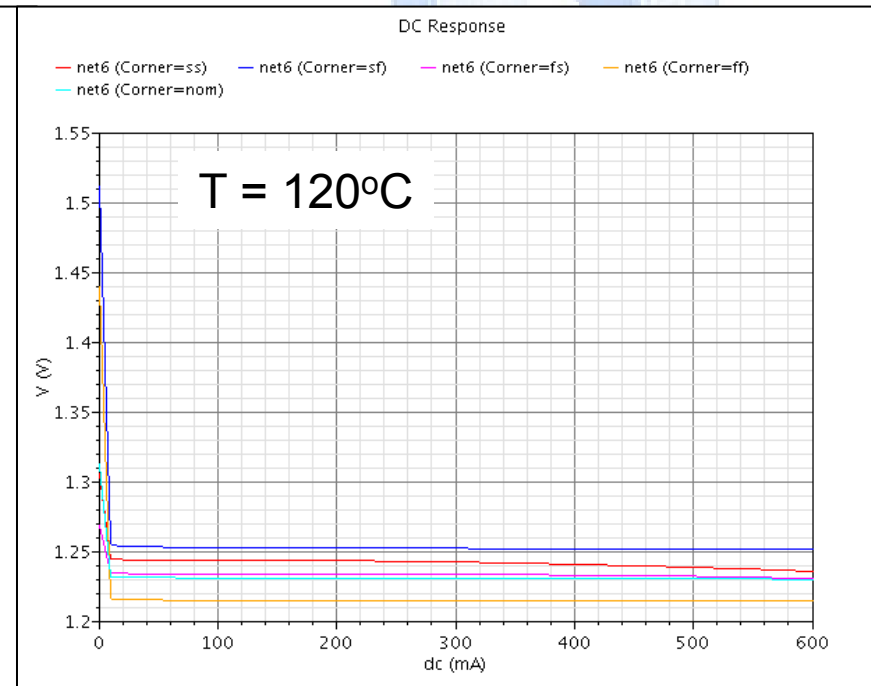
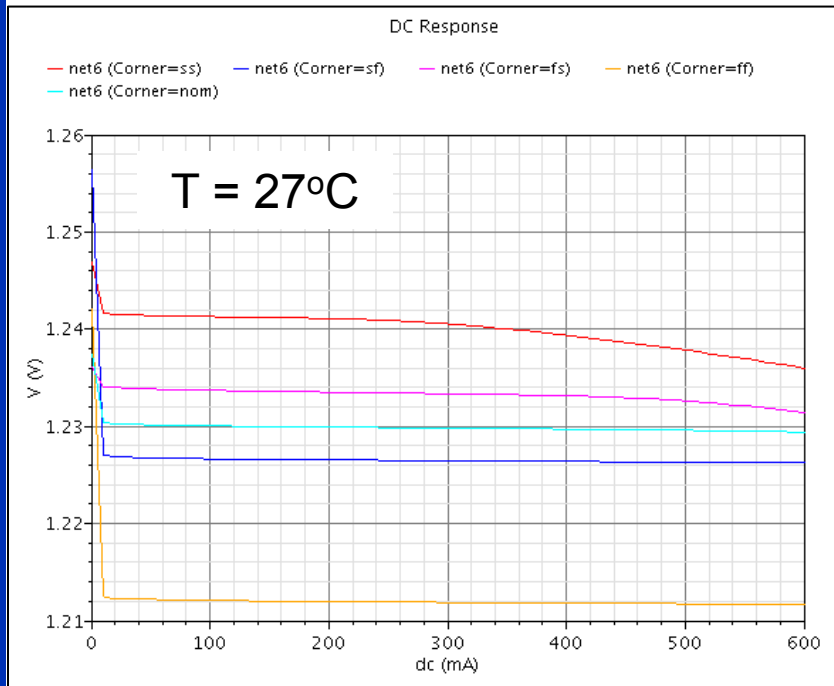
Comments on Rout value

- As far as checked, there seems to be no problem with the test setup
 - IR drop on the Vin lines has been taken into account
 - Vout is measured at the pad
 - Vref has been checked at the pad to exclude shifts
 - No parasitic current paths on the board have been observed
- Measurements were done already on regulators from 3 chips from different wafers which excludes process variation
 - The wire bonding scheme was not optimized on all chips to measure the Vin and the Vout directly at the pad, however the measurements including IR drop on the Vin and Vout line compare quite well
- The value of Rout measured could to be due to
 - the Ron of the pass transistor
 - the gain A of the error amplifier
 - the on-chip wiring resistance

Simulation

- Corners at different T
- Only the load regulation for low load current is affected
- To do: post layout simulation with parasitic extraction

$V_{in} = 1.6V$, $V_{out} = 1.2V$



Regulator safety: overvoltage

- The Shunt-LDO regulator is designed to withstand a V_{in} of maximum 2.5V
- V_{in} higher than 2.5V can harm the regulator, and possibly even destroy it
- This could be an issue for the regulator with $V_{out} = 1.5V$, i.e. the one generating the VDDA
 - In this case a V_{in} of about 1.7V is needed at the input of the regulator. The V_{drop} on the cables (flex + 6m type1) can be as high as 1V (roundtrip) at maximum load (0.6A). In the worst case assumption that a zero voltage drop on the cables occurs, the regulator will see 2.7V at the input
- A VDDA of 1.3V is recommended for safe operation

