Work Package 8:

SEU cross-section calculation using 2D TCAD modeling

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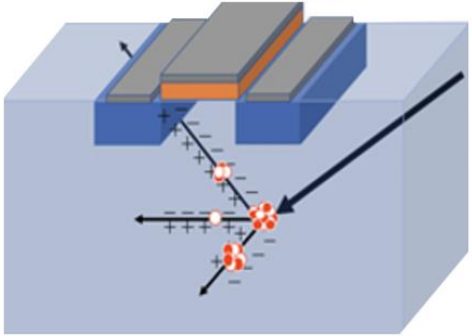
Introduction

The radiation-induced failures known as Single-Event Effects (SEE) is a major reliability issue for electronics system.

Simulation analysis is crucial step **to optimize circuit design in the early stages** before the irradiation test, and **to support the understanding of post-irradiation data.**



At device level, SEEs are extensively simulated by using **TCAD** tools.

High complexity for the end-user due to the deep understanding that it requires of device structure and physics.

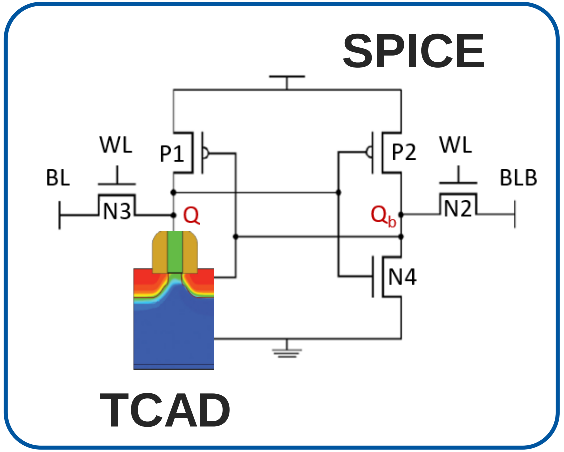
At circuit level, **SPICE** offers a simpler and quicker simulation method, well-suited for evaluating the overall behavior of basic or complex circuits.

SPICE does not appropriately consider the material composition and particle-matter interactions.

Introduction

TCAD + SPICE simulations are frequently integrated through a mixed-modeling.

This hybrid approach streamlines the simulation process by modeling **only the critical parts of the circuit using TCAD**, while the other part of the circuit is represented at a higher level of abstraction in SPICE.



TCAD and SPICE modeling critically depend on the technology's Process Design Kit (PDK) for accurate simulations.

However, obtaining the PDK parameters by manufacturers is generally not straightforward.

Introduction

In this context, we proposes a methodology to estimate the SEU cross-section dealing with the disadvantages related to the lack of technological information and the complexity of the TCAD simulations.

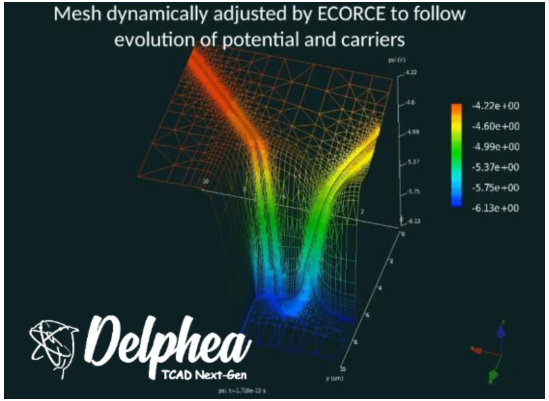
The three main objective of our approach are:

- To provide **comprehensive method** to estimate SEU cross-section by **using only basic technological information** available in the literature.
- To elaborate on **the parameters that significantly influence** 2D TCAD modeling.
- To discuss **strategies for estimating unknown parameters** due to limited technological data.

2D TCAD modeling

Although the SEE cross-section involves 3D effects, 2D modeling can be effectively used to simplify the simulation complexity and save calculation time.

In this work, we apply mixed-modeling using the **ECORCE** TCAD tool.

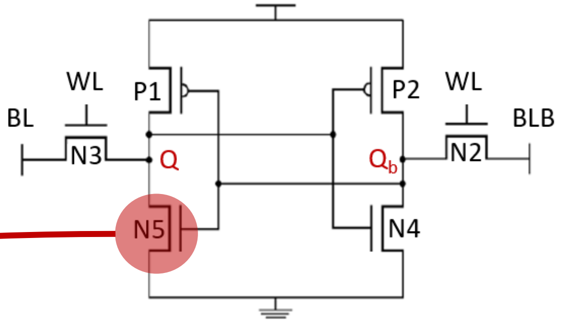


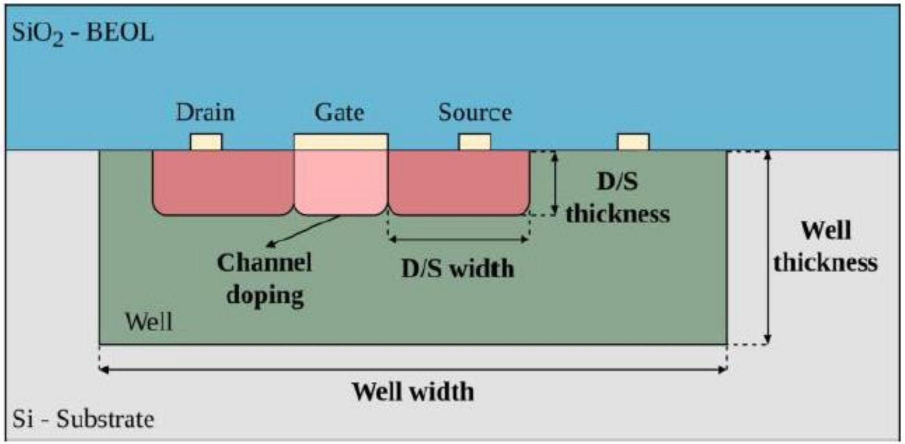
- *Graphical User Interface (GUI) for all simulation steps;*
- *Dynamically adjusts the mesh at each step of the simulation;*
- *The ion tracks are precisely described and simulated whatever its impact point in the device;*

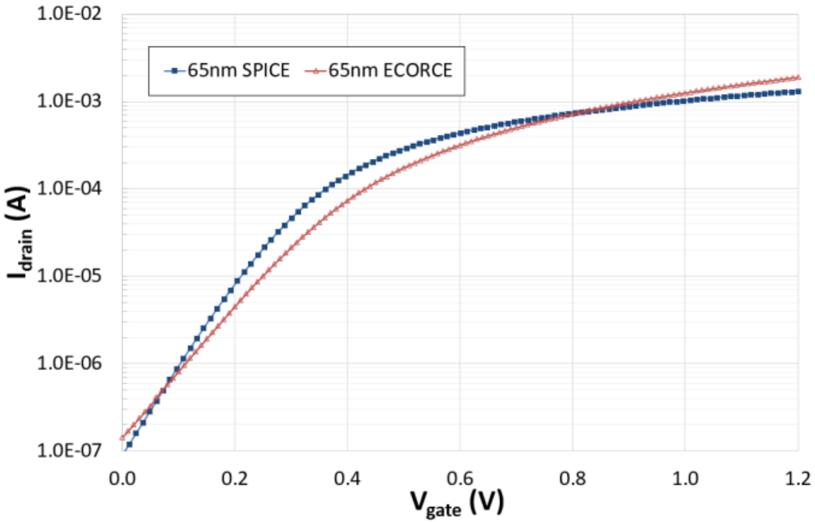
For the SPICE modeling, we used the open-access **Predictive Technology Model** (**PTM**). This model is developed at Berkeley University using the BSIM4 as a basis.

2D TCAD modeling

The standard 6T SRAM cell was the DUT for heavy-ion irradiation in 65nm and 45nm planar-bulk CMOS technology.

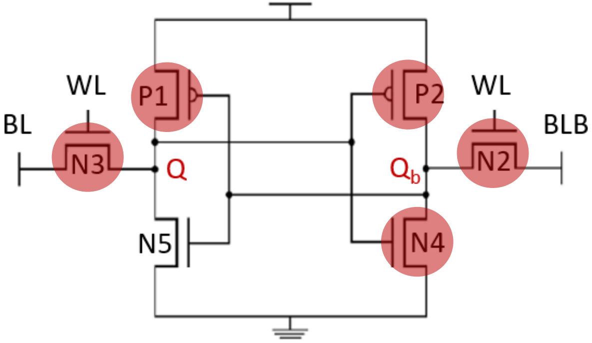






2D TCAD modeling

The SPICE model will be used to simulate the remaining 5 transistors of the 6T cells.

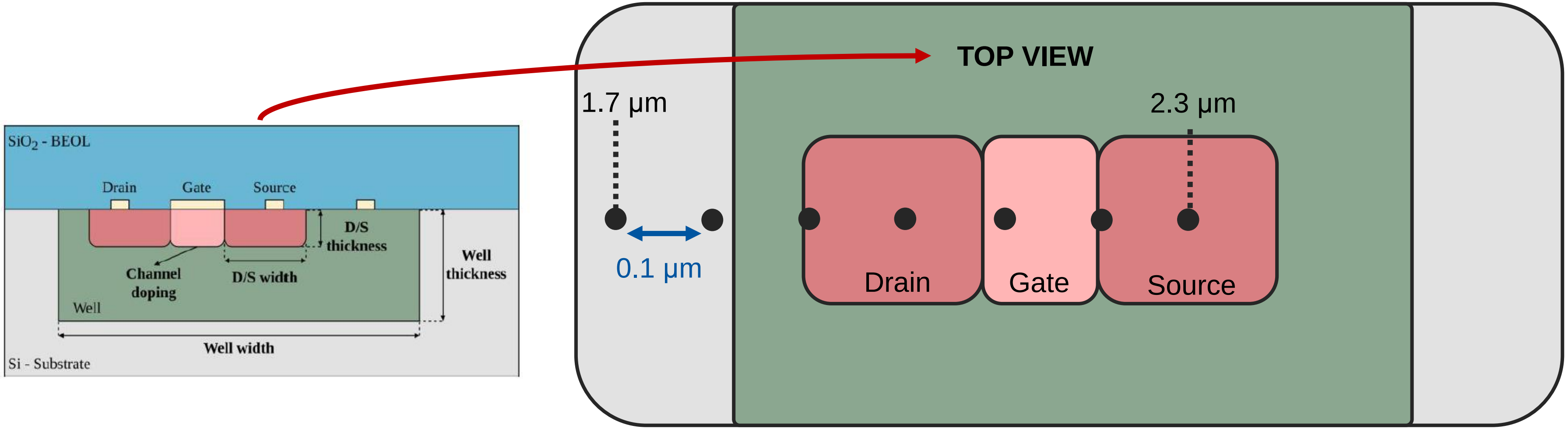


The size of the transistors are defined by :

- *Minimum W/L = 2.0*
- *Cell ratio = 1.5*
- *Pull-up ratio = 1.0*

These size and ratios represent a standard choice that allows to reach a good trade off among minimizing the cell area and access time, achieving good level of static and dynamic noise margin

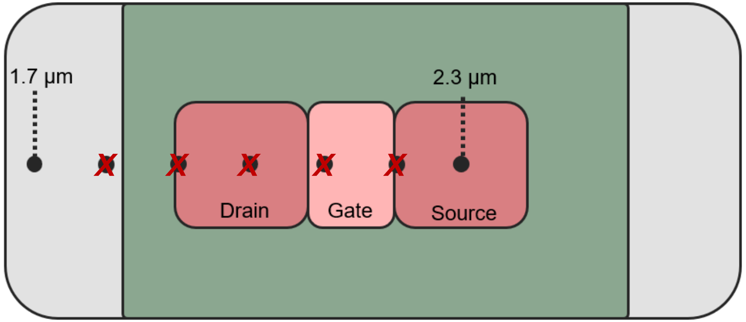
SEU cross-section calculation



In our methodology, we focus on simplified ion injections along the x-axis, maintaining a precise 0.1 µm spacing between each injection.

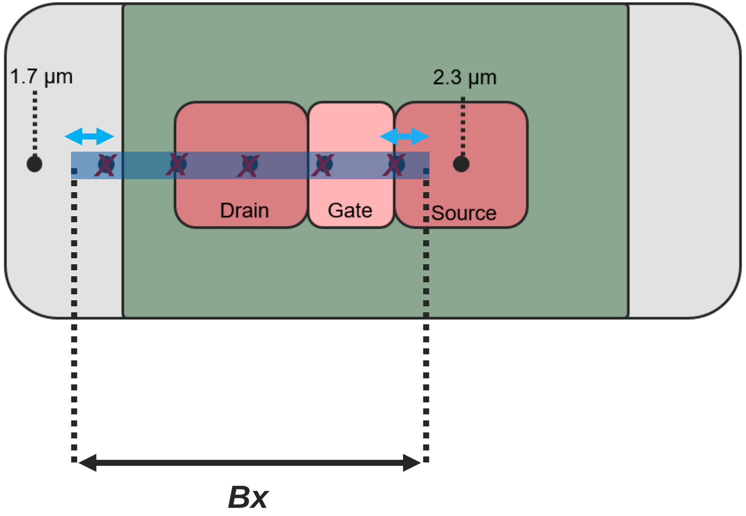
SEU cross-section calculation

- Check SEU occurrence.
    - *X = cell upset*



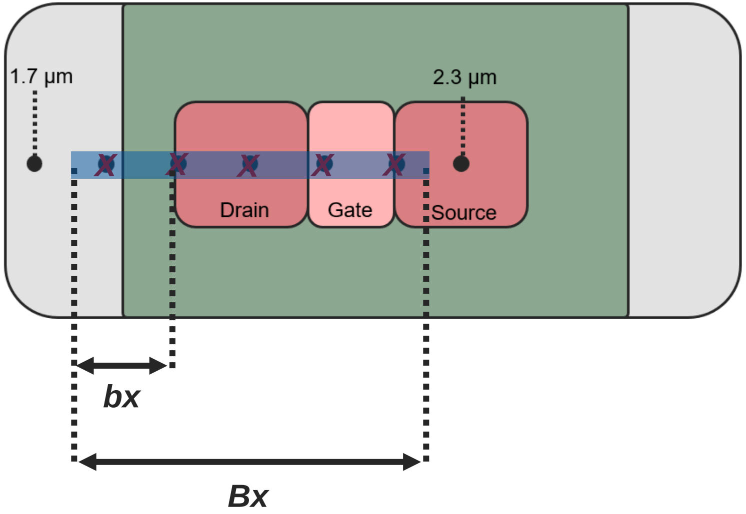
SEU cross-section calculation

- Check SEU occurrence.
  - *X = cell upset*
- The sensitivity across the x-axis ***(Bx).***
  - *Error Margin of 0.05 µm*



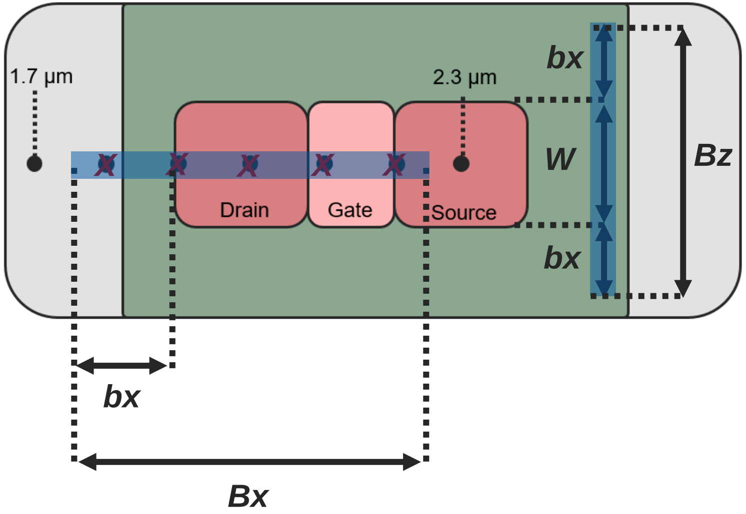
SEU cross-section calculation

- Check SEU occurrence.
  - *X = cell upset*
- The sensitivity across the x-axis ***(Bx).***
  - *Error Margin of 0.05 µm*
- The sensitive region up to the drain ***(bx).***



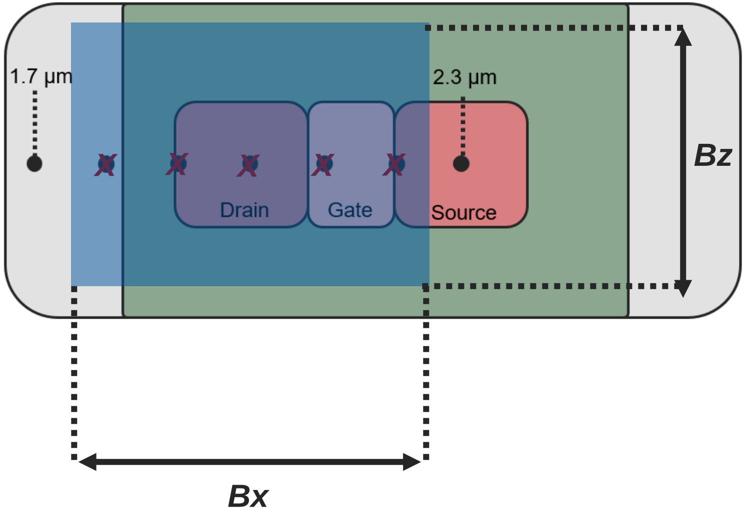
SEU cross-section calculation

- Check SEU occurrence.
    - *X = cell upset*
- The sensitivity across the x-axis ***(Bx).***
    - *Error Margin of 0.05 µm*
- The sensitive region up to the drain ***(bx).***
- Adding ***W*** + 2 times the value of ***bx***, we obtain the sensitive region along the z-axis ***(Bz).***

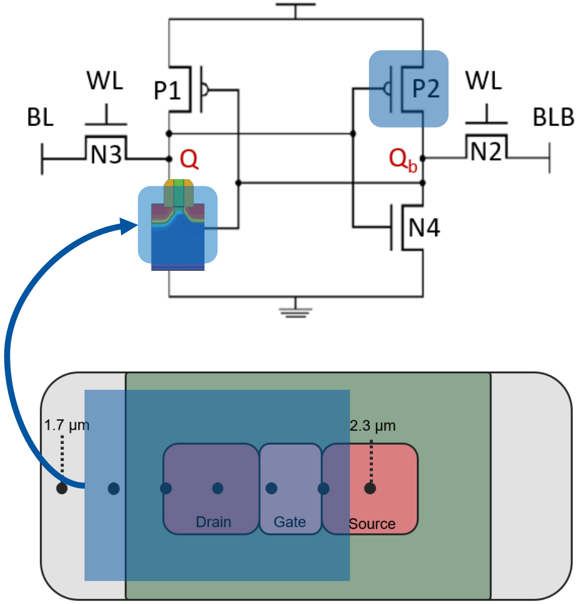


SEU cross-section calculation

- Check SEU occurrence.
  - *X = cell upset*
- The sensitivity across the x-axis ***(Bx).***
  - *Error Margin of 0.05 µm*
- The sensitive region up to the drain ***(bx).***
- Adding ***D/S Width*** + 2 times the value of ***bx***, we obtain the sensitive region along the z-axis ***(Bz).***
- Multiplying ***Bx*** by ***Bz***, we obtain the SEU cross-section related to the NMOS transistor.



SEU cross-section calculation



In an SRAM cell, the bit storage relies on a pair of inverters in feedback loop.

One NMOS transistor and one PMOS in OFF-state at the same time.

To include the PMOS transistor, without the need for a new simulation, we can consider the cell ratio between the transistors.

Given the chosen **cell ratio of 1.5**, we can multiply the calculated SEU cross-section by 1.5 and obtain the total SEU cross-section of the cell.

Results

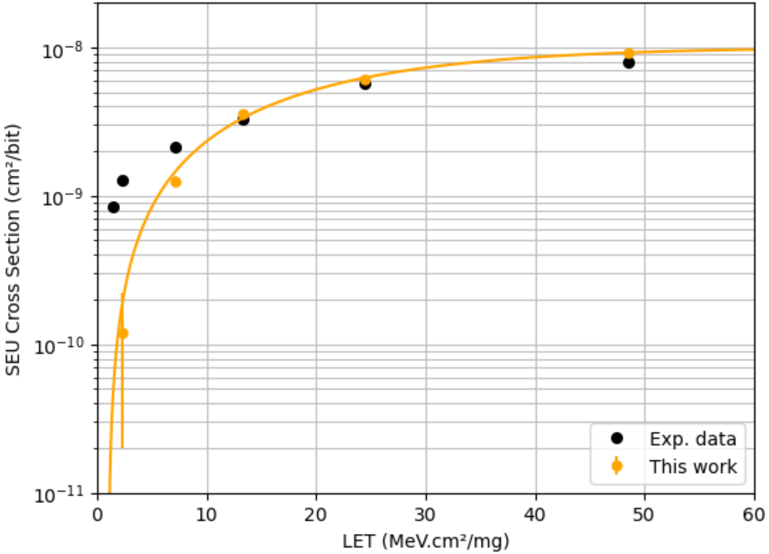
We investigated six different ions, drawing data from the **RADiation Effects Facility (RADEF) heavy-ions 16.3 MeV/u database** to ensure a broad spectrum will be covered.

Based on the simulation results for each ion a Weibull curve is generated. The error margin is $1\text{x}10^{10}$ cm^2/bit.

The SEU cross-section simulation for heavy-ion is compared with **experimental data** obtained from literature.

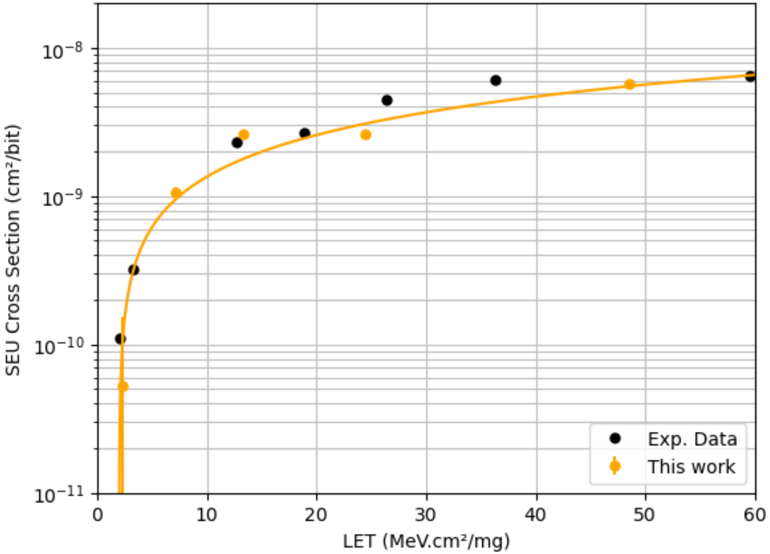
Results

Heavy-ions SEU cross-section for **65nm** SRAM. The experimental results are taken from [1].



[1] J. Wang, et al, "Study of SEU Sensitivity of SRAM-Based Radiation Monitors in 65-nm CMOS," in IEEE Trans. Nucl. Sci., vol. 68, no. 5, pp. 913-920, May 2021

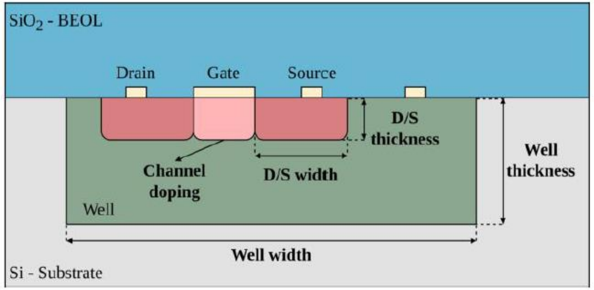
Heavy-ion SEU cross-section for **45nm** SRAM. The experimental data are taken from [2].

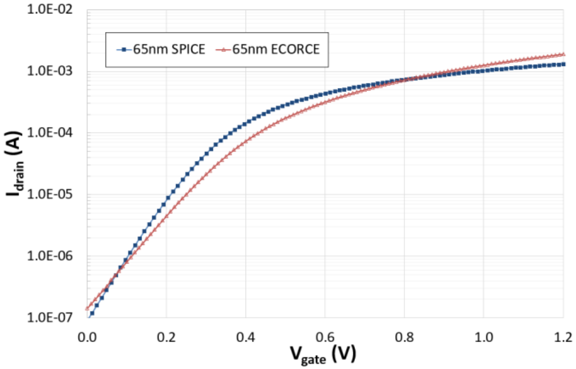


[2] C. Weulersse, et al, "Prediction of proton cross sections for SEU in SRAMs and SDRAMs using the METIS engineer tool," Microelectron. Rel., vol. 55, nos. 9–10, pp. 1491–1495, Aug. 2015.

Results

We pinpoint five parameters not obtained by SPICE models, which are crucial to our analysis:





Well thickness	Variations ranging from 0.25 µm to 2.0 µm have shown negligible effects.	Fixed at 0.5 µm
Well width	It's critical to ensure that the simulation's mesh granularity is sufficiently high, especially around the D/S regions, to prevent inaccuracies.	50 nm between the well and D/S areas to safeguard the simulation.
D/S thickness	It directly influences leakage current. Optimal control of this current requires that the thickness be equal to or less than the channel width.	40 nm for a 65 nm channel and 30 nm for a 45 nm channel .
Channel doping	Vital for optimizing transistor performance since it affects leakage current, threshold voltage, and saturation current.	Value based on SPICE benchmarks.
Substrate doping	Altering this value to 1x10^{17} increases the leakage current, impact in the LET threshold and reducing charge collection.	Fixed at 6x10^{16} cm^3

Conclusion

The **results are impressively accurate**, when considering the **simplifications made at circuit and device level**. At this point, any kind of fitting is made to reach a better SEU cross-section result.

[65 nm] = **29 injections per ion**, providing **results for an entire range of LETs in ~15 hours**.

We focuses on identifying key parameters with a significant impact on simulation outcomes, enabling users to **prioritize these critical parameters over others with minimal influence**.

Improvements can be obtained by reducing the **ion injection step**, using **more accurate SPICE models**, and fitting of the critical input parameters.

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Thank you all for the attention

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