WP6: The development of system-level observation techniques through the SEE Tester case study

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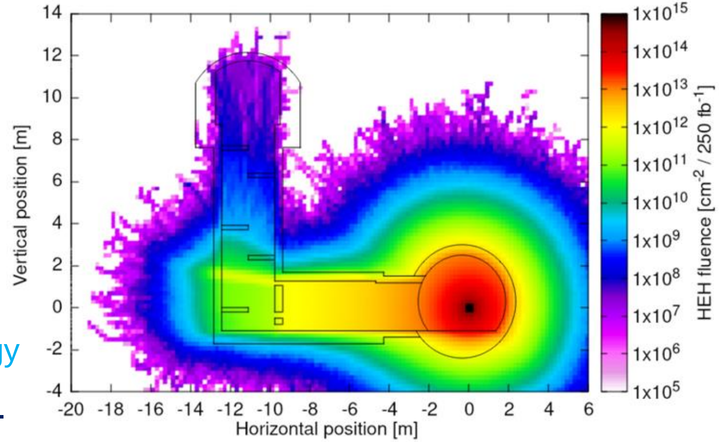
Electronics at the CERN accelerator complex

CERN accelerator complex consists of multiple distributed electronic systems with different levels of exposure to the radiation fields present in the proximity to the accelerator. The radiation field consists of multiple particle species with broad energy spectra, and is commonly the result of:

- **beam interactions with the residual gas in the beam pipe**
- **beam interactions with the elements of the accelerator (collimators, dumps, beam instrumentation)**
- **particle collisions for physics research.**

Radiation effects in electronics are most frequently induced by high-energy hadrons (protons, neutrons, pions, kaons), photons and thermal neutrons.

Current requirements for the systems' reliability are driven by the **High-Luminosity LHC** project (5x improvement of failure rate per unit luminosity compared to the operation in 2017).



Example simulation of the cumulative High-Energy Hadron fluence in the LHC tunnel during one year of High-Luminosity operation [1]

System-level testing of new electronics at CERN

System-level testing is a necessary part of the **R**adiation **H**ardness **A**ssurance (RHA) procedure for new designs of radiation-tolerant systems at CERN.

During system-level testing, many aspects of SEE sensitivities of individual components are not accounted for (specific device configuration, ELDRS, mechanical obstructions etc.), therefore only in combination with component-level test data a complete evaluation of system performance in the radiation field is possible.

However, a thoroughly designed test will give a good evaluation of system operation in the destination environment. Moreover, system observations will give insight into the performance of system components and can be helpful to investigate the root causes of system-level failures.

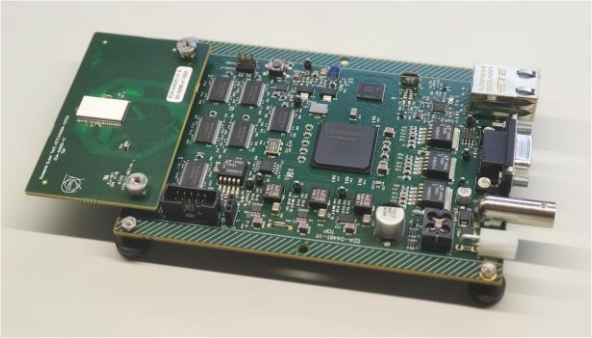
SEE Tester v2 is a case study for the development of **system-level observation techniques**.
It is a universal platform for component-level testing of digital and analog ICs at the CHARM facility at CERN, which consists of:

Motherboard

- Based on Microchip SmartFusion2 (M2S010T-1FGG484)
- RS-485, Ethernet interfaces to the host PC
- 4 Gbit DDR3 SDRAM for event storage
- Vcc-isolated digital I/O to the DUT

Daughterboard

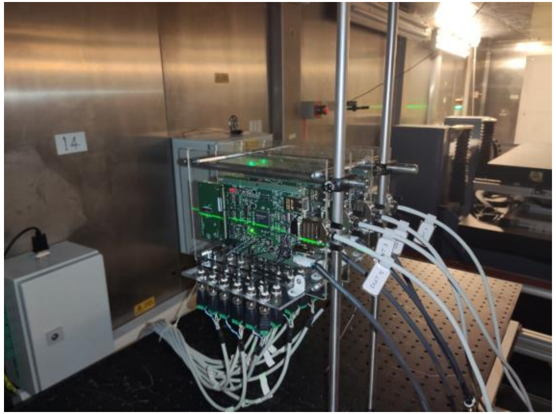
- Customizable board for the tested IC
- Powered from the motherboard or externally
- Attached directly to the motherboard or through the extension cable



SEE Tester v2 with the attached daughterboard

Analysis of the SUT current consumption

The possibility of SUT total current observation for system-level failure analysis was investigated during the test campaign performed at the **ChipIr** facility (Rutherford Appleton Laboratory, Didcot, UK) in February 2023. Four SEU Tester v2 SUTs were irradiated in the atmospheric neutron field up to the total high-energy neutron fluence (> 10 MeV) of $1 \cdot 10^{12}\ cm^{-2}$.



The stack of 4 SUTs installed in the irradiation room

Two types of observations were performed during the test:

1. Software observations using the default communication link
2. Periodic sampling (T=1s) of the SUT total current consumption

Main findings:

- The total current consumption can be used as immediate feedback about proper SUT operation during the test. However, all normal current consumptions in different modes of operation should be known in advance.
- The observation of total current consumption can reveal malfunctions in system operation, that are transparent for the other observation techniques (e.g., digital communication with the SUT).

The timeline of the total current consumption evolution of one of the SUTs

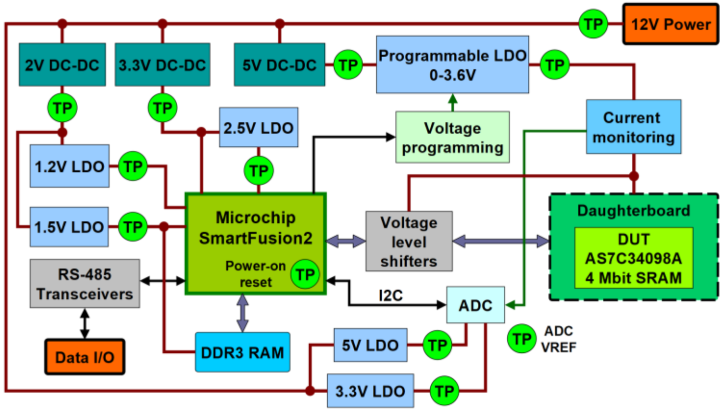
SUT voltage monitoring

Certain voltages of the SUT should remain stable during its normal operation. Any transient or permanent deviation from their nominal value may result in system failures.

The explored set of hardware observations is based on periodic sampling of certain SUT voltages, including:

- Power supply system
- Power-on reset circuit
- ADC reference voltage

The test campaign at the **CHARM** facility (CERN) was performed in April 2024. Two SEE Tester v2 SUTs were irradiated in the mixed radiation field (mainly protons, neutrons, gamma rays) up to the total fluence of $2{,}9 \cdot 10^{11}\ cm^{-2}$, and TID of ~150 Gy.



The block diagram of SEE Tester v2 with the locations of the monitored voltages

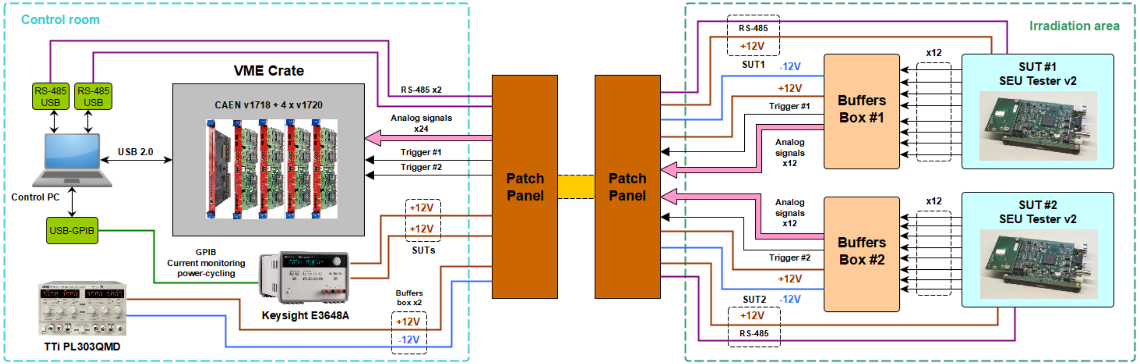
Three types of observations were performed during the test:

- Software observations using the default communication link
- Periodic sampling (T=20s) of voltages in the SUT
- Fast sampling (T=20ns) of the same voltages with Single-Event Transient detection

Test campaign at CHARM – discussion

Fast voltage acquisition was implemented with a combination of VME modular electronics (CAEN v1718 and v1720) and a custom, radiation-tolerant analog voltage buffering device (Buffers Box).

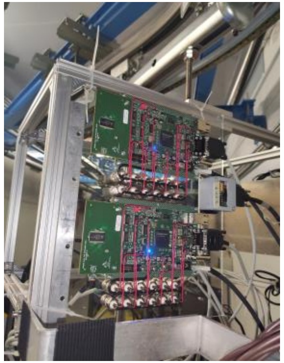
Each of the monitored voltages was compared with two thresholds, at around 120% and 80% of the nominal value.



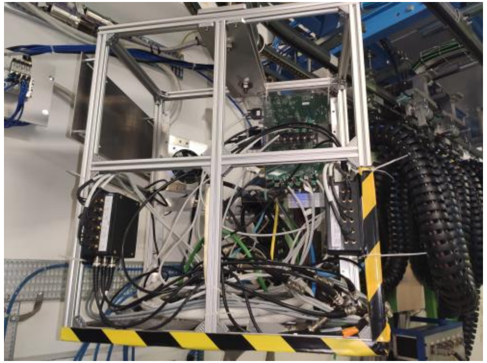
Main findings:

- Performed hardware observations allowed to determine the causes of unrecoverable failures of both SUTs, that limited their operation time (TID-induced failures of LDO regulators)
- Certain system-level failures were correlated with the SETs in the power supply system – performed observations helped to determine the sensitive components
- Around 95% of the recorded SETs in the SoC power supply lines caused system-level failures
- The contribution of the power supply system to the total system-level failure cross-section was determined

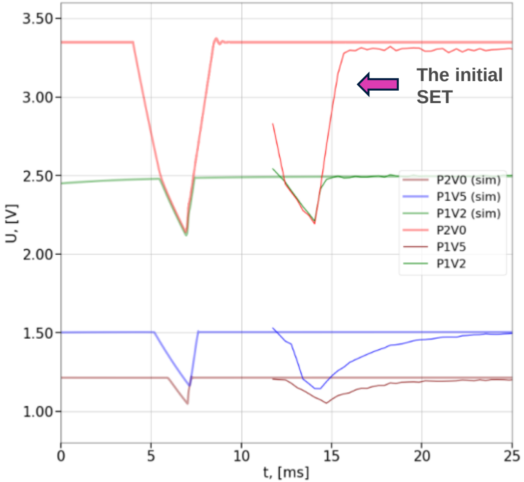
Two SUTs installed at the facility

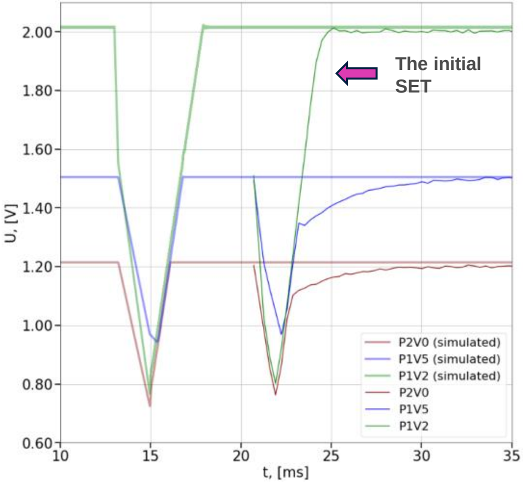


Complete installation with the buffering devices



Hardware observations of the SUTs at CHARM

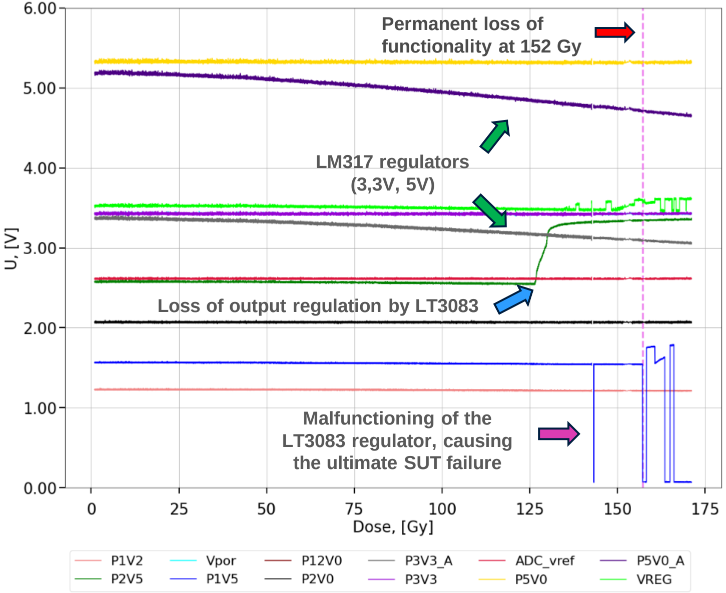




Transients were observed in the outputs of 3.3 V (left) and 2.5 V regulators (right). Originating from two switching regulators, they were causing a cascade of SET on other power supply lines.

Most of the SETs were correlated with system-level failures, observed through the default digital communication link. The same transients were recreated through the Spice simulations of the power delivery circuit of the SEE Tester.

The evolution of SUT1 voltages during system-level irradiation



Both SUTs suffered from the permanent loss of functionality cause by the degradation of one of the linear regulators (1.5V).

Conclusions

The possibilities to improve the observability of the electronics during system-level testing were explored in two test campaigns.

- Both total current and SUT voltage monitoring facilitate the analysis of the performance the SUT based on the collected data (failure criticality classification, calculation of failure cross-sections)
- Total current monitoring may be used during system-level test execution for the real-time diagnostics of the SUT state. The SUT will be brought back to normal operation by reconfiguration or power-cycling immediately after the loss of normal operation, even if it is transparent to the rest of the observations. Overall, this increases the effective system-level testing time.
- The observation of SUT voltages gives insight into the TID degradation of particular ICs, which might result in an unrecoverable SUT failure, which was the case for the studied system.
- Monitoring of sensitive voltages, such as power supply lines, helps to determine system elements that contribute to system failure rates, thus limiting its availability. The radiation tolerance of a system can be improved by replacing such components or by the implementation of mitigation techniques.

Thank you for your attention

Literature

[1] G. Lerner, R García Alía, K. Biłko, M. Sabaté Gilarte, F. Cerutti and Y. Kadi, Radiation level specifications for HL-LHC, CERN LHC-N-ES-0001, EDMS no. 2302154, 10 December 2019