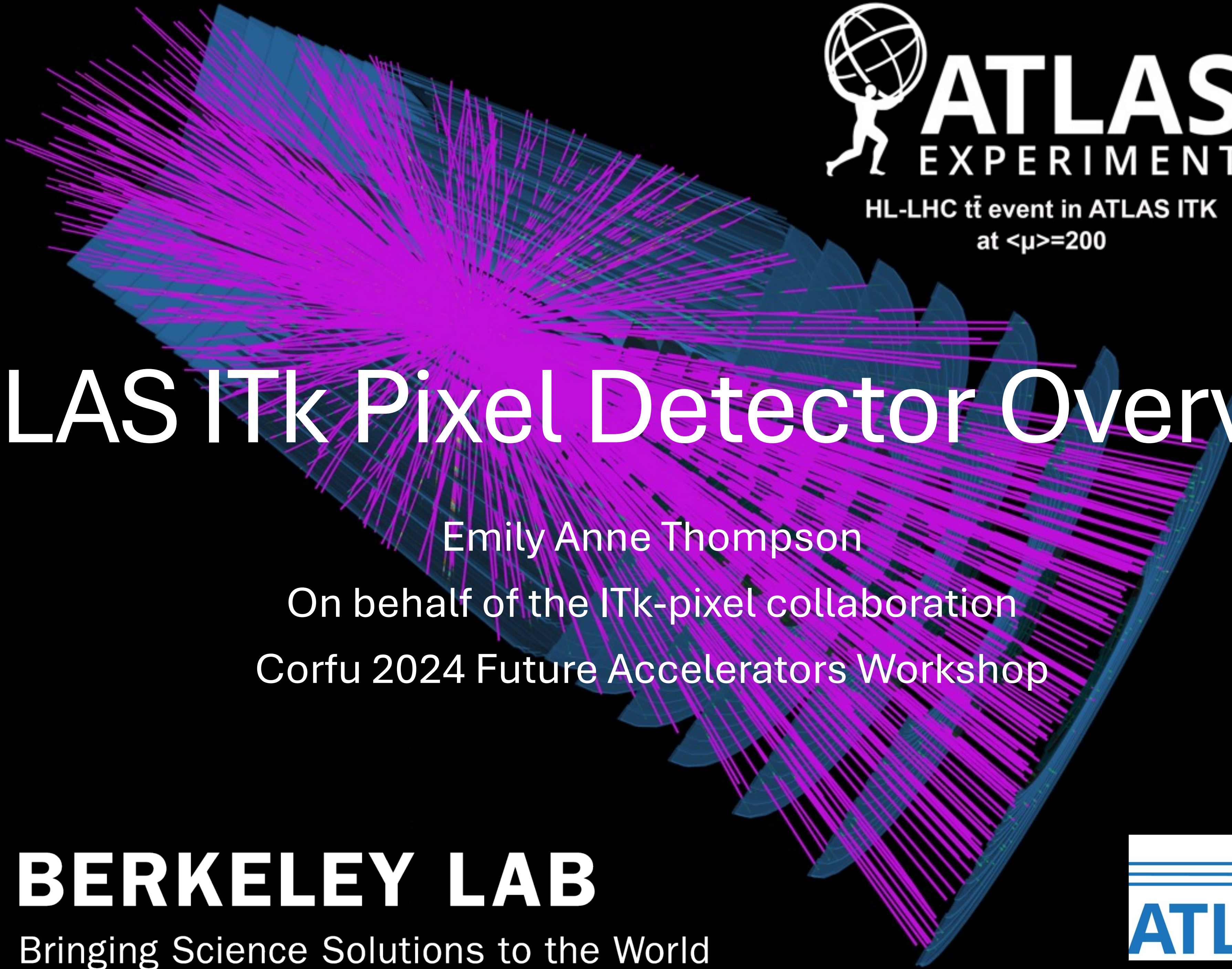
ATLAS EXPERIMENT



HL-LHC $t\bar{t}$ event in ATLAS ITK at $\langle\mu\rangle=200$

# ATLAS ITk Pixel Detector Overview

Emily Anne Thompson

On behalf of the ITk-pixel collaboration

Corfu 2024 Future Accelerators Workshop

BERKELEY LAB

Bringing Science Solutions to the World

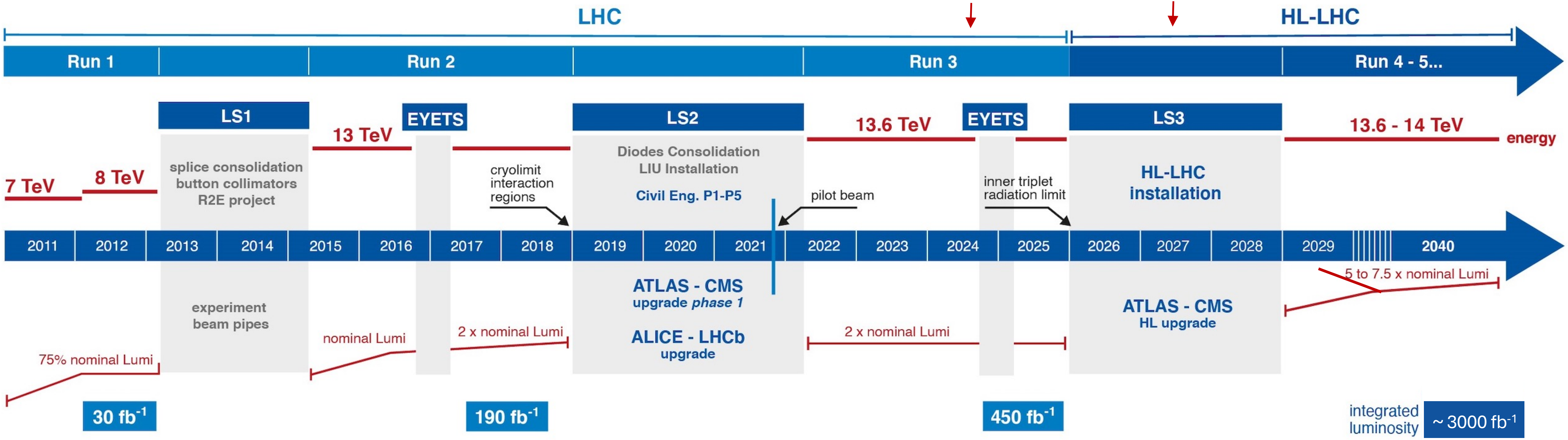
ATLAS ITk

# High-Luminosity LHC

The HL-LHC will significantly increase the luminosity of the LHC beyond its nominal value

- Projected to collect **~ 2500 fb$^{-1}$ of data in 10 years**
- Average of **200 proton-proton interactions** / bunch crossing

More data will allow us to perform more precise tests of the SM (Higgs couplings), observe more rare SM processes, and search for new physics



We are here

Upgrade of LHC
and detectors

Start of HL-LHC
in 2029!

lhc-commissioning.web.cern.ch

# ATLAS ITk overview

The HL-LHC will provide a challenging environment for charged particle tracking

- Much higher particle density and radiation damage compared to Run-3 conditions
- Increased trigger rate (100 kHz → 1 MHz)

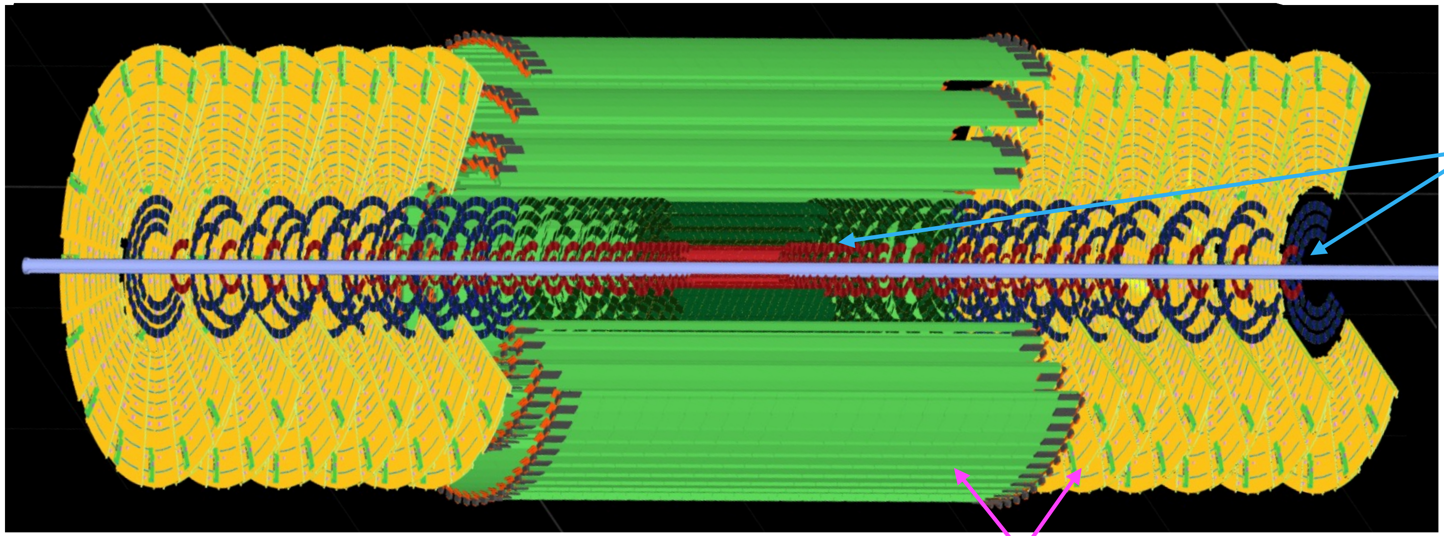
A **new, all-silicon tracking detector (ITk)** designed to meet these challenges will replace the current inner detector

✓ higher granularity (keep occupancy < 0.1%)

✓ higher radiation hardness – up to 2 x $10^{16}$ $n_{eq}/cm^2$

✓ *reduced material budget*

✓ Extended tracking coverage: $|\eta| = 2.5 \rightarrow 4$



itk-viewer.web.cern.ch

ITk pixel detector

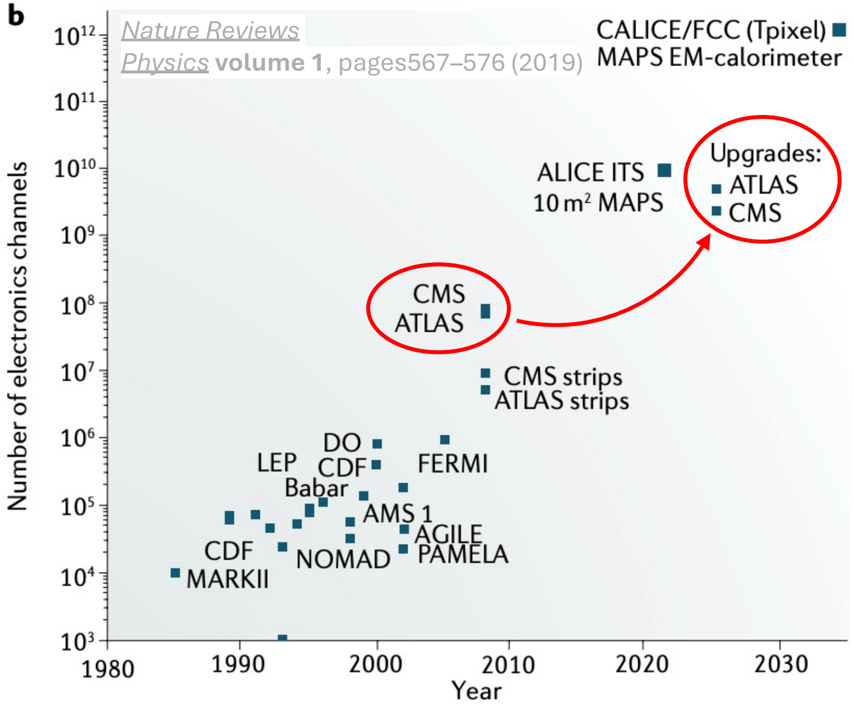
(this talk)

ITk strip detector

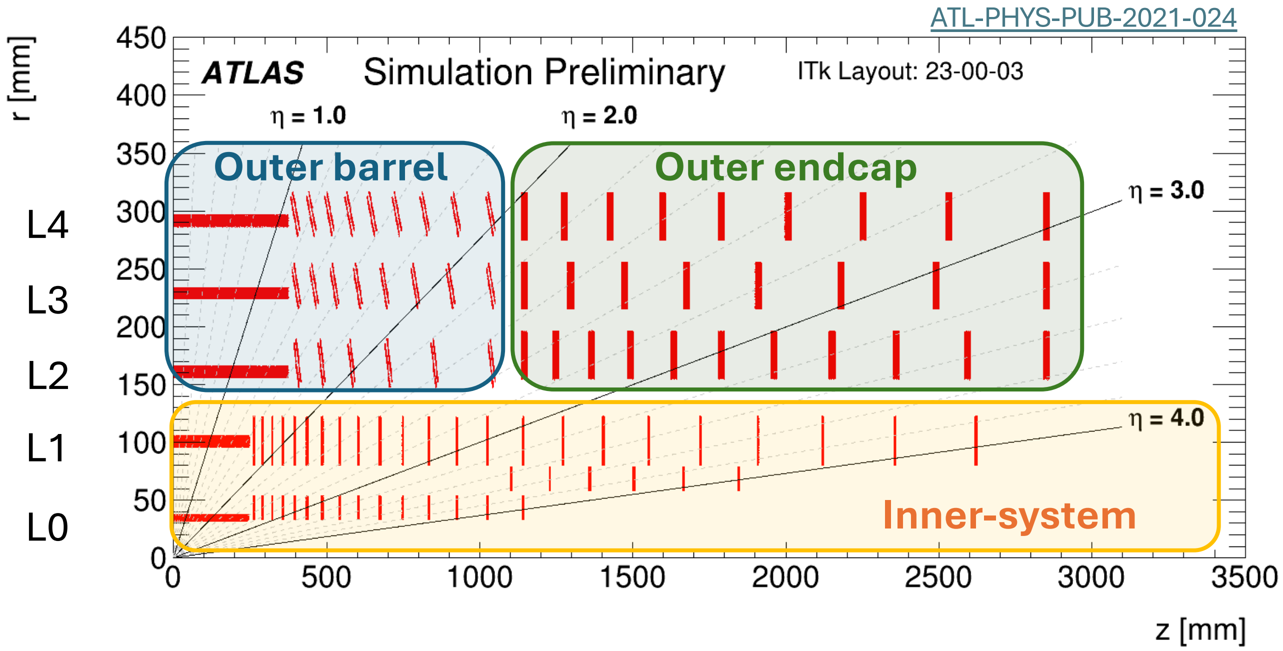
(S. Ordek’s talk)

# ATLAS ITk pixel overview

The ITk pixel detector will consist of 5 silicon tracking layers split into 3 regions



| Pixel detector | Current | ITk | |
|---|---|---|---|
| Number of modules | 1744 | 9164 | → 5x |
| Active area $[m^2]$ | 1.6 | 13 | → 8x |
| Channels | 92M | 5083M | → 55x |



How to design layout of new tracking detector?
Need to balance **tracking performance** (hermeticity, reduce material) with **detector buildability** (cost, ease of construction)

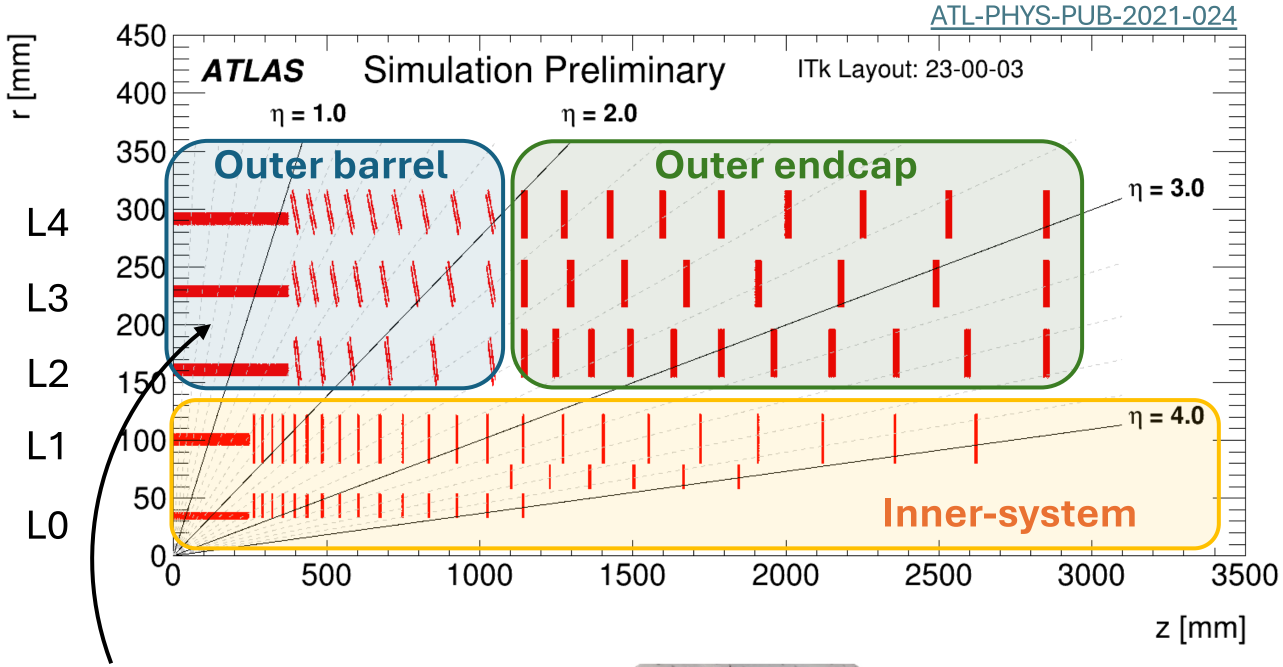
# ATLAS ITk pixel overview

The ITk pixel detector will consist of 5 silicon tracking layers split into 3 regions

Layout design choices:

Inclined layout: Keep sensors ⊥ to direction of tracks → less material interaction, but more complex to build

- Active elements on rings tilted: 55°-67° with respect to beam axis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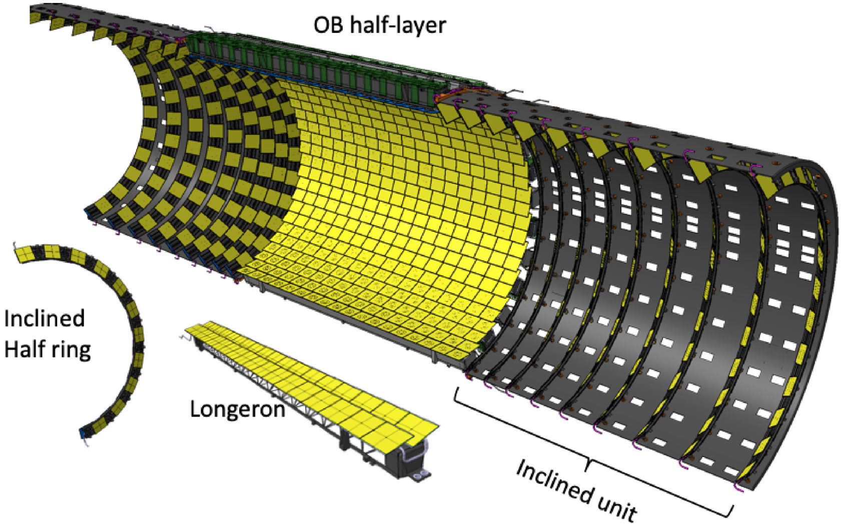
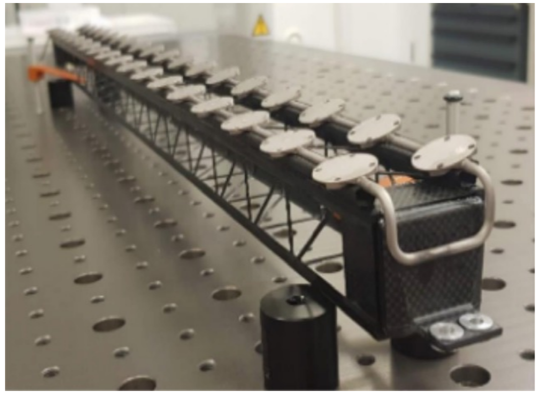
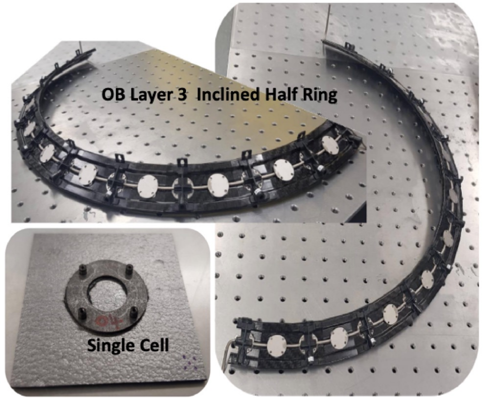






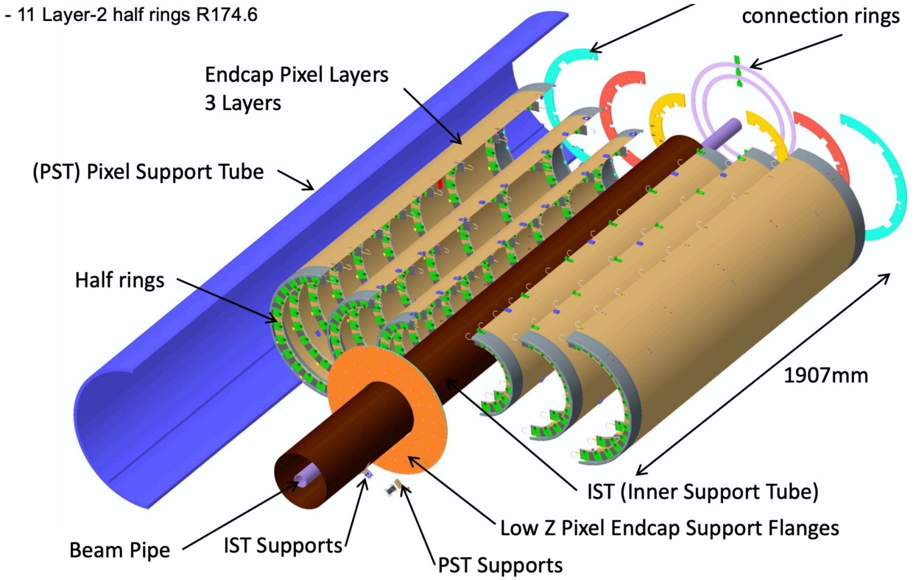
# ATLAS ITk pixel overview

The ITk pixel detector will consist of 5 silicon tracking layers split into 3 regions

Layout design choices:

Endcap half rings (instead of traditional disks)

- More flexibility to place sensors where needed for optimal coverage, avoiding excess hits/material
- Can route services in between rings



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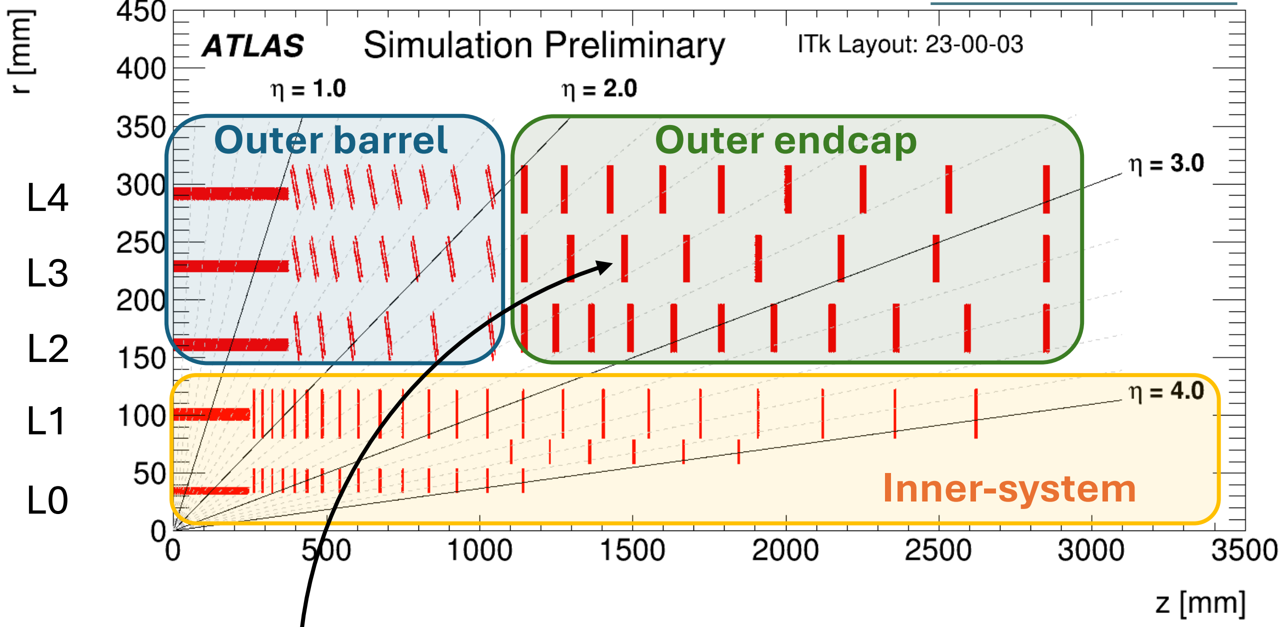
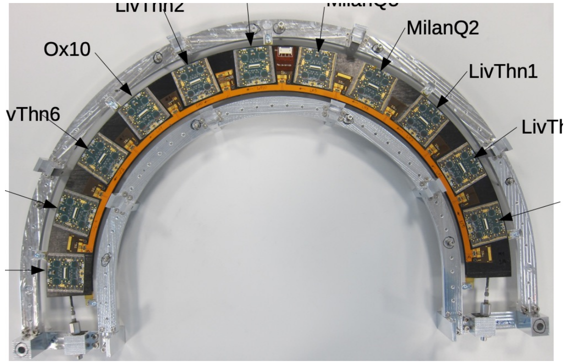


2 support shells / layer → each ring can be adjusted in |z| for layout optimisation



# ATLAS ITk pixel overview

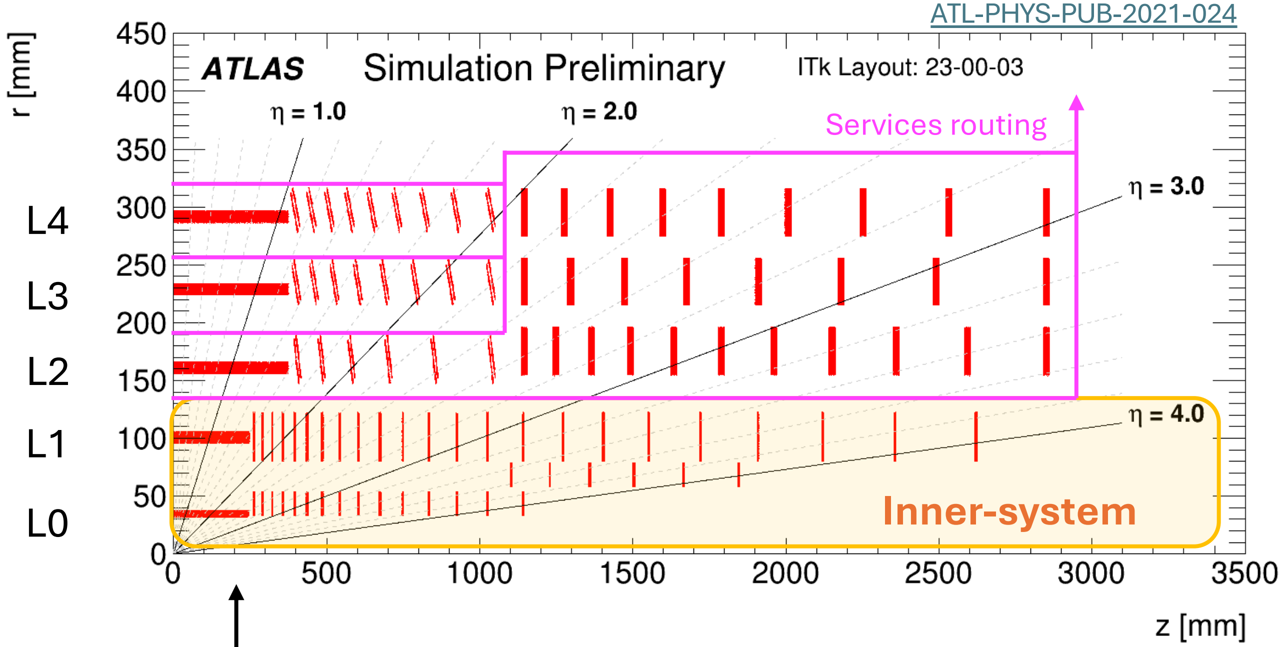
The ITk pixel detector will consist of 5 silicon tracking layers split into 3 regions

Layout design choices:

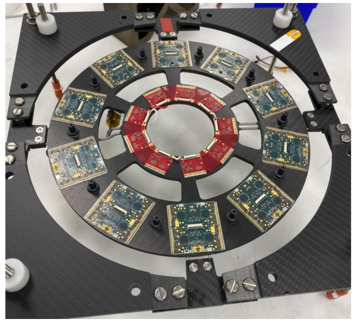
<u>Inner-system coupled rings</u>

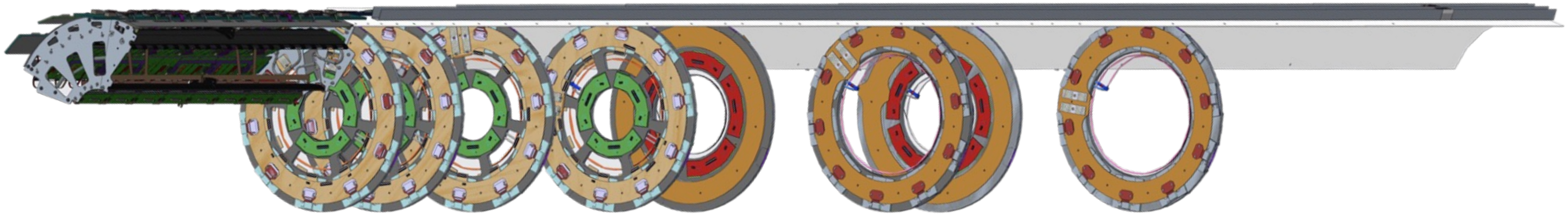
- Same principle as end-cap half rings
- Innermost 2 layers share support structure → designed to reduce services (material) within innermost layers
- No inclined rings (due to complexity)

Entire inner-system is independent of outer pixel → designed to be replaced after certain radiation dose



Inner-system “quarter shell”



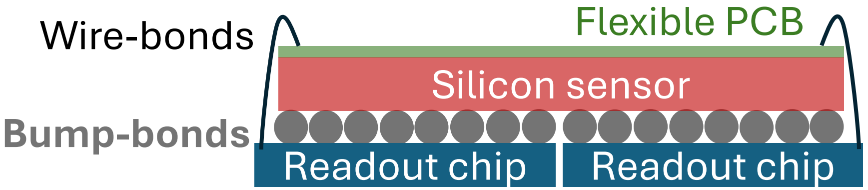


# Pixel modules

The basic building block of ITk is the **pixel module**

Pixel modules use **hybrid pixel detector** technology – passive silicon sensor bump-bonded to readout chips

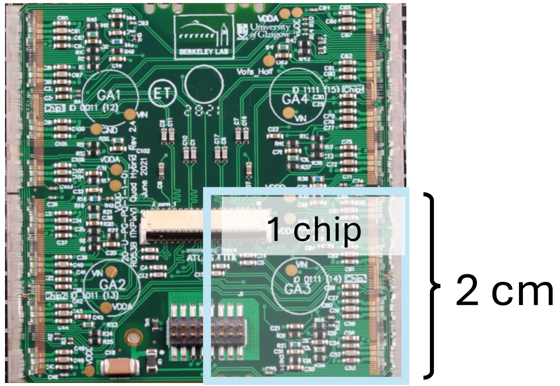
- Separate optimization of sensor & readout chips
- Produced with commercially-available technology



400 columns x 384 rows = 153,600 pixels / chip

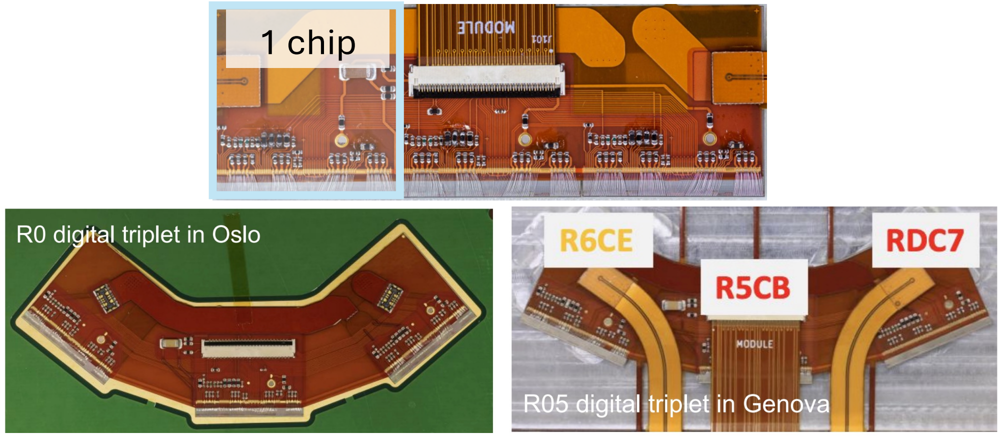
Entire detector built from singular module design, apart from the innermost layer

Quad module – 4 readout chips



Single 150 μm planar silicon sensor
(L1: 100 μm → radiation hardness)
50 x 50 μm pixels

Triplet module – 3 readout chips (innermost layer only)



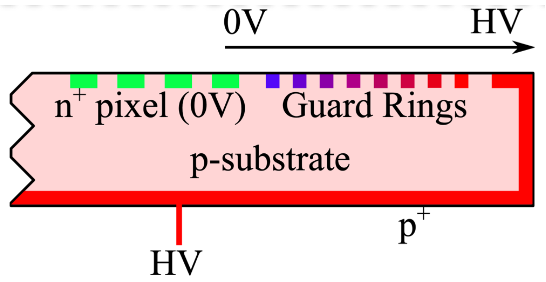
3 x 250 μm 3D silicon sensors,
50 x 50 μm pixels
(barrel: 25 x 100 μm → $d_0$ resolution)

# Sensors

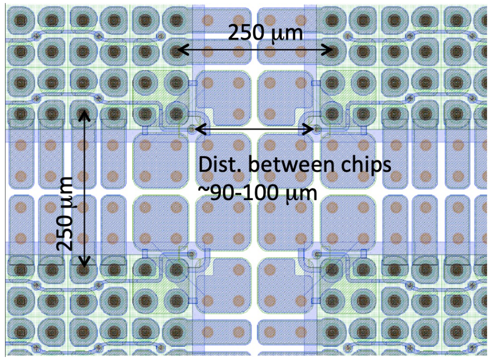
Extensive R&D has been done to create silicon sensors that can withstand the intense radiation of the HL-LHC

**Planar sensors:**

- Radiation hard to $\approx 4$ x $10^{15}$ n/cm$^{2}$ (@ 4000 fb$^{-1}$)
- n-in-p technology
- Bias voltages up to 600 V
- Vendors: HPK, Micron, FBK

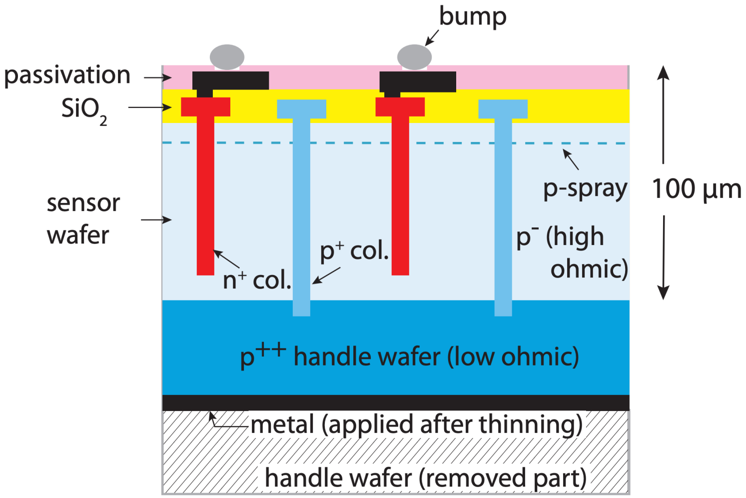


Pixel size varies in inter-chip region:

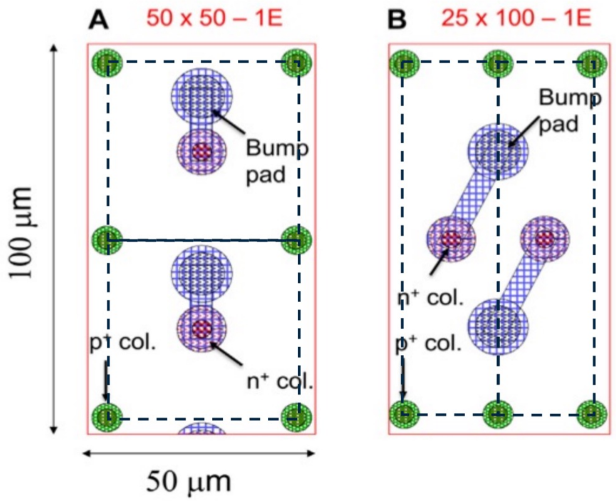


**3D sensors:**

- Radiation hard to $\approx 2$ x $10^{16}$ n/cm$^{2}$ (@ 2000 fb$^{-1}$)
- Used only in innermost ITk layer (L0)
- Technology demonstrated in ATLAS IBL
- Bias voltage up to 250 V
- Vendors: SINTEF, FBK



Pixel geometry:



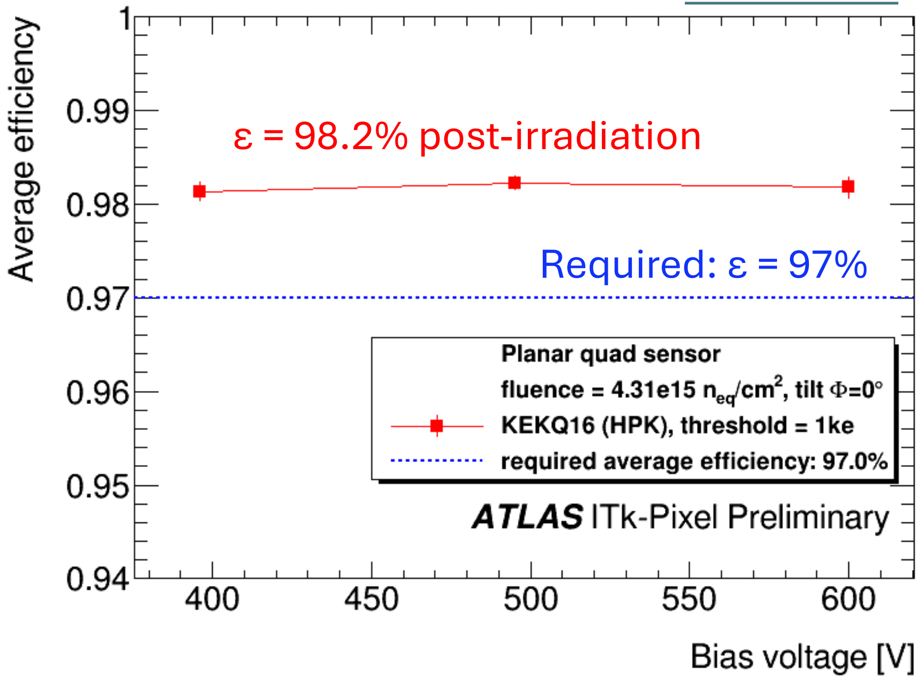
# Test beam results

It is of utmost importance to test modules and understand their behavior **post-irradiation**

- Planar quad modules have been irradiated up to $10^{15}$ n/cm$^2$, 3D single chip cards irradiated up to $10^{16}$ n/cm$^2$
- Modules tested in September 2023 test-beam campaign at CERN SPS

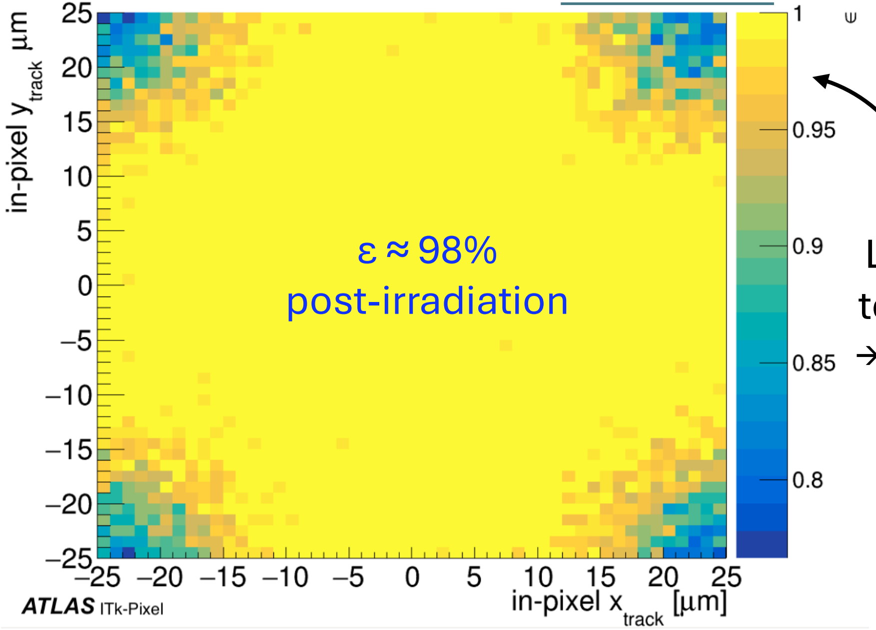
HPK planar quad module:

ITK-2023-005



FBK 3D single-chip cards:

ITK-2023-004



Lower efficiency due to electrode columns → improved with tilted configuration

✅ Irradiated modules meet hit efficiency requirements

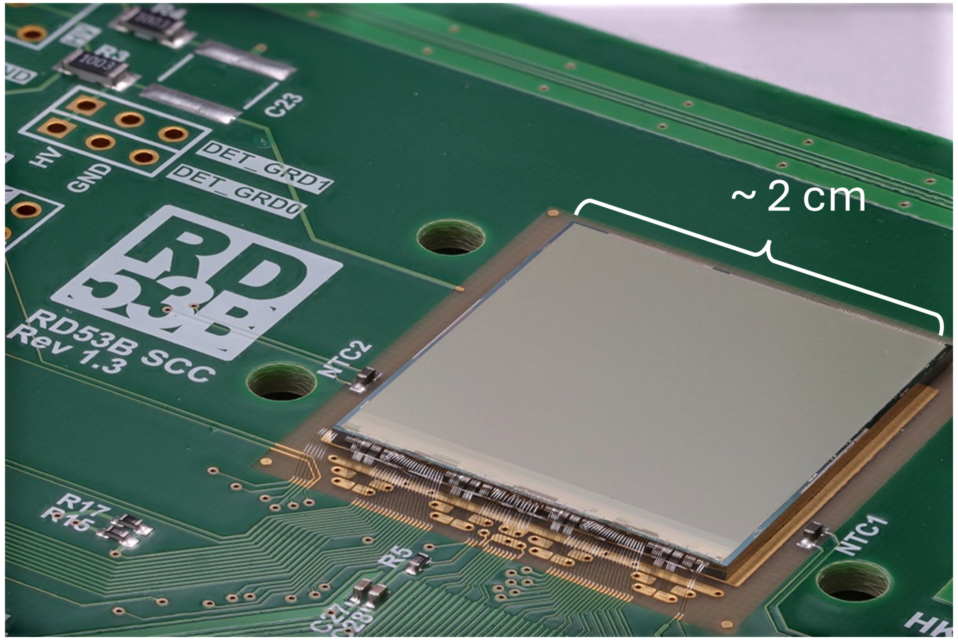
# Readout chip

All modules will be read out with **ITkPix front-end readout chip**

- 65 nm CMOS technology
- Radiation hard up to 1 Grad
- 4-bit charge measurement / pixel (ToT)
- Designed by RD-53 collaboration over ~ 10 years

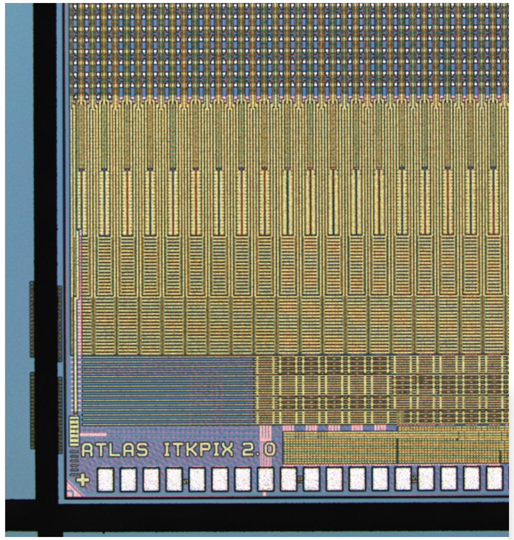
Stringent requirements compared to current FE-chips:

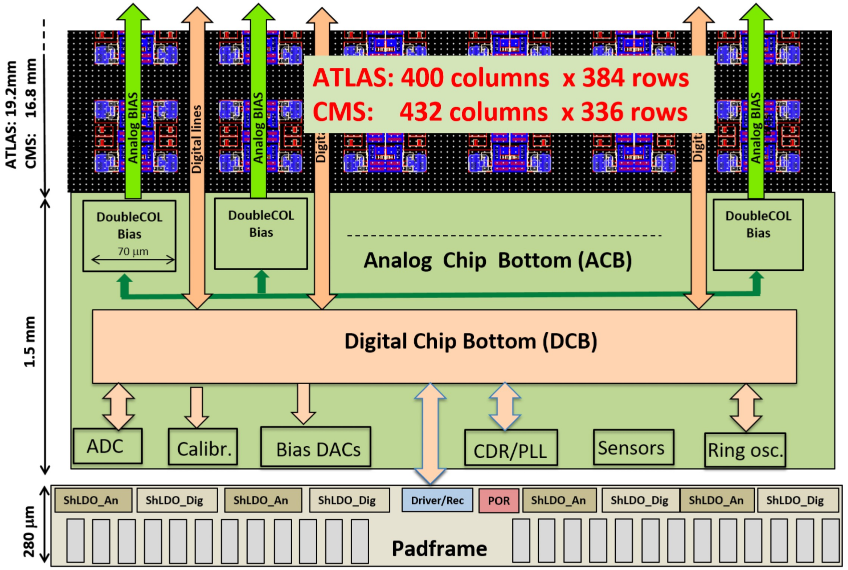
- 10 x higher radiation hardness
- 10 x larger effective trigger latency hit buffering
- 100 x larger effective readout bandwidth
- Same power consumption (< 1 W/cm²)



ITkPixv1.1 used for preproduction

ITkPixv2 is production chip – first wafer delivered in September 2023!



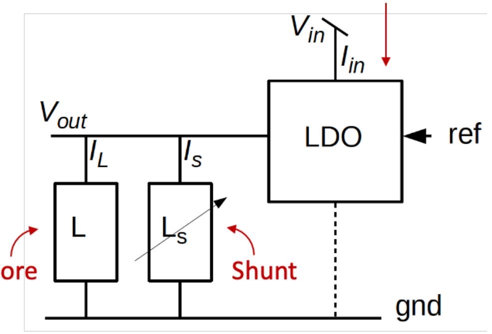


# Serial powering

In order to minimize material budget, a **serial powering scheme** will be utilized

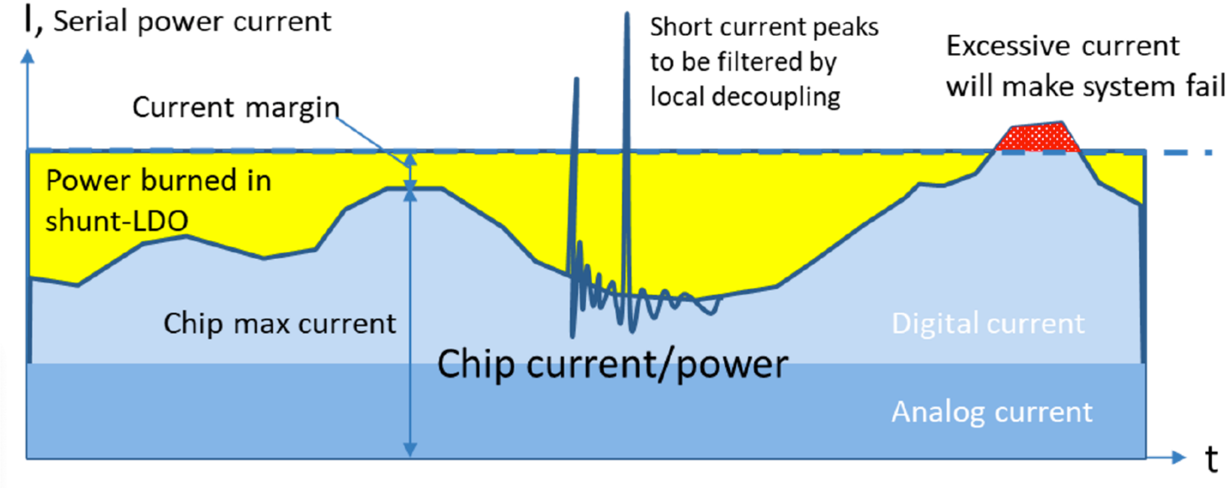
ITkPix chips are equipped with Shunt Low Drop Output (SLDO) power regulators

- When powered with constant current, SLDO’s dynamically adjust shunt current to have constant local voltages on chip

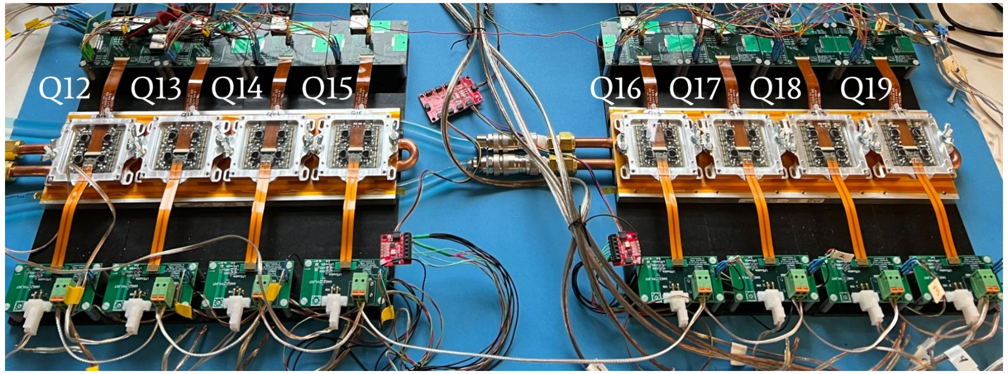


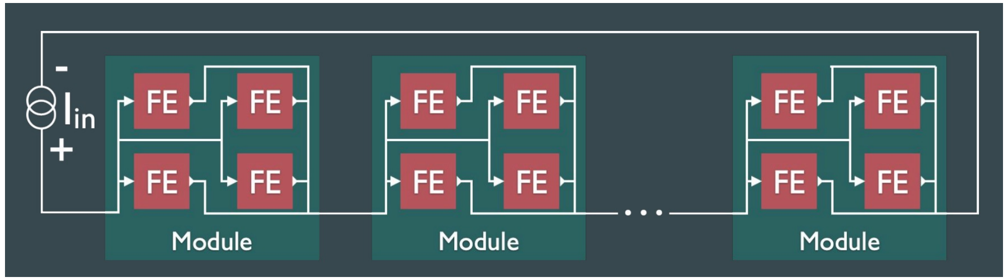
$$I_{in} = I_L + I_s = \frac{V_{in} - V_0}{R_{\text{eff}}} \qquad [V_{in} > V_0]$$

Modules will be powered in series with constant current in serial powering chain, chips on a module will be powered in parallel → improve reliability of chain in case of chips breaking



Challenges: operation with minimum overhead, uniform current draw of chips in one module, inter-module compatibility, …





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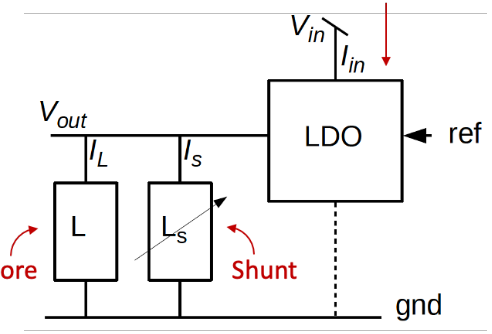

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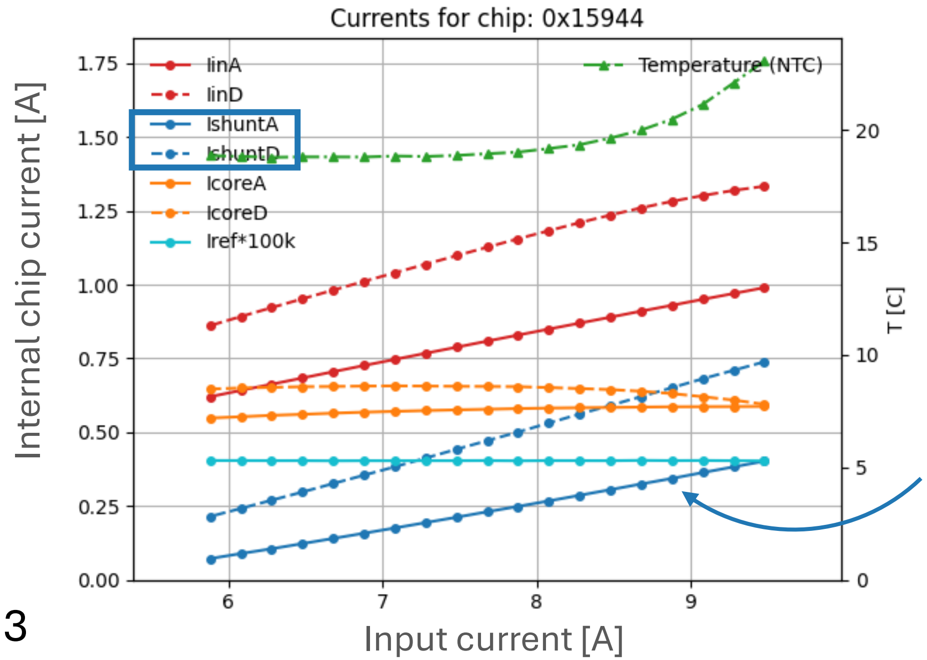
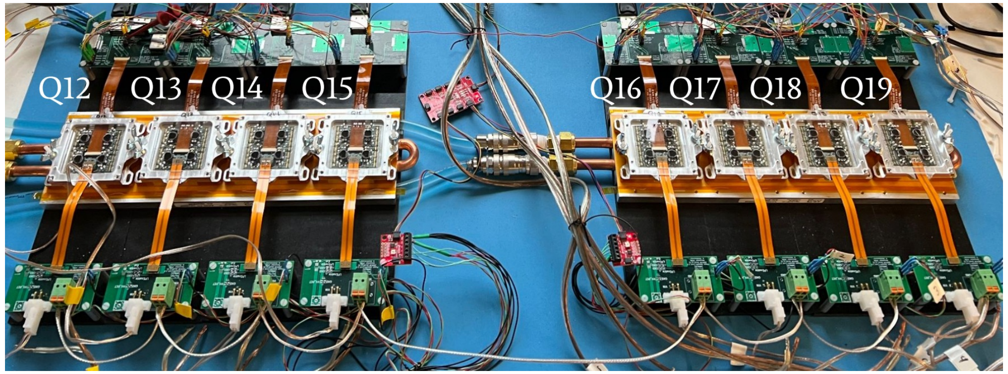
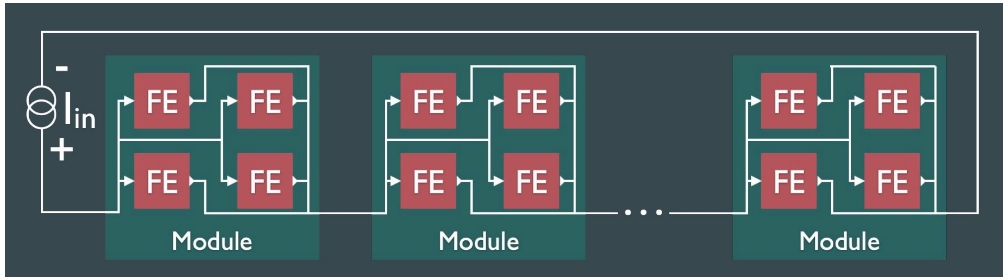


Shunt currents on chip increase with module input current

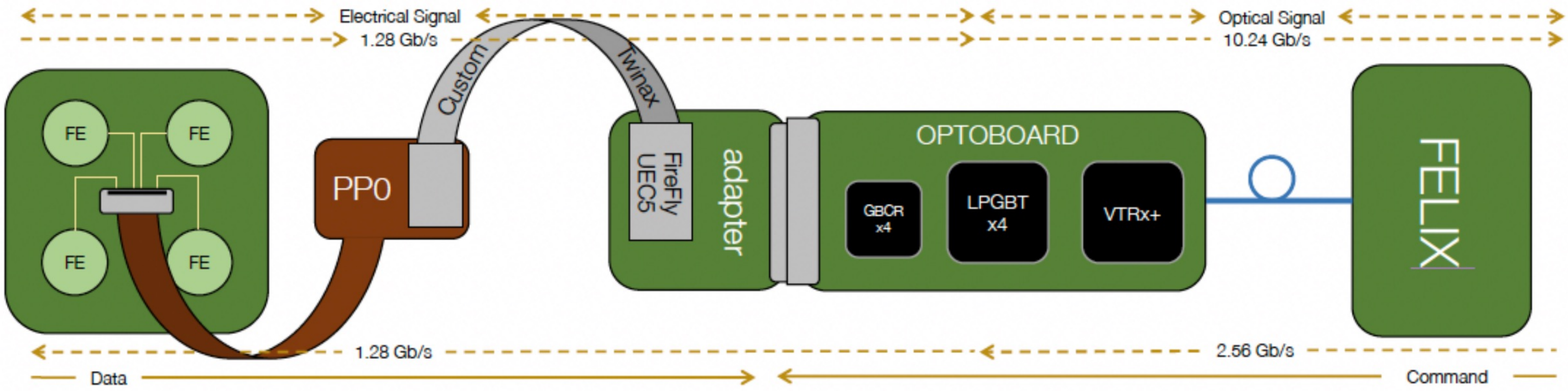
Serial powering chain with quad modules at LBNL





# Data transmission

Reading out the data from a detector with > 5 billion channels is a challenge!



- Readout of FE-chip with up to 4 links / chip at 1.28 Gb/s
- Custom low-mass twinax cable for transmission from detector to optoboards (up to 6 m)
- Optoboard: aggregates electrical links into high speed optical links via lpGPT chip
- FELIX: **common** detector interface hardware, reads out optical signal (10.24 Gbps fibre)

To reduce material, links are shared at all stages

# Data merging

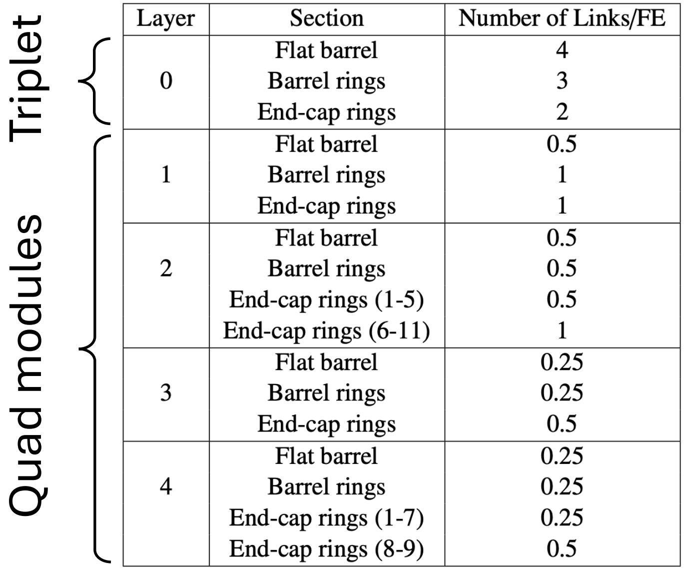
Requirements on module design vary significantly depending on position in detector

- Readout bandwidth varies from ~4 Gb/s/chip in innermost layer to 20-50 x lower in outer regions

Key feature of ITkPix chips are a **high level of readout link modularity** and flexibility

- Each chip as available 4 serial output links (1.28 Gb/s), single link can be used
- However majority of detector needs < 1 link → introduce capability to merge multiple links

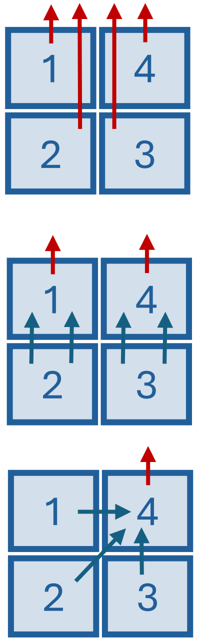
Link configurations:



Triplet

Quad modules

| Layer | Section | Number of Links/FE |
|---|---|---|
| 0 | Flat barrel<br>Barrel rings<br>End-cap rings | 4<br>3<br>2 |
| 1 | Flat barrel<br>Barrel rings<br>End-cap rings | 0.5<br>1<br>1 |
| 2 | Flat barrel<br>Barrel rings<br>End-cap rings (1-5)<br>End-cap rings (6-11) | 0.5<br>0.5<br>0.5<br>1 |
| 3 | Flat barrel<br>Barrel rings<br>End-cap rings | 0.25<br>0.25<br>0.5 |
| 4 | Flat barrel<br>Barrel rings<br>End-cap rings (1-7)<br>End-cap rings (8-9) | 0.25<br>0.25<br>0.25<br>0.5 |



↑ 1.28 Gb/s ↑ 320 Mb/s

Low dataflow (0.25 links / FE)

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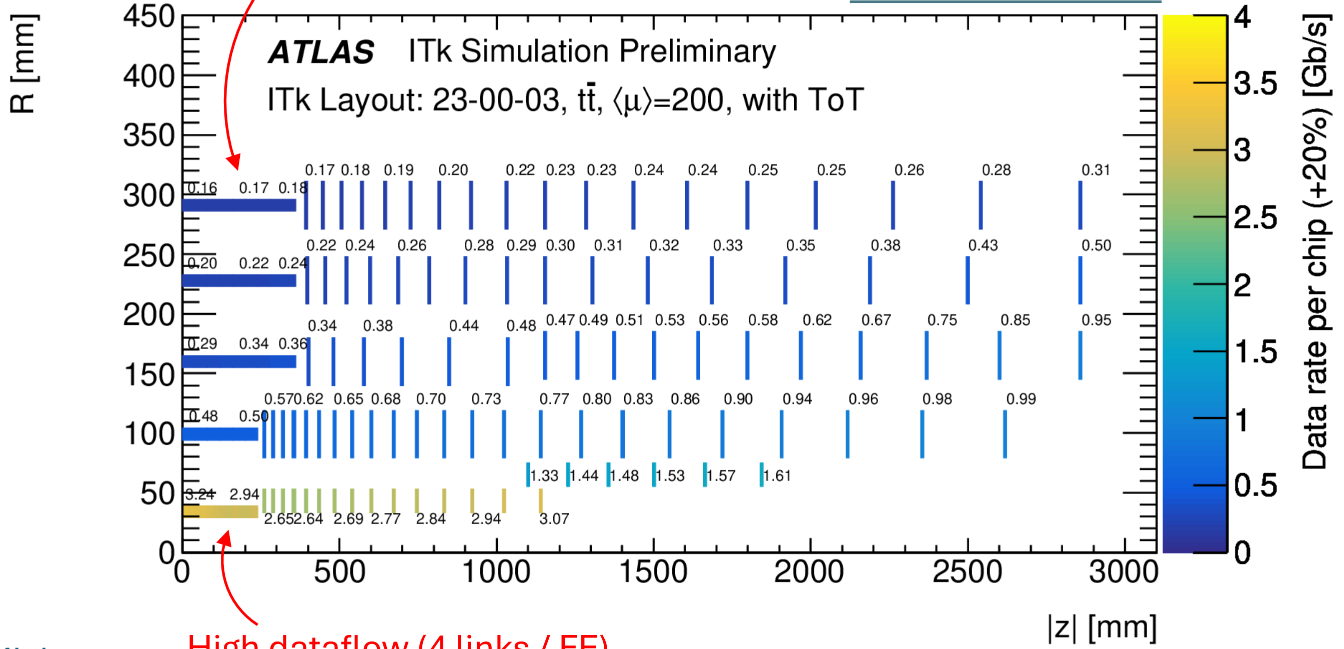


High dataflow (4 links / FE)

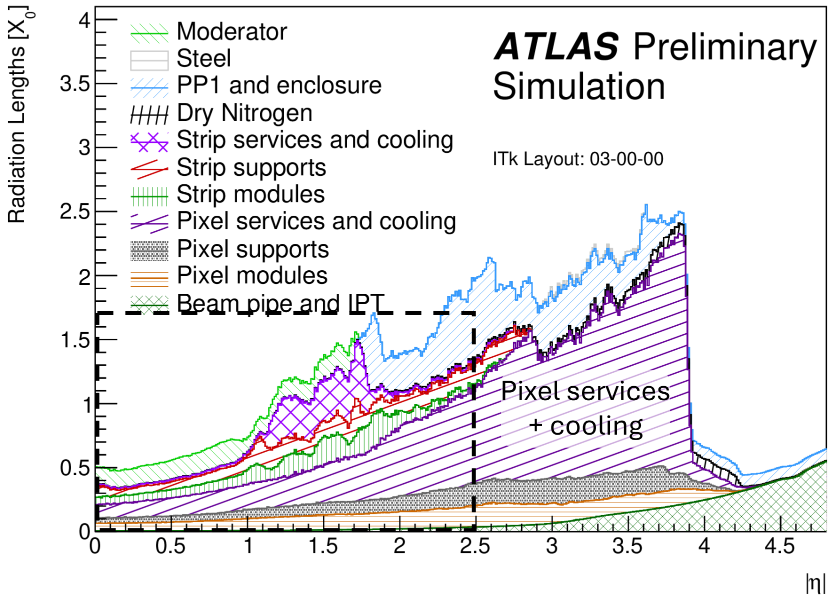
# *Reduced* material budget

The ITk aims to achieve a reduced material budget – important for tracking efficiency in dense environment

- How? Reduce cabling with serial powering scheme, thinner chips, low mass support structures, evaporative $C0_2$ cooling with thin titanium pipes…

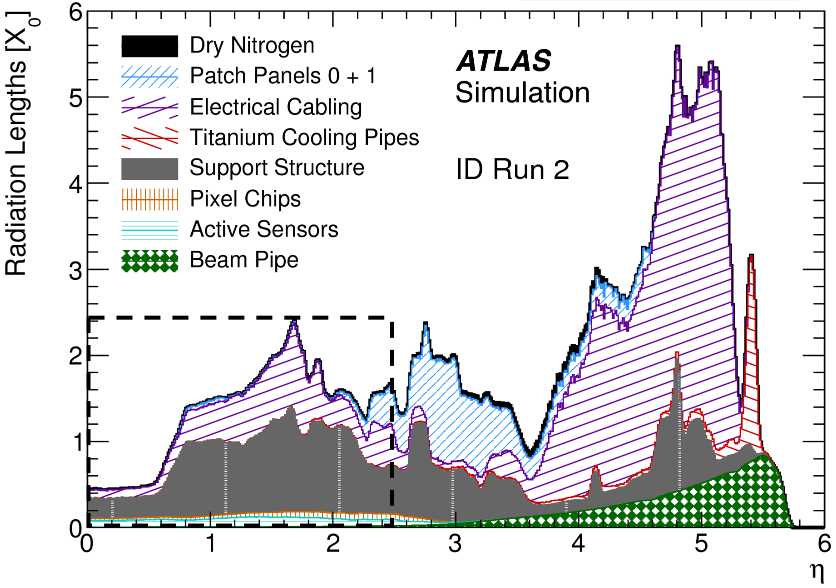
Expected ITk material distribution:

ITK-2023-001



Current detector:

CERN-LHCC-2017-021



Significant reduction in material (pixel powering cables) due to serial powering scheme ✅

Nevertheless, slightly more material in central (|η|<1.5) region – more channels to read out

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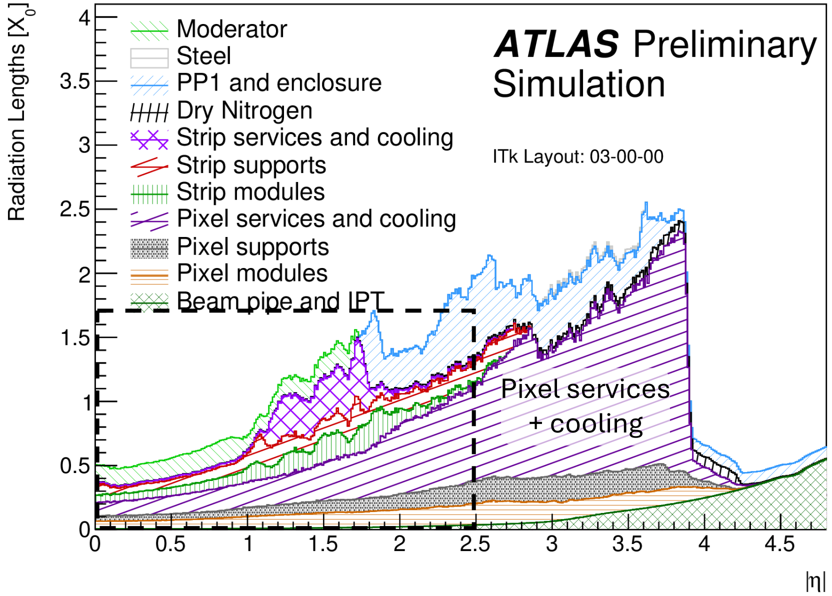
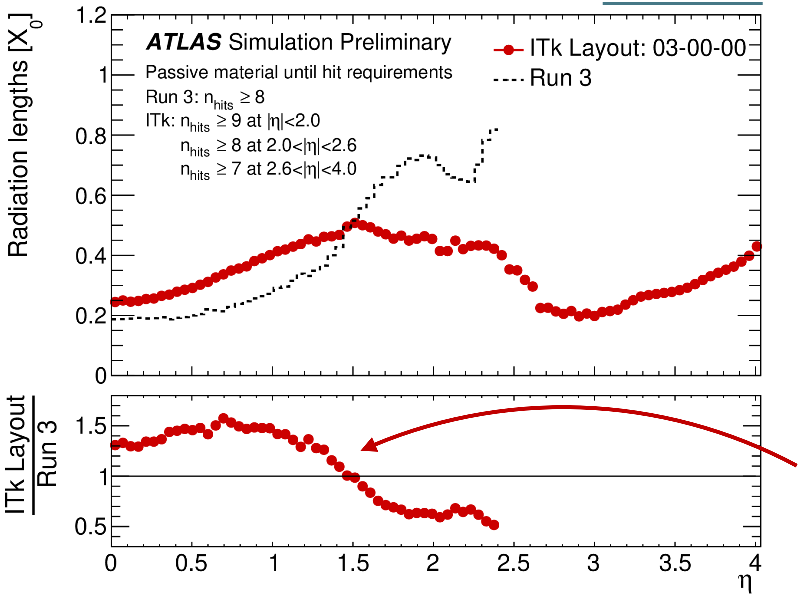


Comparison with current detector:

ITK-2023-001



More material in ITk

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# *Reduced* material budget

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Expected ITk performance

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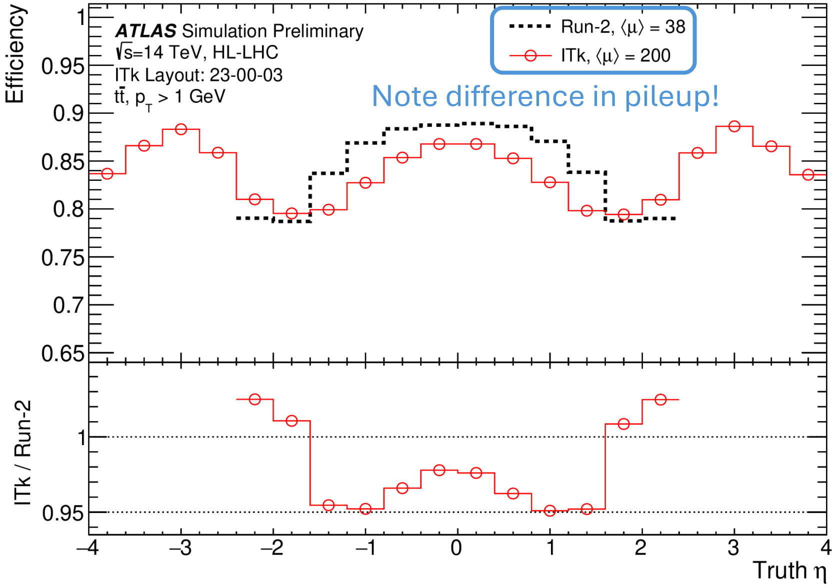
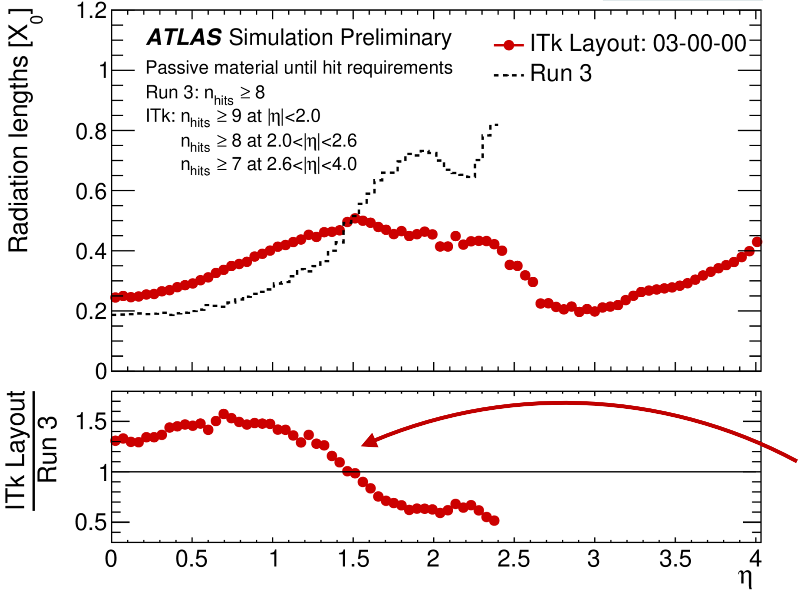


Note difference in pileup!

Comparison with current detector:

ITK-2023-001



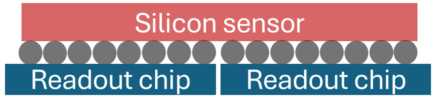
More material in ITk

Despite additional material, expected tracking performance of ITk is within 5% of the Run-2 performance in the barrel region, and comparable in forward region, despite harsher conditions (μ = 200)

# Mass production procedure

Module **pre-production** is currently underway – produce 10% of total modules to test assembly, testing, and loading procedures

Module assembly:



Bare module (from industry)

\+

Flexible-PCB

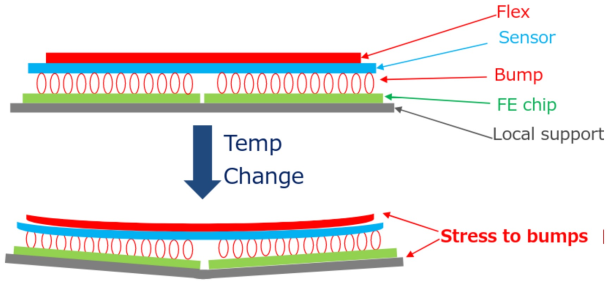
\+ wirebond

After assembly, modules undergo rigorous electrical Quality Control (QC) testing procedure, with several stages:

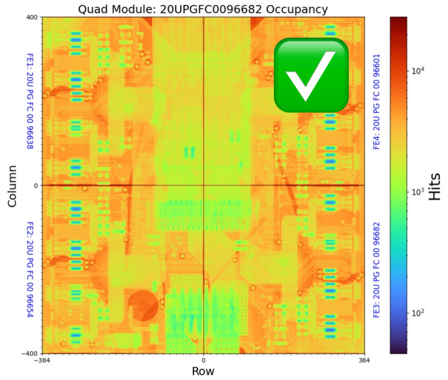
Assembly → **Initial characterization** → Parylene coating → **Post-parylene characterization** → Wirebond protection → Stability (~10 hours) → Thermal cycling -45°C to 40°C (x10), -55°C to 60°C (x1) → **Final characterization** → To loading site

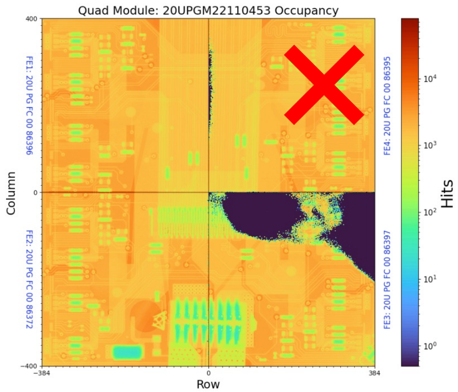
**Characterization**: All electrical tests at 20°C and -15°C
All other stages: Minimal set of electrical tests

Testing procedure includes 13 tests checking chip powering, sensor IV, and performance of **individual pixels**:



ATL-ITK-PROC-2024-018





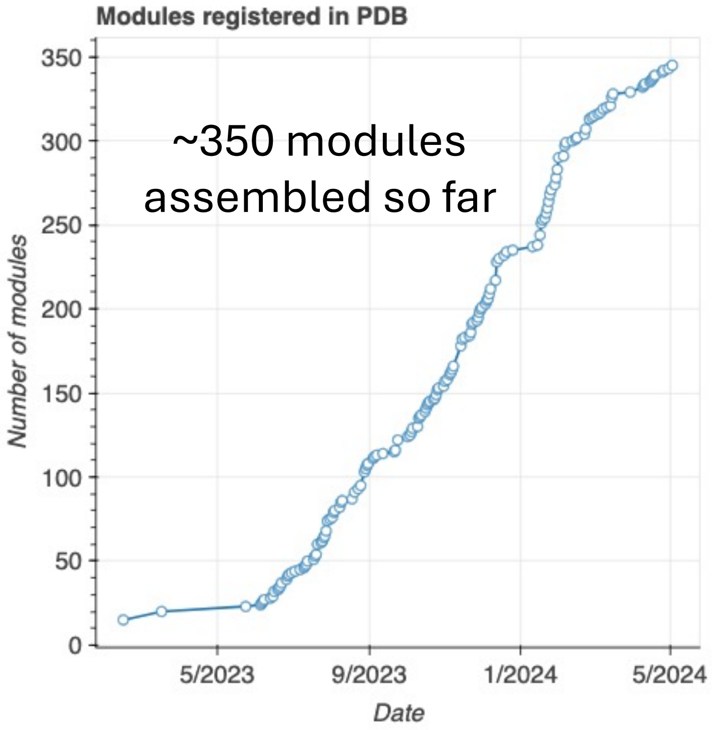
Expect fewer than 0.39% of disconnected bumps after thermal cycling

# Mass production status

Module production is a **global** effort – modules are assembled/tested at 25 different sites and loaded at 9 sites

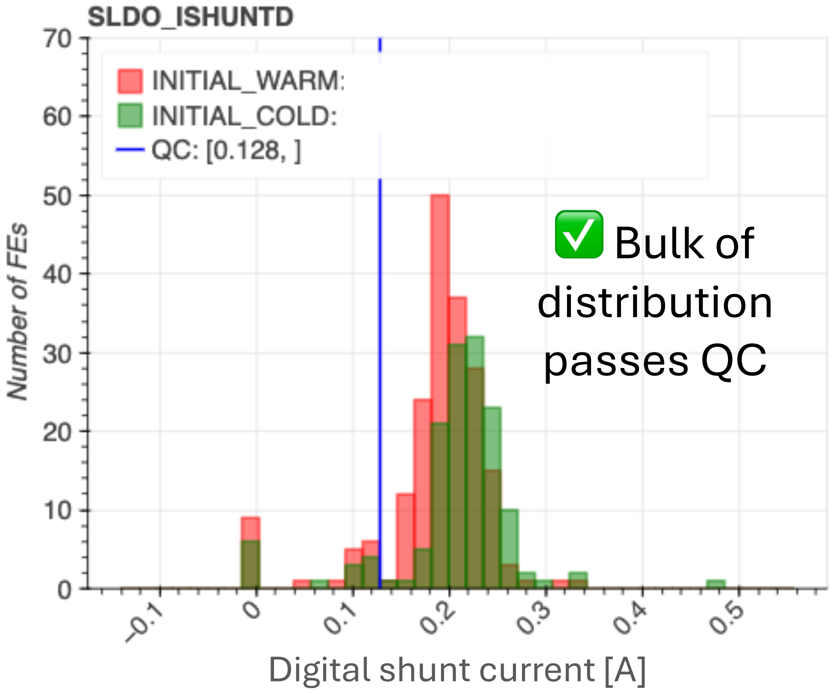
Huge book-keeping effort (need to keep track of ~12,000 modules and testing results!) → using common testing tools and database

Pre-production progress:



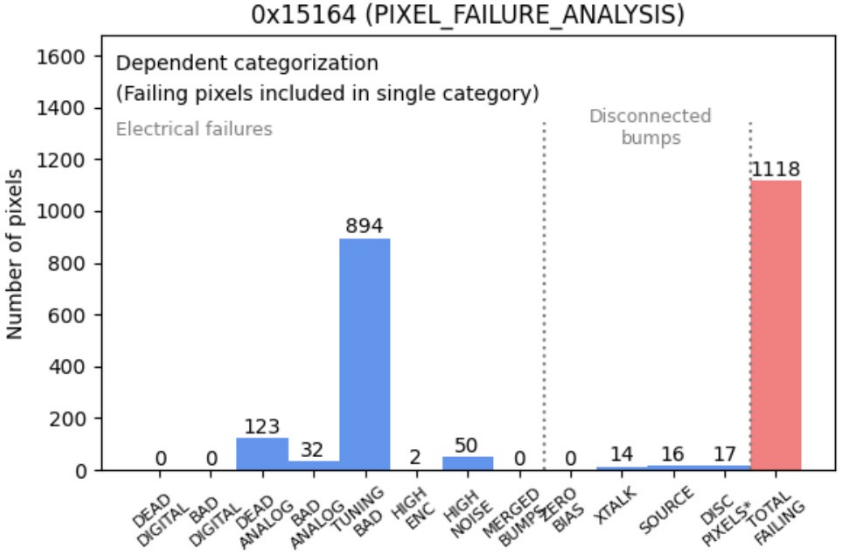
~350 modules assembled so far

SLDO verification:



✅ Bulk of distribution passes QC

Pixel categorization for one module:



# Loaded local supports

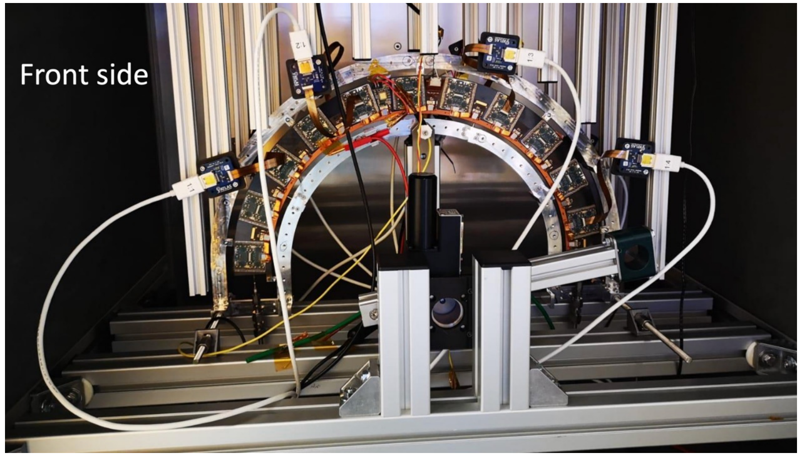
Moving from building individual modules to loading local support structures – critical test of **loading procedure, cooling, services, and readout**

Various loaded-local supports have been built with module using prototype version of ITkPix chip

→ Valuable lessons in understanding how to overcome challenges with operating larger detector

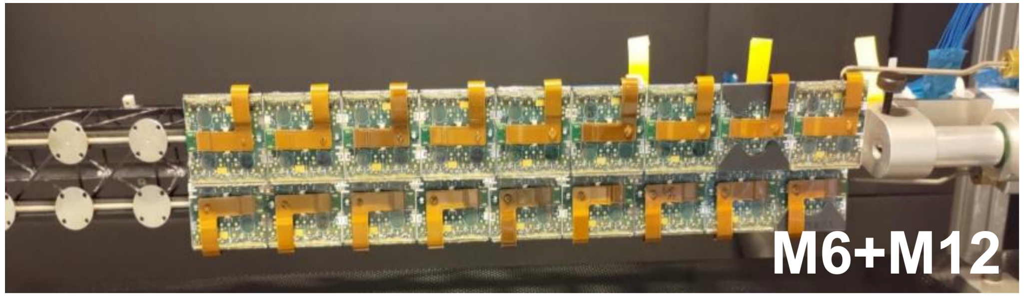
Next step: test similar structures with pre-production modules

Outer end-cap ring:

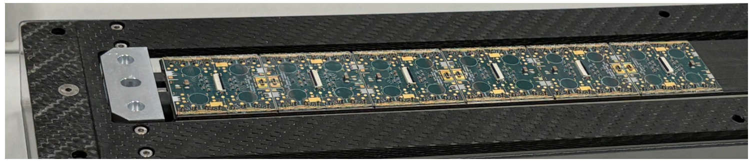


Inner system coupled-ring:

Outer barrel longeron:



Inner system (L1) barrel:



# Summary

HL-LHC will pose significant challenges for charged particle tracking

The **ATLAS ITk pixel detector** will overcome these challenges – with next generation sensors and readout chips, serial powering, novel layout, …

Tracking performance of ITk expected to be **comparable to Run-2** performance, despite more challenging environment!

Project is entering **mass production** stage:

| Area | PDR | Prototyping | FDR | Preproduction | PRR | Production |
|---|---|---|---|---|---|---|
| Planar Si sensors | 🟩 | 🟩 | 🟩 | 🟩 | 🟦 | 🟦 |
| 3D Si sensors | 🟩 | 🟩 | 🟩 | 🟩 | 🟦 | 🟦 |
| FE-ASIC | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟦 |
| Hybridisation | 🟩 | 🟩 | 🟩 | 🟦 | 🟦 | 🟥 |
| Module assembly | 🟩 | 🟩 | 🟩 | 🟦 | 🟥 | 🟥 |
| On-detector services | 🟩 | 🟩 | 🟩 | 🟦 | 🟥 | 🟥 |
| Off-detector services | 🟩 | 🟩 | 🟩 | 🟦 | 🟥 | 🟥 |
| Data Transmission | 🟩 | 🟩 | 🟦 | 🟥 | 🟥 | 🟥 |
| Bare Local Supports | 🟩 | 🟩 | 🟩 | 🟦 | 🟦 | 🟥 |
| Loaded Local Supports | 🟩 | 🟩 | 🟩 | 🟥 | 🟥 | 🟥 |
| Global Mechanics | 🟩 | 🟩 | 🟥 | 🟥 | 🟥 | 🟥 |
| Integration | 🟩 | 🟩 | 🟥 | 🟥 | 🟥 | 🟥 |
| Power supplies | 🟩 | 🟩 | 🟩 | 🟦 | 🟥 | 🟥 |

🟩 Complete 🟦 Ongoing 🟥 Upcoming

→ ITk Pixel ready for insertion 2027