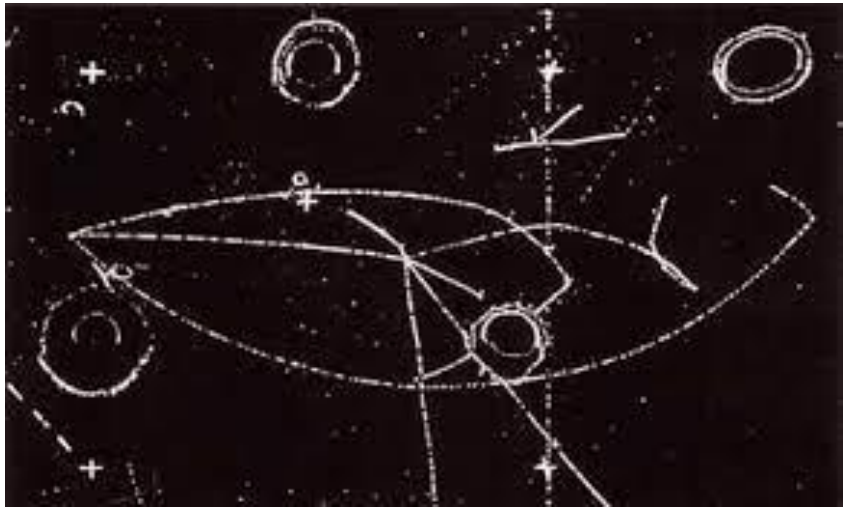
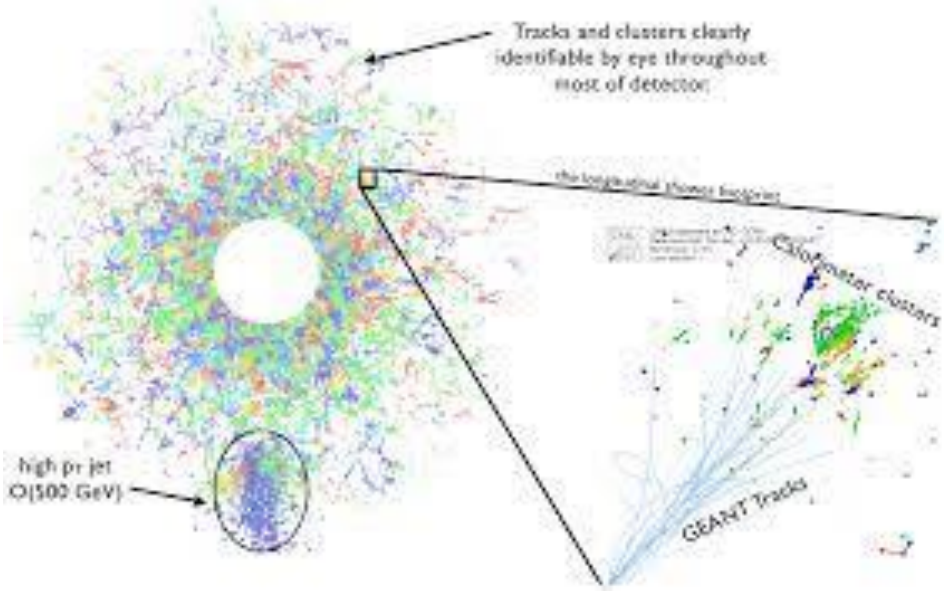
Front-end electronics for future calorimetry

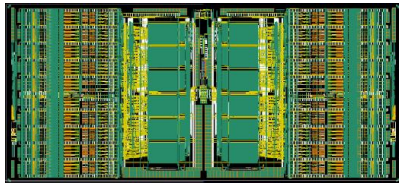
Ch. de LA TAILLE Corfu meeting 2024

Need for electronics

- Better electronics make better detectors or even new detectors (eg trackers, 5D calos, timing)

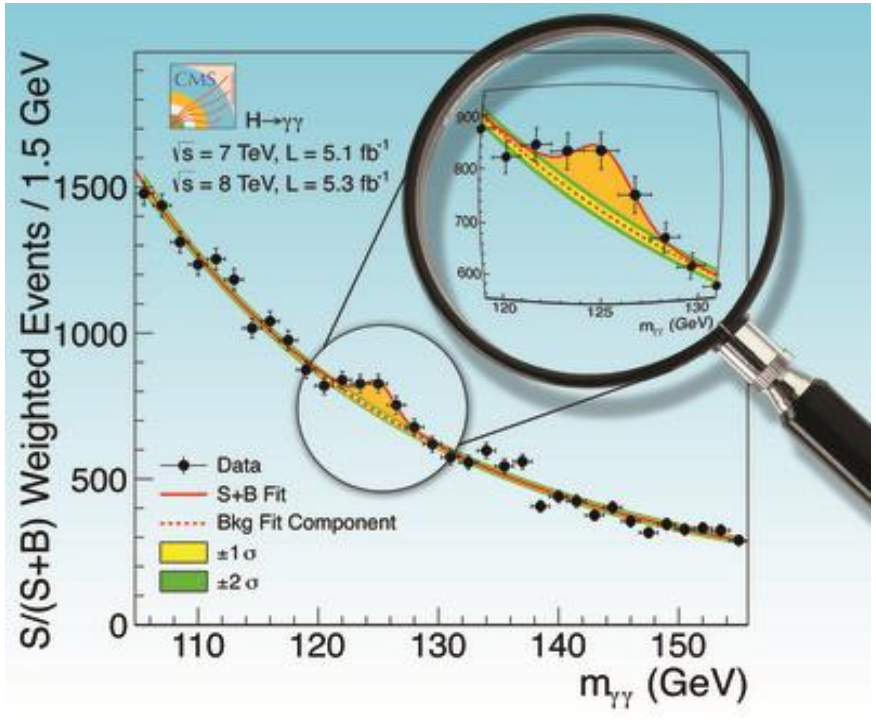


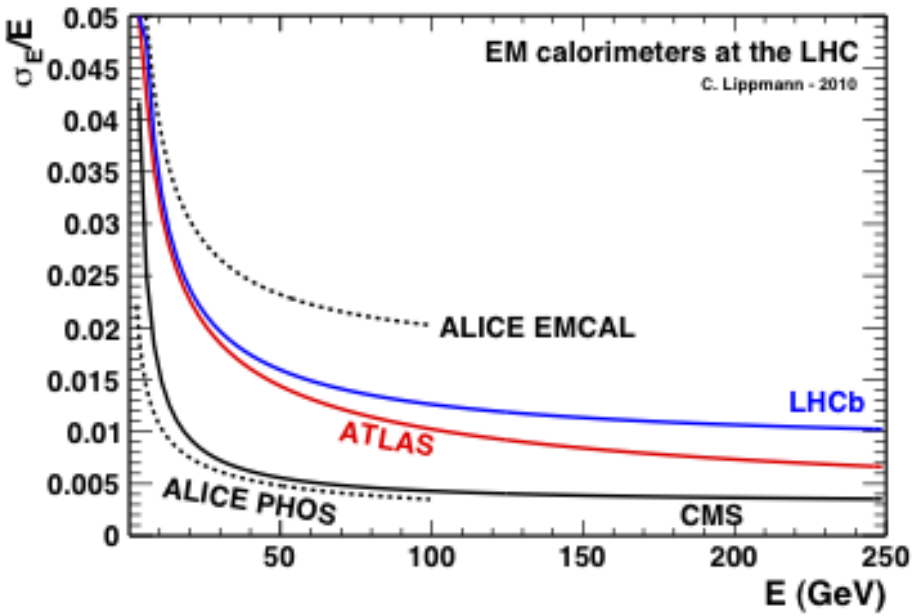


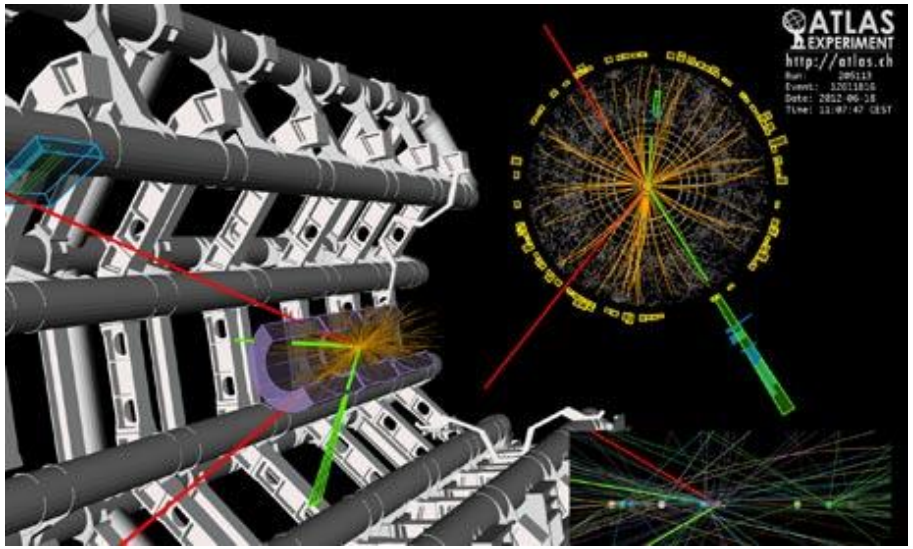


Importance of electronics : calorimeters

- Large dynamic range (10^4-10^5)
- High Precision ~1%
  - Importance of low noise, uniformity, linearity…
  - Importance of calibration
- Resolution : $\sigma(E)/E = a/E \oplus b/\sqrt{E} \oplus c$

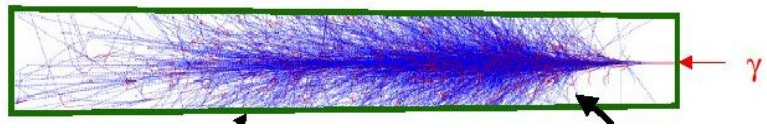


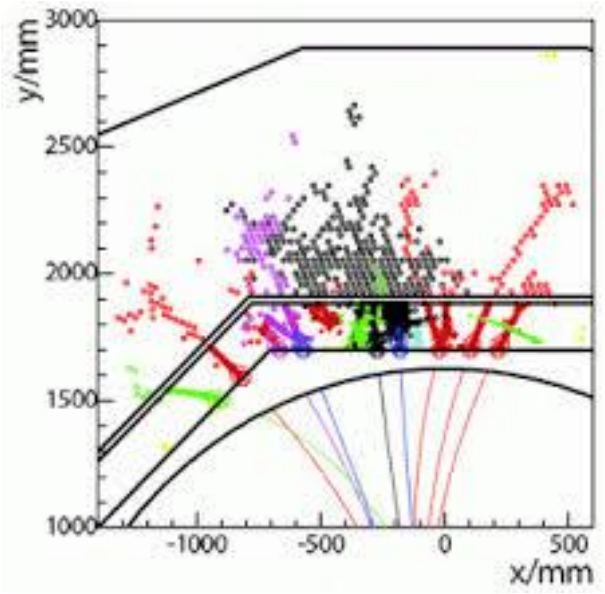


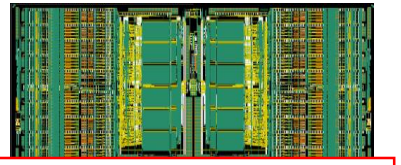


Evolution of calorimetry : « imaging calorimetry »

- 3D calorimetry : eta, phi, Energy
- 4D calorimetry : x,y,z,E
- 5D calorimetry : x,y,z,E,t
  - High granularity=> Millions of channels = > Low power !
    - Power pulsing ~1% for ILC
    - Low power + C02 cooling for CC
  - Energy measurement : Large dynamic range
    - MIP sensitivity => low noise (~0.1 fC)
    - Up to thousands of MIPs (~10 pC)
  - Timing information
    - Nice addition for LC for PID : few ns is enough
    - Crucial for HL-LHC : pileup mitigation, need few tens of ps
  - Embedded electronics vs data out
    - Daisy chain and low power busses for e+e-
    - High speed e/optical links for HL-LHC
  - Radiation levels
    - Negligible at an e+e-
    - Daunting at HL-LHC : >200 Mrad 1^{E}16N







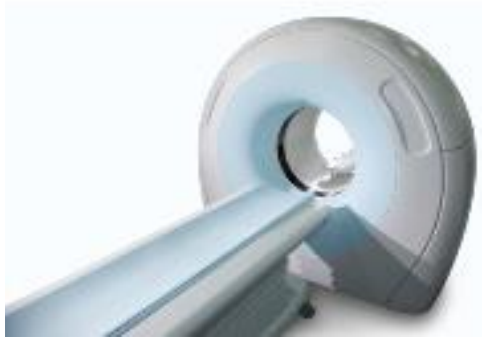
CMS HGCAL ~20mW/ch

ATLAS LAr FEB ~1W/ch

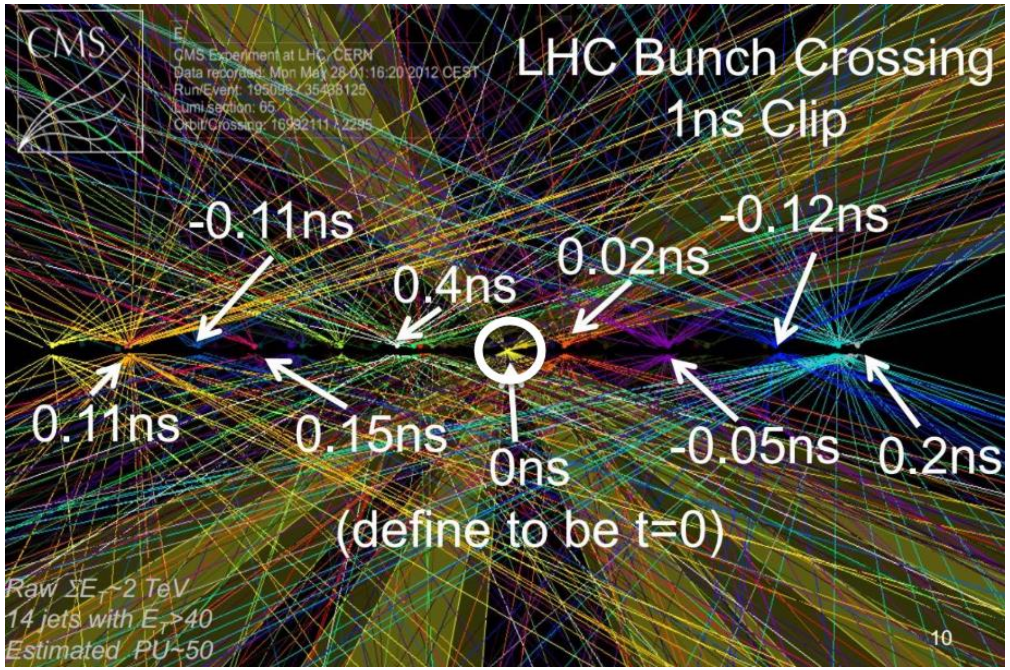
Need for timing

- Time resolution <50ps required by many experiments/applications keeping low power, large dynamic range ….

- **PET/ Time of Flight** measurements
  - SiPMs, lots of light
  - Time resolution <100ps



- **« 5D Calorimetry » CMS HGCAL**
  - Si PIN diodes : no gain.
  - . Timing ability ~50ps (for > 10 mips desirable)



- **Pileup rejuection : MIP timing detectors (ATLAS & CMS)**
  - LGAD sensors : Time performance ~30 ps : To reject Time Pile up events => better particle identification

- **TOF detectors/ PID** (SiPM)
  - MCPs, SiPMs… Few photoelectrons.
  - Time performance ~30 ps

- …

Timing optimization : common view

- Jitter due to electronics noise:

$$\sigma_t^J = \frac{N}{\frac{dV}{dt}}$$

- also presented as j = tr / (S/N)
- dV/dt prop to BW, N prop to √ BW => jitter prop to 1/√BW

⇒ « the faster the amplifier the better the jitter ? »

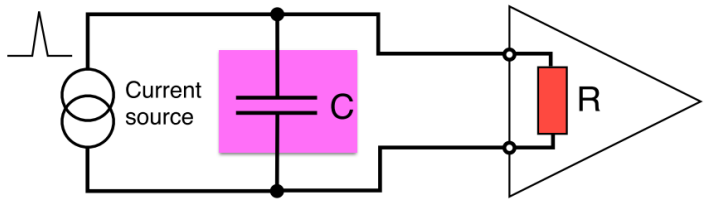
⇒ « High speed preamps need to be low impedance (50 Ω or less) »

NB : tr = $t_{10\text{-}90\%}$ = 2.2 tau.

f_{-3dB} = 1/2πtau = 0. 35 / $t_{10\text{-}90\%}$

f_{-3dB} = 1 GHz <-> $t_{10\text{-}90\%}$ = 300 ps

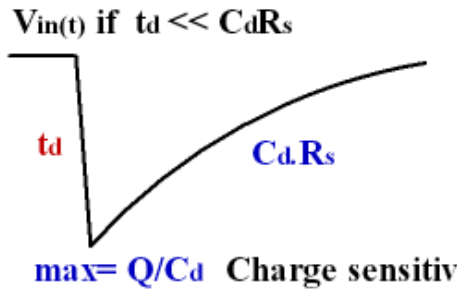
1 ps = 300 µm in vacuum

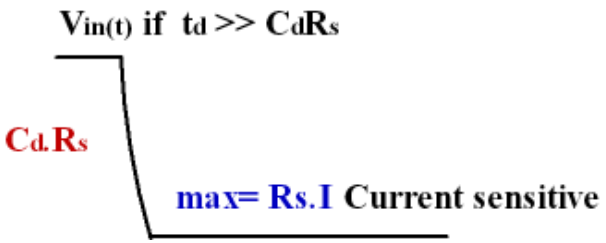


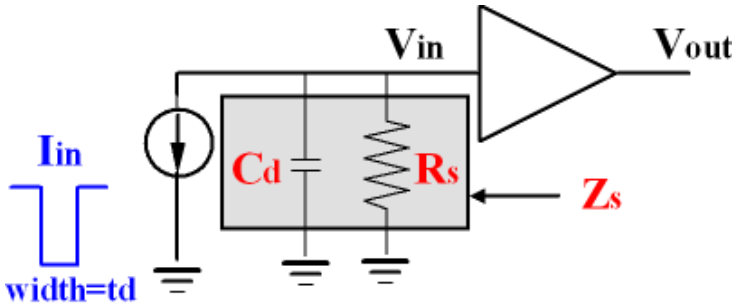
Detector impedance and input voltage

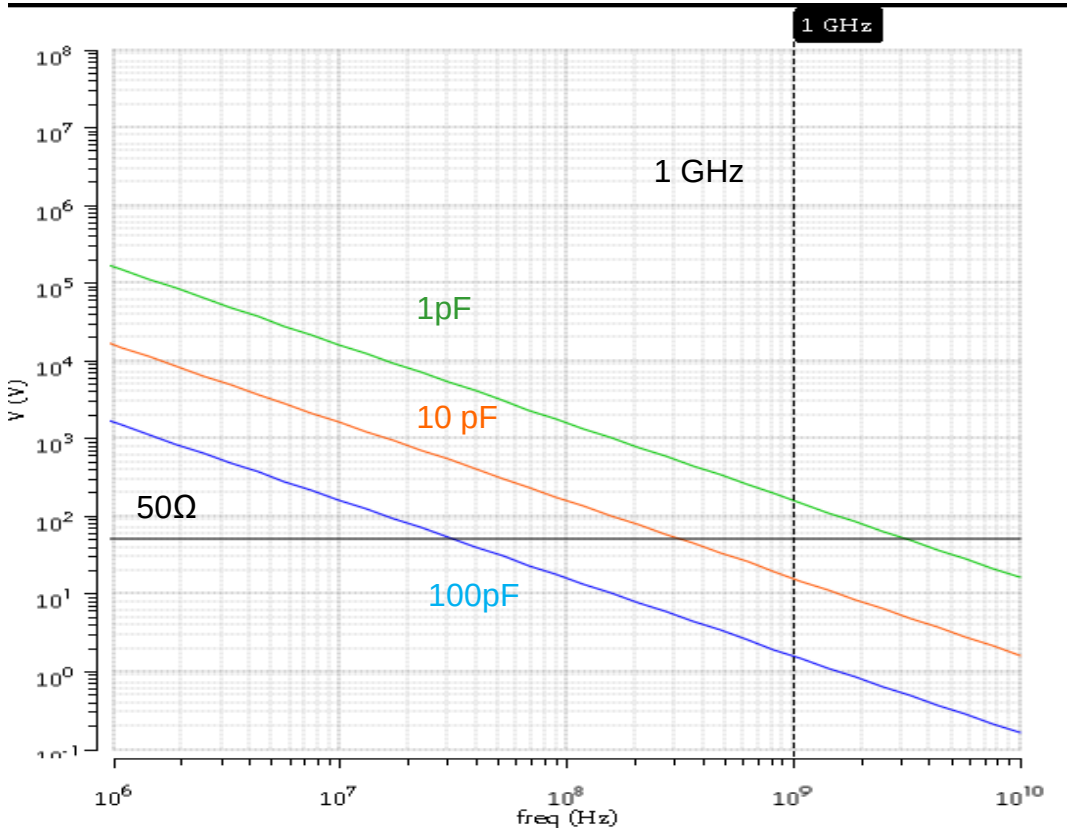
- 1 GHz, Cd=few tens of pF, input signal width <1ns
- Cd>1 pF, Zs@1GHz dominated by Cd
- Rise time: tr= td when td<< $R_S C_d$ and tr= $R_S C_d$ when td>> $R_S C_d$

At HF : difficult to beat the capacitance => signal integrated on Cd



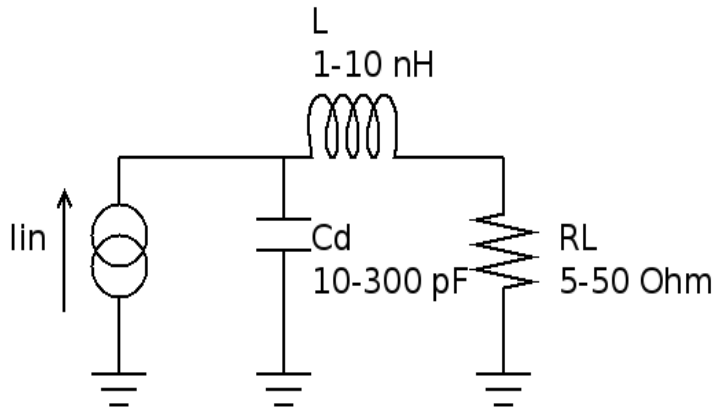


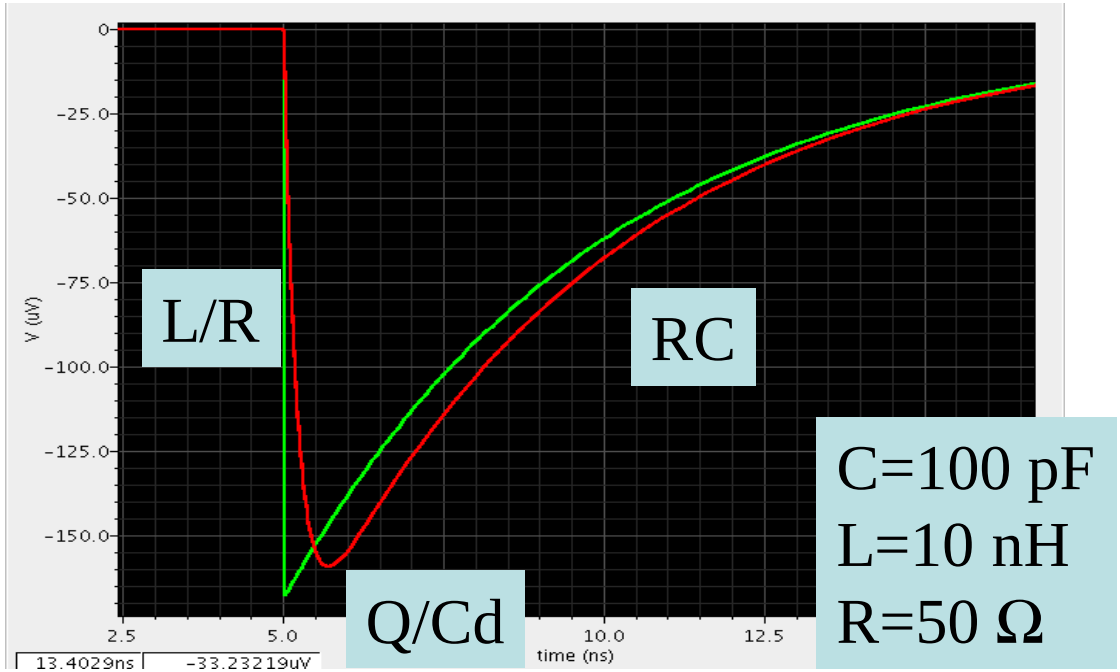


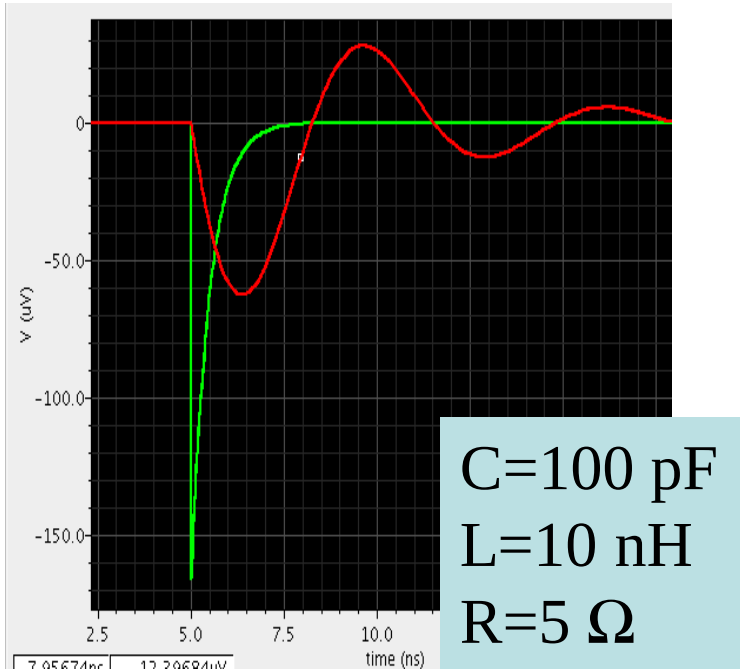


Examples of pulse shapes

- SiPM pulse : Q=160 fC, Cd=100 pF, L=0-10 nH, R_{PA}=5-50 Ω
- Sensitivity to parasitic inductance
- Choice of R_{PA} : decay time, stability
- Small R_{PA} not necessarily the fastest
- Convolve with current shape… (here delta)







Jitter optimization

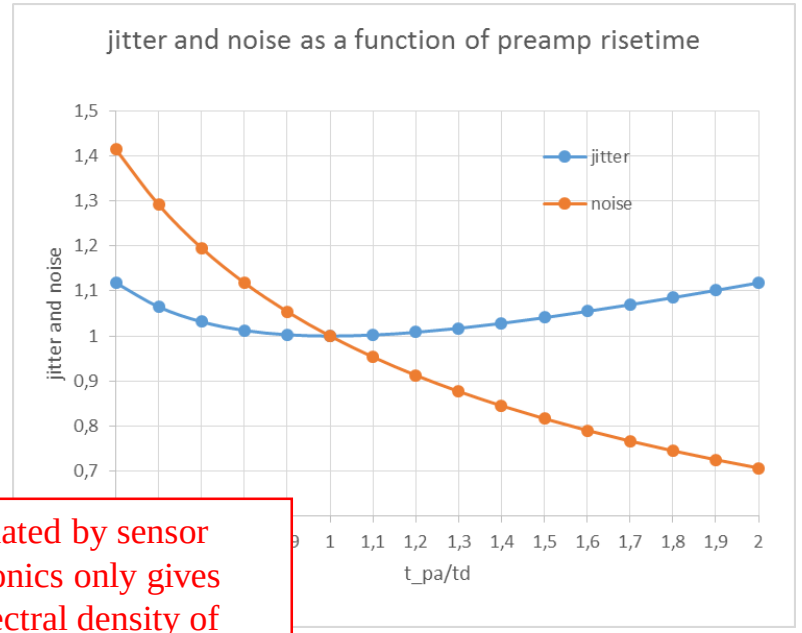
- Jitter is given by [details in backup] :

$$\sigma_t^{\ J} = \frac{N}{dV/dt} = \frac{e_n}{\sqrt{2t_{10-90\_PA}}} \frac{C_d\sqrt{t_{10-90\_PA}^2 + t_d^2}}{Q_{in}} = \frac{e_n C_d}{Q_{in}} \sqrt{\frac{t_{10-90\_PA}^2 + t_d^2}{2t_{10-90\_PA}}}$$

- Optimum value: $t_{10\text{-}90\_PA} = t_d$ (current duration)

$$\sigma_t^{\ J} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

Cd: detector capacitance
$t_{10\_10\_PA}$: rise time of the PA
t_d= drift time of the detector
e_n preamp noise density

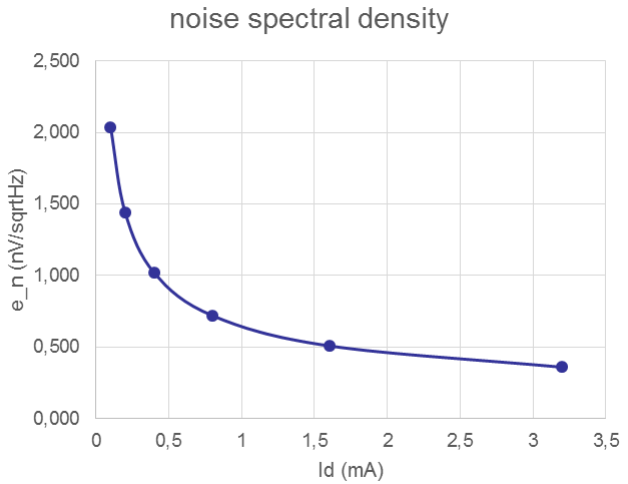


Dominated by sensor
Electronics only gives the spectral density of the input transistor e_n

- Gives ps/fC as scales with 1/Qin

- Electronics noise e_n given by the input transistor transconductance g_m:

$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_D}}$$



Examples : expectations and measurements

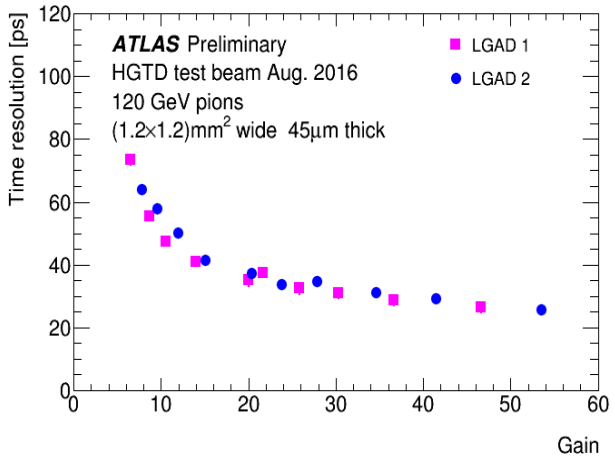
- NA62 tracker : PIN diode thickness 300 µm A=0.09 mm²
  - C_d = 0.1 pF e_n = 11 nV/√Hz t_d = 3 ns σ = 60 ps/Q(fC)
  - 1 MIP = 3 fC => σ = 20 ps/#MIP (~60-200 ps measured)

- CMS HGCAL : PIN diode thickness 300 µm A=25 mm²
  - C_d = 8 pF e_n = 1 nV/√Hz t_d = 3 ns σ = 420 ps/Q(fC)
  - 1 MIP = 3.8 fC => σ = 110 ps/#MIP (~200 ps measured)

- ATLAS HGTD : LGAD diode thickness 50 µm A= 2 mm² G = 10
  - C_d = 2 pF e_n = 2 nV/√Hz t_d = 0.5 ns σ = 50 ps/Q(fC)
  - 1 MIP = 5 fC (G=10) => σ = 10 ps/#MIP (~40 ps measured)

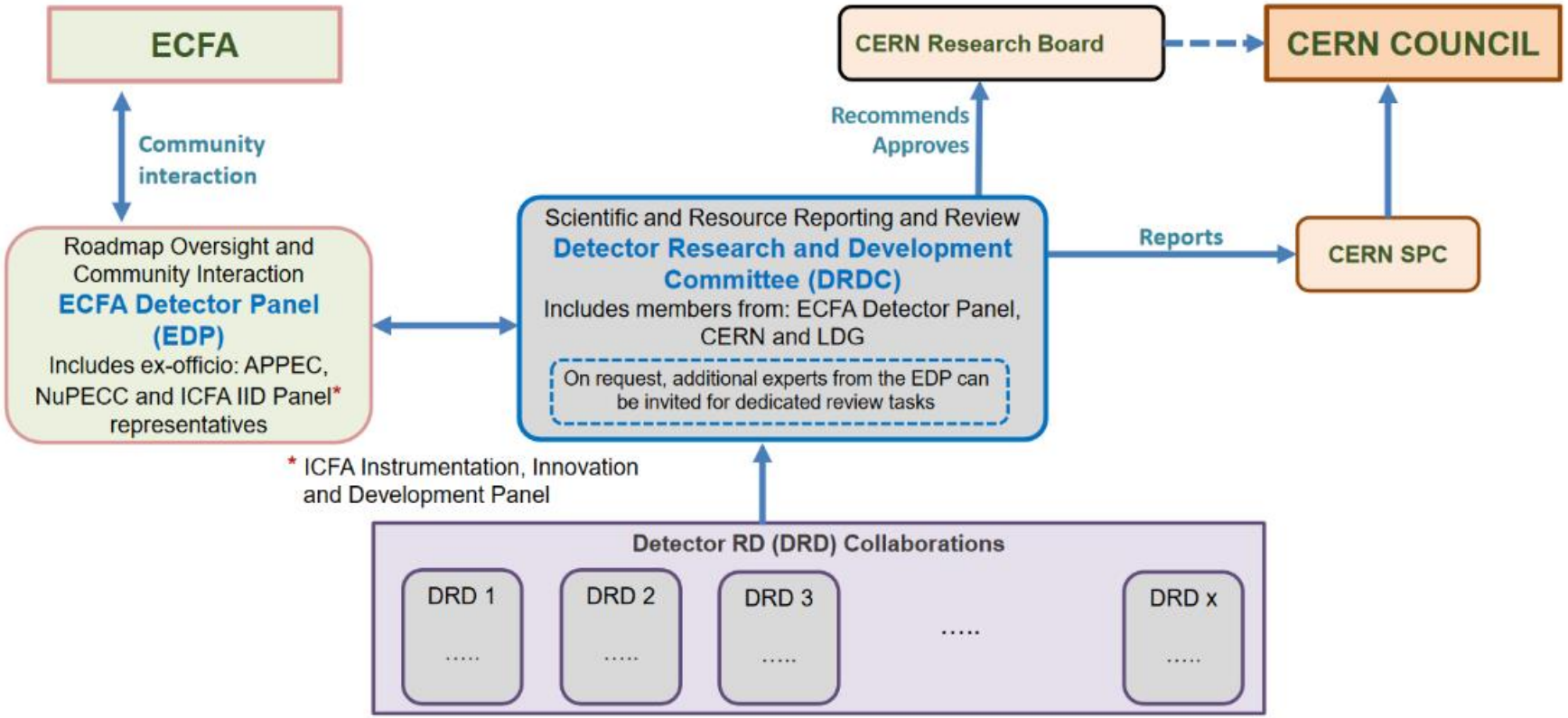
- SiPM G = 1^E6
  - C_d = 300 pF e_n = 1 nV/√Hz t_d = 100 ps σ = 3 ns/Q(fC)
  - 1 pe = 160 fC => σ = 20 ps/#pe (~60 ps measured)

$$\sigma_t^J = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$



ECFA detector R&D roadmap

- DRD1 : gas detectors
- DRD2 : liquid detectors
- DRD3 : semiconductors
- DRD4 : photon detectors
- DRD5 : quantum
- DRD6 : calorimetry
- DRD7 : electronics



DRD6 (calorimetry) readout schemes

Name	Track	Active media	readout
LAr	2	LAr	cold/warm elx"HGCROC/CALICElike ASICs"
ScintCal	3	several	SiPM
Cryogenic DBD	3	several	TES/KID/NTL
HGCC	3	Crystal	SiPM
MaxInfo	3	Crystals	SIPM
Crilin	3	PbF2	UV-SiPM
DSC	3	PBbGlass+PbW04	SiPM
ADRIANO3	3	Heavy Glass, Plastic Scint, RPC	SIPM
FiberDR	3	Scint+Cher Fibres	PMT/SiPM,timing via CAENFERS, AARDVARC-v3,DRS
SpaCal	3	scint fibres	PMT/SiPMSPIDER ASIC for timing
Radical	3	Lyso:CE, WLS	SiPM
Grainita	3	BGO, ZnWO4	SiPM
TileHCal	3	organic scnt. tiles	SiPM
GlassScintTile	1	SciGlass	SiPM
Scint-Strip	1	Scint.Strips	SiPM
T-SDHCAL	1	GRPC	pad boards
MPGD-Calo	1	muRWELL,MMegas	pad boards(FATIC ASIC/MOSAIC)
Si-W ECAL	1	Silicon sensors	direct withdedicated ASICS (SKIROCN)
Si/GaAS-W ECAL	1	Silicon/GaAS	direct withdedicated ASICS (FLAME, FLAXE)
DECAL	1	CMOS/MAPS	Sensor=ASIC
AHCAL	1	Scint. Tiles	SiPM
MODE	4	-	-
Common RO ASIC	4	-	common R/O ASIC Si/SiPM/Lar

Trends for calorimeter readout

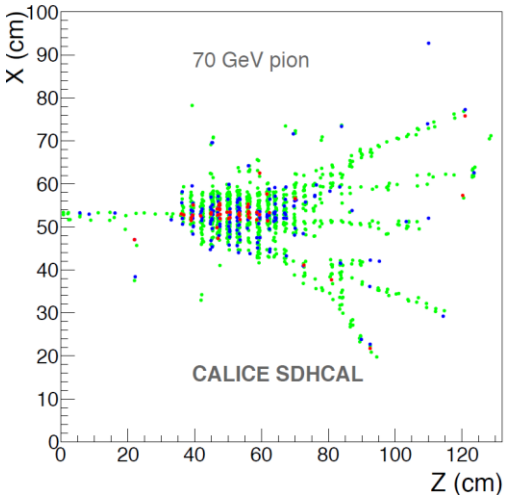
- On-detector embedded electronics, low-power multi-channel ASICs
  - CALICE SKI/SPI/HARDROC, FLAME, CMS HGCROC, FCC LAr, FATIC…
  - Challenges : #channels, low power, digital noise, data reduction
- Off-detector electronics : fiber/crystal readout
  - Wavefrom samplers : DRS, Nalu AARD, LHCb spider…
  - Challenges : low power, data reduction
- Digital calorimetry : MAPs, RPCs…
  - DECAL, ALICE FOCAL, CALICE SDHCAL
  - MAPS for em CAL : eg ALPIDE ASIC for FOCAL, DECAL…
  - Challenges : #channels, low power, data reduction

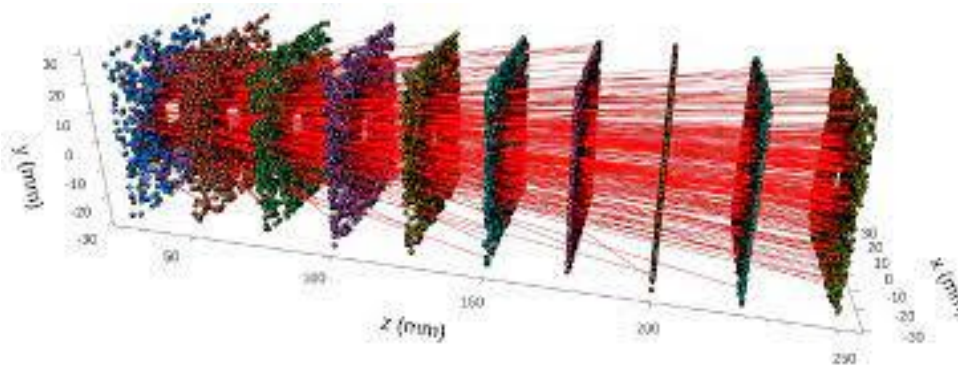
Digital calorimetry

- Hadronic : e.g. CALICE RPCs or µmegas
  - ~1 cm² pixels, low occupancy, ~1 mW/cm² (unpulsed)
  - Performance improvement with semi-digital architecture
  - Timing capability can be added

- Electromagnetic : e.g. DECAL, ALICE FOCAL…
  - Based on ALPIDE : (30µm)² pixels, high occupancy, ~ 100 mW/cm², slow
  - To be compared with embedded electronics ~10 mW/cm²
  - Most power in digital processing => would benefit a lot from ≤ 28 nm node
  - Semi-digital and/or larger pixels couldl be an interesting study

- Upcoming R&D
  - Power reduction, dead area minimization
  - Coping with high occupancy, managing data bandwidth



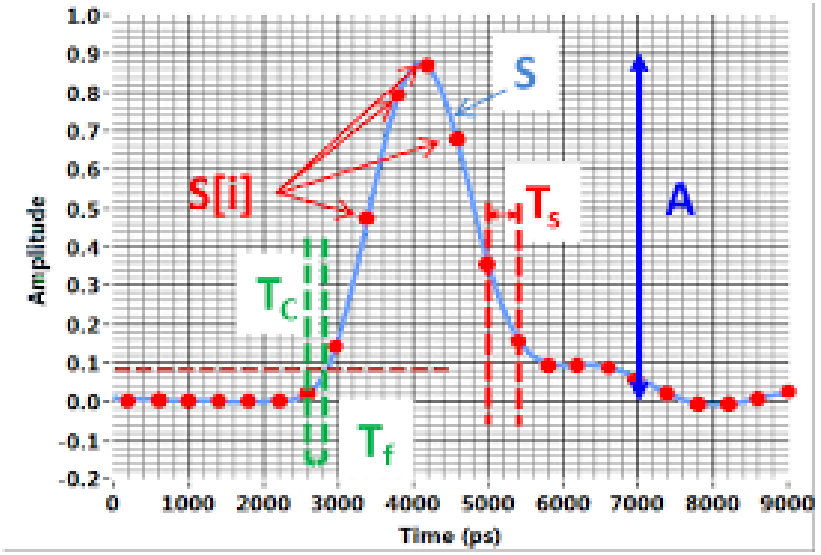


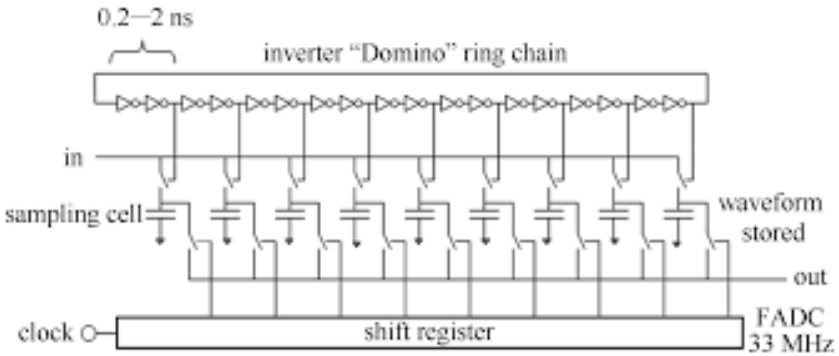
Waveform sampling

- Switched capacitor arrays (DRS4, Nalu, SPIDER…)
  - Pulse shape analysis
  - High accurcay timing, digital CFD
  - Sizeable power to provide GHz BW on large capacitance
  - large data volume

- Often used in off-detector electronics
  - Space and cooling available
  - Small/medium size detector readout and/or characterization
  - See LHCb calorimeter upgrade

- Upcoming R&D
  - Power reduction, Front-end integration
  - Data bandwitdth
  - Time walk correction, potentially best for ps accuracy

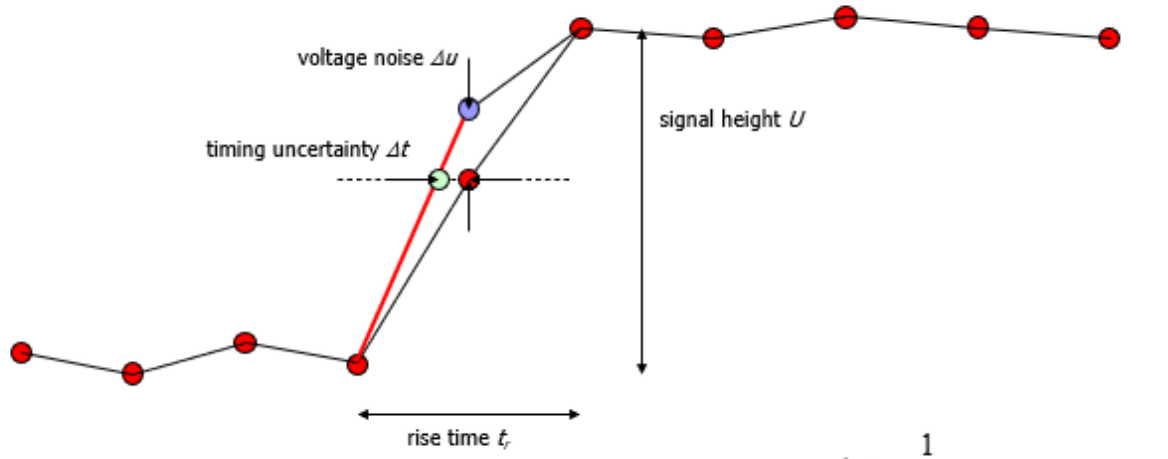




Timing resolution

- Depends on sampling frequency f_s
  - Currently 2-20 Gs/s
- But also on analog bandwidth
  - Currently 0.3-3 GHz
  - Sensitive to stray inductance
  - Needs power to drive capacitive load of SCA

How is timing resolution affected?



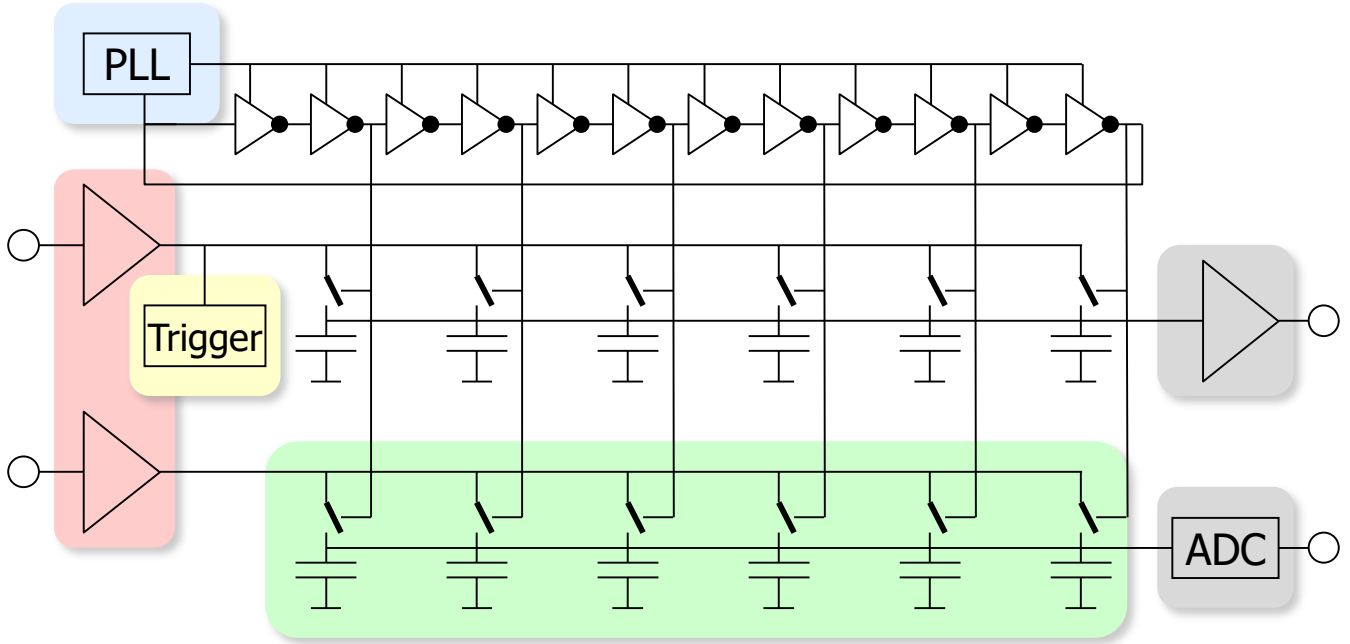
$$t_r \approx \frac{1}{3 f_{3dB}}$$

$$\Delta t = \frac{\Delta u}{U} \cdot t_r = \frac{\Delta u}{U\sqrt{n}} \cdot t_r = \frac{\Delta u}{U} \cdot \frac{t_r}{\sqrt{t_r \cdot f_s}} = \frac{\Delta u}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_s}} = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

	U	Δu	f_s	f_{3db}	Δt
today:	100 mV	1 mV	2 GSPS	300 MHz	~10 ps
optimized SNR:	1 V	1 mV	2 GSPS	300 MHz	1 ps
next generation:	1V	1 mV	10 GSPS	3 GHz	0.1 ps

Design Options

- CMOS process (typically 0.35 … 0.13 μm) → sampling speed
- Number of channels, sampling depth, differential input
- PLL for frequency stabilization
- Input buffer or passive input
- Analog output or (Wilkinson) ADC
- Internal trigger
- Exact design of sampling cell



Waveform digitizers overview

- Different
  - Speed (BW)
  - Depth

- 4 main groups :
  - PSI [S. Ritt et al.] : DRS4
  - NALU [G. Varner et al] : ASoC, HDSoC…
  - IJCLAB [D. Breton et al.] : SAMPIC
  - Chicago [ ] : PSEC4

Project	Sampling Frequency (GHz)	Input Bandwidth (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (psec)
ASoC	3-5	0.8	16,000	4	35
SAMPIC	3-10	2.5	64	16	10
HDSoC	1-3	0.6	2000	64	80
AARDVARC	8-14	2.5	32,000	4	10
AODS	1-2	1.0	8000	4	100
UDC	8-10	1.5-2	4000	16/32	10
PSEC4	5-17	1.6	256	6	5
PSEC5	5-40	**3.0**	**4096/64**	**9**	**1**

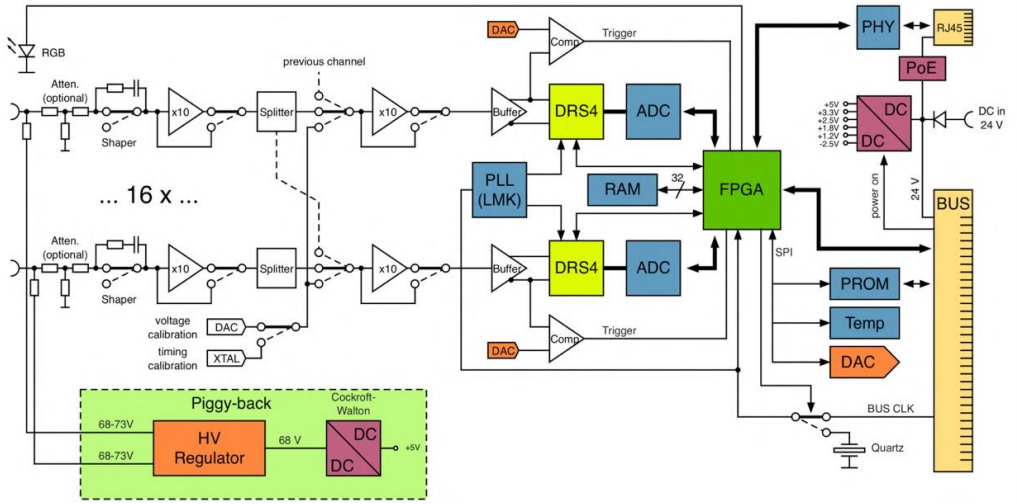
Comments

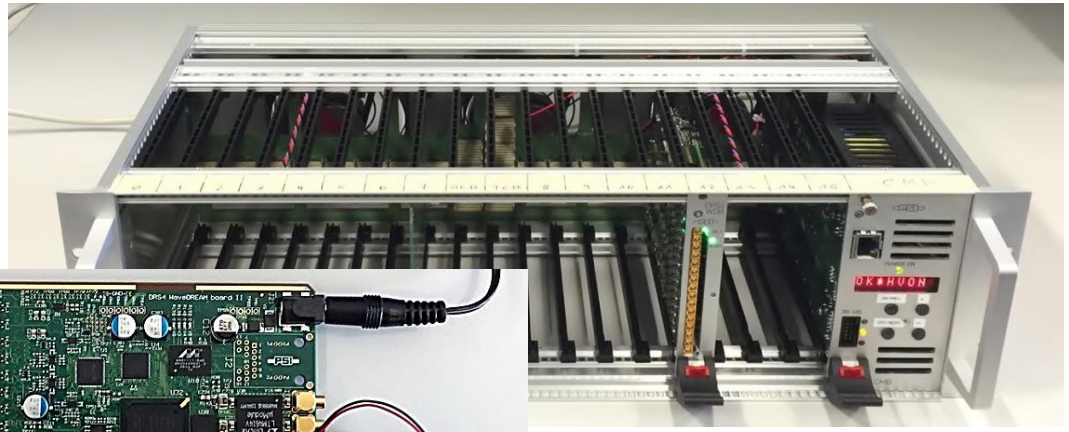
- Trends for SCAs
  - Reduce dead time
  - increase analog bandwidth
  - Increase depth, give more latency
  - Include high speed low noise preamps (NALU…)

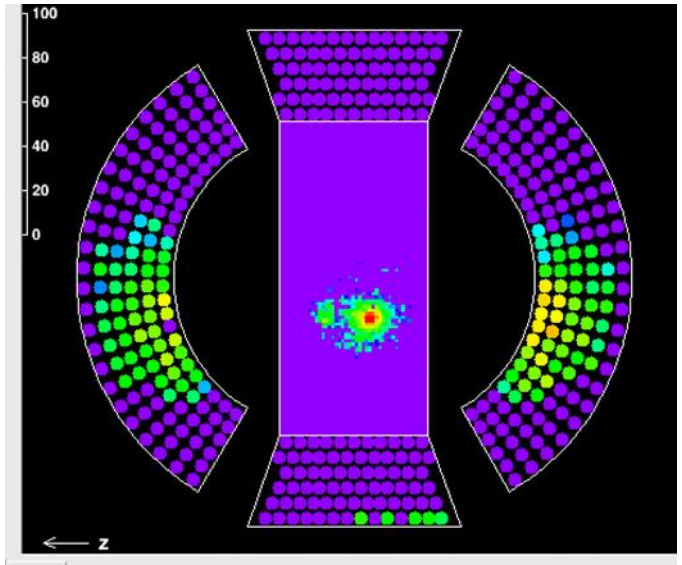
- Comments
  - Unbeatable for pulse shape analysis or discrimination or if you don’t know what you want to measure
  - Ultra low timing measurements (ps)
  - More power hungry than dedicated front-end (many CdV/dt…)
  - rarely affodable for large systems (data volume and power), still several kchannels done (eg MEG2)

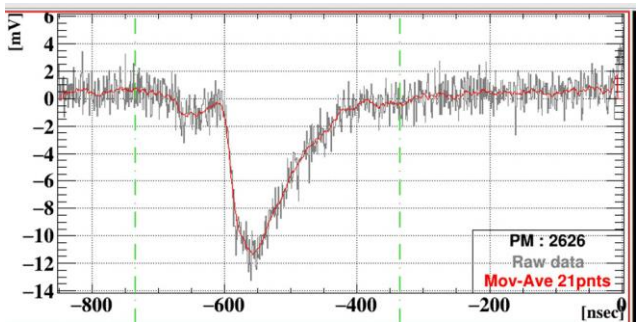
Example : MEG2 LXe calorimeter readout

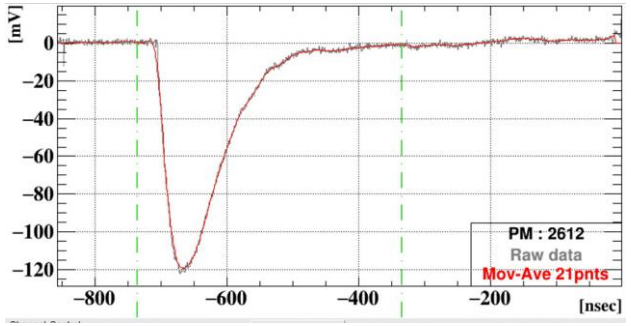
- 4k channels of SiPM readout with DRS4 waveform sampler [S. Ritt et al.]





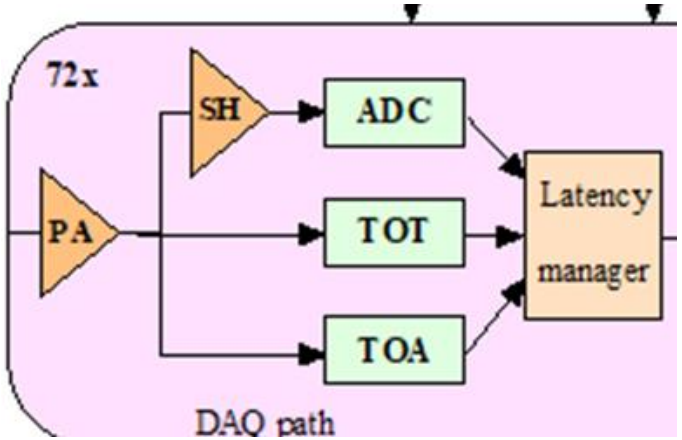




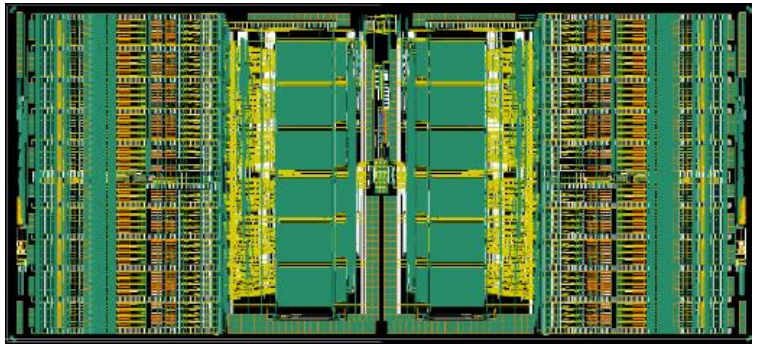


Embedded ASICs

- Pioneered with CALICE R&D (SKIROC, SPIROC..)



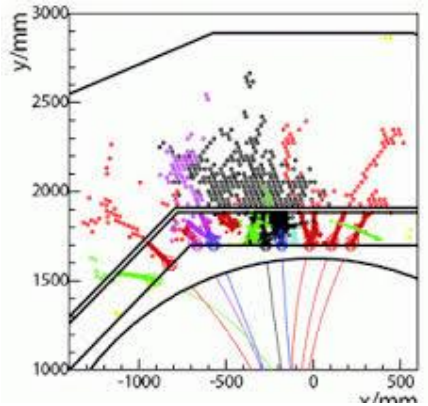
- Multi-channel charge/time readout
  - Fast preamp
    - Full dynamic range. Possible extension with ToT
  - Fast path for time measurement (ToA)
    - High speed discriminator and TDC
    - Time walk correction with ADC (or ToT)
  - Slow path for charge measurement
    - ~10 bit ADC ~40 MHz
  - Low power for on-detector implementation (~10 mW/ch) e.g. CMS HGCAL



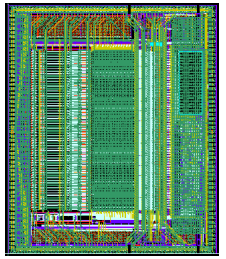
- Upcoming R&D
  - Power reduction,
  - Auto-trigger, Data-driven readout

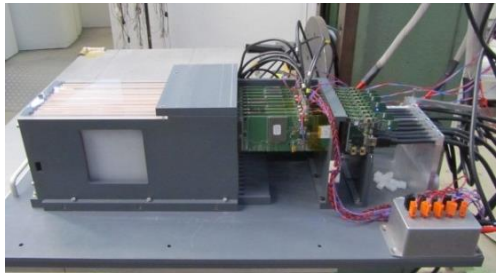
CALICE technological prototypes

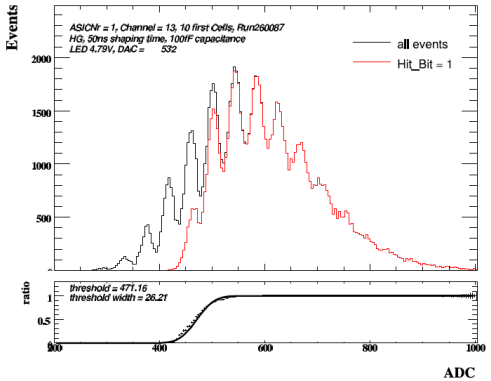
- R&D on imaging calorimetry (2004-2024)
  - Particle Flow Algorithms *[Brient, Videau et al.]*
  - Electronics crucial (low noise, low power, fully integrated)
  - Several innovative features (power pulsing, SiPM…)
  - Validation of technological prototypes
  - Common R/O features
  - Applied to CMS HGCAL



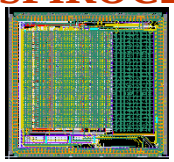
SKIROC2



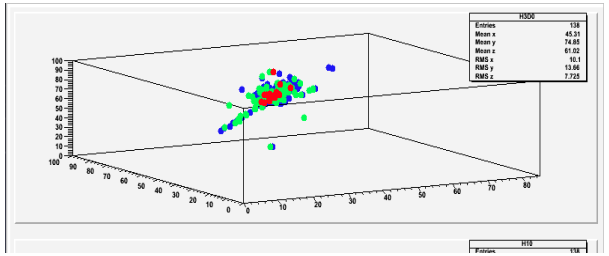




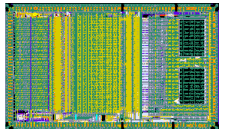
SPIROC2



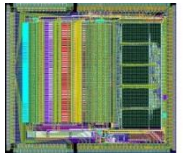
AIDA



HARDROC2



MICROROC



HGCROC (CMS HGCAL)

Overall chip divided in two symmetrical parts

- Each half is made of:
  - 39 channels: 36 channels, 2 common-mode, 1 calibration
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

Measurements

- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.16 fC binning. TOT: 2.5 fC binning
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows

- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links (CLPS)
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links (CLPS)

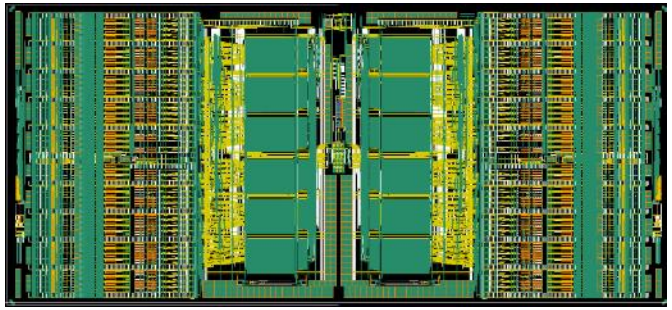
Control

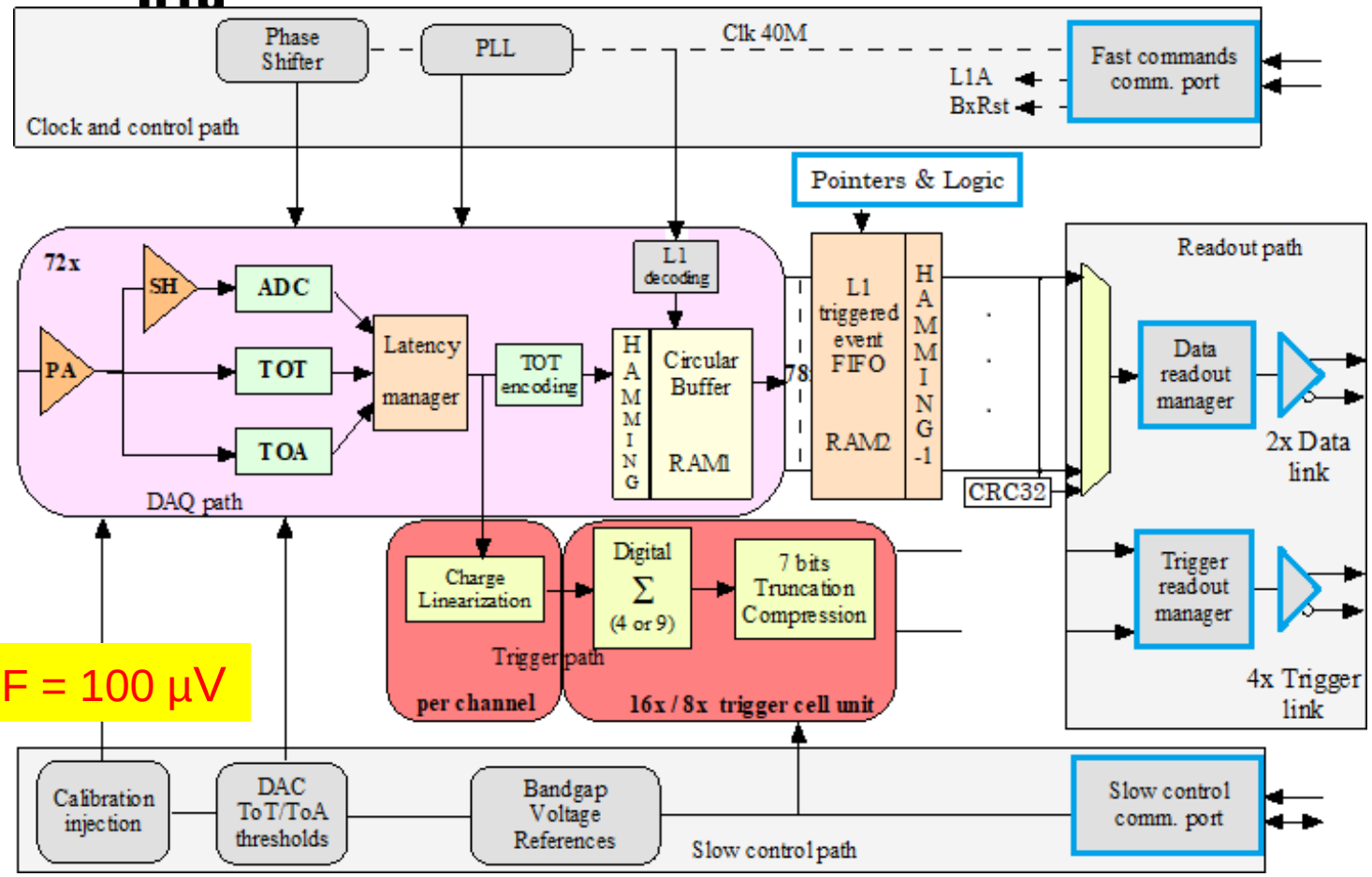
- Fast commands
  - 320 MHz clock and 320 MHz commands
  - A 40 MHz extracted, 5 implemented fast commands
- I2C protocol for slow control

Ancillary blocks

- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain

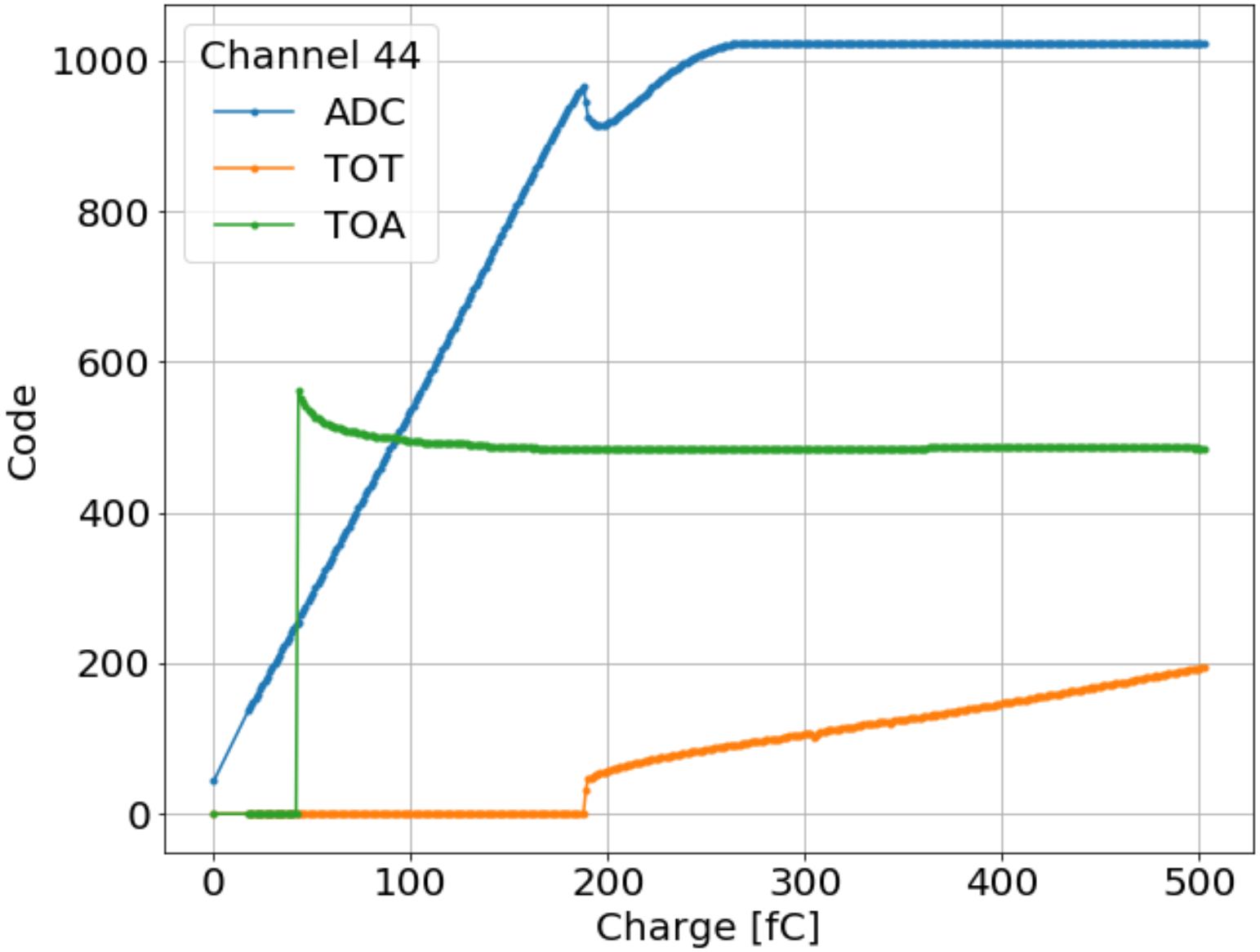
$Q_{MIP}/Cd \sim 3\ fC/30\ pF = 100\ \mu V$



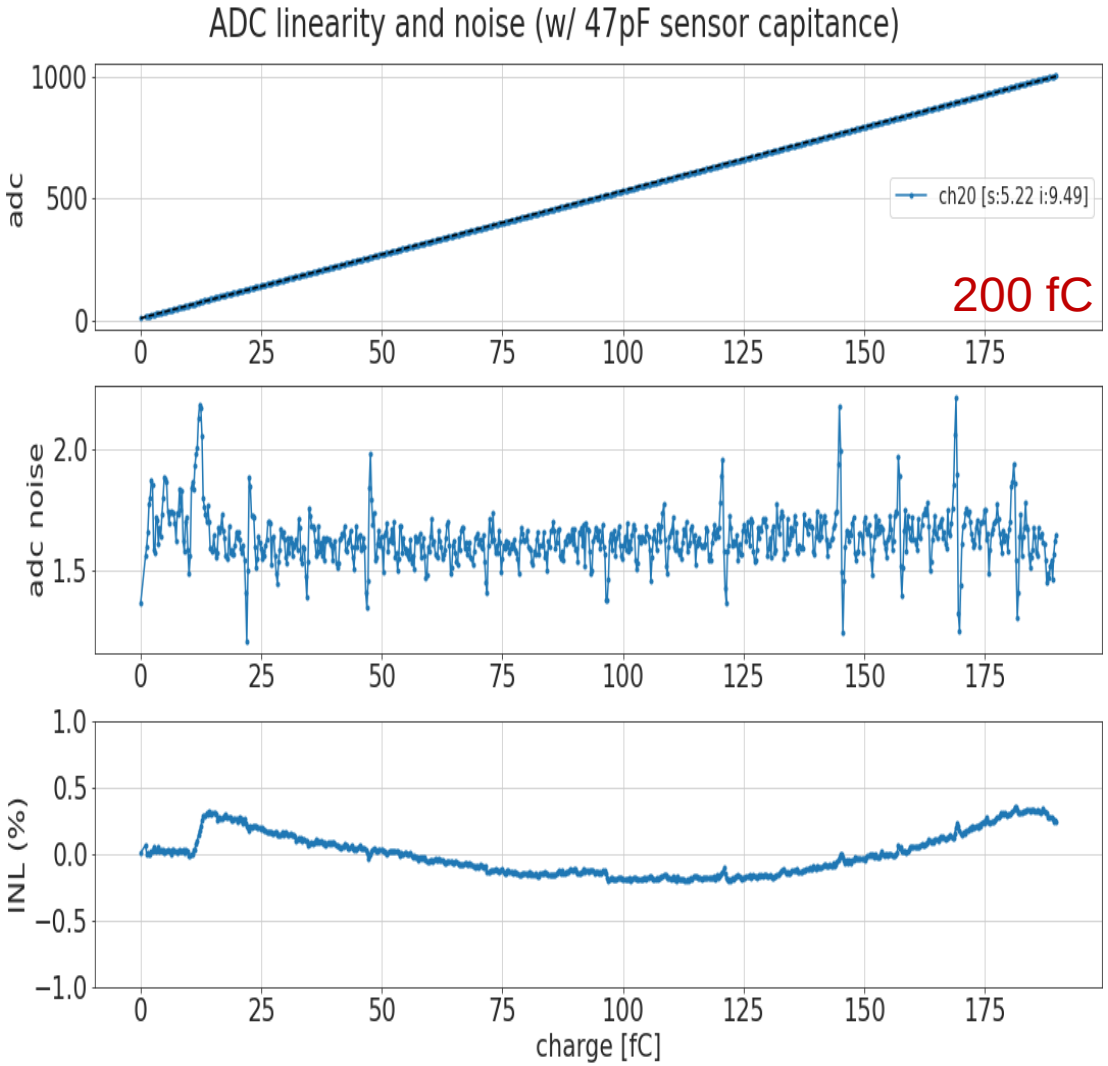


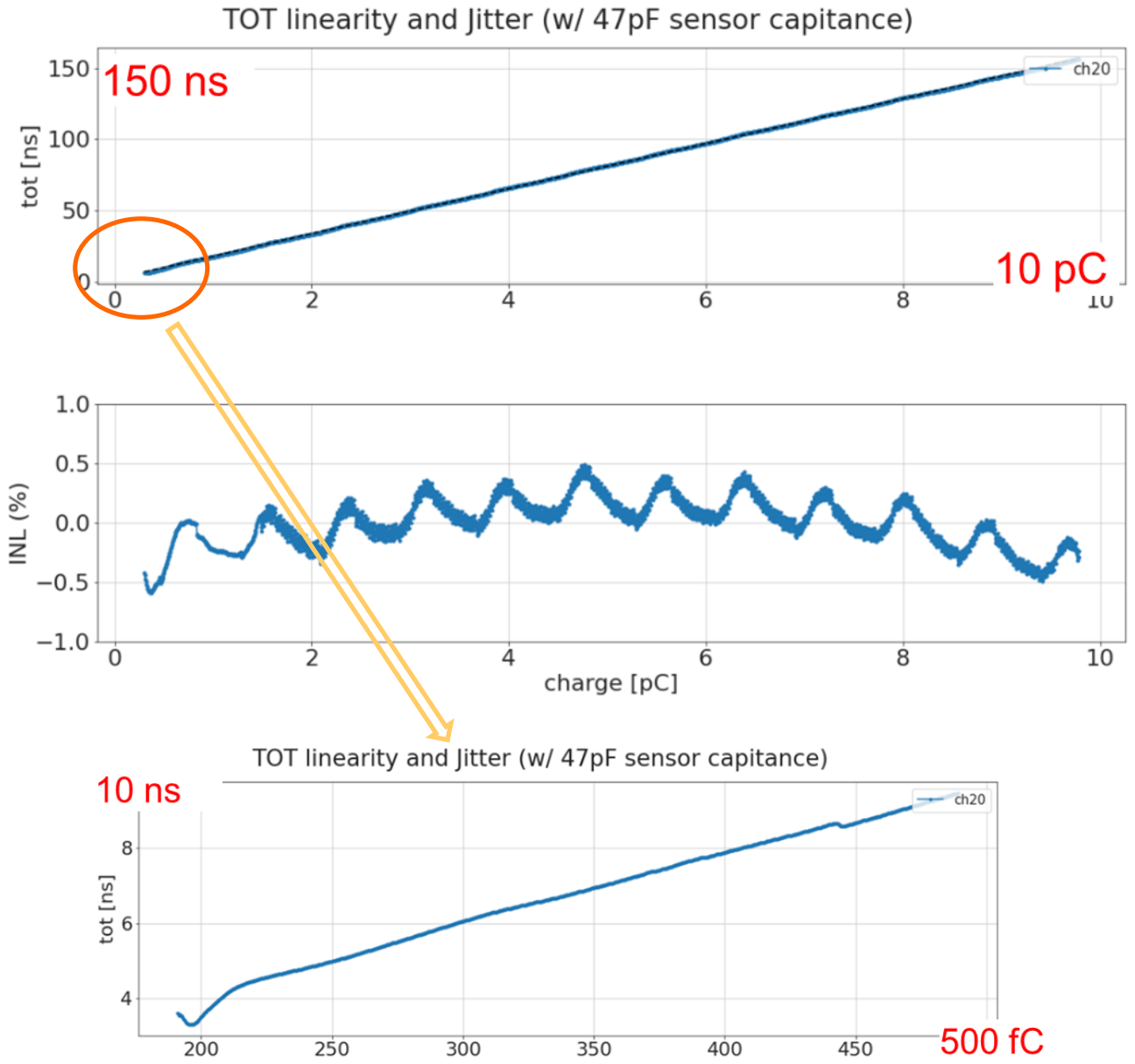
Handling the dynamic range : ADC and TOT

- ADC range 0 - 200 fC
- TOT range 200 fC - 10 pC
- Non-linear inter-region
- But 200 ns dead time



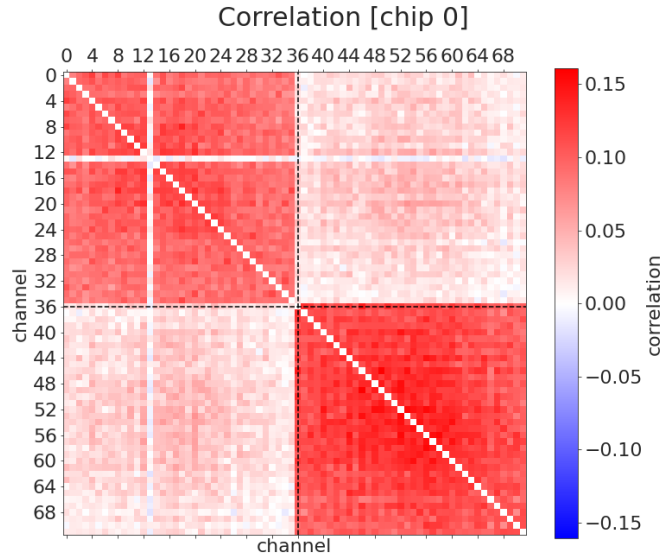
Performance : charge measurement



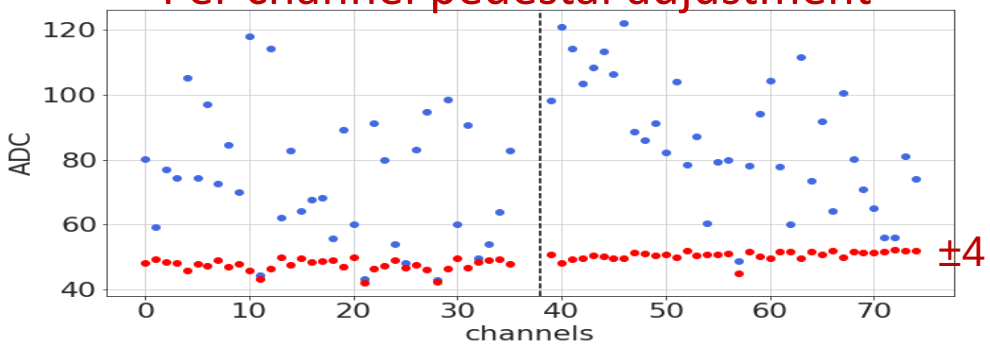


HGCROC3: Noise and pedestal measurements

- Measured noise with 47 pF input cap = 0.3 fC (~ 2000 e-) (0.7 nV / √Hz)
- Very low correlated noise contribution: max 15%
  - Comparable with HGCROC2 even if the digital activity was doubled
- ADC pedestal adjustment done manually with local 6b DAC

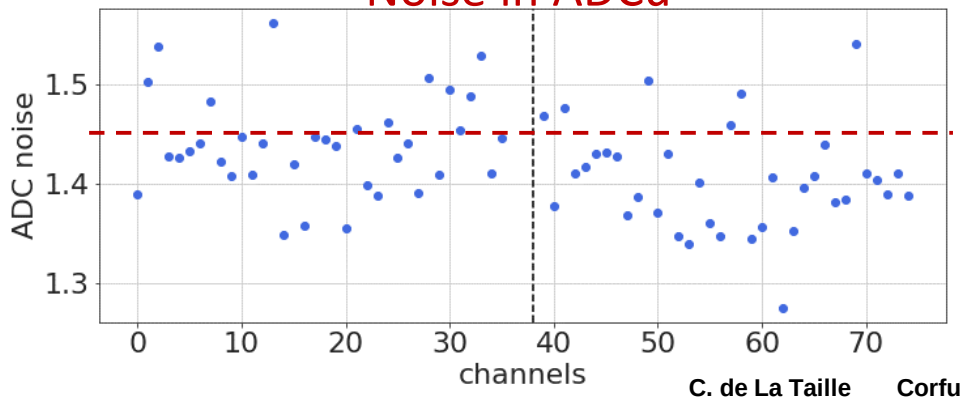


Per channel pedestal adjustment



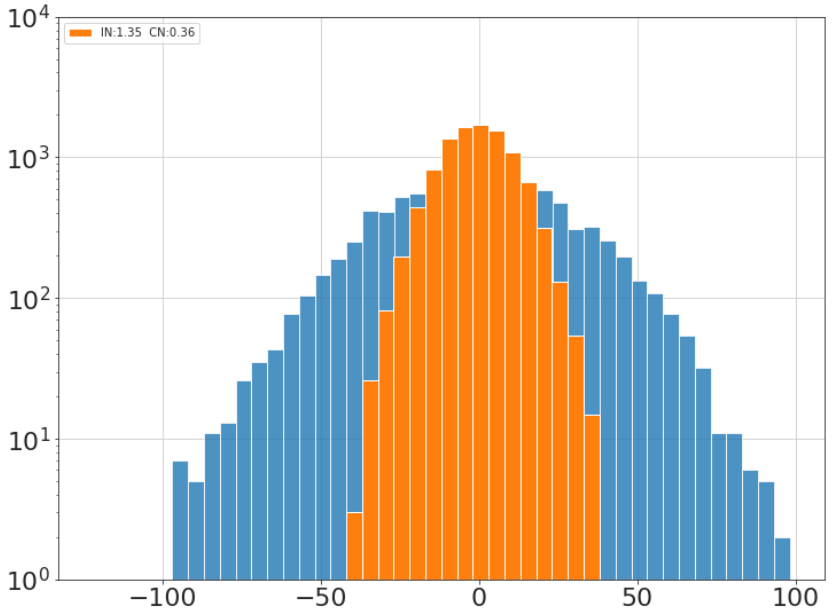
±4 ADCu

Noise in ADCu



~0.3 fC

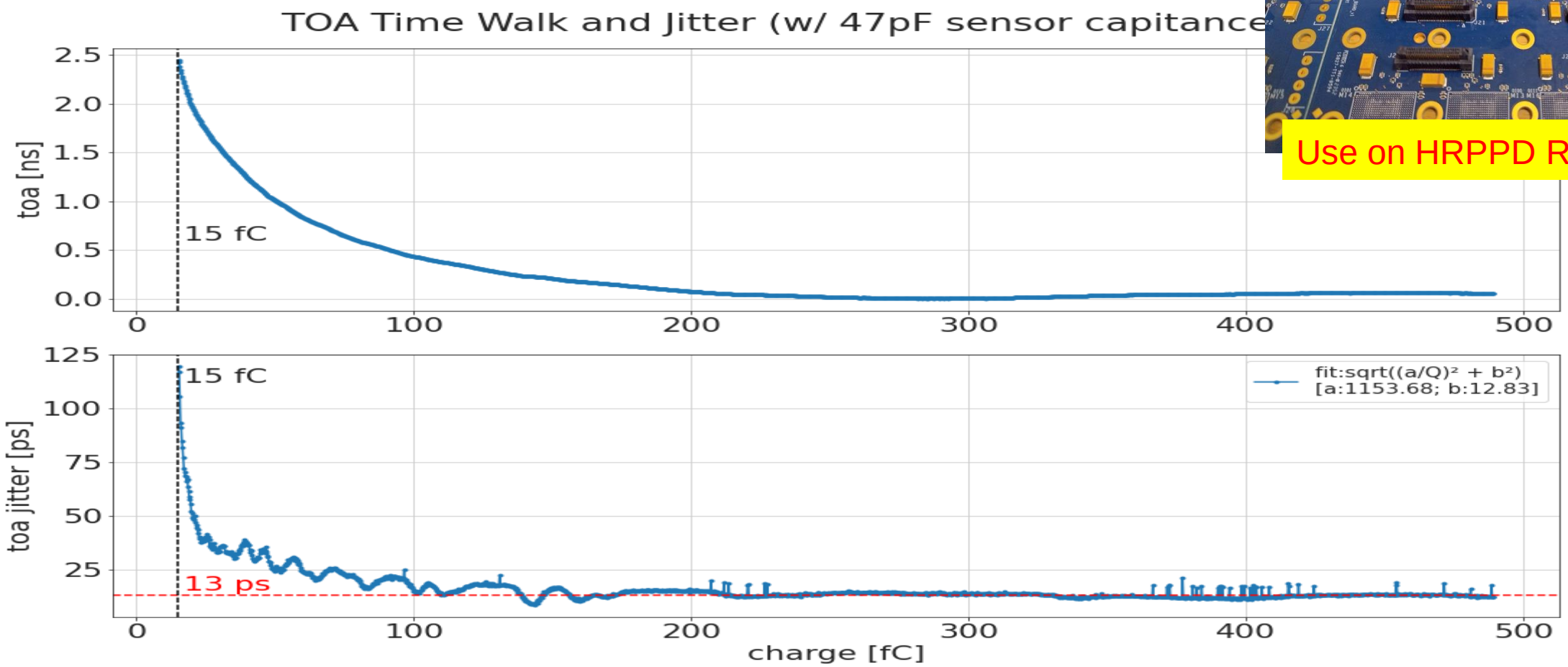
Full chip (72 channels)



Zoom on timing

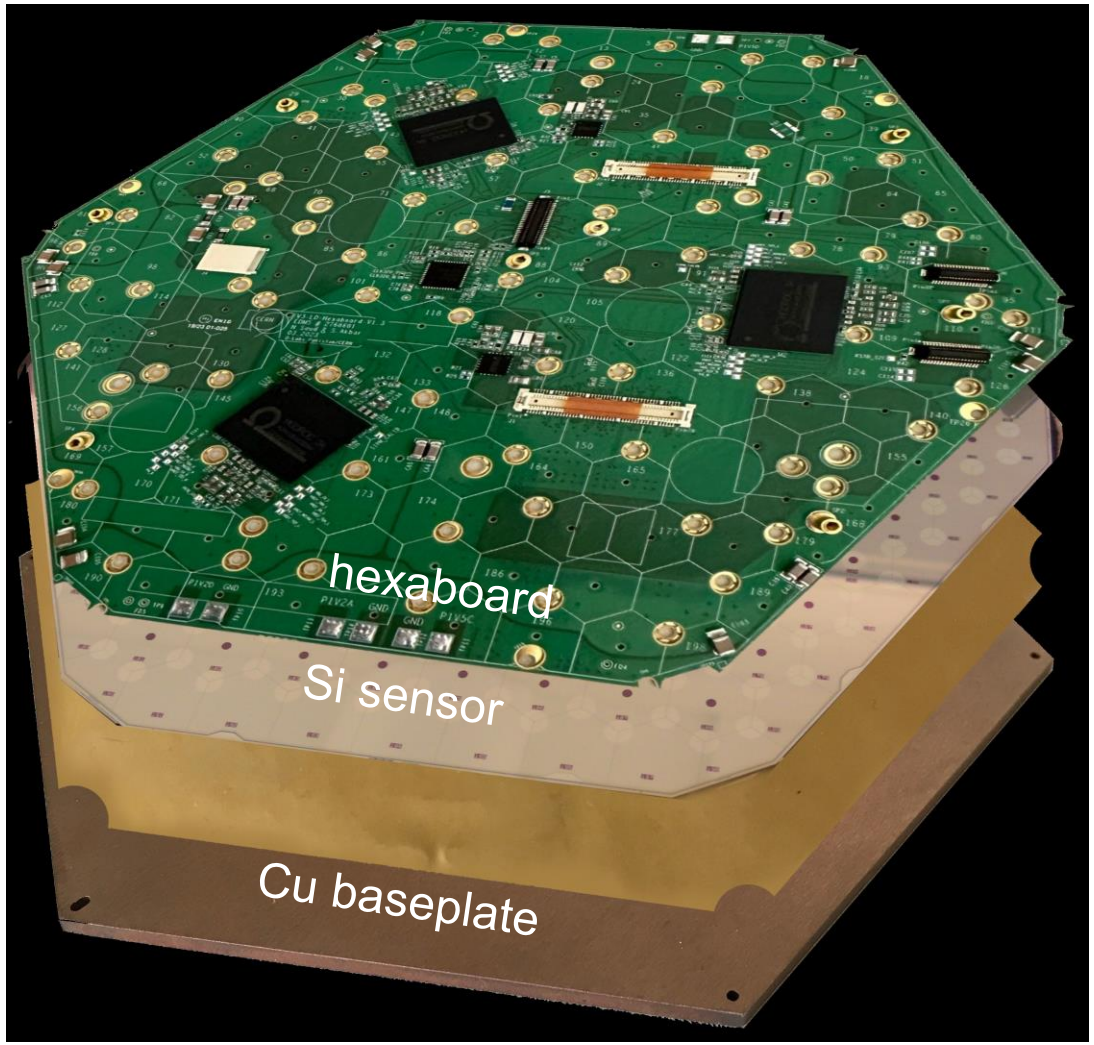
- ~2.5 ns time walk, 13 ps jitter for Q>100fC at Cd = 47 pF
- Fits also well MCPs for PID @EIC (HRPPD)

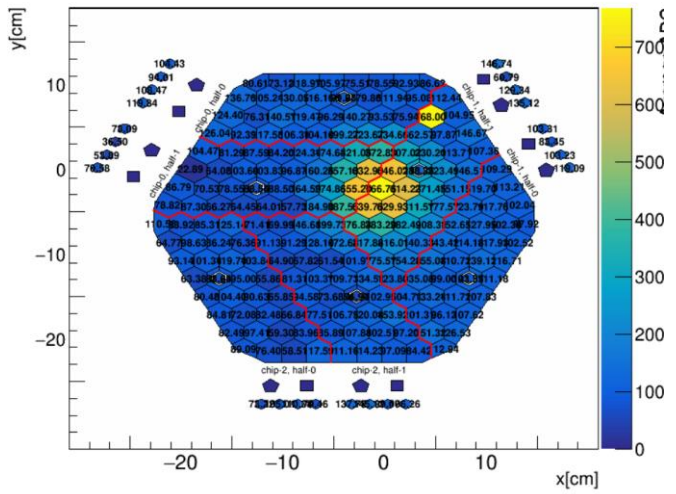
Use on HRPPD RICH @EIC

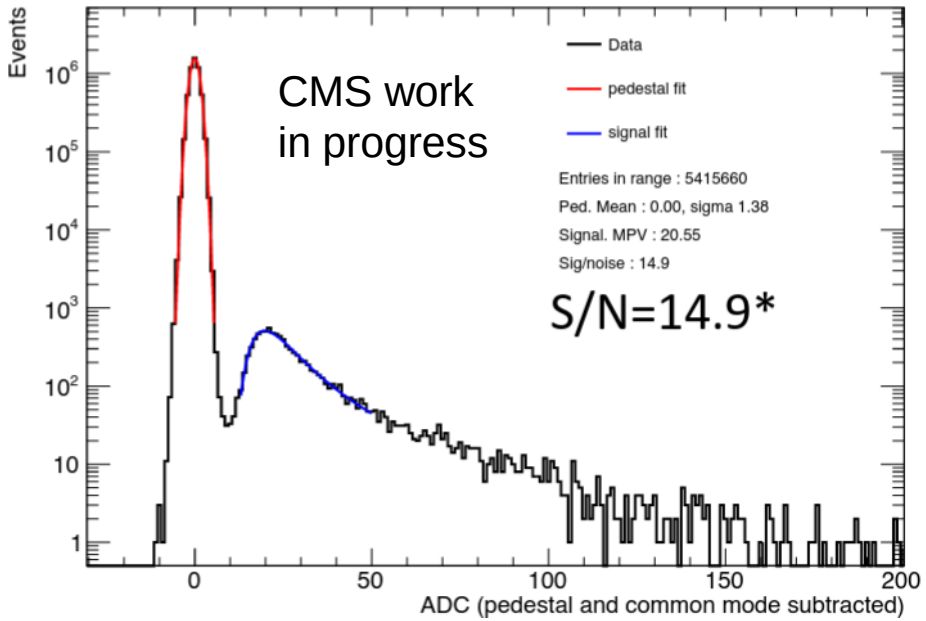


HGCAL modules

- Good performance in test beam

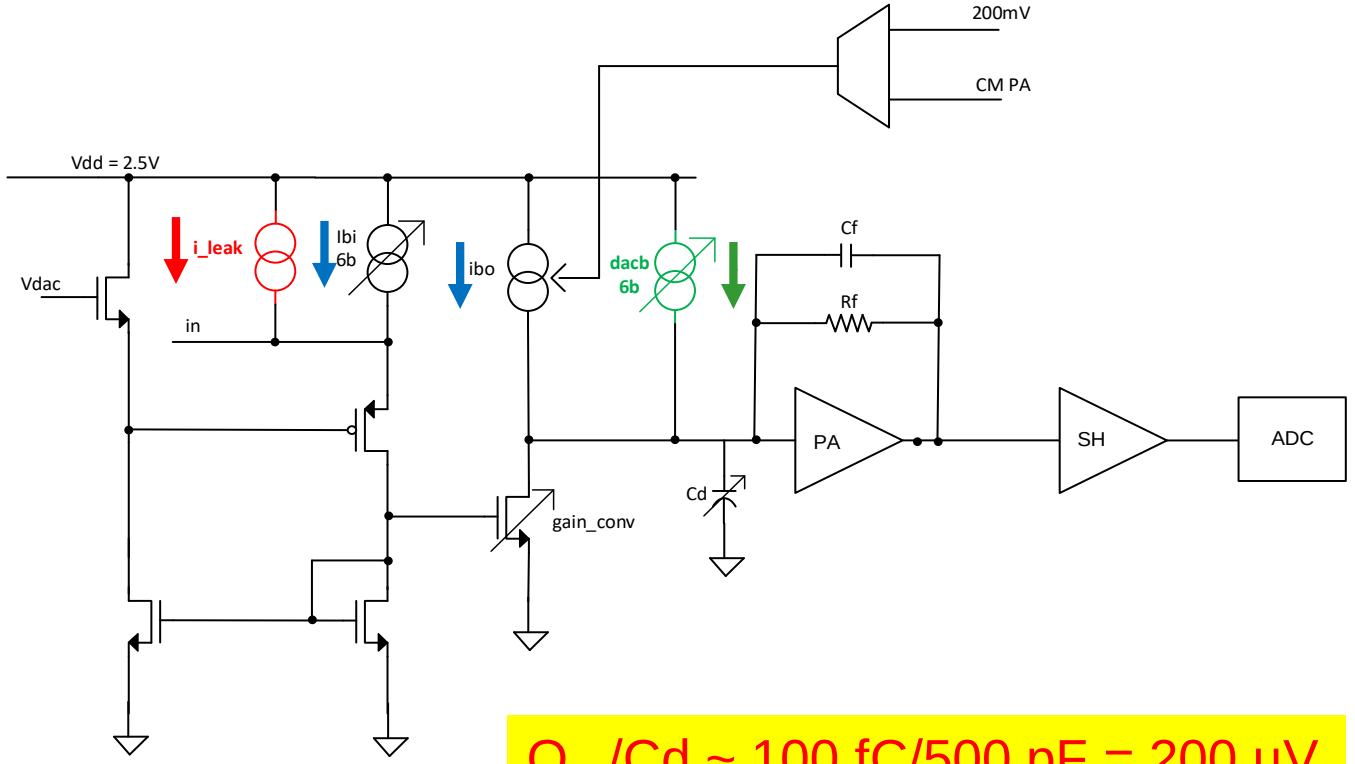




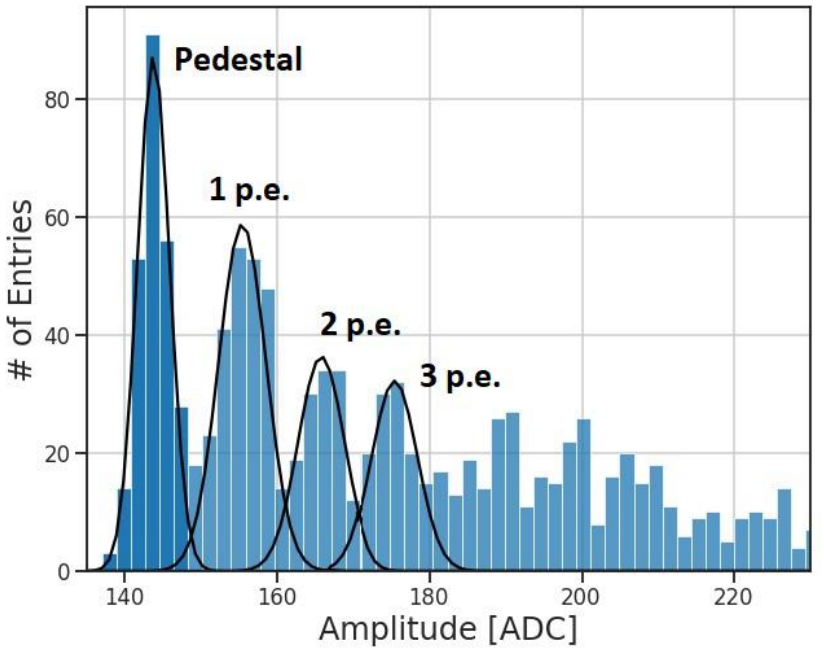


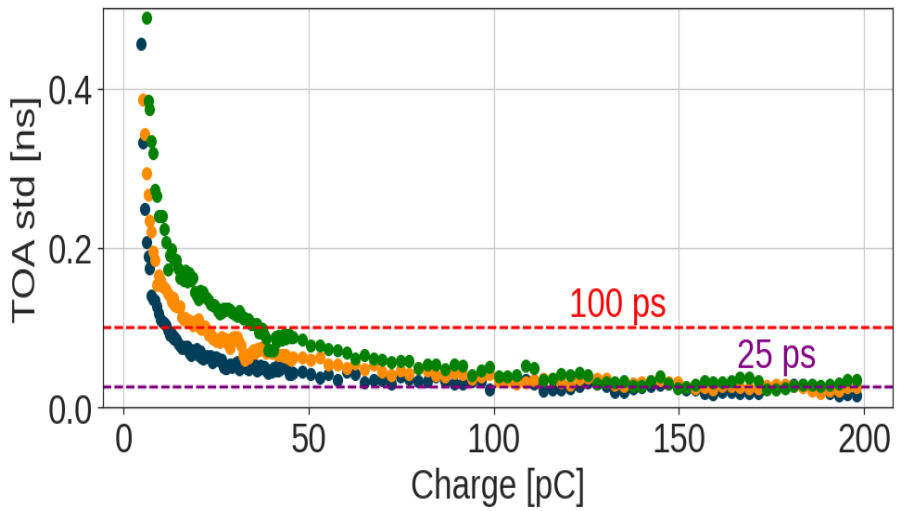
H2GCROC: SiPM version current conveyor

- **Current conveyor (Heidelberg design) to adapt to Si version**
- **Dynamic range : 50 fC – 300 pC**
- **2 typical gains**
  - Low gain (Physics mode): **44 fC/ADC gain, 50 fC noise (1.25 ADCu)**
  - High gain (Calibration mode): **10 fC/ADC gain, 20 fC noise (2 ADCu)**
- **Measurements in backup slides**



Q_{pe}/Cd ~ 100 fC/500 pF = 200 µV





Evolution of embedded calorimeter readout chips

- Further reduction in power dissipation
- Auto-trigger and data-driven readout
- More SiPM readout
- Addressed in DRD6 proposal

DRD6 Common readout ASICs proposal [AGH, Omega, Saclay]

- Develop readout ASIC family for DRD6 prototype characterization
  - Inspired from CALICE SKIROC/SPIROC/HARDROC/MICROROC family
  - Targeting future experiments as mentionned in ICFA document (EIC, FCC, ILC, CEPC…)
  - Addressing embedded electronics and detector/electronics coexistence + joint optimization
  - Detector specific front-end but common backend

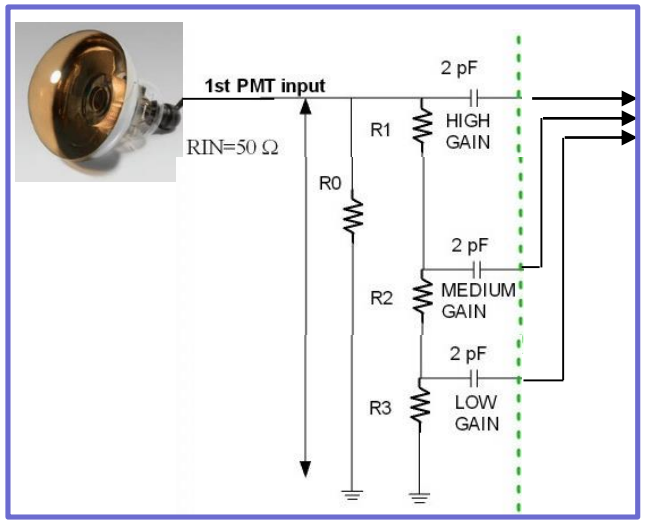
  ⇒ allows common DAQ and facilitates combined testbeam

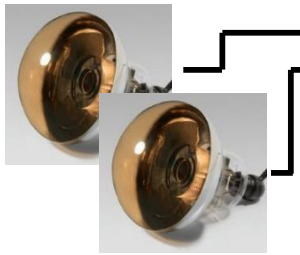
- Start from HGCROC / HKROC : Si and SiPM
  - Reduce power from 15 mW/ch to few mW/ch. Lower occupancy, slower speed
  - Allows better granularity or LAr operation
  - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
  - Extend to MCPs (PID) or HRPPD. First tests with EIC calo/PID

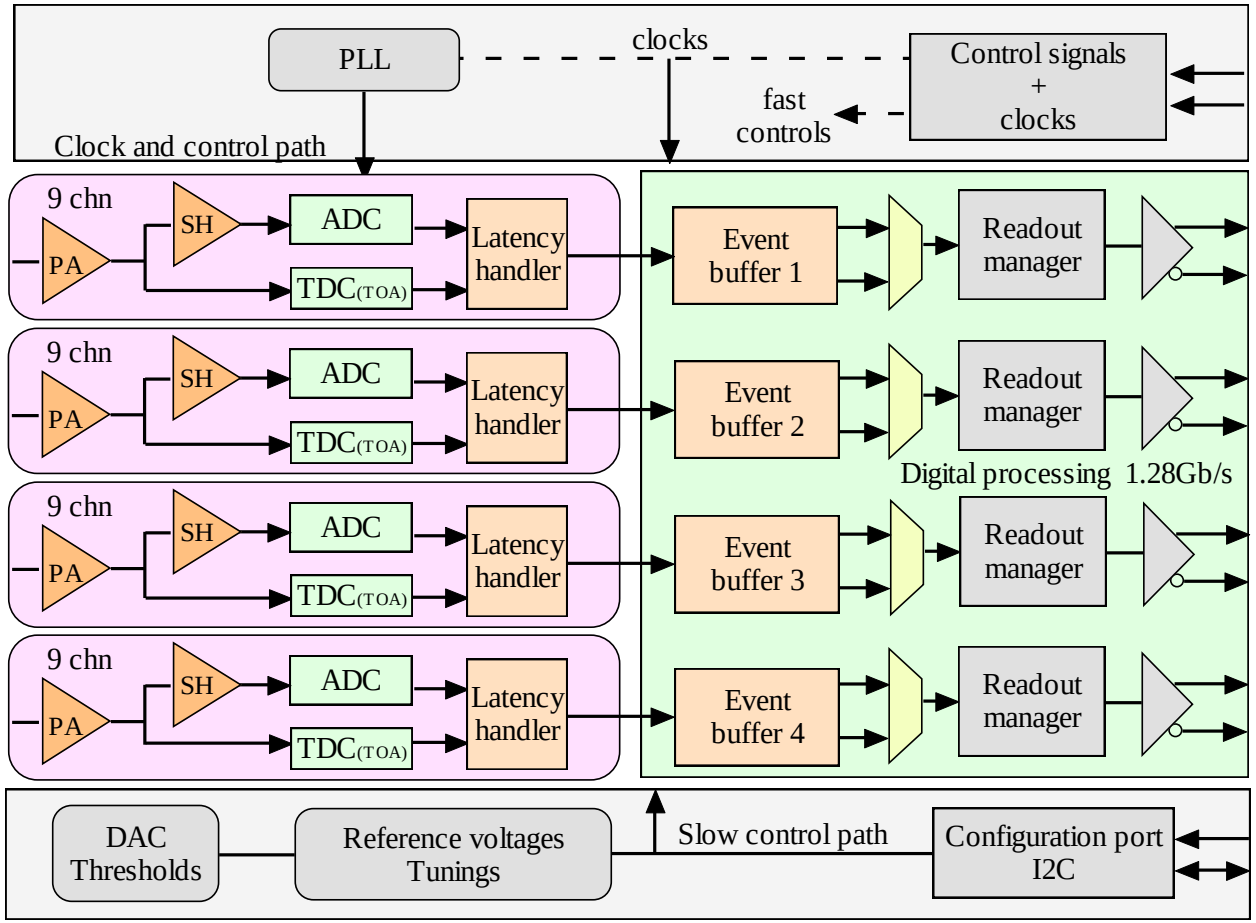
- Several other ASICs R/Os also developed in DRD6 and it is good !
  - FLAME/FLAXE, FATIC…
  - Waveform samplers : commercial or specific (e.g. SPIDER)
  - DECAL

HKROC main features

- HKROC is 36 channels: 12 PMTs with High, Medium and Low gain
  - Or 36 PMTs with one gain



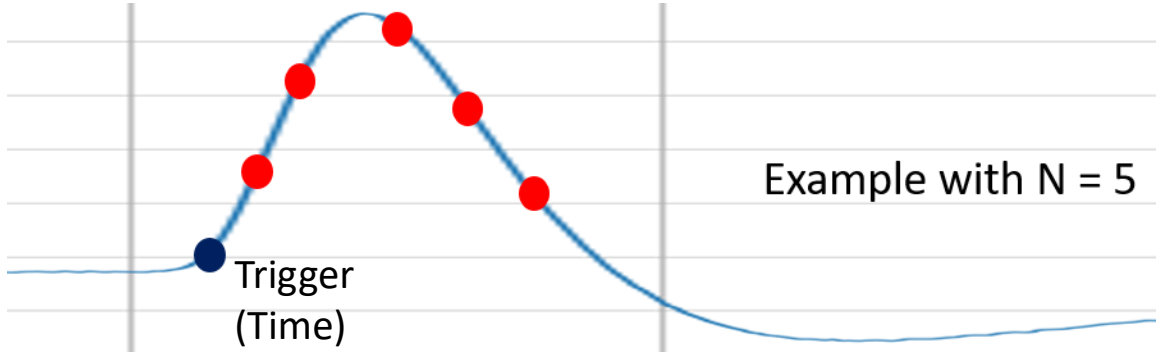




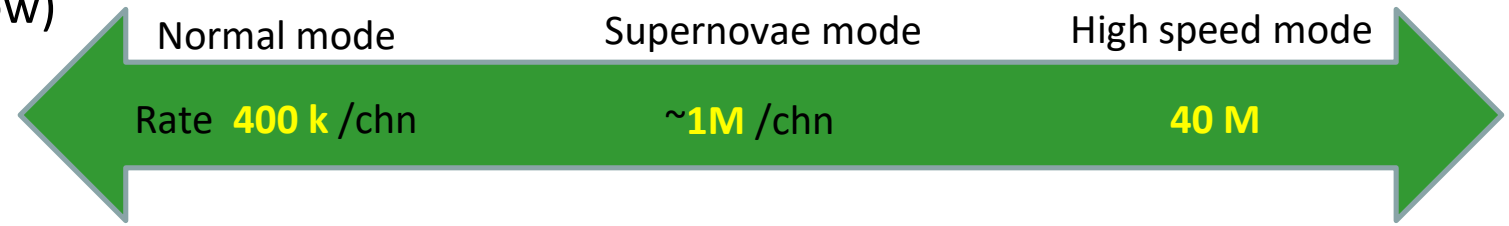
- ASIC in TSMC 130 nm node
- Low power: 10 mW per channel
- Large charge measurement with 3 gains (up to 2500 pC)
- Integrated timing measurements (25 ps binning)
- Readout with high speed links (1,28 Gb/s)
- HKROC is a waveform digitizer with auto-trigger

HKROC: (slow) waveform digitizer with TDC and auto-trigger

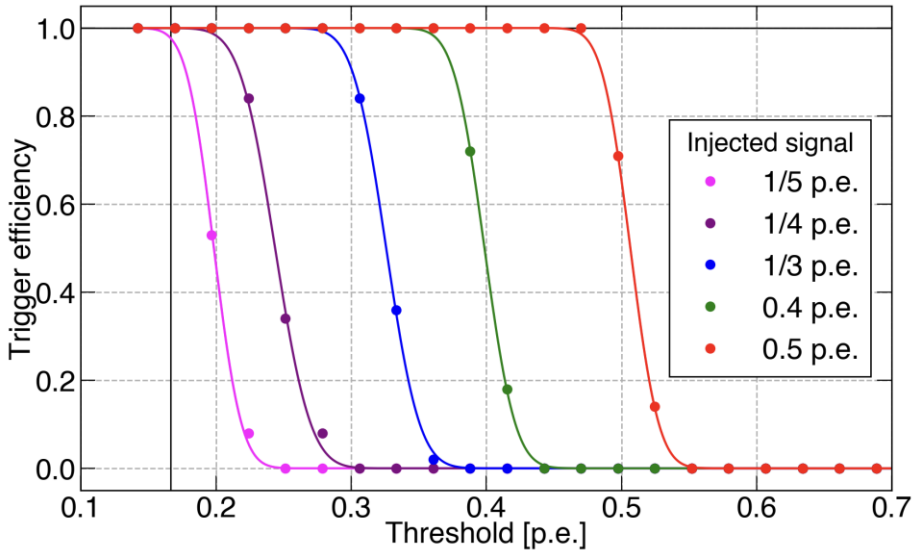
- HKROC is waveform digitizer working @ 40 MHz
  - Number of charge sampling points from 1 to 7
  - Fast channel for precise timing (25 ps binning)
  - Charge reconstruction algorithm in FPGA
    - 5% resources of a modern XILINX FPGA

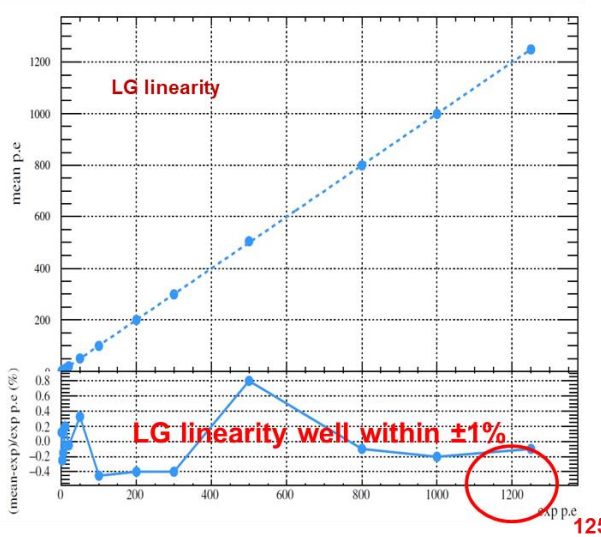


- When using 3 gains / PMT (high, medium, low)
  - Hit rate capability up to 400 kHz / PMT
  - Increased up up to 1 MHz by focusing on high gain
    - Dynamic selectable by the user
  - Average values only limited by readout speed

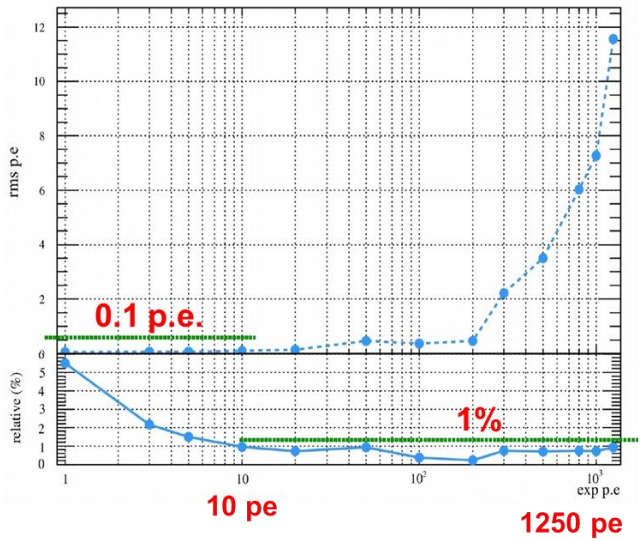


HKROC performance





1250 p.e. = 2500 pC



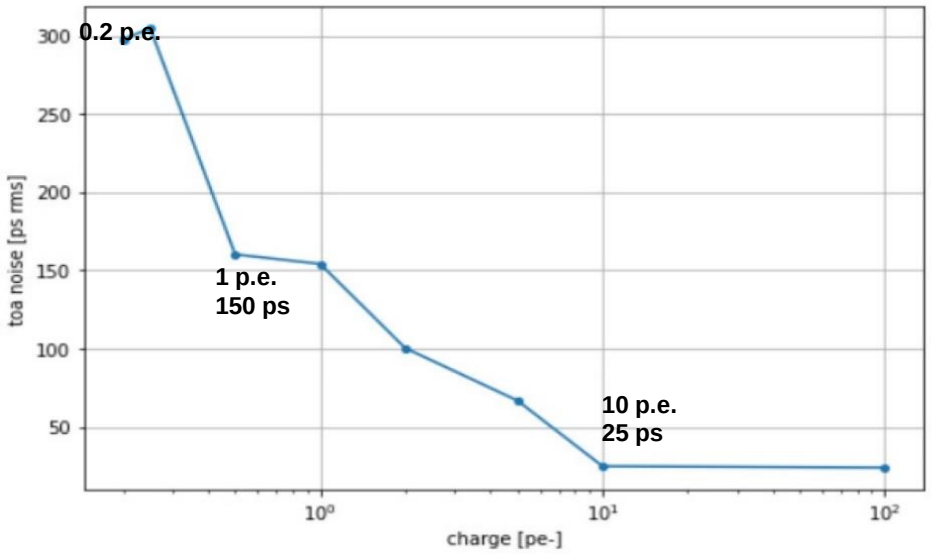
HG, MG and LG tested!!

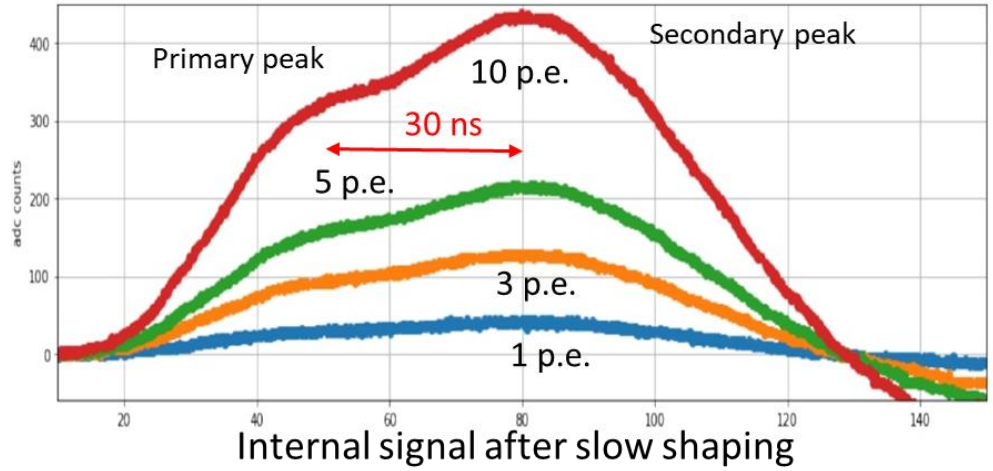
Charge linearity < **±1%** from 1 to **1250 p.e. (2500 pC)**

Charge resolution :

< **0.1 p.e (200 fC)** at ≤ 10 p.e

< 1 % otherwise



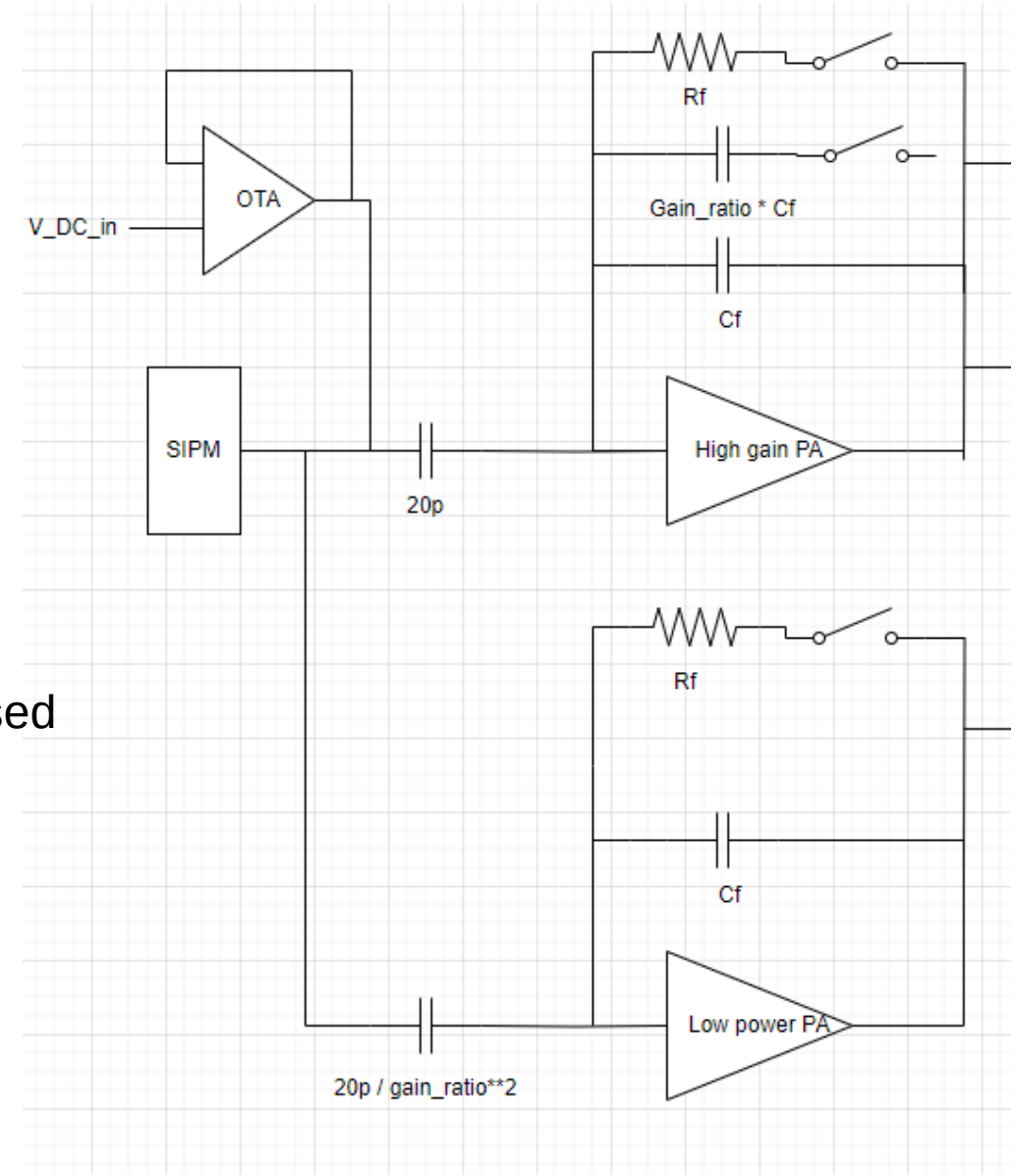


Further steps : CALOROC

- SiPM readout calorimetry : CMS H2GCROC with EIC readout (200 MHz clock and fast commands)
  - SiPM from 500 pF to 2.5 nF (or 10 nF)
  - ~5-10 mW/channel

- 2 versions : conservative and exploratory
  - Conservative : uses H2GCROC (ADC, TOT) as it is and replaces the backend
  - Exploratory : new analog part (dynamic gain switching).
  - Pin to pin compatible
  - Backend « à la HKROC » : auto-triggered, zero-suppressed
  - 40 MHz internal clocking (ADC, TDCs)

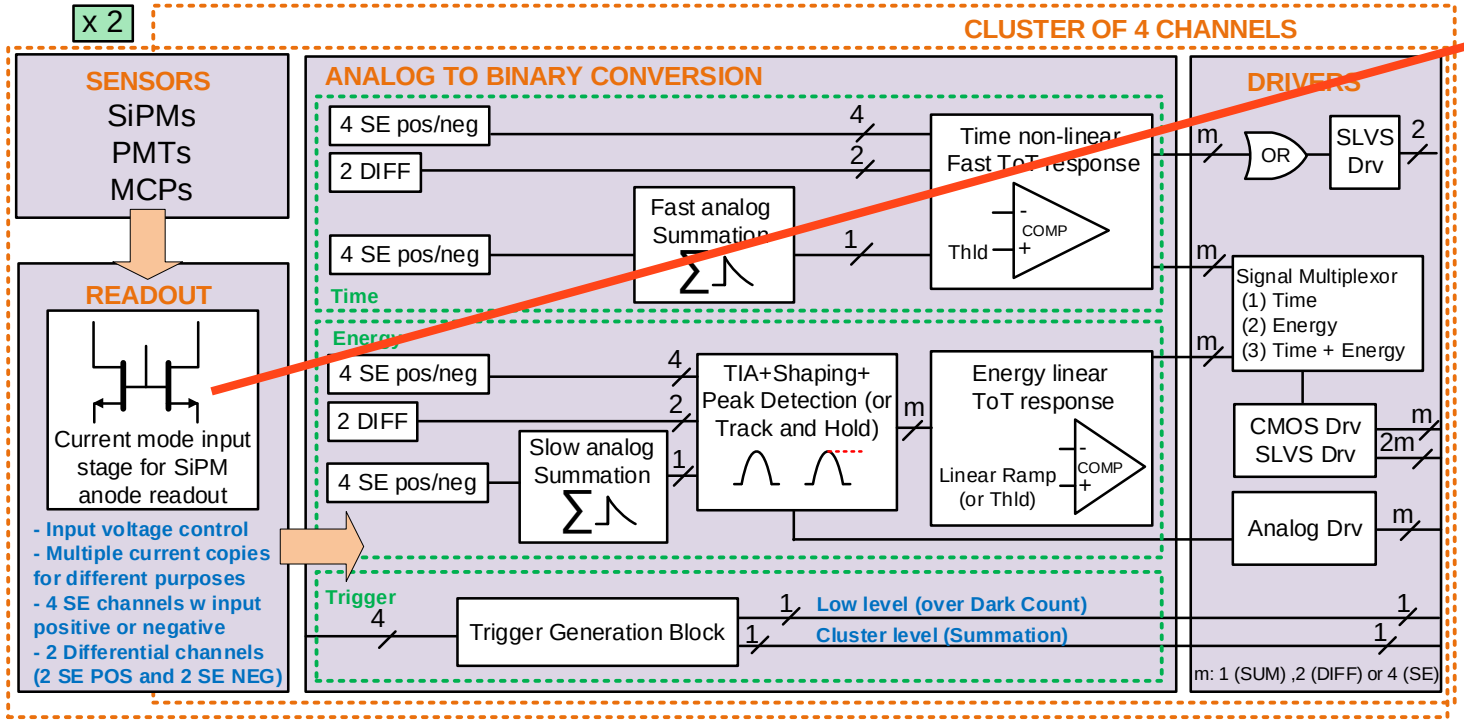
- Could fit FCC SiPM calorimeters
- A Si version would fit FCC Si calorimeter



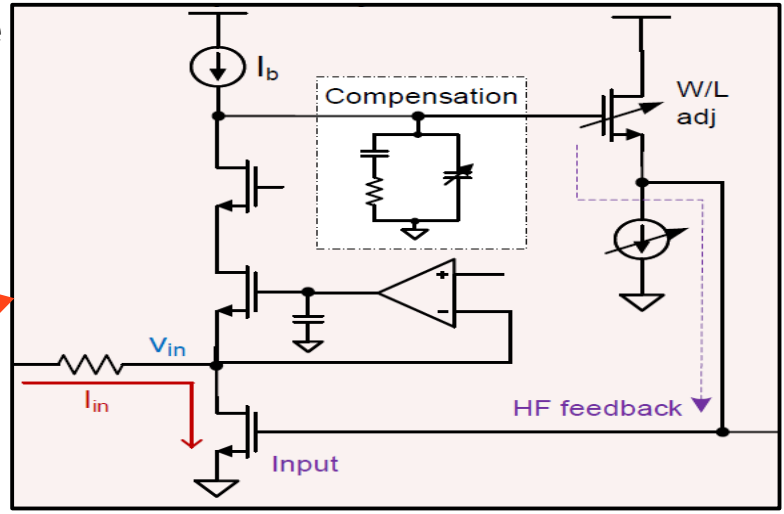
II. FastIC architecture

D. Gascon et al. (ICCUB) https://indico.cern.ch/event/1214183/contributions/5385308/attachments/2655564/4598975/20230530_FastIC_FAST23.pdf

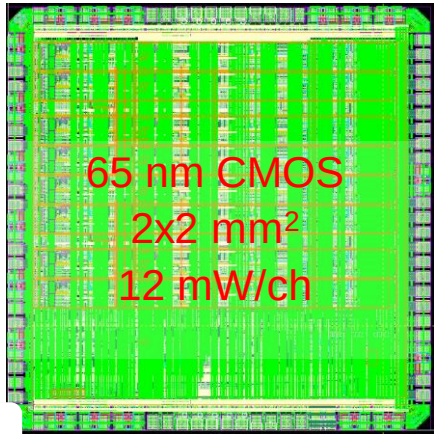
- **FASTIC** current mode ASIC.
  - **8 Inputs:** 8 Single Ended (POS/NEG), 4 differential and summation (POS/NEG) in 2 clusters of 4 channels.
  - **3 Output modes:** (1) SLVS; (2) CMOS; and (3) Analog.
  - Active analog summation of up to 4 SE channels to improve time resolution
  - **Fast current mode input stage**
  - **Current mode comparator for timing**



Input stage "amplifier" < 3 mW/ch



Based on HRFlexToT ASIC [1]

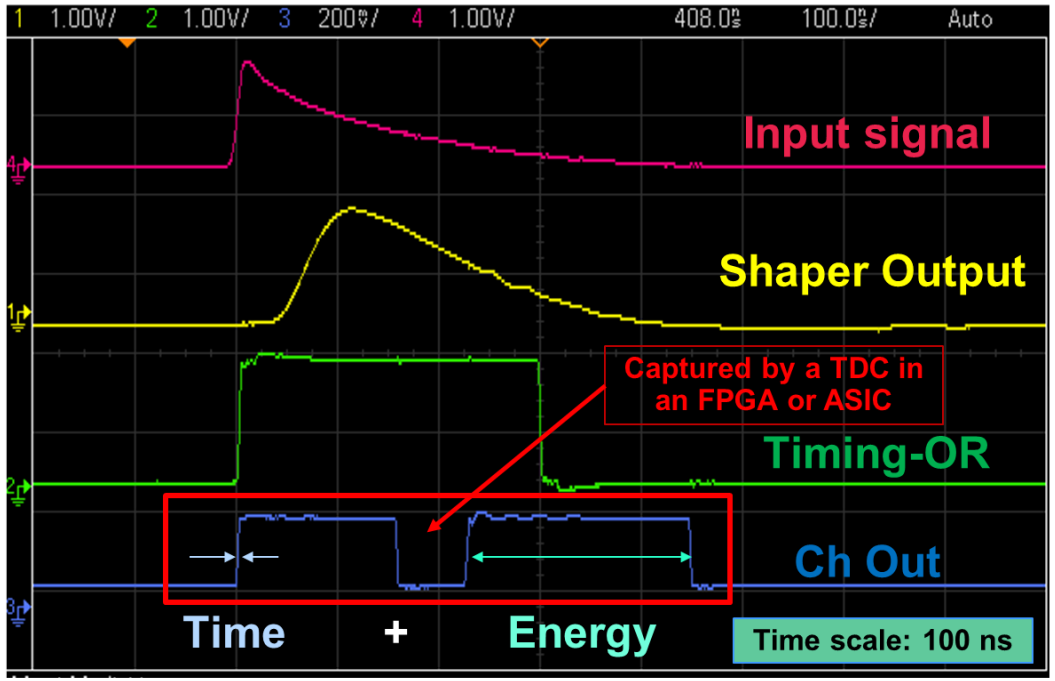


Collaboration of the ICCUB (Univ. Barcelona) and CERN-MIC

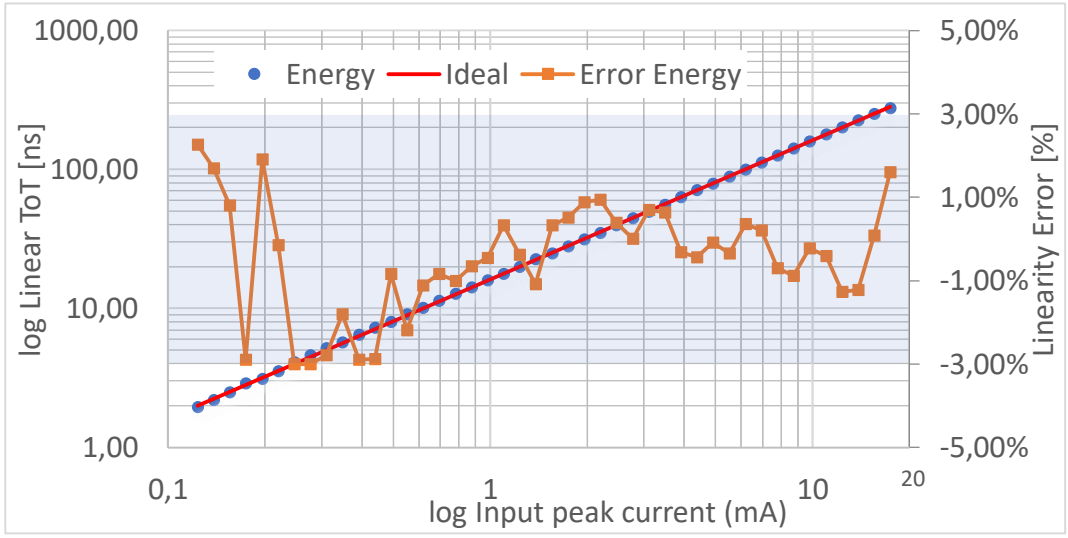
Institute of Cosmos Sciences

II. FastIC: Linearity of the Energy measurement

- **FastIC** provides a measurement of the **time** and **energy** per channel in two consecutive pulses
  - Based on HRFlexToT ASIC [1]
  - Linear energy by pulse width encoding
    - "Wilkinson ADC-like" conversion
    - Controlled by on-chip state machine



- Linearity error is **below 3%**
  - Saturation is reached at 25 mA of input current.
  - Other operating modes (negative, differential and summation) behaves similarly with a low linearity error.



- **This makes FastIC suitable to different detectors: LYSO/LSO, BGO, Cherenkov, Monolithic, etc**
- Different trigger modes, including cluster trigger for monolithic

[1]: Sanchez, D., Gomez, S., et. al. HRFlexToT: A High Dynamic Range ASIC for Time-of-Flight Positron Emission Tomography, 2021, IEEE TRPMS, https://doi.org/10.1109/TRPMS.2021.3066426

VI. FastICPix

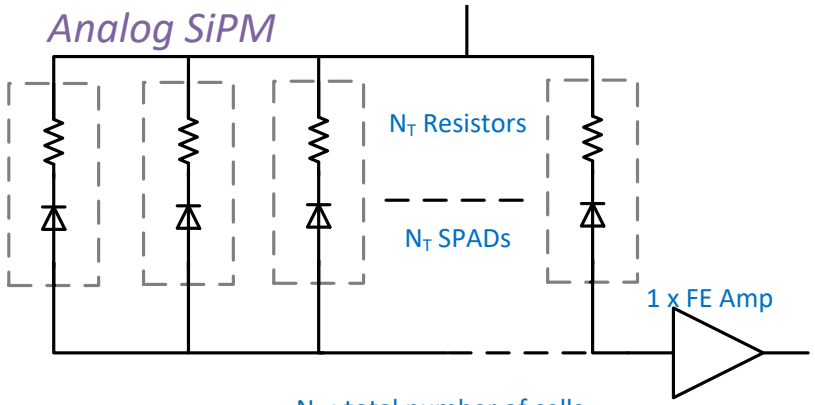
- FastICpix: try to exploit optimal segmentation
  - Optimization for a given *power budget !*
  - Investigation of new circuit topologies
  - 3D integration

Electronic noise jitter < 1 ps for next generation of detectors based on prompt light

Time tagging of first(s) photons

Optimal and adaptable segmentation: with hybrid detector

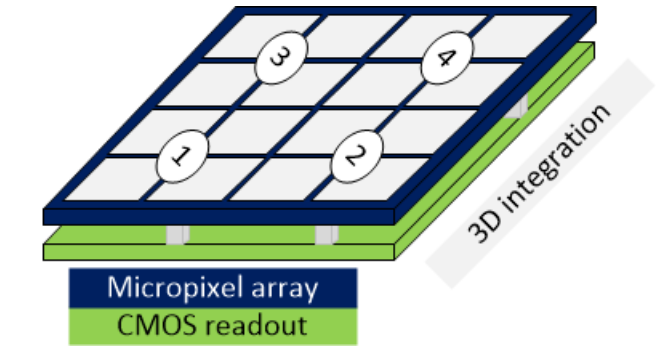
Analog SiPM

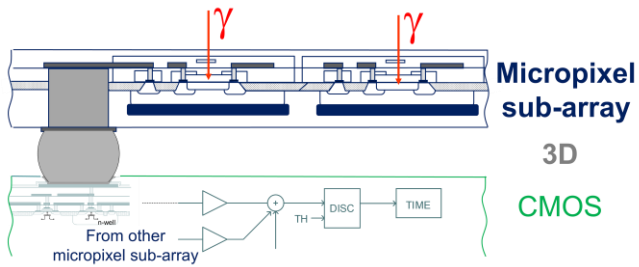


Pros
- Simplicity
- High Fill Factor (PDE)

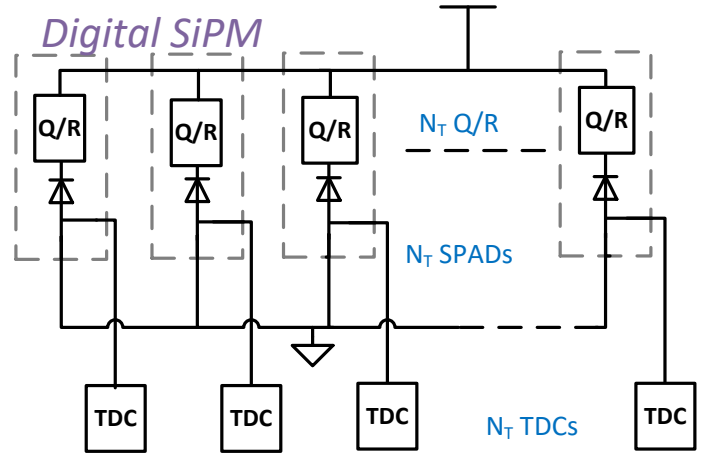
Cons
- Large capacitance degrades timing
- Xtalk deagrades timing

No segmentation





Digital SiPM



Q/R: Quenching and recharge circuit

Pros
- Individual photon timing available

Cons
- Complexity (cost and power)
- Fill factor degradation
- Xtalk degrades timing

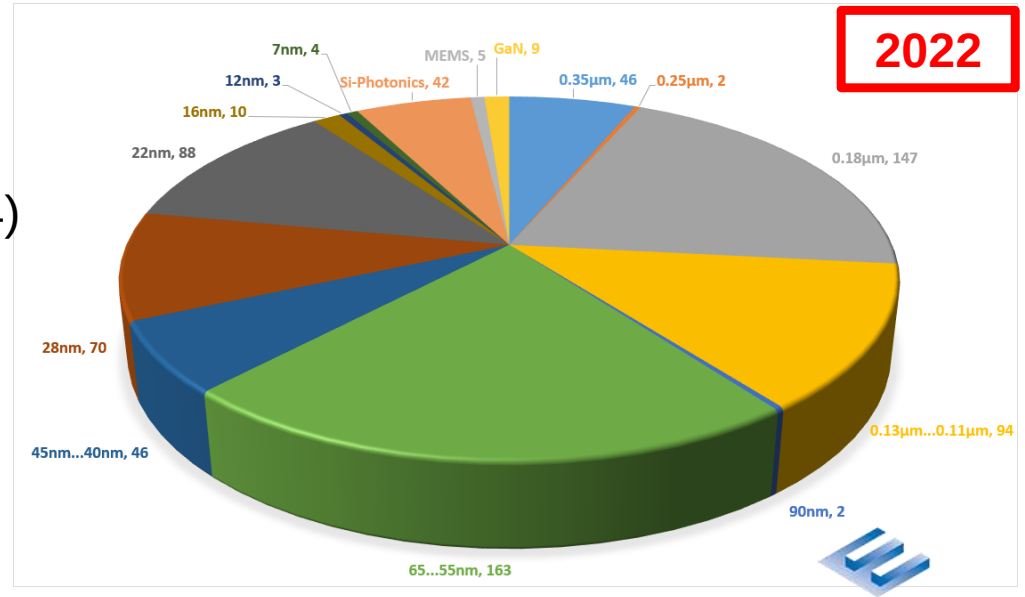
Maximum segmentation

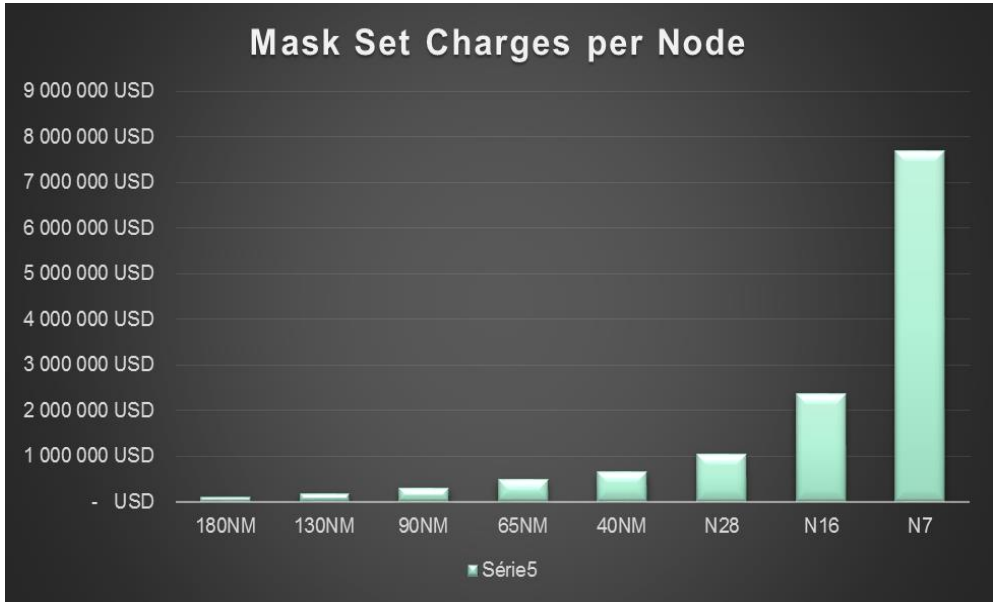
Technology choice for mixed signal ASICs

- TSMC 130nm : mixed signal, cheap
  - Very mature technology with good analog performance
  - 2.5 k€/mm² MPW, 300-350 k€/engineering run (20 wafers C4)
  - Perenity ?

- TSMC 65 nm : mixed signal, main stream
  - ~2-3 times lower power in digital, similar in the analog (compared to 130n)
  - 5 k€/mm², 700-800 k€/ engineering run

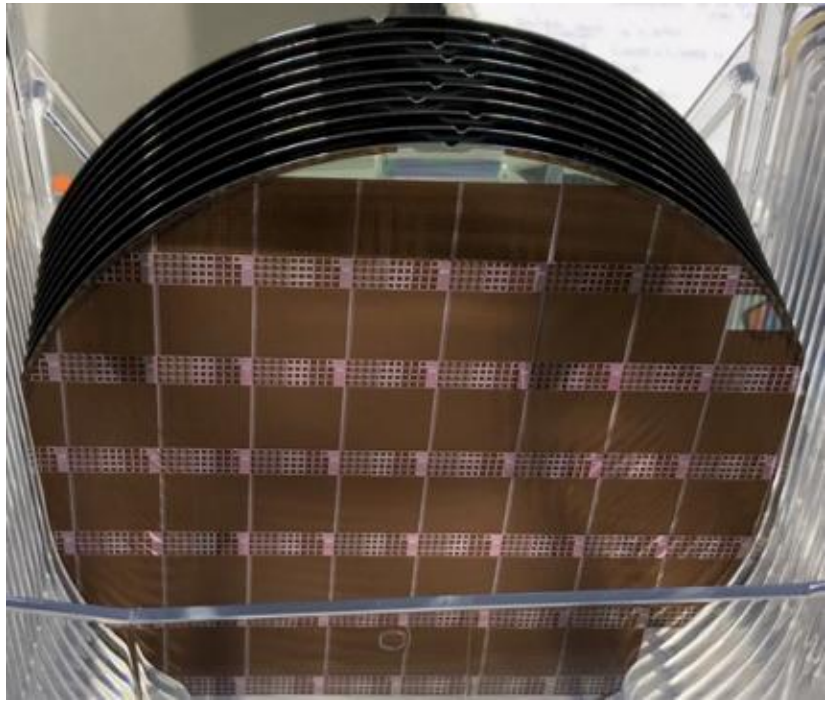
- TSMC 28 nm : digital oriented
  - High density integration (pixels)
  - High performance, lower power digital, similar in the analog
  - 10 k€/mm², 1-1.5 M€/ eng run





conclusion

- Importance of joint optimization detector/readout electronics



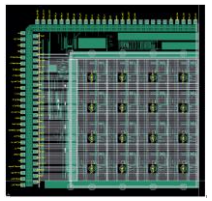
- Trend to reduce power and data volume
  - Pileup will be less of an issue, better granularity will be appreciated !
  - Low occupancy, auto-trigger, data-driven readout
  - Low power ADCs and TDCs (DRD7 with AGH&CEA)
- Picosecond Timing important R&D area
  - PID and/or calorimetry, several new detectors appearing : need R/O
- Next chips at OMEGA will target EIC, DRD1-4-6-7
  - Calorimetry and timing : CALOROC1 and 1A
  - Further R&D needed to bring power down to ~1 mW/ch (Lar)
- Technology choice to be addressed in coordination with other design groups
  - Cost sharing for engineering runs

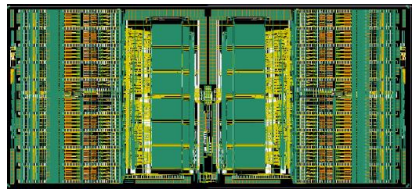
backup

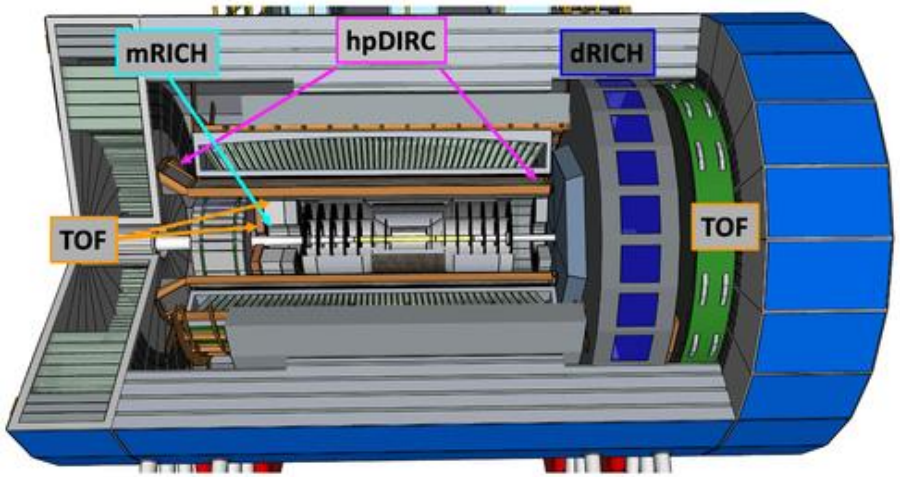
Chips for EIC : electron-ion collider at BNL

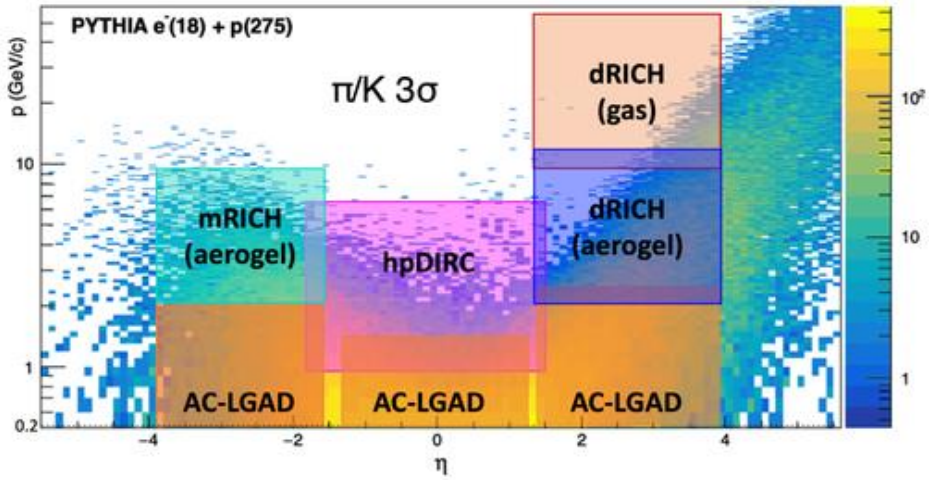
- PID and calorimeters
  - EICROC for AC-LGAD roman pots
  - H(2)GCROC for calorimeters
  - « Event driven » DAQ

Detector Group	Channels			
	MAPS	AC/DC-LGAD	SiPM/PMT	MPGD
Tracking	32 B			100k
Calorimeters	50M		67k	
Far Forward	300M	2.3M	500	
Far Backward		1.8M	700	
PID		3M-50M	600k	
TOTAL	32 B	7.1M-54M	670k	100k
ASIC	ITS-3	EICROC FCFD HPsOC ASROC FAST	Discrete/COTS HGCROC3 ALCOR-EIC	SALSA









SiPM : ADC and TOT readout

- 16bit dynamic range split in 10 bit ADC and 12 bit ToT
- Tests with 2 sizes of SiPM : 2mm² (120 pF) and 9 mm² (560 pF)