Single Event Effects

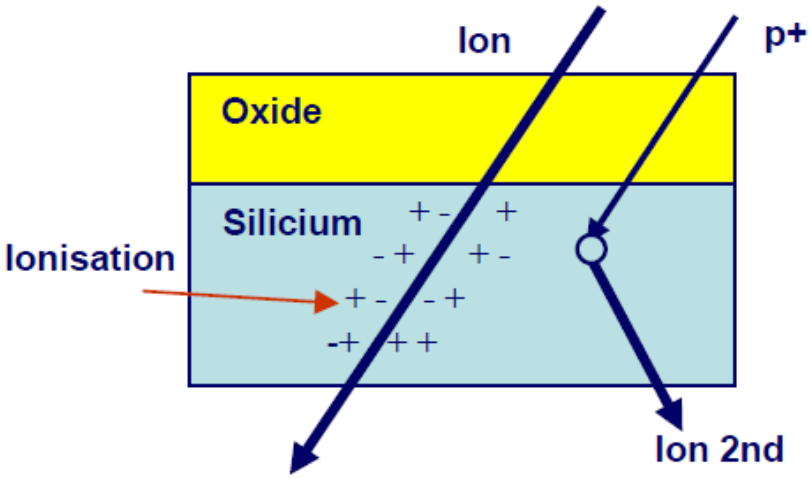
1. Overview of single event effects
2. SEE basic mechanisms and models
3. Rate calculation methodology

Introduction

- A Single Event Effect is
  - An isolated event taking place in an active device
  - Due to only one energetic particle strike

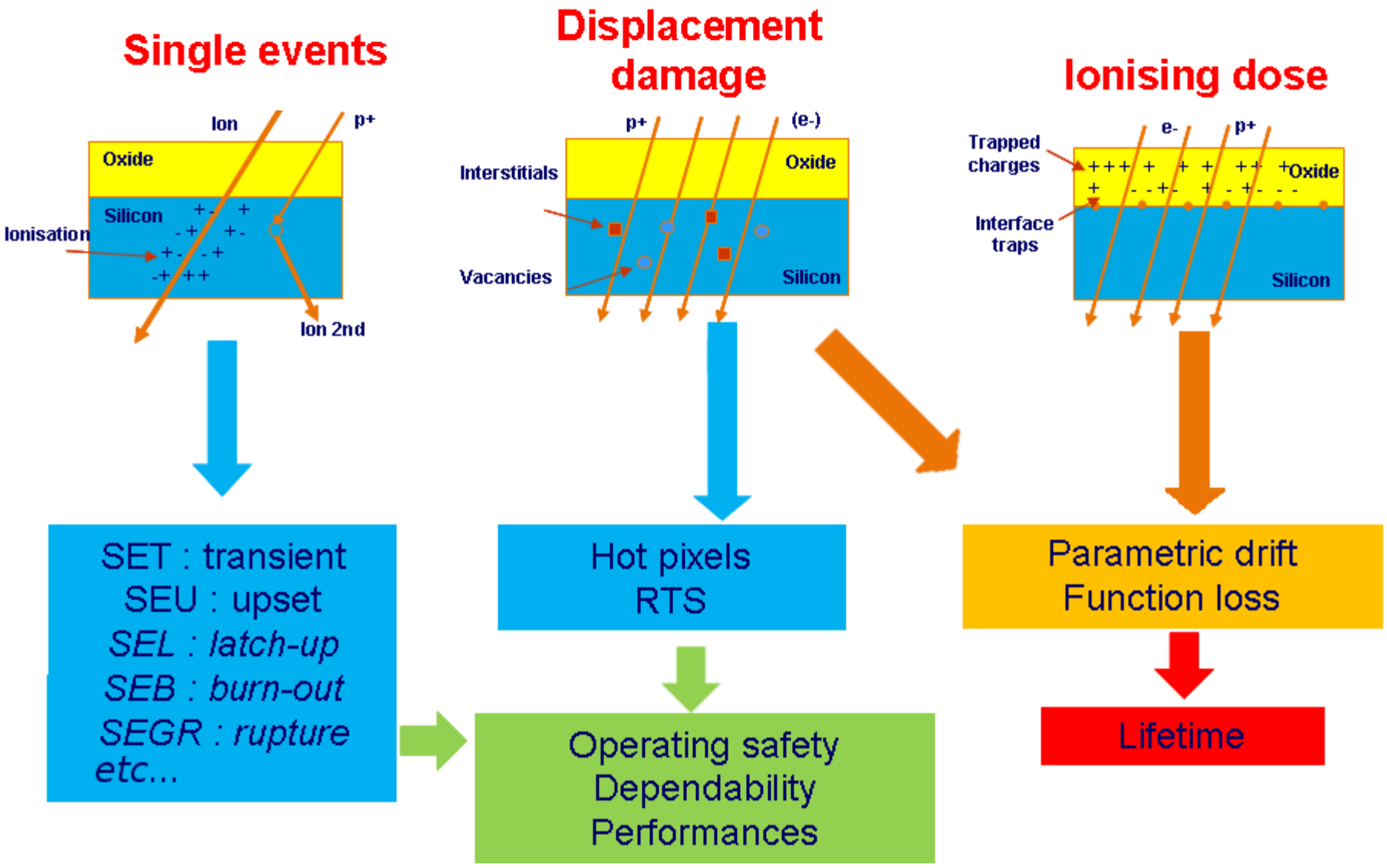
- A Single Event Effect can be
  - Destructive
  - Non-destructive

- Single Event Effect are caused by
  - Heavy ions
  - Protons

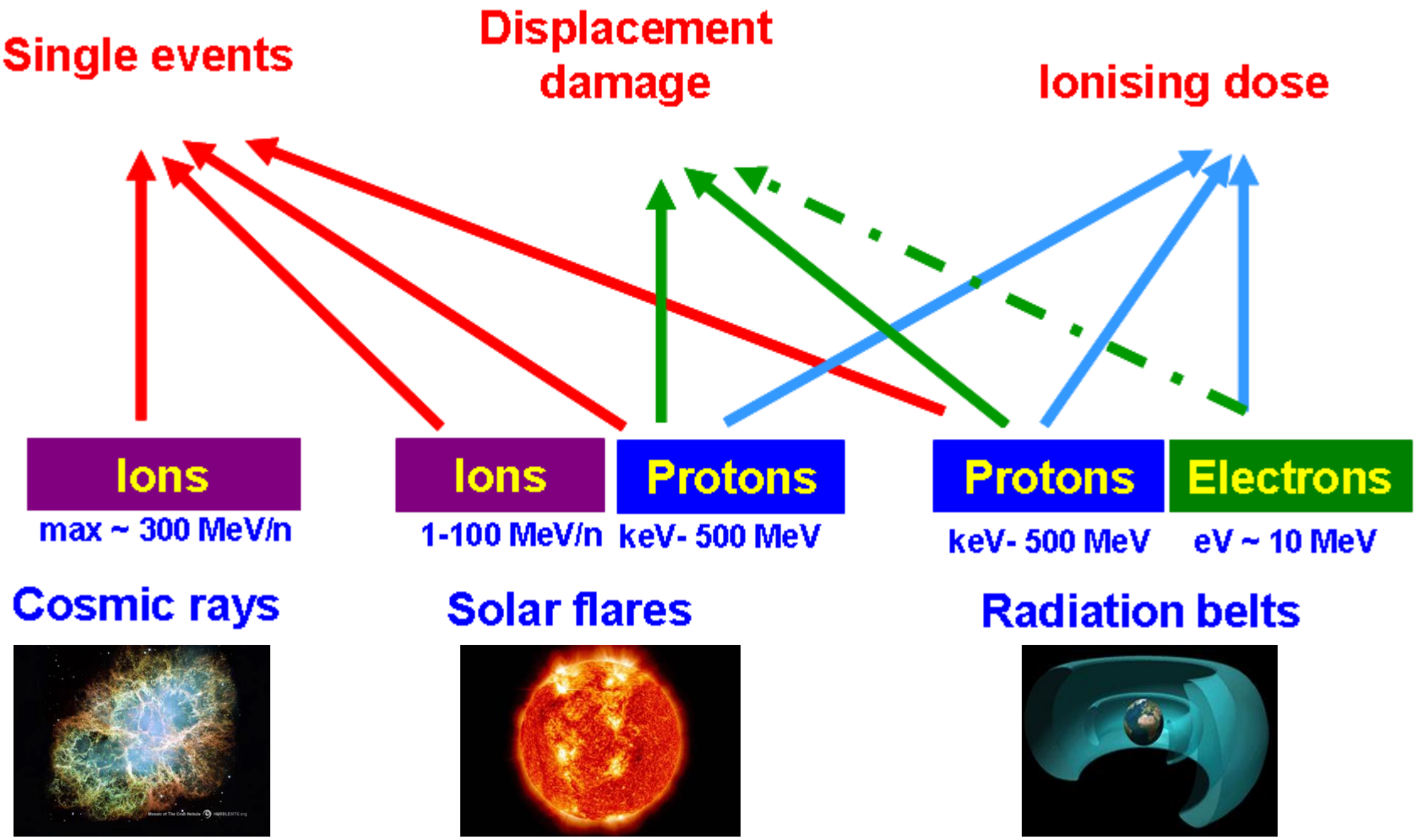


- The environment contributions to the SEE are
  - Trapped protons
  - Solar particles (protons and ions)
  - Cosmic rays

Radiation Effects



Environment Sources and Radiation Effects



Introduction

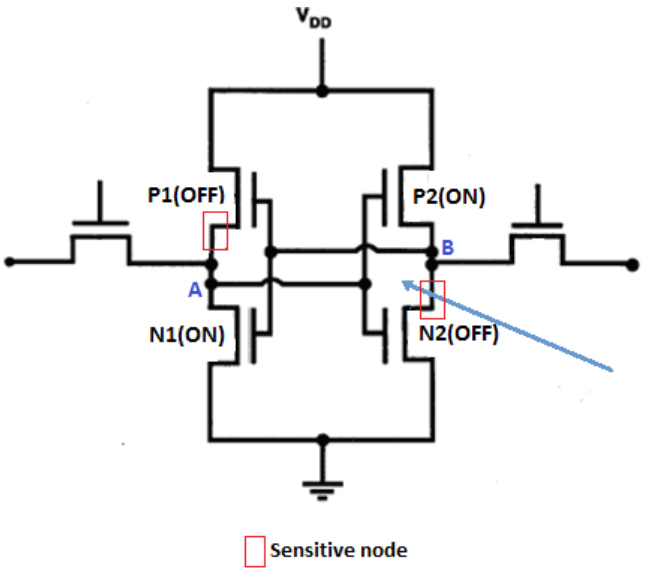
- **Non-destructive effects**
  - SEU (Single Event Upset)
    - A change of state induced, that may occur in digital, analog, and optical components, these are “soft” errors in that a reset or rewriting of the device causes normal device behavior thereafter
  - MBU (Multiple Bit Upset)
    - An event inducing the corruption of several bit in the same word/memory address
  - MCU (Multiple Cell Upset)
    - An event induced by a single energetic particle that causes multiple upsets or transients during its path through a device or system
  - SET (Single Event Transient)
    - Transient perturbation in analog devices
  - SEFI (Single Event Functional Interrupt)
    - Functionality loss in complex devices

Introduction

- **Destructive effects**
  - SHE (Single Hard Error or Stuck Bit)
    - An SEU which causes a permanent change to the operation of a device, like a stuck bit in a memory.
  - SEGR (Single Event Gate Rupture)
    - An ion induced condition in power Mosfet which may result in the formation of a conducting path in the gate oxide.
  - SEB (Single Event Burnout)
    - A condition which can cause device destruction due to a high current state in a power transistor.
  - SEDR (Single Event Dielectric Rupture)
    - Destructive event occuring in FPGA, AOP…
  - SEL (Single Event Latch-up)
    - A condition which causes loss of device functionality due to a single event induced high current state, that may (or may not) cause permanent damage, but requires power reset of the device to resume normal operation.

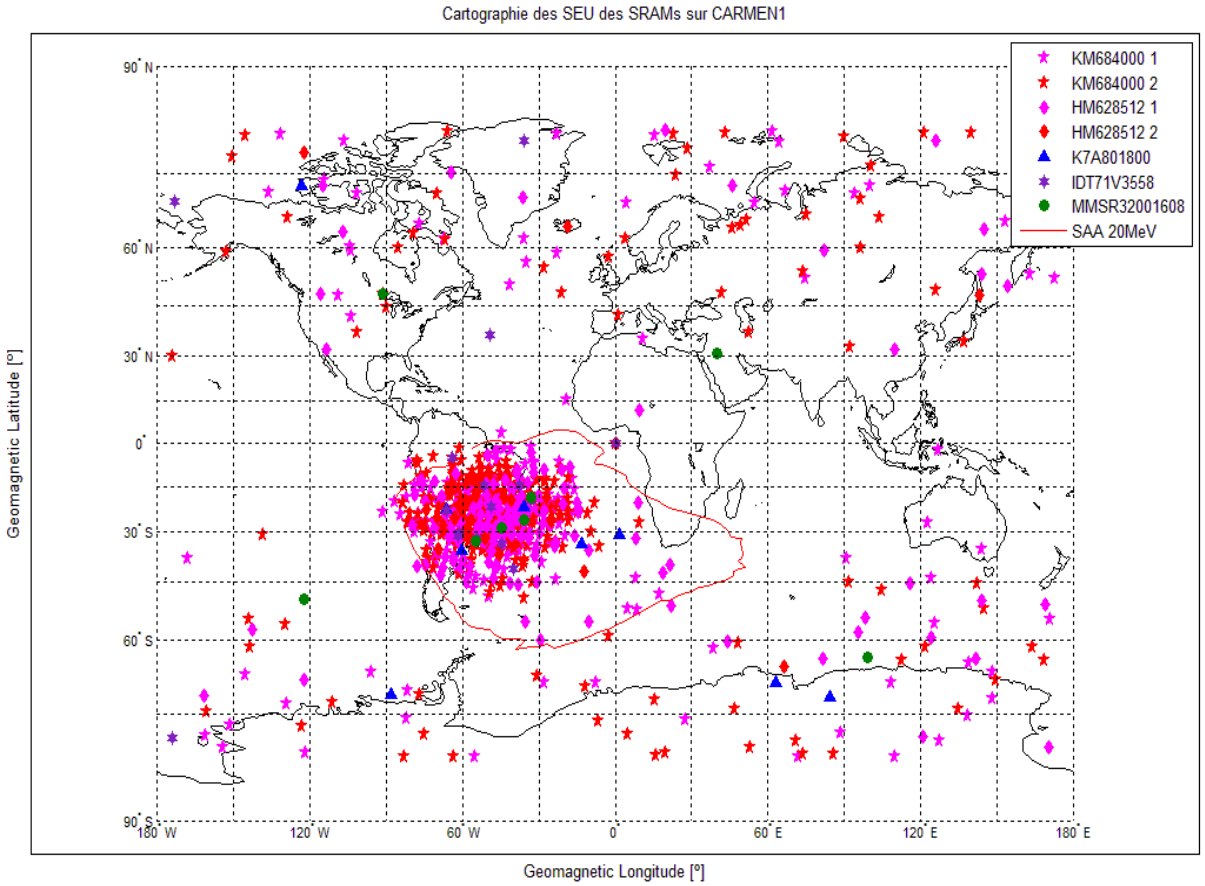
Single Event Upset

- Single Event Upset
  - Non-destructive effect
  - SEU is the corruption of the information stored in a memory element
  - Occurs in memories, buffers, D-flip-flop, latches…
  - Sensitive areas are indentified as the OFF NMOS drain transistor and the OFF PMOS drain transistor



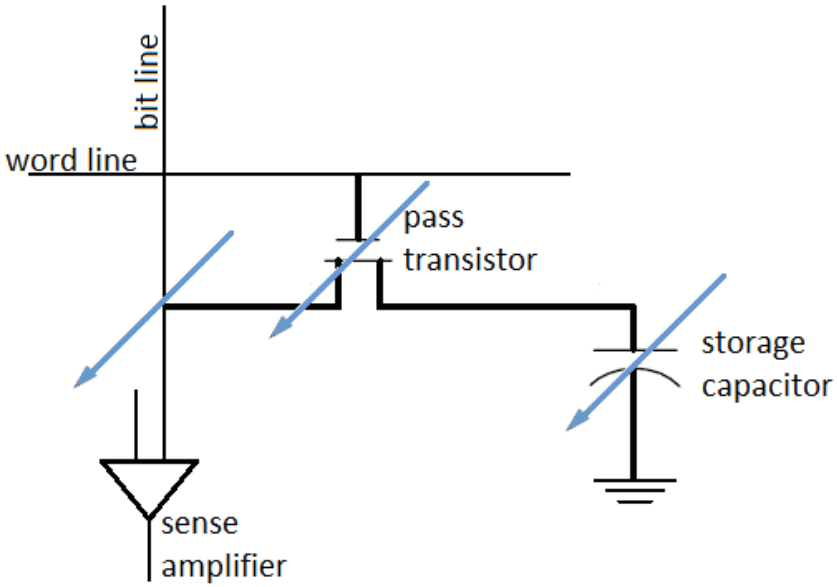
Single Event Upset

- In flight event detection
  - SEU on SRAM (CARMEN1 on SAC-D)



Single Event Upset

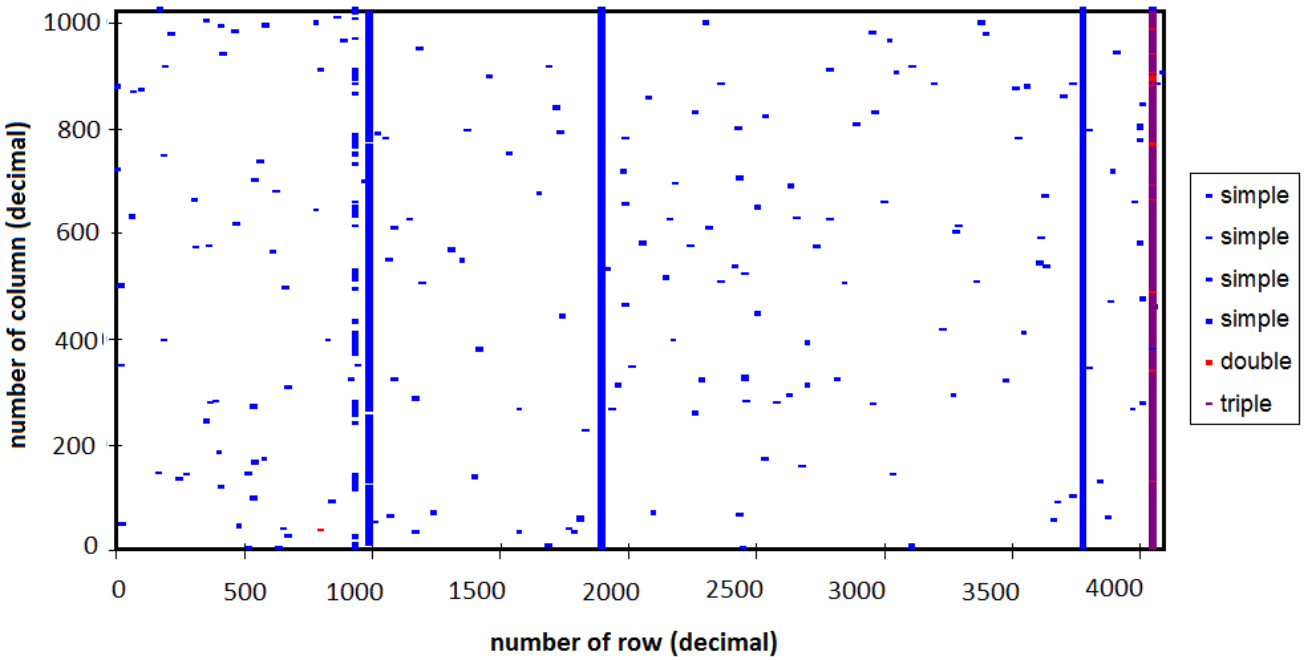
- SDRAM Case
  - Cell error : a particle strike in or near either the storage capacitor or the source of the access transistor
  - Error detected as SEUt
  - Bit line errors : a particle strike in or near either the drain of the access transistor (connected to the bit line) or the sense amplifier during a critical timing window
  - This error type can lead to a partial or complete corrupted row.
  - A particle strike in the decoding circuit of the spare rows/columns may also lead to erroneous data



→ Watch out the technology !

Single Event Upset

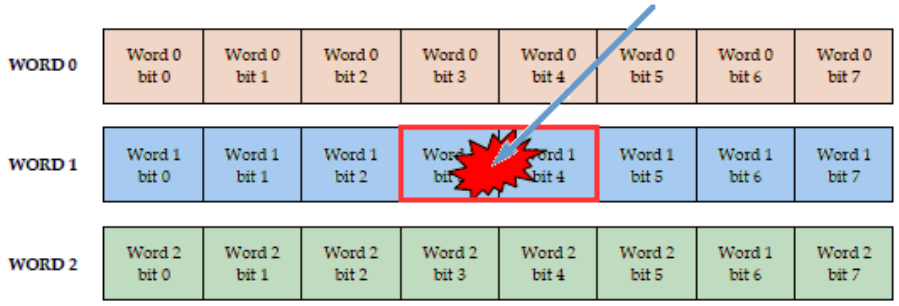
- Example
  - Error signature on Texas Instruments 16 Mbit dynamic RAM (CNES/ONERA data)
    - Single errors
    - Dual errors
    - Row / column errors



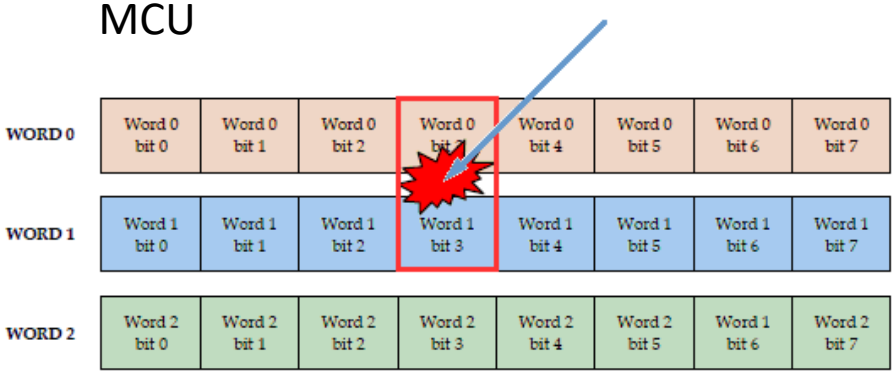
Single Event Upset

- Multiple Bit Upset (MBU) / Multi Cell Upset (MCU)
  - Several bit-flips are triggered by a single particle
  - Several upsets in a memory word are called MBU
  - Several upsets triggered by the same incident particle are called MCU
  - Error-Correcting Codes (ECC), such as Hamming codes, are well adapted to mitigate SEU (detection et correction), but not MBU

MBU



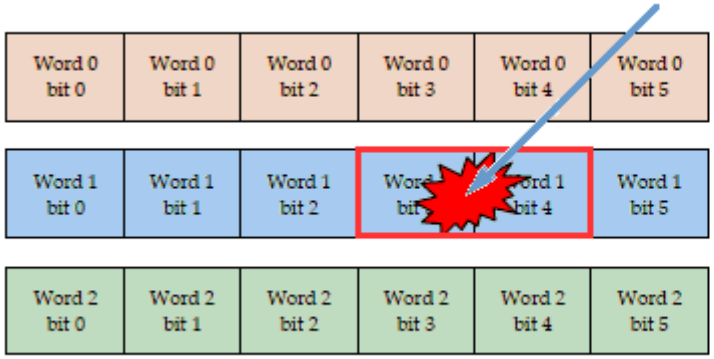
MCU



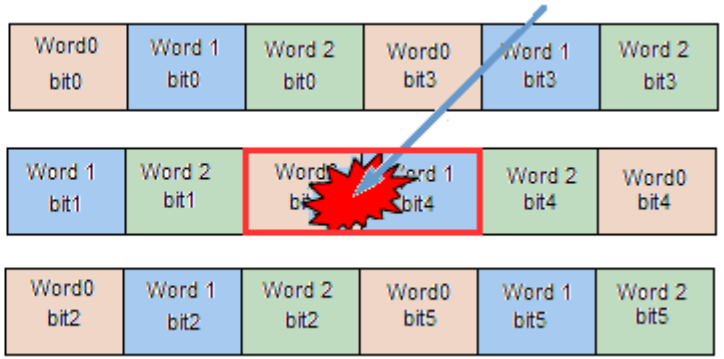
Single Event Upset

- Multiple Bit Upset (MBU) / Multi Cell Upset (MCU)
  - Scrambling : the logical structure differs from the physical or topological internal structure of the chip
  - logically adjacent addresses are not physically adjacent (address scrambling)
  - logically adjacent data bits are not physically adjacent (data scrambling)
  - MBU mitigation technique

Standard memory structure : MBU



Scrambling structure : MCU



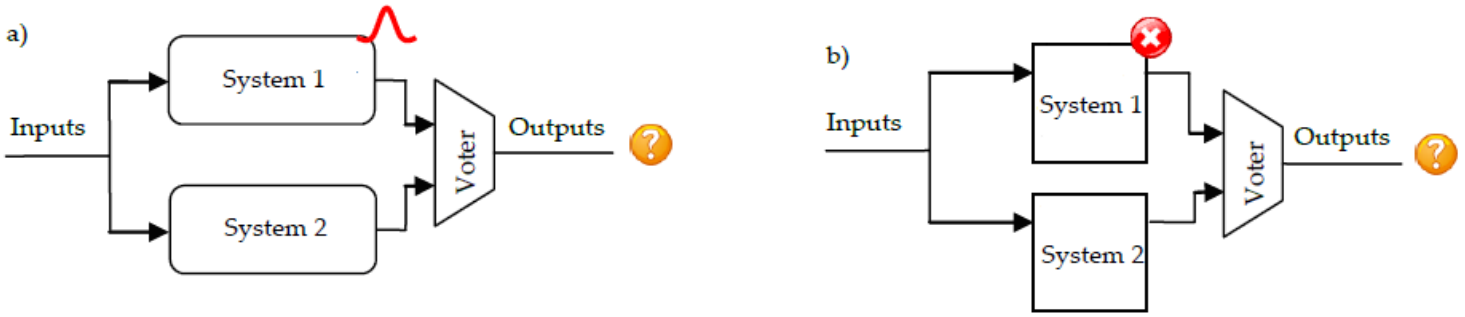
Single Event Upset Mitigation

- Error-Correcting Codes (ECC) or Error Detection And Correction (EDAC)

EDAC Method	**EDAC Capability**
Parity Check	Detects single bit error
CRC Code	Detects if any errors occurred in a given data stream
Hamming Code	Double bit error detection ,Single bit error correction
Reed-Solomon Code	Corrects consecutive and multiple bytes in error
Convolutional encoding	Corrects isolated burst noise in a communication stream
Overlying protocol	Specific to each system implementation

Single Event Upset Mitigation

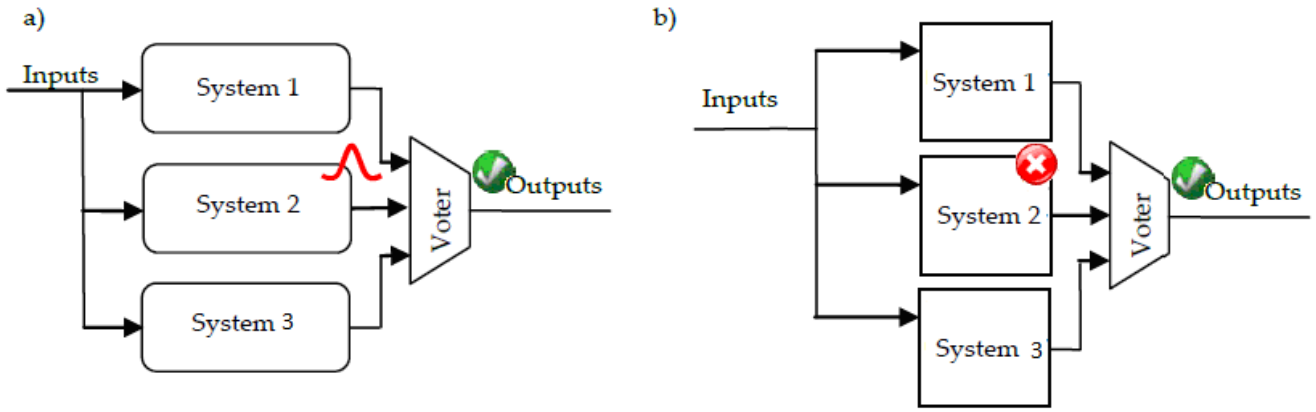
- Bi-Modular Redundancy
  - The Bi-MR (Bi-Modular Redundancy) is issued from the spatial redundancy concept
  - It uses two replicas of a processing unit and votes the outputs to detect potential differences provoked by SEE
  - This scheme can be applied for both combinational and sequential logic and can provide respectively SET and SEU (MBU and SEFI) detection



- The voter being the critical element, it must be robust to faults
- Such architecture is mainly fail-stop architecture as it is able to detect faults but not to recover them

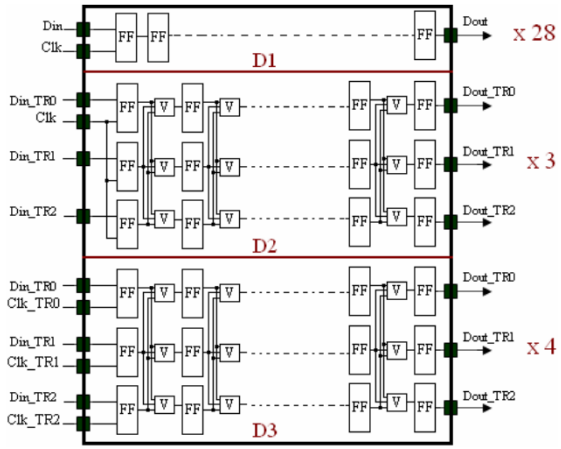
Single Event Upset Mitigation

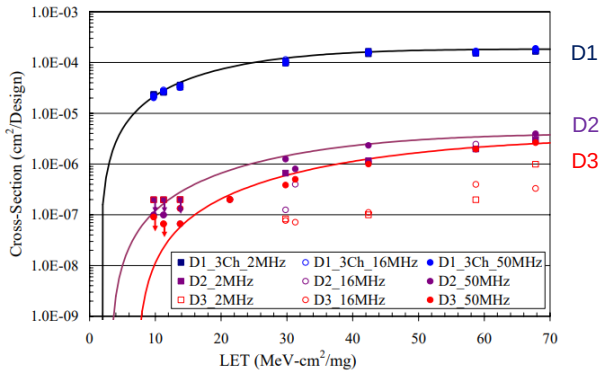
- Triple Modular Redundancy
  - The Triple Modular Redundancy (TMR) architecture is based on three redundant elements whose outputs are voted by a majority comparator in order to determine the correct result
  - When an upset provokes an error, it is expected that at least two results remain correct, allowing the voter to forward the correct result



Single Event Upset Mitigation

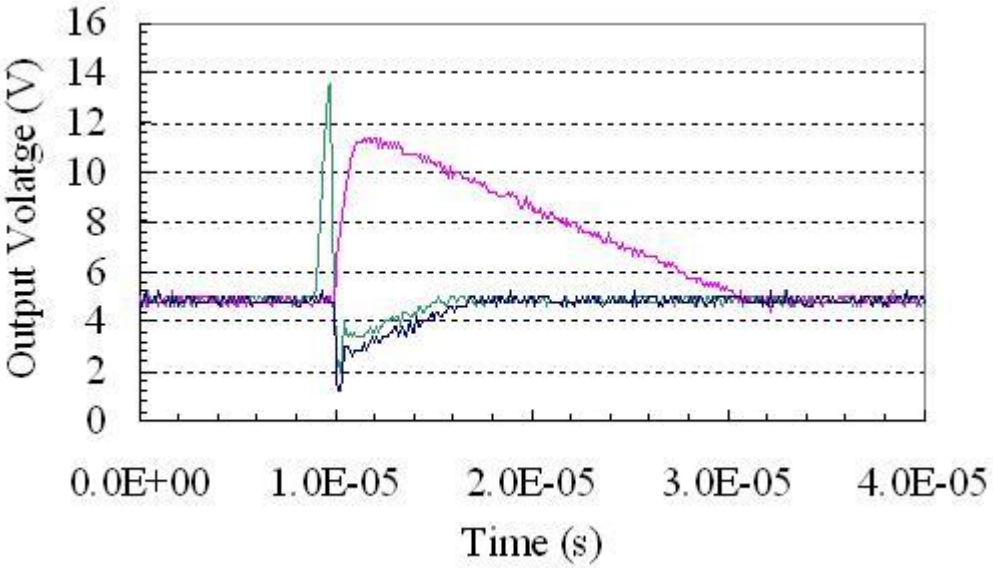
- Triple Modular Redundancy
  - The main advantage of this technique is it simplicity and high correcting power (fault coverage close to 100%) for SET, SEU, MBU and SEFI effects
  - Its main disadvantage is the need to implement three times more memory capacity on-board than is strictly necessary
  - An SET occurring in the voter itself may output a wrong value which will be propagated (Rad-hard voter, TMR on voter)
  - Temporal redundancy can also mitigate SET with lower duration than the sampling time.
    - Redundancy for the ProAsic FPGA Family →





Single Event Transient

- Single Event Transient
  - Non-destructive effect
  - Occurs in linear device
    - Voltage references
    - Operational amplifier
    - Voltage regulator
    - Comparator
  - SET is an electrical pulse ignited in the device and propagated from the device to the system
  - An SET is characterized by
    - A voltage amplitude
    - A duration
  - Strongly depending on the application (electrical design, bias condition…)
    - SET can be filtered

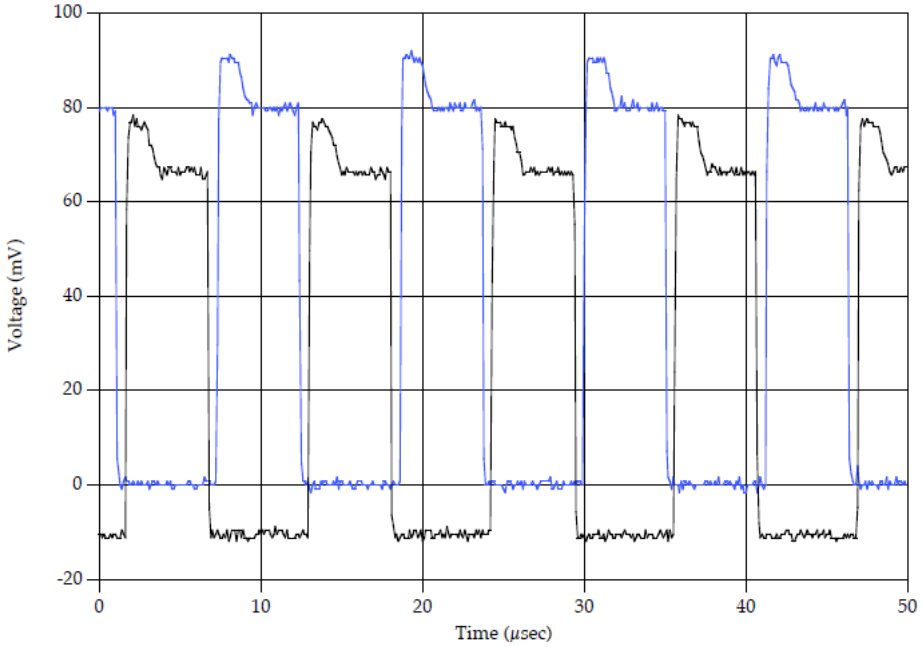


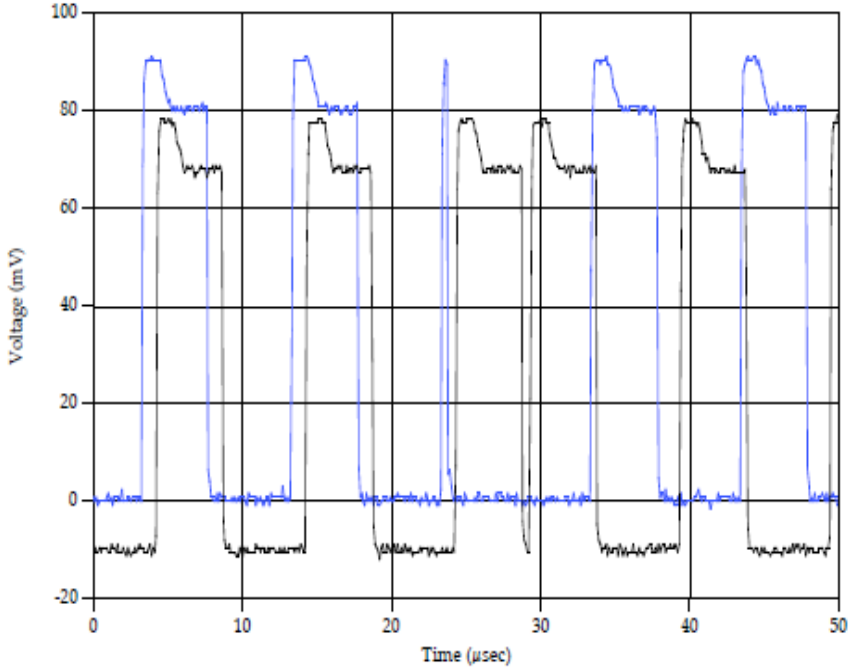
- SET shape in an operational amplifier (LM124)
  - Static mode

Single Event Transient

- Single Event Transient
  - Dynamic mode

- Nominal and during irradiation voltage of SG1525A oscillator





Missing or additional clock cycle

Single Event Transient

- SET mitigation technique
  - Hardening design rules exist in order to prevent the propagation at system level of the short perturbation of the output signal
  - They consist in choosing output equivalent charges high enough to filter the spike without changing the analogue function

- Redundancies are also an SET mitigation technique

- The worst-case SET shapes are defined for each component family with a specific duration and amplitude
  - SET signal envelopes usable for system specified in ECSS-Q-ST-60-15C are provided in next Table as a function of semiconductor family type

Table 5-4: Worst case SET templates

Device type	SET nature at device output
OP-amps	$\Delta V_{max} = \pm V_{cc}$ & $\Delta t_{max} = 15\ \mu s$
Comparators	$\Delta V_{max} = \pm V_{cc}$ & $\Delta t_{max} = 10\ \mu s$
Voltage Regul.	$\Delta V_{max} = \pm V_{cc}$ & $\Delta t_{max} = 10\ \mu s$
Voltage Ref.	$\Delta V_{max} = \pm V_{cc}$ & $\Delta t_{max} = 10\ \mu s$
Optocouplers	Susceptible to SEU $\pm V_{cc}$ & $\Delta t_{max} = 100ns$
PWMs	Double Pulses, two missing pulses, multiple missing pulses in a row, device shut off. Assess impact in specific application.
PLL	Transients and permanent changes in output voltage. In synthetizer circuits can cause phase, amplitude and frequency transients with duration determined by loop response.

Single Event Transient

- For the SET analysis, the approach is composed with several steps

- **Step 1**
  - Simulate the injection of a worst-case SET shape in an electrical model of the system
    - SPICE model for example
  - The worst-case SET shapes is injected at the device output

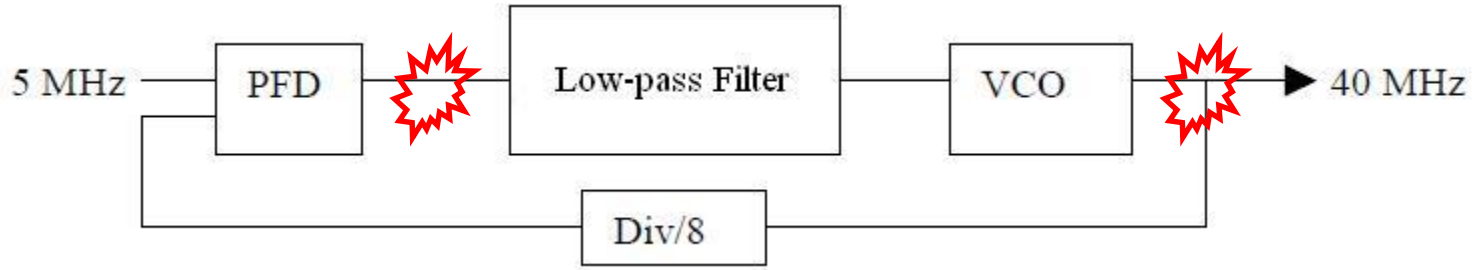
- **Step 2**
  - Analyze the impact(s) of the perturbation on the system

- **Step 3**
  - If there is a critical impact
    - System redesign to filter/harden against the SET
    - Device SEE testing in the application in order to measure the real SET shape and duration and to be able to calculate the associated SET rate

Single Event Functional Interrupt

- Single Event Functional Interrupt
  - SEFI is the loss of nominal operation
  - The device falls into an unknown/unmanaged state
  - Reset or power cycling to recover nominal operation
  - Occurs in complex devices with built-in state/control sections
    - DRAM, FPGA, ADC/DAC, PLL…

- Example
  - Functionality loss of a Phase Locked Loop due to SEFI



Single Event Hard Error

- Single Event Hard Error
  - Single Event Stuck Bit (SESB)
    - Non destructive but semi-permanent damage due to
      - local dose deposition
      - Displacement damage cluster
      - Leakage of stored charges
      - Can be stuck to 0 or 1
    - Annealing required to recover functionality

RADECS 2015: Experimental characterization and In-flight observation of Weakened Cell in SDRAM

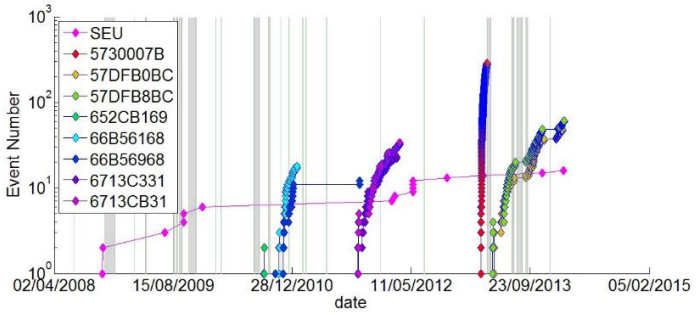


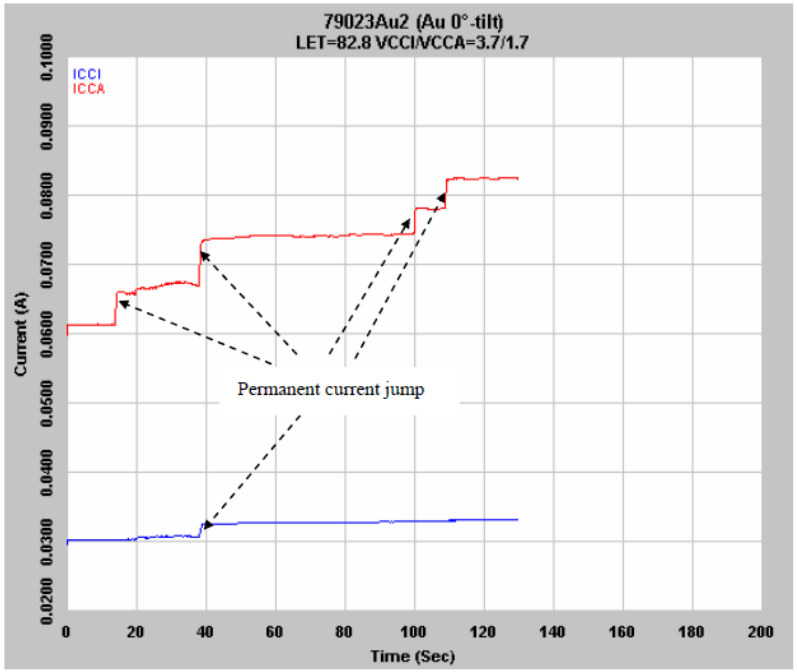
Fig. 1 MMSD08512408S-Y Z35 Number of soft errors in function of the time and in function of the address for weakened cells

  - The « Real » SHE is an unalterable change of state in a memory element
    - Impossibility to change the bit value by write operation
  - Occurs in memories and buffers

Single Event Dielectric Rupture

- Single Event Dielectric Rupture
  - Thin oxide breakdown in programmable IC, linear devices…
  - Combination of harsh biasing conditions and high LET

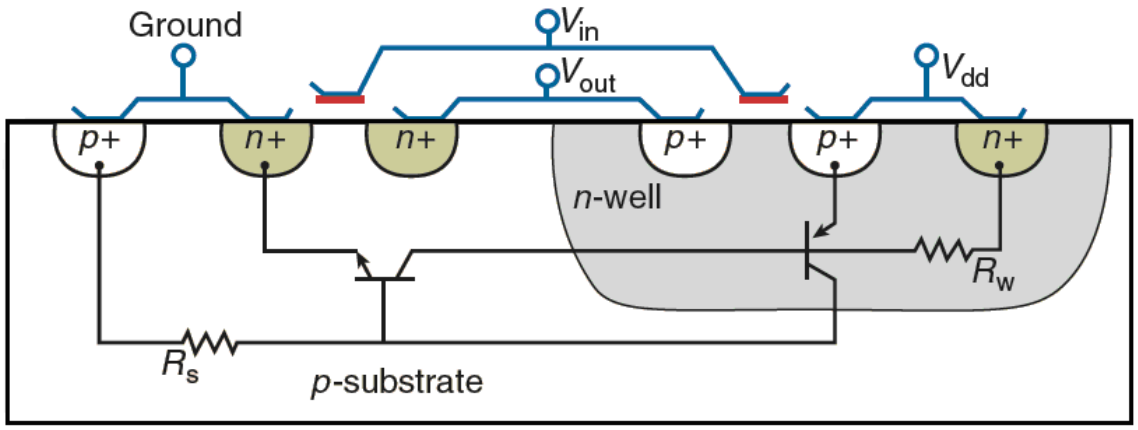
- RTAX family Microsemi – LET 82 MeV.cm²/mg



Single Event Latch-up

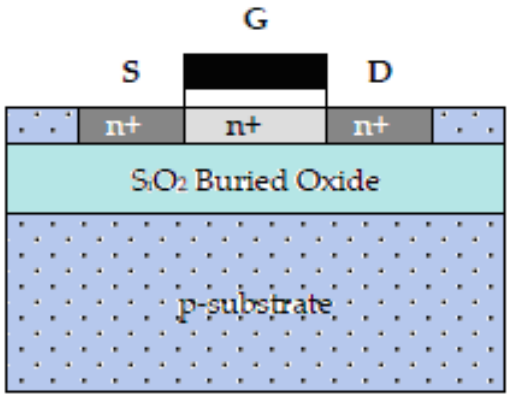
- Single Event Latchup
  - Destructive event
  - SEL is a short-circuit between GND and Vcc
  - Occurs in CMOS technologies (and BiCMOS…)

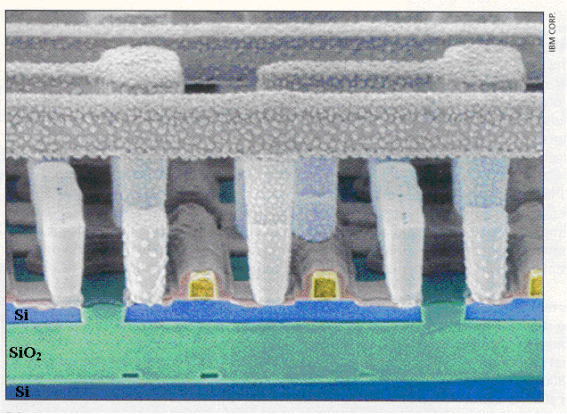
- SEL is due to the activation of a parasitic NPNP path (thyristor) caused by the ion strike
  - Favorised by temperature



Single Event Latch-up Mitigation

- Single Event Latchup
  - SEL mitigation technique : SOI technology (Silicon On Insulator) (FD-SOI)





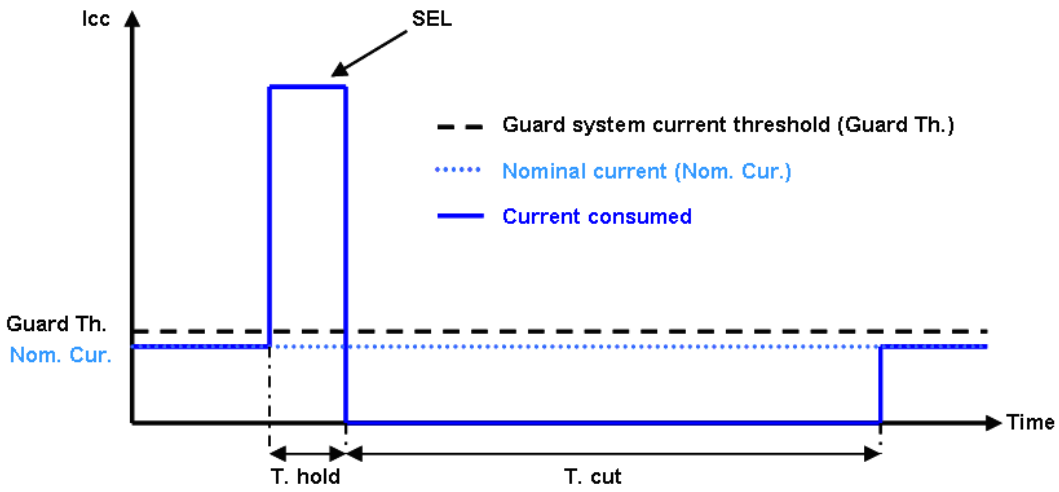
  - Problem : may increase Total Ionizing Dose sensitivity

Single Event Latch-up Mitigation

- The latch-up phenomenon may be detected by
  - Over power consumption
  - A loss in component functionality (with a watchdog for a microprocessor)

- The phenomenon can be stopped by cutting off the power supply to the component for a sufficiently long time for the current to become null
  - A few tenth of ms are generally sufficient

- Furthermore, care should be taken to isolate the component input pins because there is a risk of a parasitic re-supply of the circuit through the protection diodes which will thus stop the current from dropping to zero when the main power supply has been cut-off
  - In this case the latch-up phenomenon will persist when the component is powered up again



Single Event Latch-up Mitigation

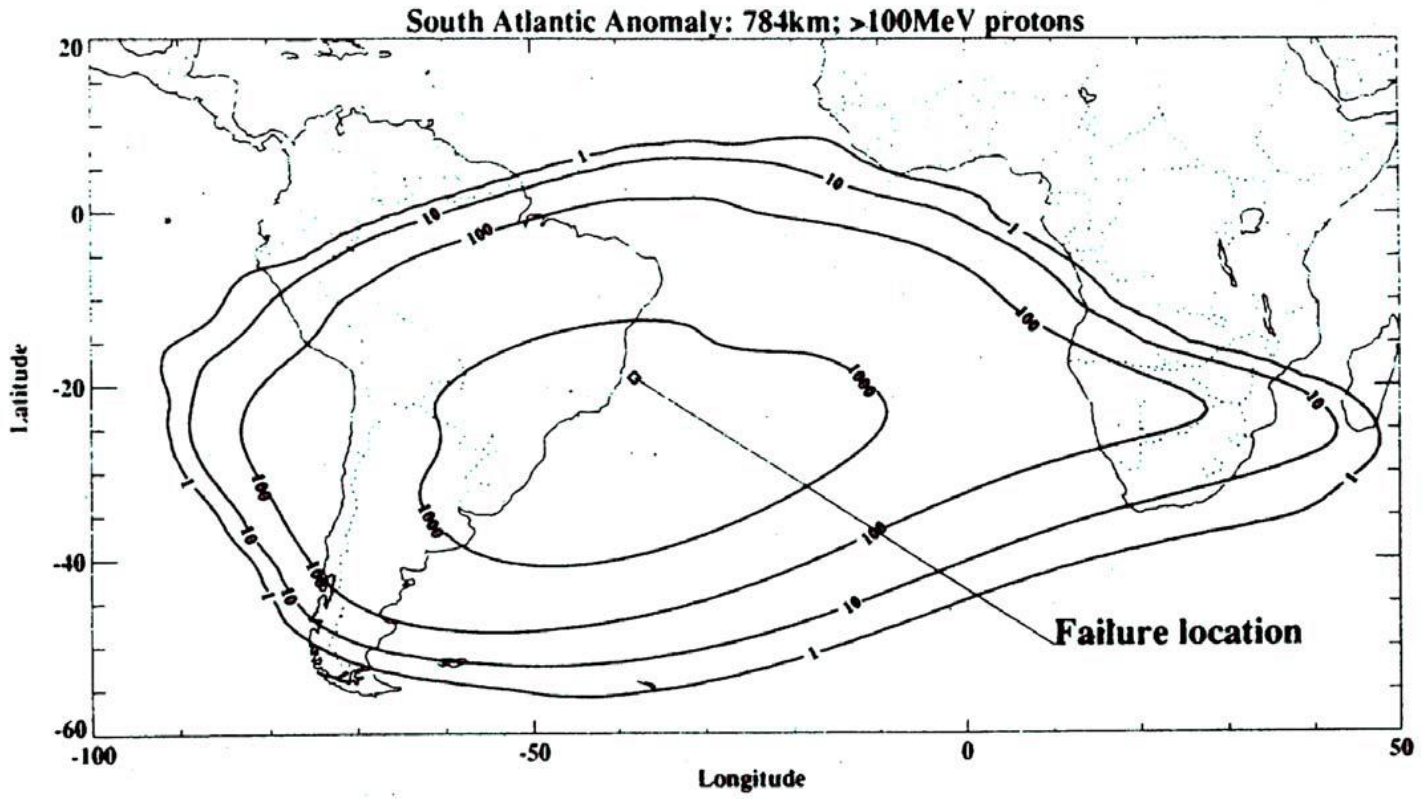
- If a component is sensitive to latch-up then mitigation technique (cut off power supply) will affect the availability of the function
  - May not be acceptable for the availability of the entire system

- This temporary malfunction must be taken into account at a higher level in order to limit the consequences on the general operation of the equipment or of the satellite

- Take in consideration the power up current (in-rush current)
  - Current surges observed during power-up can lead to dramatic consequences making it impossible to switch on the equipment due to current limiters
  - Risk of de-latching cycles

Single Event Latch-up

- In flight event detection
  - PRARE / ERS-1 instrument loss (SSO)

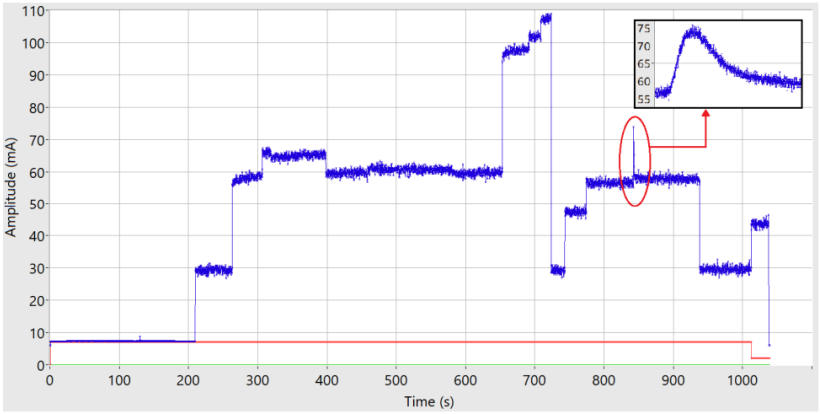


- Latch-up on 64-kbit CMOS SRAM, after 5 days, instrument lost

High Current Event

- High Current Events (HCE)
- SEE induced increase in current consumption, not directly destructive.

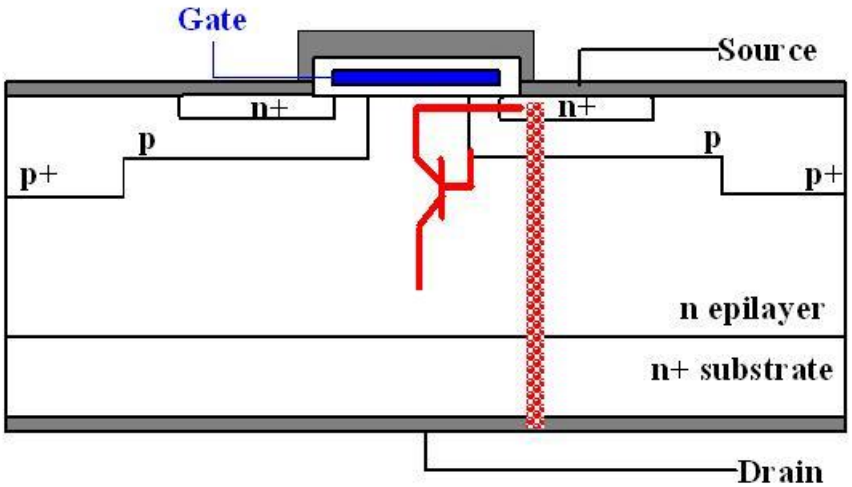
- Several phenomena under the same name, the most common are:
  - µLatchups
    - Perturbation of local sensitive areas inducing incremental current surges that require a power cycle.
  - Pseudo-Latchups
    - Upsets leading to conflicts in the data buses and a transient high current consumption.



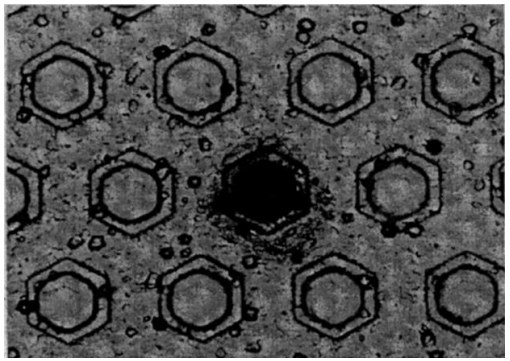
RADECS 2018: High Current Event and Single Event Functional Interrupt in Non-Volatile Memories

Single Event Burn-out in Mosfets

- Single Event Burnout
  - Destructive event
  - SEB is caused by the activation of a parasitic NPN bipolar transistor in vertical power Mosfet
  - Occurs in N-channel power Mosfet (P-channel Mosfets are SEB free)
  - Sensitive at blocked/over-blocked state

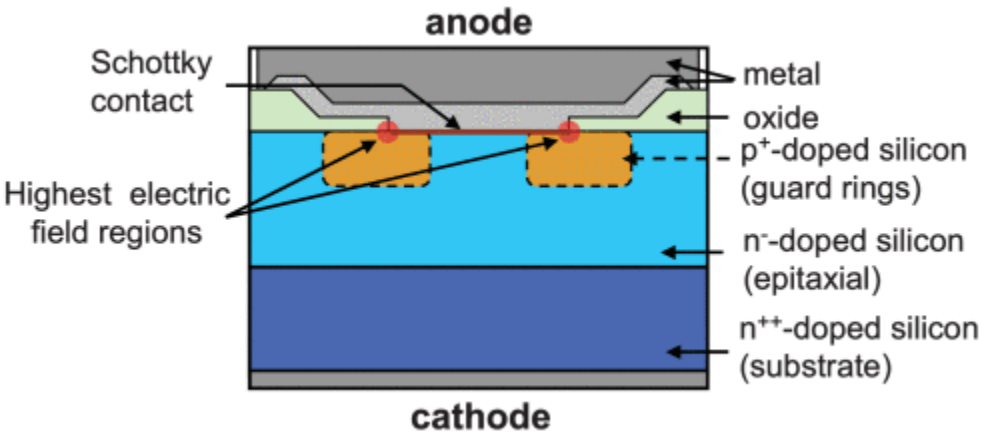


- Forward E/B of parasitic BJT
  - Forward active regime
  - Junction breakdown

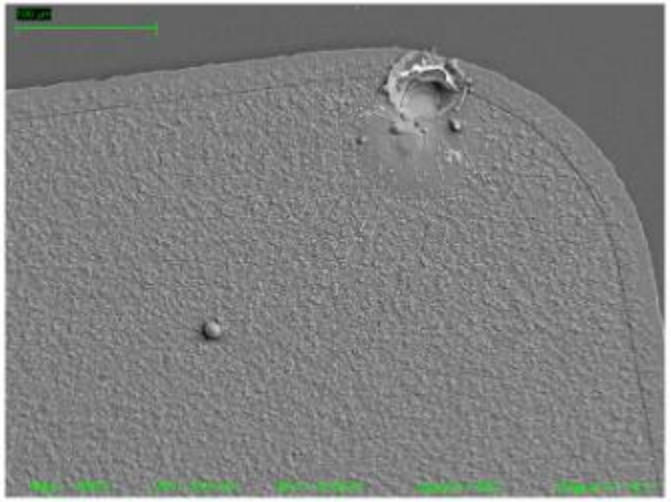


Single Event Burn-out in Power Diodes

- Different mechanism than Mosfets
  - Charge injection in areas of intense electric field
    - Close to contacts
    - Defects
  - Impact ionisation and avalanche effect
  - Temperature locally increase up to melting point

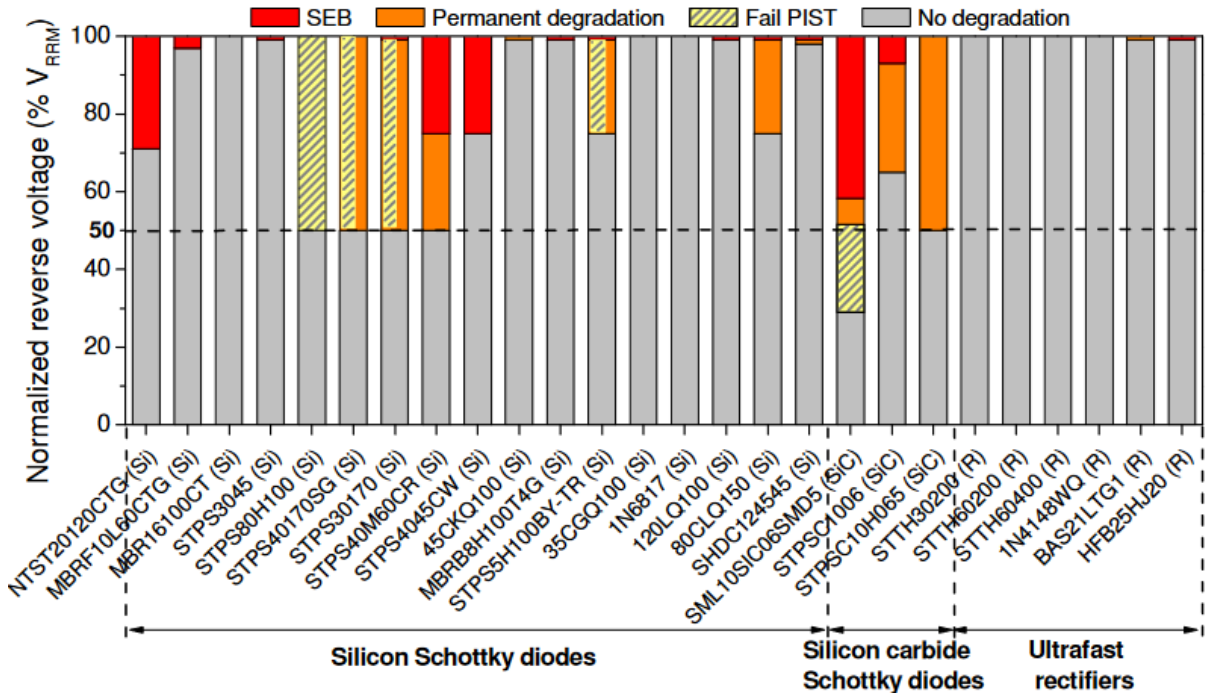


Local fusion of the material
Close to the Schottky contact



Single Event Burn-out in Power Diodes

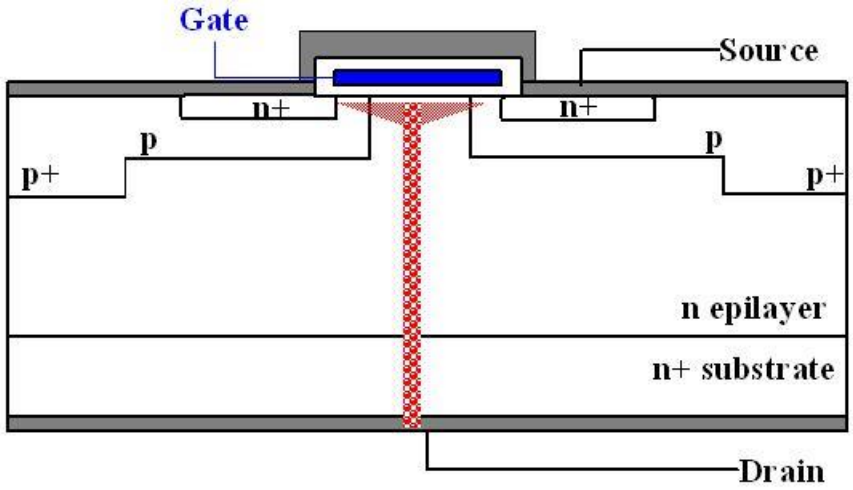
- Schottky power diodes have shown a sensitivity to SEB at high reverse voltage.



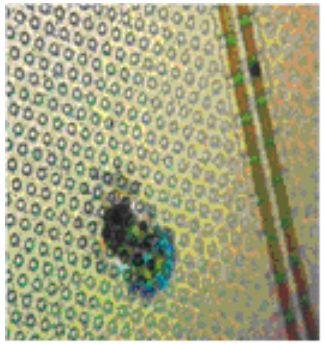
- A derating of 50% of V_{RRM} is usually recommended for every unqualified Si Schottky power diode.

Single Event Gate Rupture

- Single Event Gate Rupture
  - Destructive event
  - SEGR is the dielectric breakdown of a power mosfet gate
  - Occurs in N-channel and P-channel power mosfet
  - Sensitive at blocked/over-blocked state

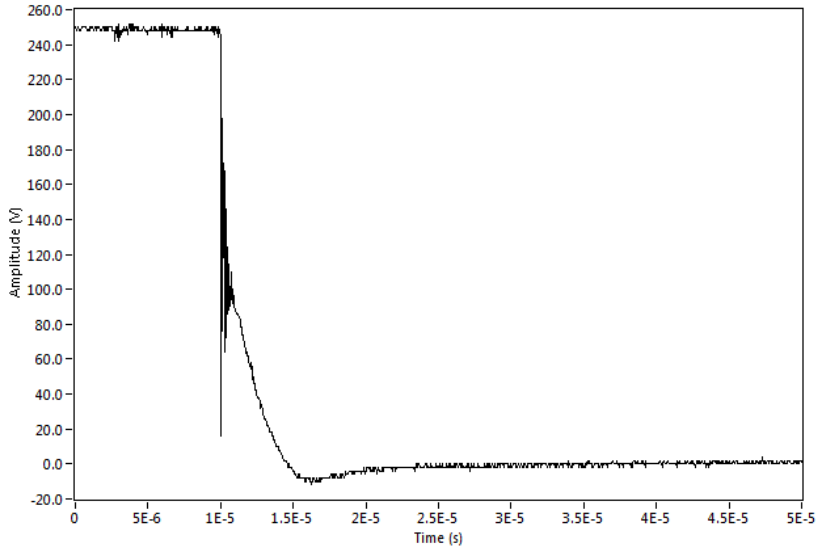


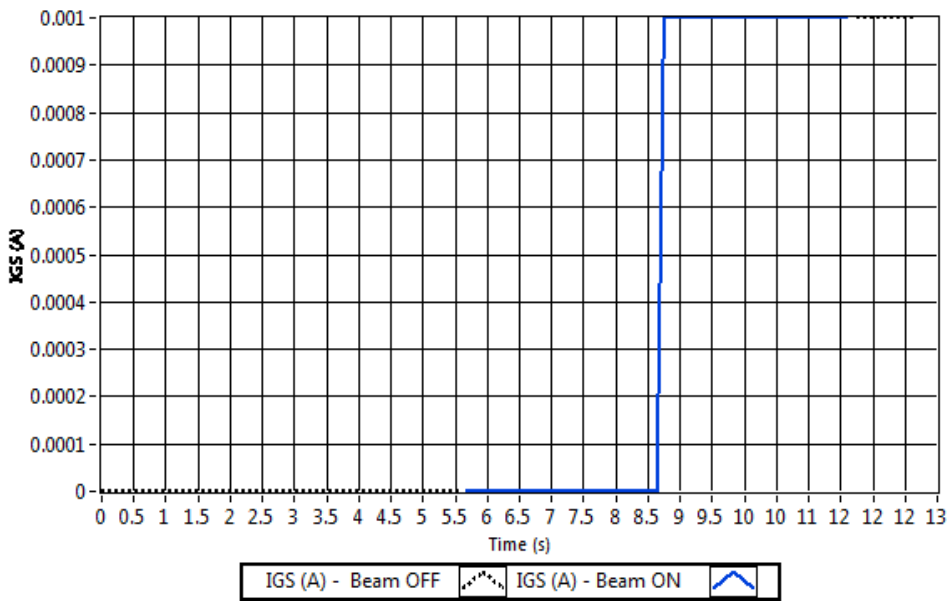
- Excess of charge accumulated under the gate
  - Excess electric field
  - Oxide breakdown



Type of events

- Example: Power MOSFET
  - SEB and SEGR
    - Strongly dependent to the biasing
    - Penetration of the particles → all the collection region needs to be adressed





SEB/SEGR Mitigation

- Derating rules are used to protect components against SEB and SEGR
  - Derating rules are described in the ECSS documents
  - Acceptable evaluation phase data will give drain-to-source threshold voltages ($V_{DS(th)}$) versus LET and gate-to-source voltage (V_{GS})

- Worst case $V_{GS(th)}$ will be defined

Ion	LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	VDS(V) @VGS=0V	@VGS=-5V	@VGS=-10V	@VGS=-15V	@VGS=-20V
Cu	28	285	43	100	100	100	80	60
Br	36.8	305	39	100	90	70	50	—

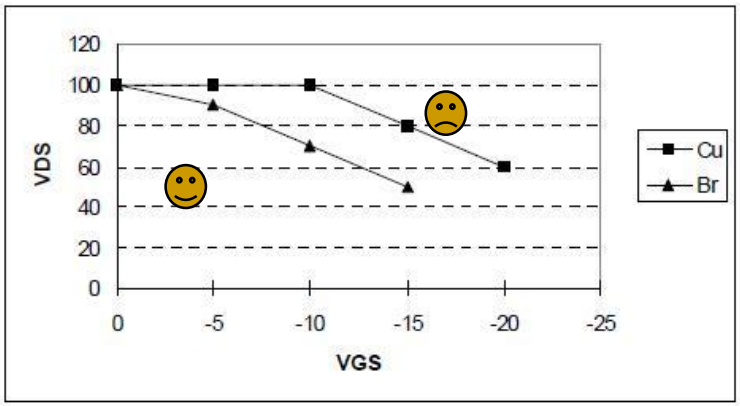


Fig a. Single Event Effect, Safe Operating Area

SEB/SEGR Mitigation

- The derating consists of maintaining Vds within safe operation limits over the full design life time as
  - VDS ≤ 0.80.VDSth(WC), with |VGS| < |VGSmax| used during testing for VDSth(WC) estimate
  - Ttest < Tcase where Ttest is the case temperature used during testing, for VDSth (WC) estimate

- Then if no data or not enough data are available, testing is required
  - Bias for the application or SOA
  - Minimum range (ESA recommendations)

Max rated Vds (V)	Minimum ion range (µm)
Up to 100	60
101 to 200	90
201 to 400	150
401 to 1000	200

- Derating rules are possible for discrete power devices only, they are not appropriate for SEGR or SEB in integrated circuits

- As for SEL, the circuit design may also include protection measures to circumvent SEB (drain voltage cycling, limitation of the current available, etc)
  - No protections for SEGR