Precision Timing at High-Luminosity LHC with the CMS MIP Timing Detector

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CHANG-SEONG MOON

CENTRE FOR HIGH ENERGY PHYSICS (CHEP), KYUNGPOOK NATIONAL UNIVERSITY (KNU)

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High-Luminosity LHC at CERN

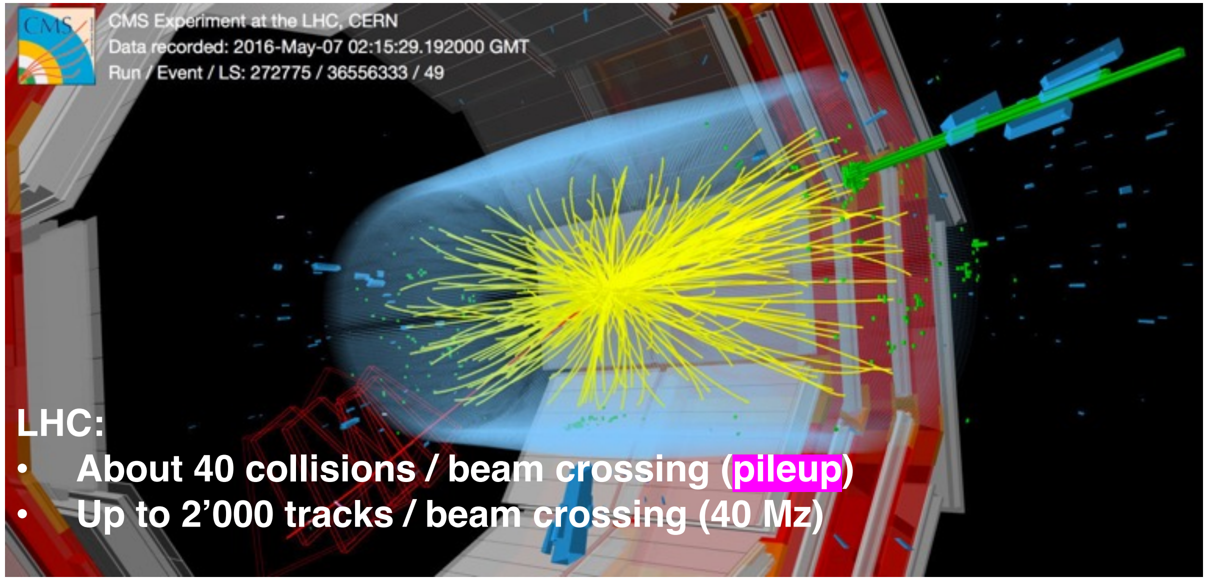
Goal: precision tests of the standard model and Higgs physics, and searches for (rare) BSM phenomena

- **Precision measurement of Higgs boson couplings** (few percent)
- Measurement of the **Higgs boson self-coupling** via direct observation of the di-Higgs boson production
- Search for heavy **dark matter candidates, SUSY particles, new gauge bosons, Long-Lived Particles**, …

Means: upgrade of the LHC optics and injectors to increase the beam intensity

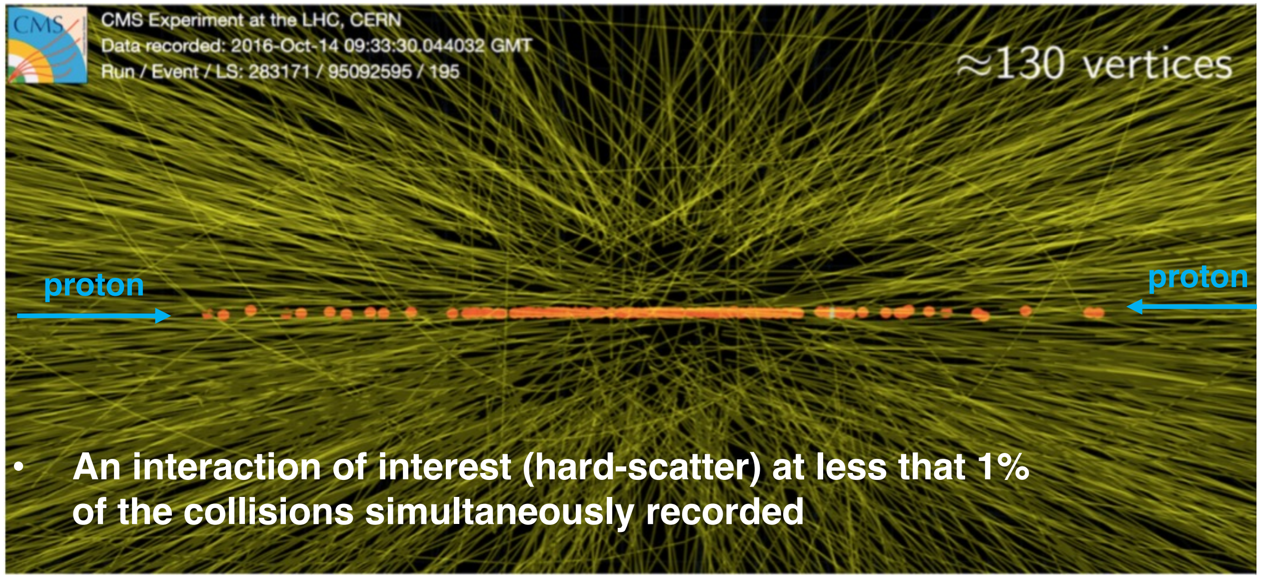
- Luminosity delivered by **LHC** (2009-2025): **~ 400 fb^{-1} / experiment** *[~250 fb^{-1} collected so far]*
- Target luminosity for **HL-LHC** (2029-2042): **>3000 fb^{-1} / experiment** ***[one year of HL-LHC equivalent to ~10 years of LHC]***

Collision event with 35 reconstructed vertices



LHC:
- **About 40 collisions / beam crossing (pileup)**
- **Up to 2’000 tracks / beam crossing (40 Mz)**

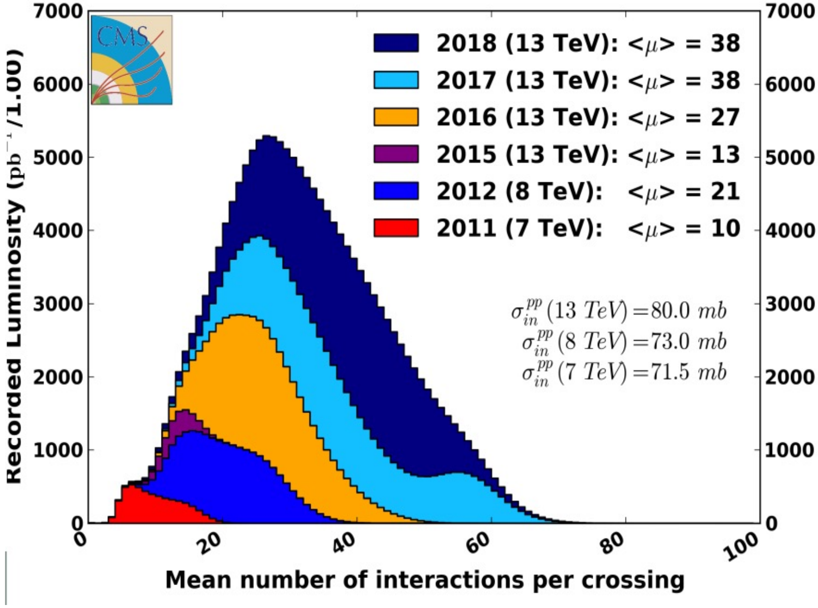
Real life event at the LHC emulating HL-LHC conditions



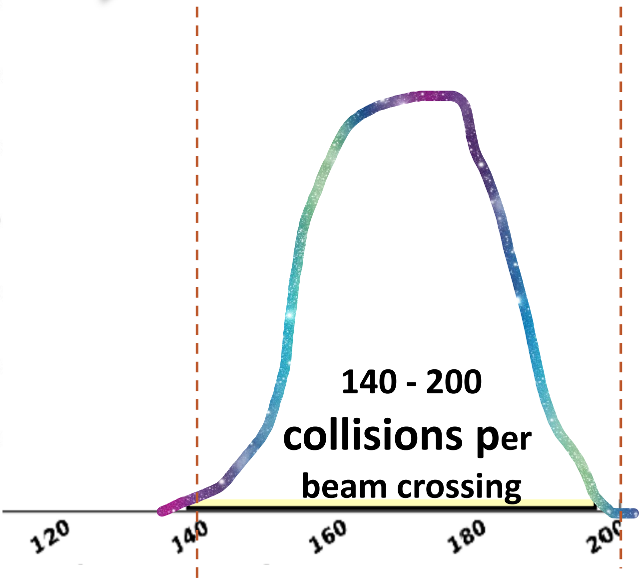
- **An interaction of interest (hard-scatter) at less that 1% of the collisions simultaneously recorded**

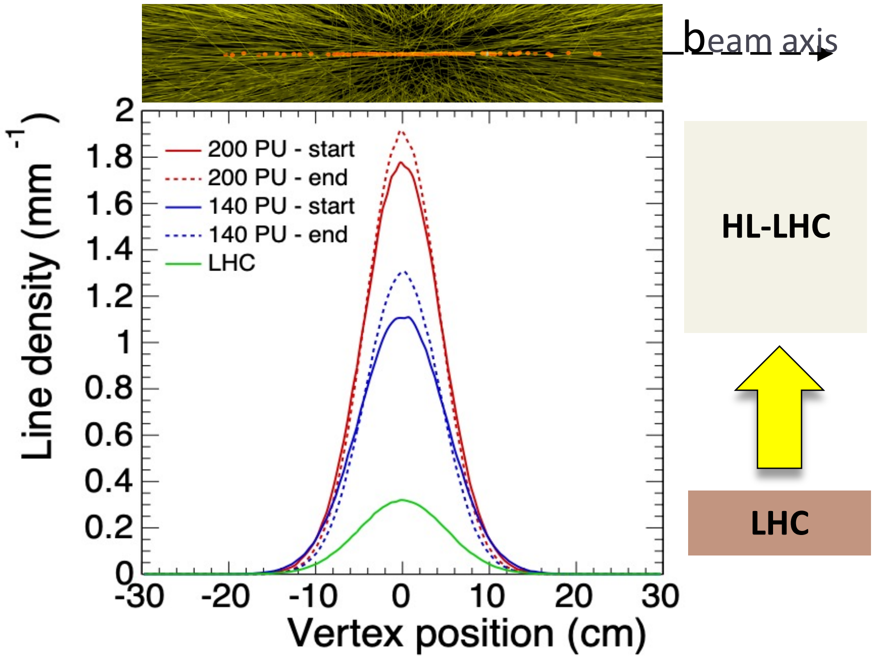
HL-LHC: experimental challenges

CMS average pileup at LHC



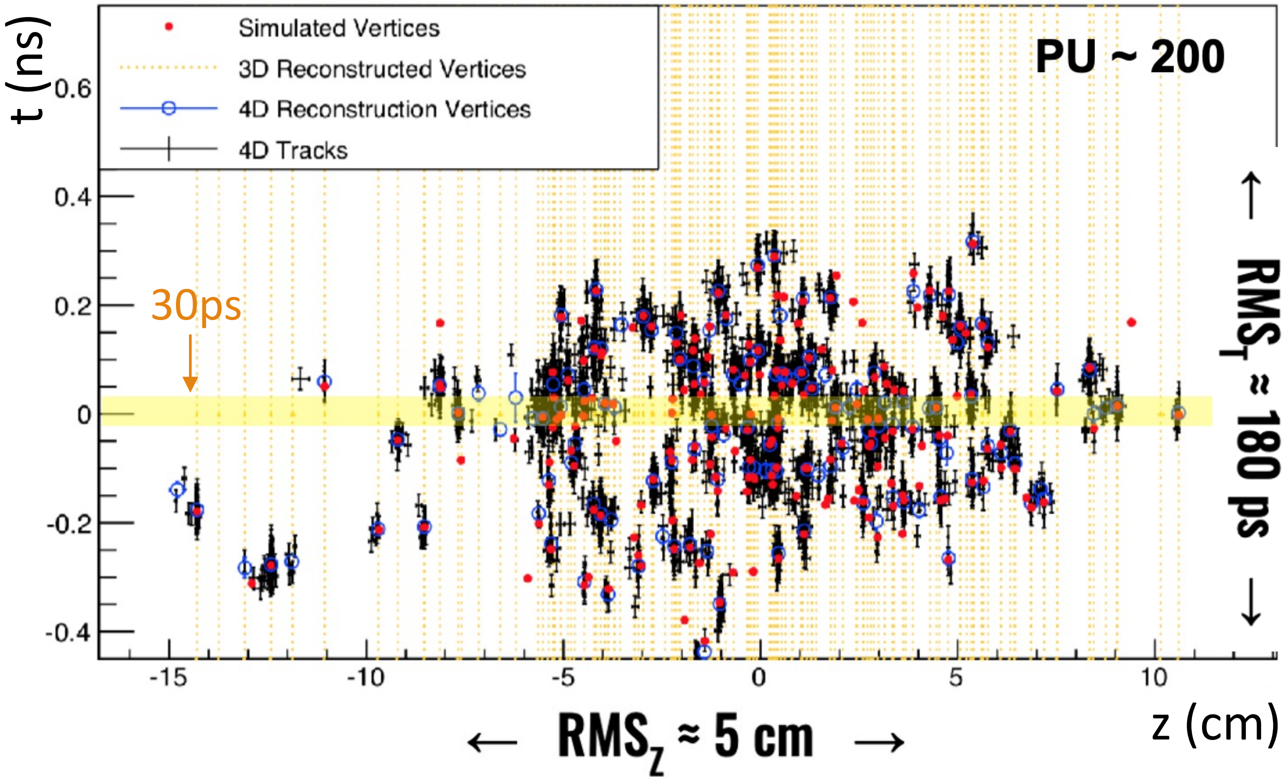
HL-LHC

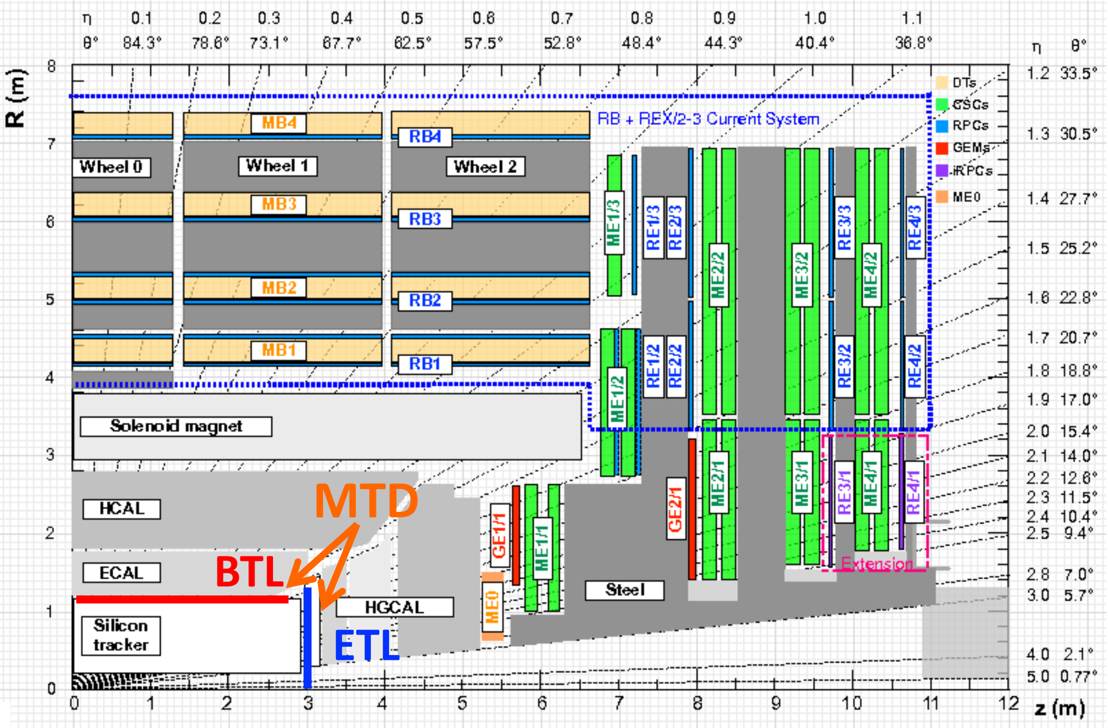




- Detector upgrades required to deal with enhanced pileup interactions and radiation damage levels
  - >5x collision events per beam crossing, **same spatial spread of the vertices along the beam lines**
  - Up to **200 pileup events**, about **10’000 tracks per event**, and vertex densities >1.5 mm^{-1}
- Reconstruction quality depends on *track-vertex assignments,* which become ambiguous when track resolution is comparable to vertex separation
  - Vertex merging, fake association of “pileup” tracks with vertices, final state kinematics distorted, jet, lepton, photon identification affected

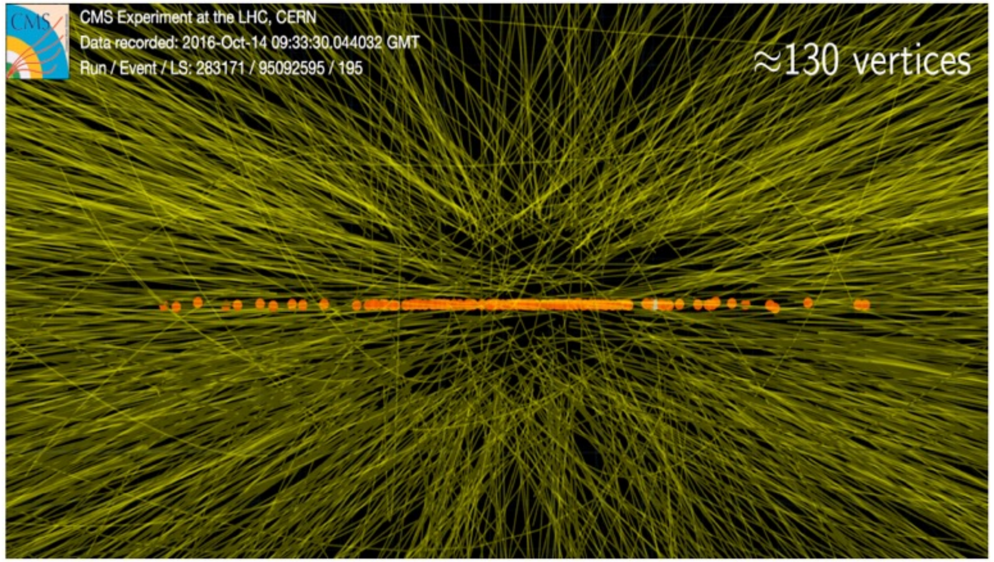
MIP Timing Detector (MTD) for CMS Phase-2 Upgrade

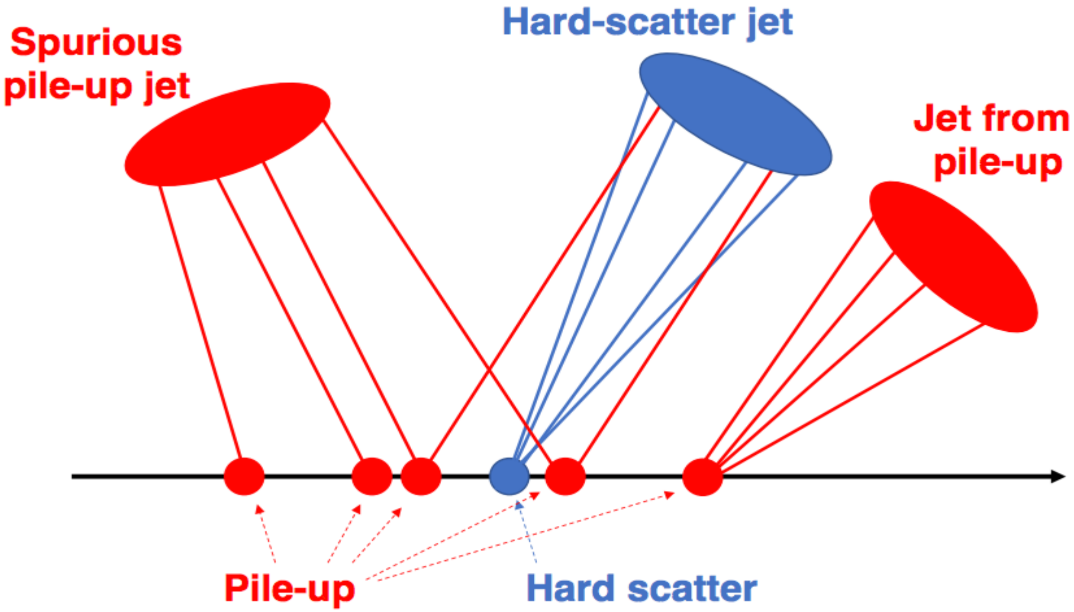




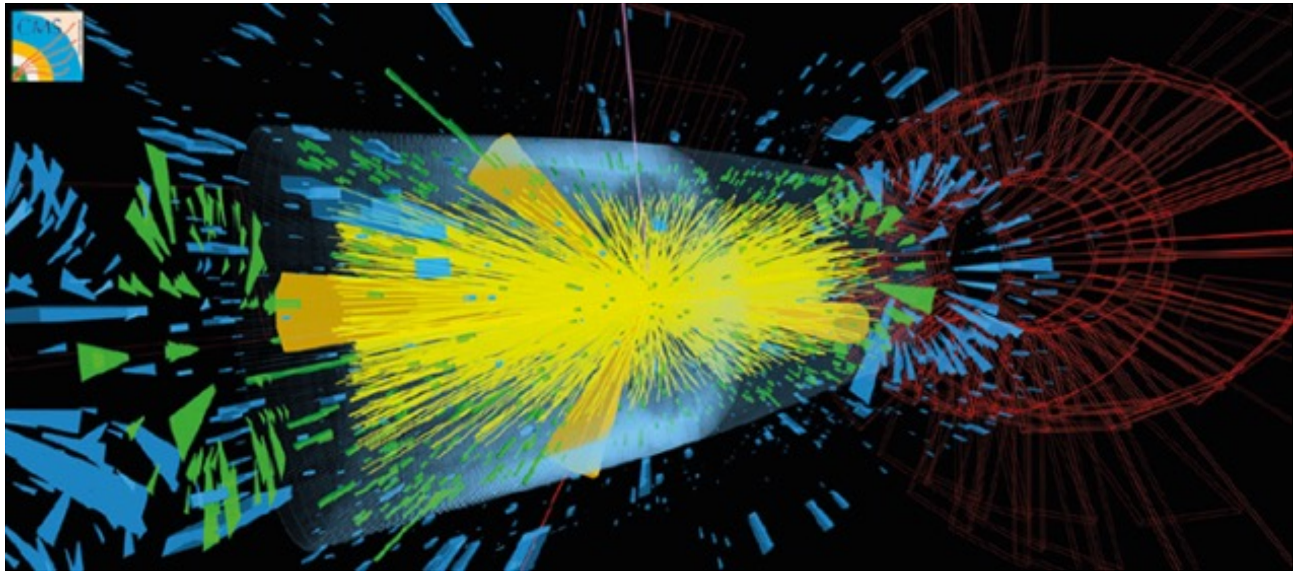
- Important to maintain detector performance during HL-LHC running
  - Time information will help to reduce pileup effects from approximately 200 simultaneous interactions
- MIP timing detector (MTD) consists of barrel timing layer (BTL) and endcap timing layer (ETL), providing 30-50 ps time resolution per track
  - BTL: LYSO crystal scintillator + SiPM readout
  - ETL: Silicon based sensor (LGAD) + ASIC readout
  - Two different detector technologies for radiation hardness and costs

MTD Physics motivation: pile-up mitigation



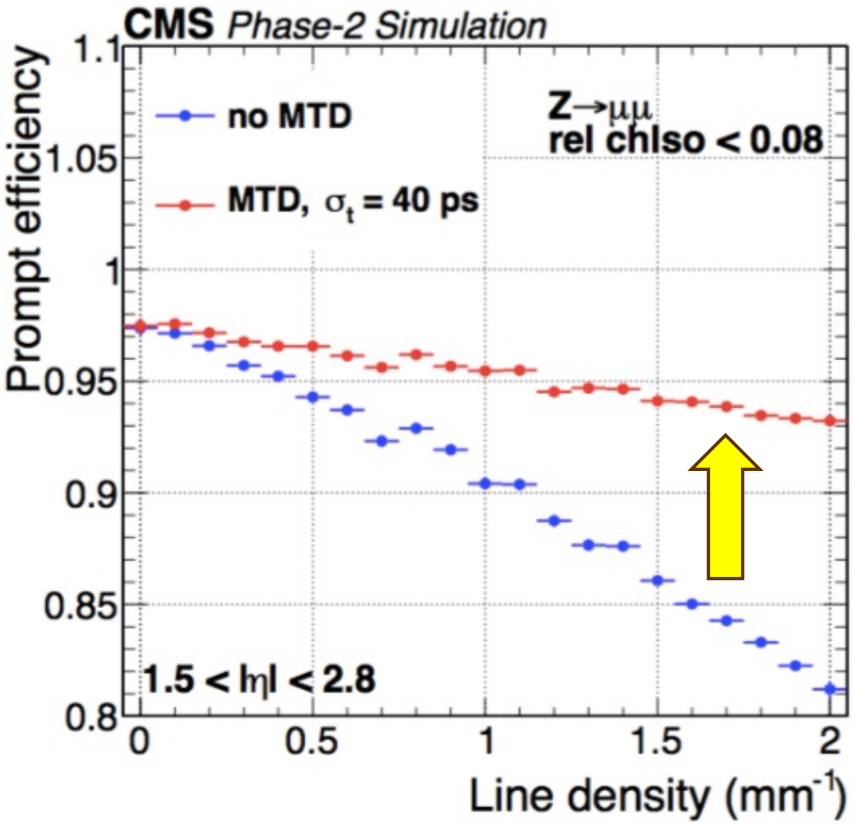


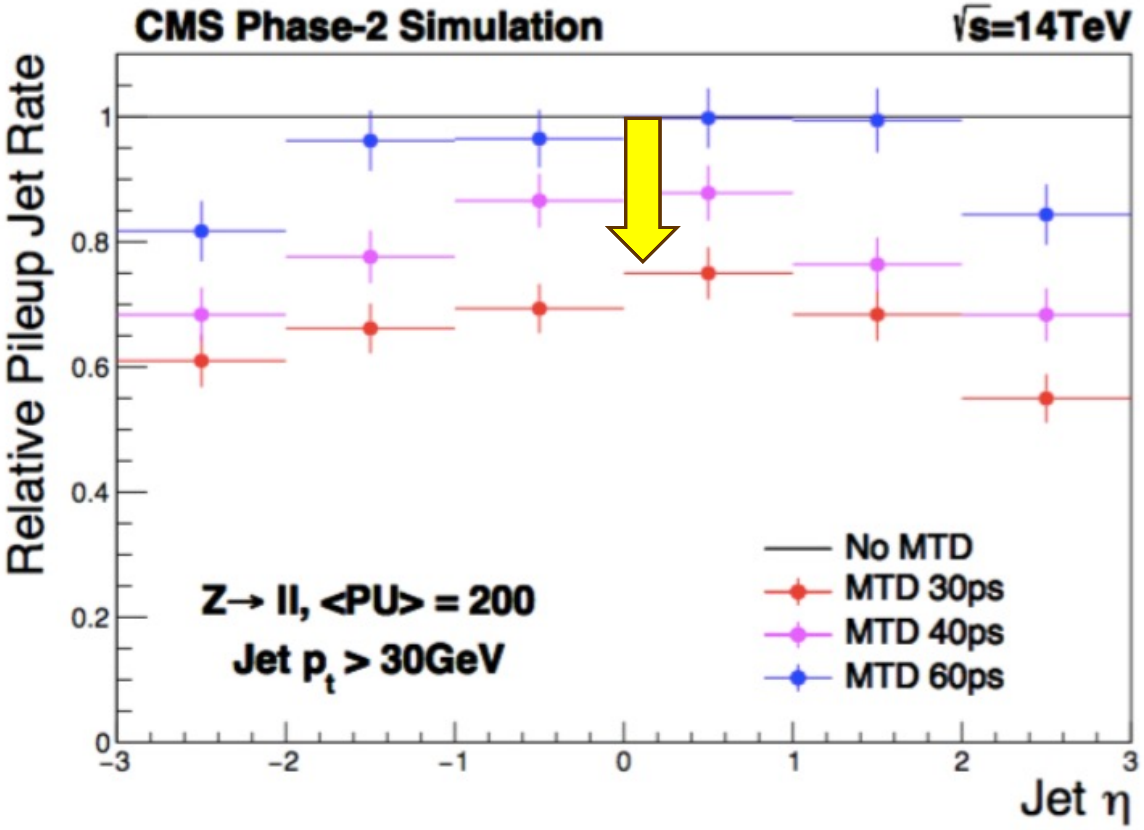
- ❑ Important to maintain detector performance during HL-LHC running
  - ◦ Time information will help to reduce pileup effects from approximately 200 simultaneous interactions



The display of an event with a Higgs boson produced in the VBF process on top of 200 pile-up collisions.

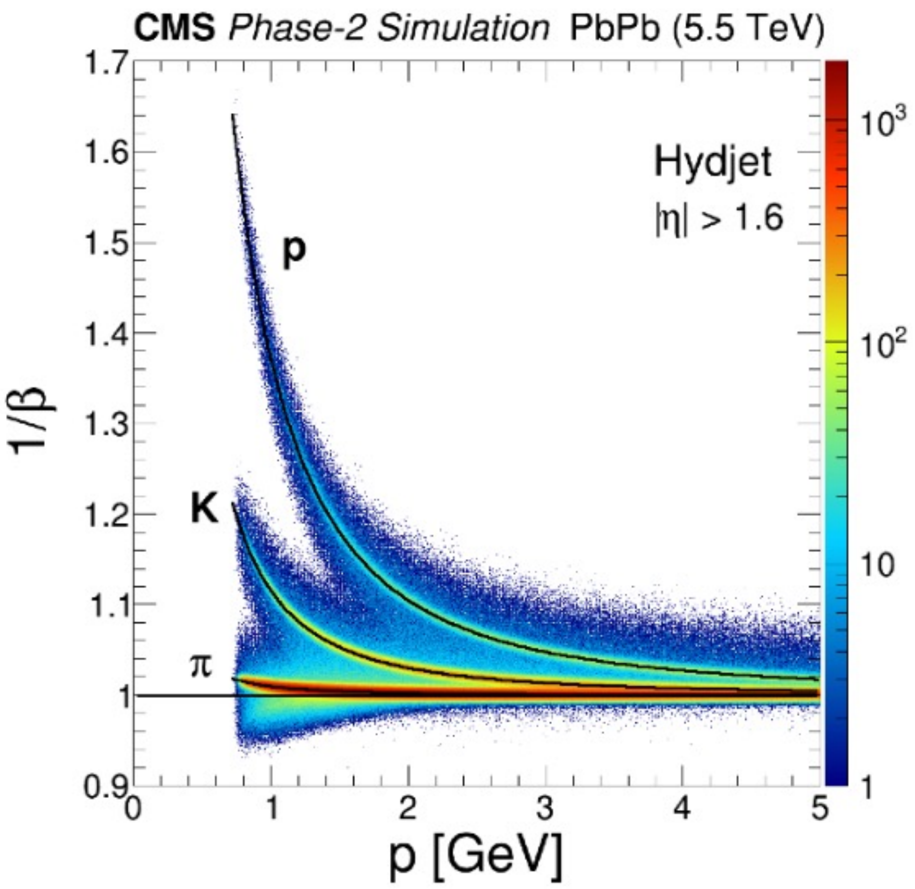
MTD Physics motivation: pile-up mitigation

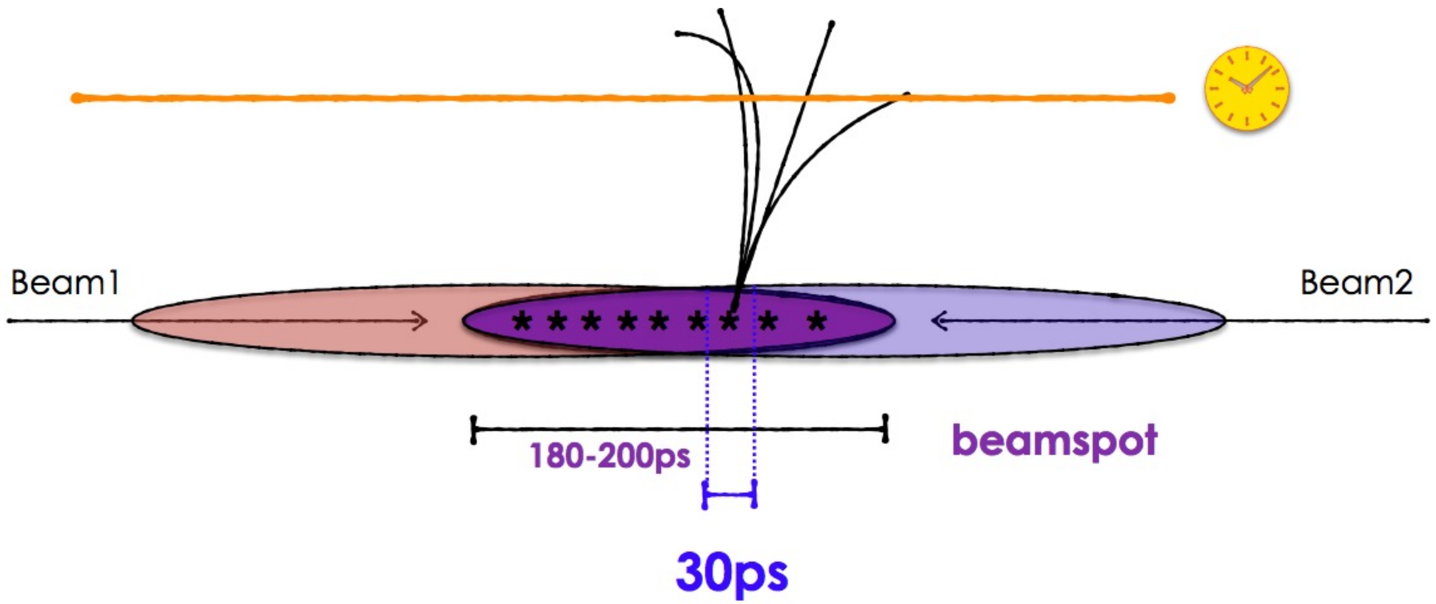




- The mitigation of pile up effect improves all physics objects
- 4D vertexing (position+time) can remove
  - Spurious pileup tracks from “isolation cone” around leptons
  - Rejects spurious jets formed from pileup particles.

MTD Physics motivation: particle ID





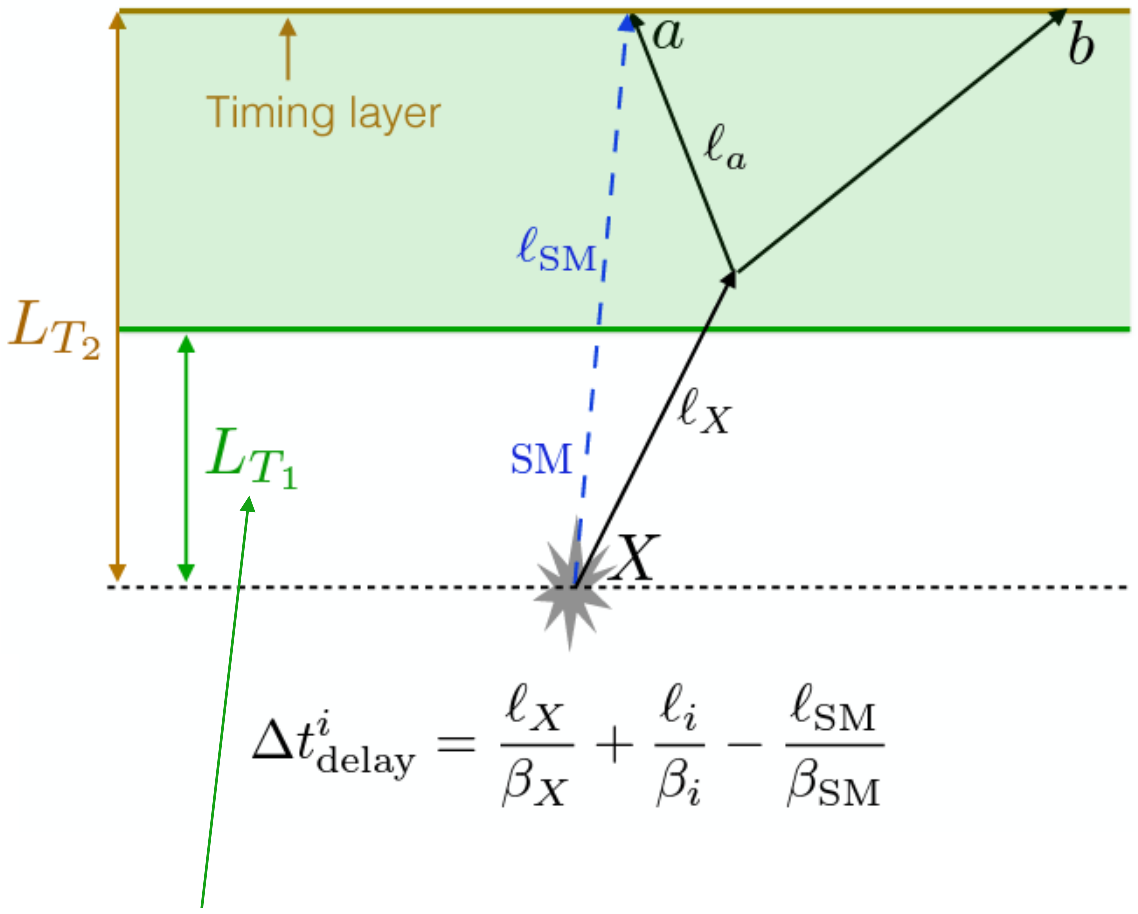
Significant reduction of beamspot uncertainty

- MTD can provide significant improvement for particle ID
  - Heavy ion charm tag
- Significant gains for searches for long-lived new particles

4D vertex reconstruction of primary and secondary vertices

Provides a close kinematic for Long Lived Particles decaying within MTD

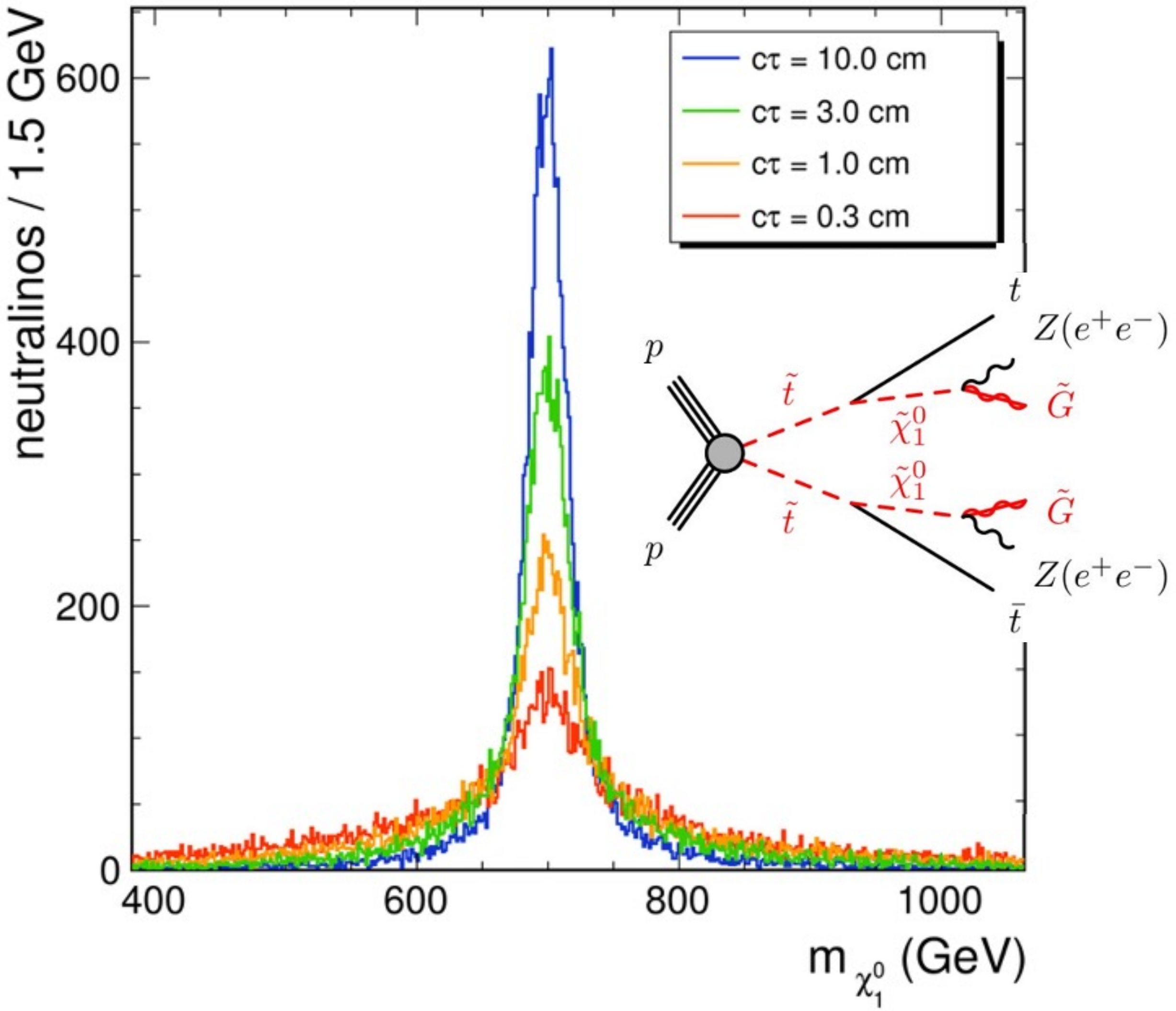
PRL 122.131801



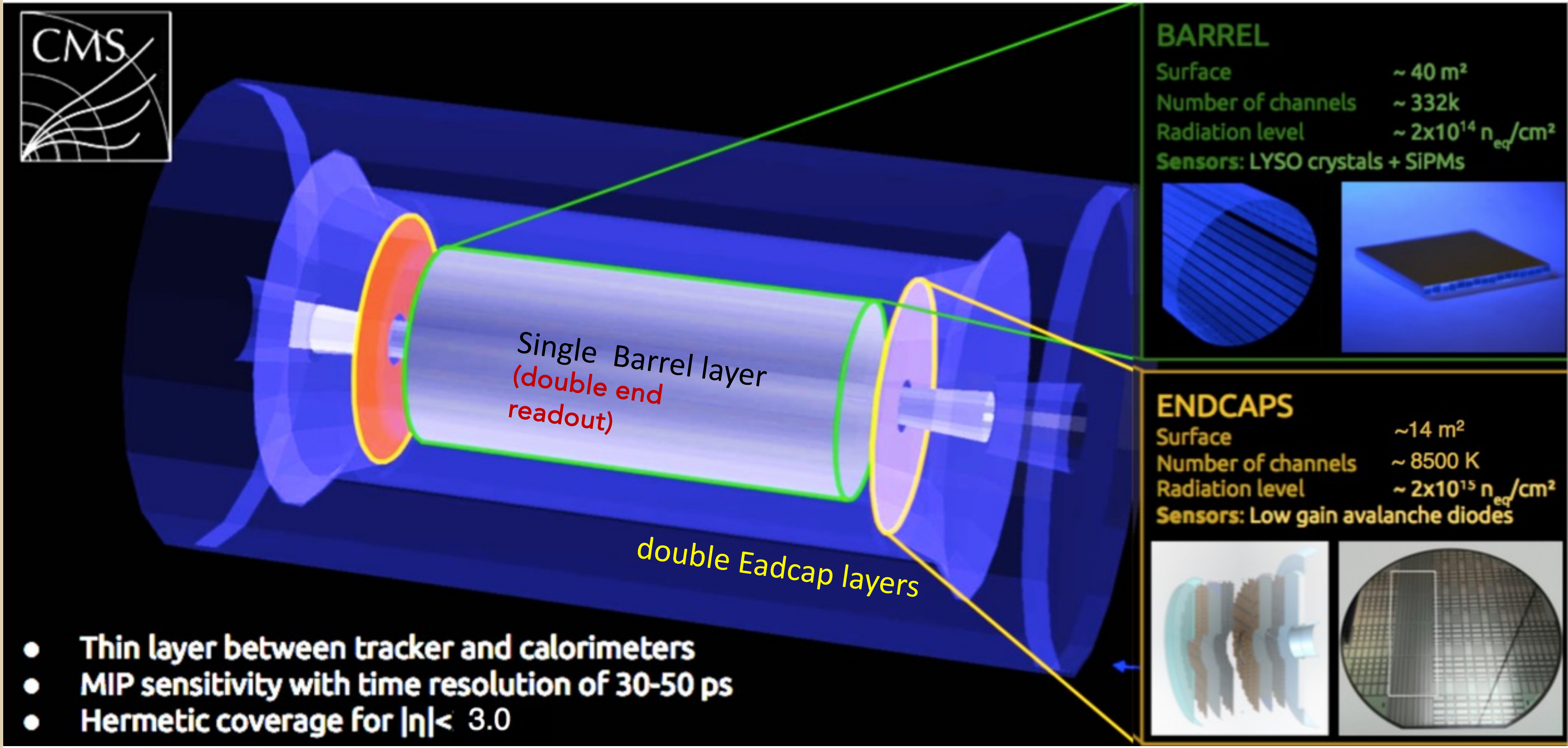
$$\Delta t^i_{\text{delay}} = \frac{\ell_X}{\beta_X} + \frac{\ell_i}{\beta_i} - \frac{\ell_{SM}}{\beta_{SM}}$$

Minimal displacement requirement

700 GeV neutralino (SUSY)



Mip Timing Detector (MTD)


Single Barrel layer

(double end readout)

double Eadcap layers

BARREL

Surface	~ 40 m^2
Number of channels	~ 332k
Radiation level	~ 2x10^{14} n$_{eq}$/cm^2

Sensors: LYSO crystals + SiPMs

ENDCAPS

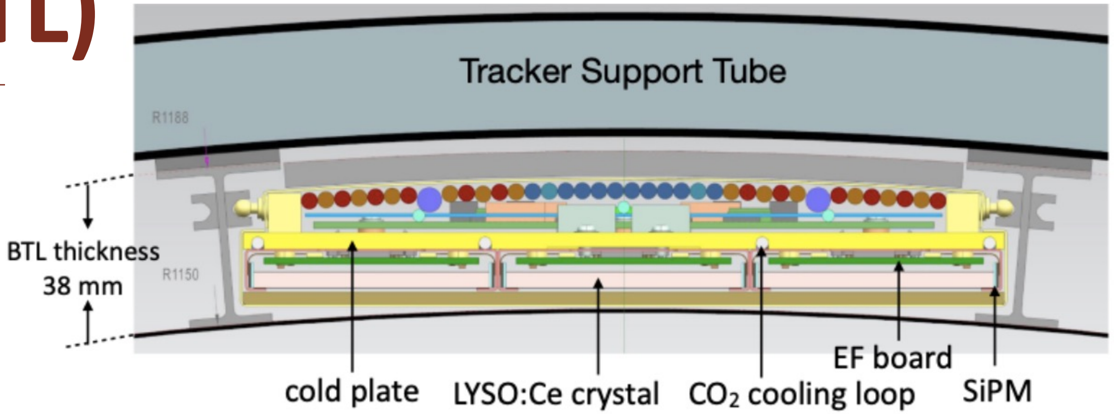
Surface	~14 m^2
Number of channels	~ 8500 K
Radiation level	~ 2x10^{15} n$_{eq}$/cm^2

Sensors: Low gain avalanche diodes

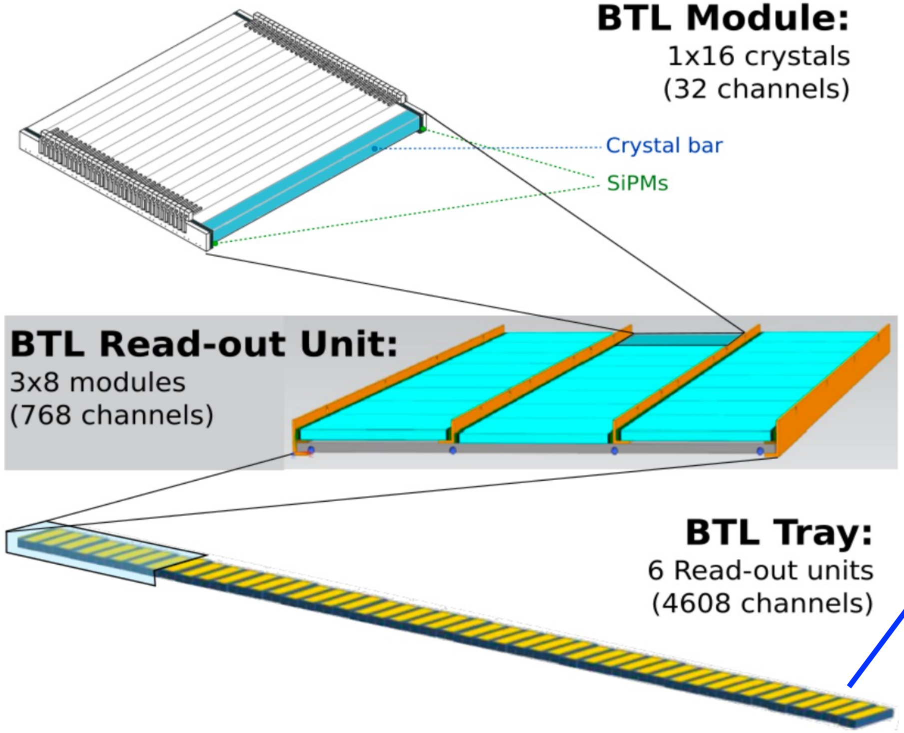
- Thin layer between tracker and calorimeters
- MIP sensitivity with time resolution of 30-50 ps
- Hermetic coverage for $|\eta| <$ 3.0

MTD : Barrel Timing Layer (BTL)

- ❑ 3.8 cm thin cylindrical detector
  - located inside the tracker support tube, |η| < 1.45
  - ~5 m long, 38 m^2 surface



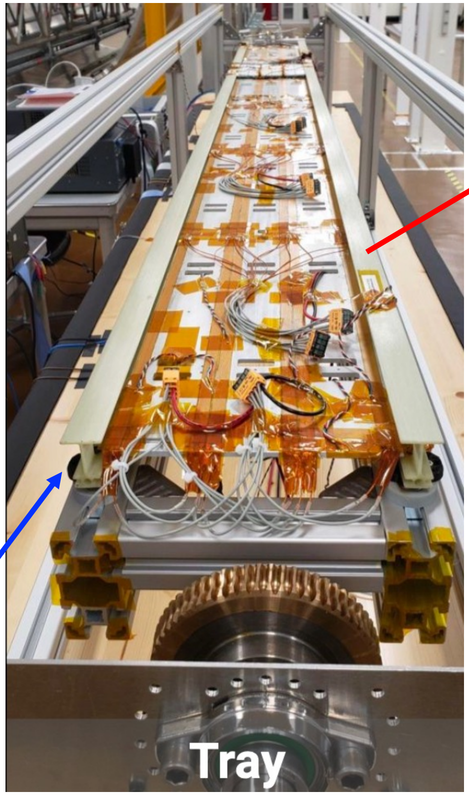
2 SiPMs per crystal



BTL Module:
1x16 crystals
(32 channels)

BTL Read-out Unit:
3x8 modules
(768 channels)

BTL Tray:
6 Read-out units
(4608 channels)



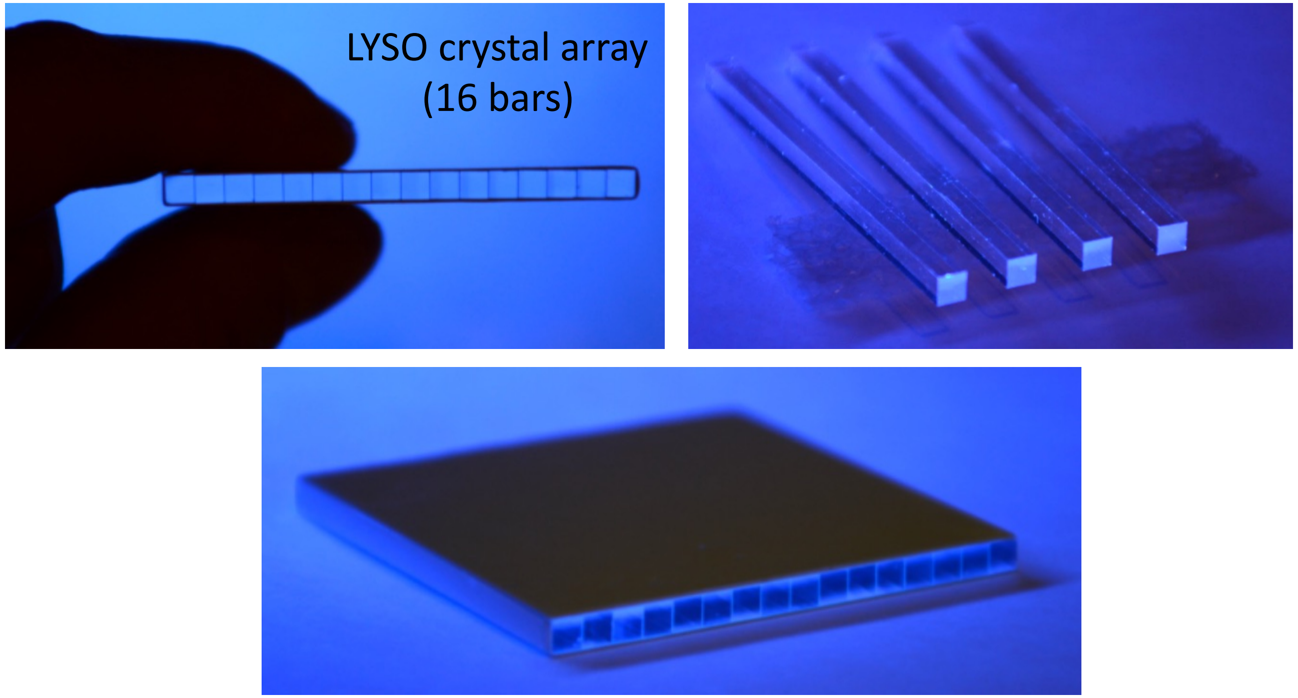
BTL detector
72 trays: 2(z) x 36(φ)
332k channels

- ❑ BTL construction: starting in early 2024!

BTL sensors : LYSO crystal

❑ LYSO crystal bars (166k)

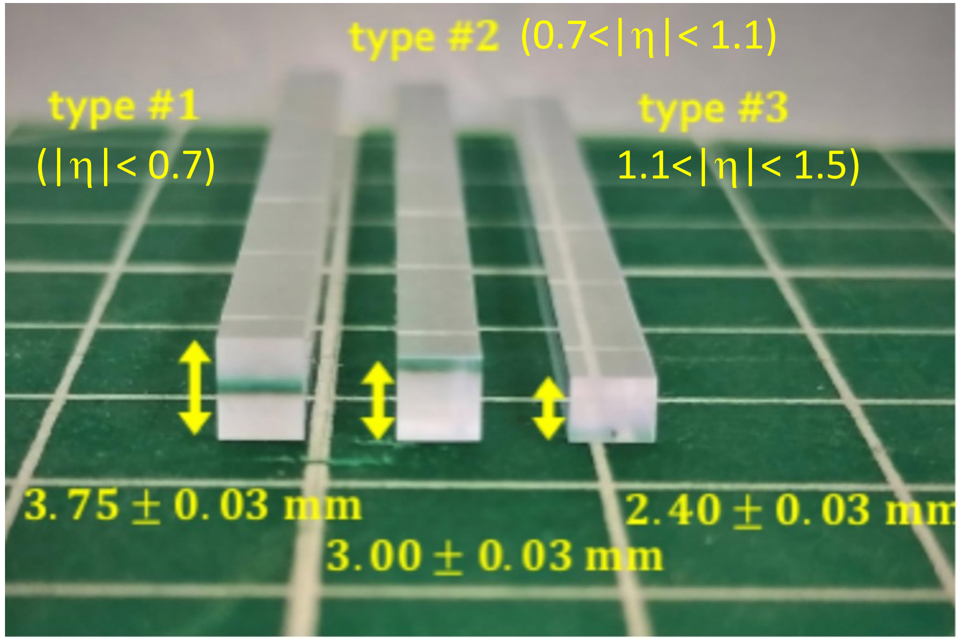
- Cerium-doped lutetium yttrium orthosilicate (LYSO:Ce) scintillation medium
- Well established in PET applications and vendors widely available
- High radiation tolerance
- τ_{rise} : ~100 ps, τ_{decay} : ~ 40 ns
- High Light Yield : 40000 γ/MeV



❑ LYSO current status

- Single vendor selected
  - ➢ Considerably better offer
  - ➢ One of best vendor for performance-wise
  - ➢ Reliable vendor (large production capacity)
- Pre-production in progress
  - ➢ Ordered in March (2% of the total LYSO arrays)
  - ➢ QA/QC and construction database ready

Maximize the crystal light output for 3 η regions



BTL sensors : SiPM

❑ SiPM (166k x 2 = 332k channel)

- Well consolidated technology
- Photon Detection Efficiency (PDE) : 20–40%
- Compact, robust, insensitive to magnetic fields
- Good radiation hardness
- Fast recovery time <10 ns
- High dynamic range (10^5)

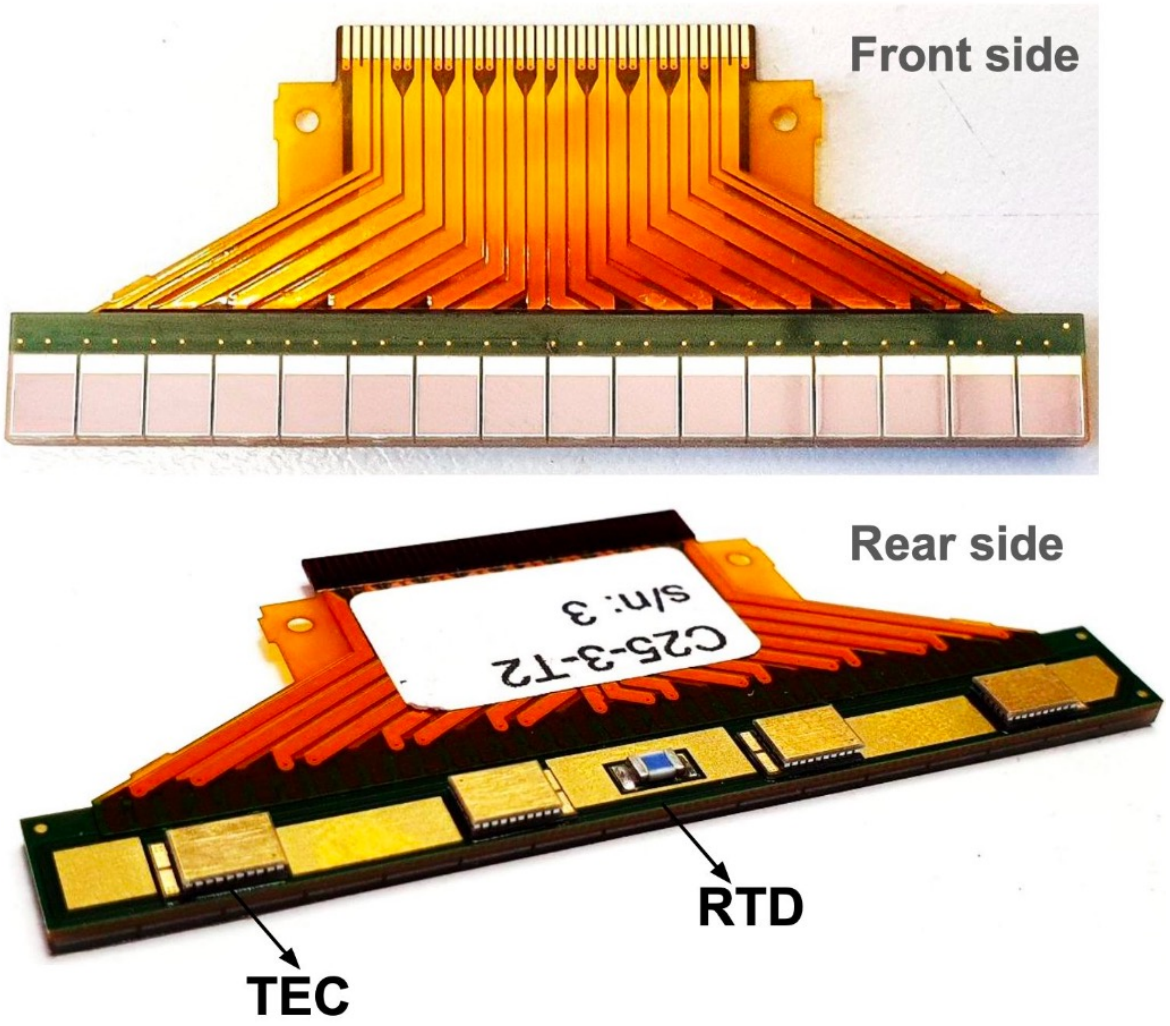
❑ SiPM current status

- Optimized cell size (25 µm) as a default for BTL
    - Additional performance gain to boost signal
- SiPM die size (3.8×2.9 mm^2) fixed to match with the thickest LYSO geometry

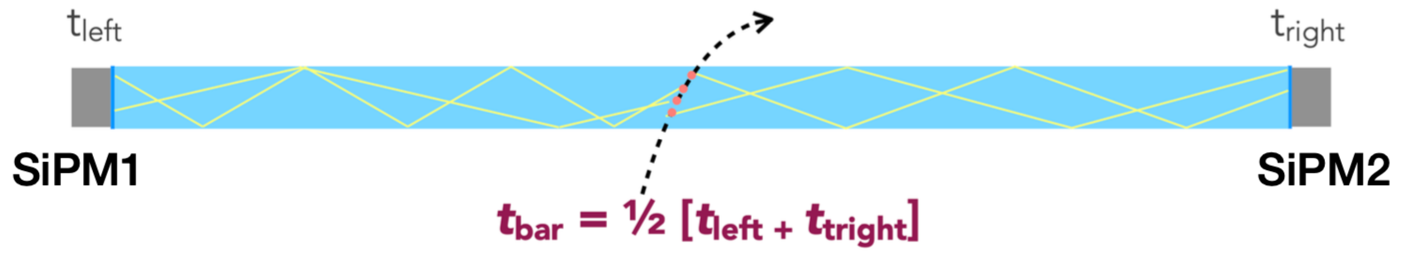
❑ SiPM plans

- Tender starts in July
- Sign the production contract in September
- First batch delivered ~ Feb. 2024 (for 7 months)

SiPM Module



BTL sensors : LYSO crystal and SiPM

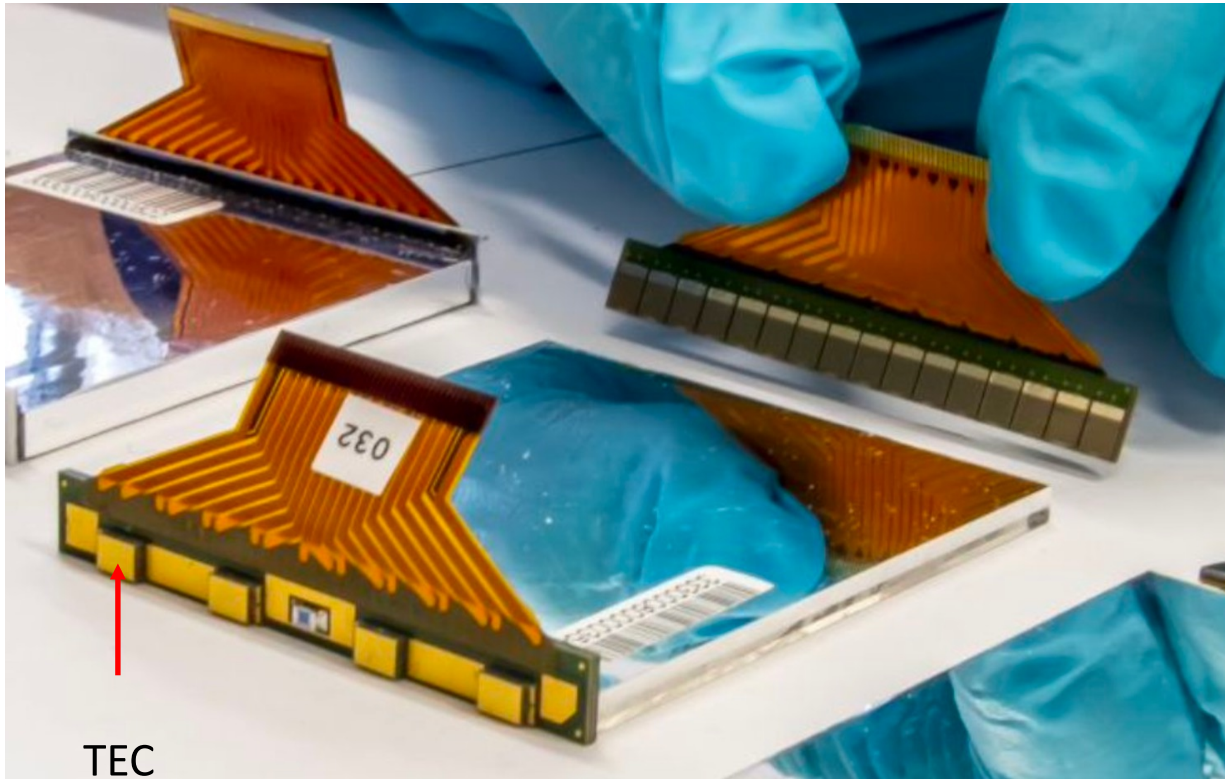


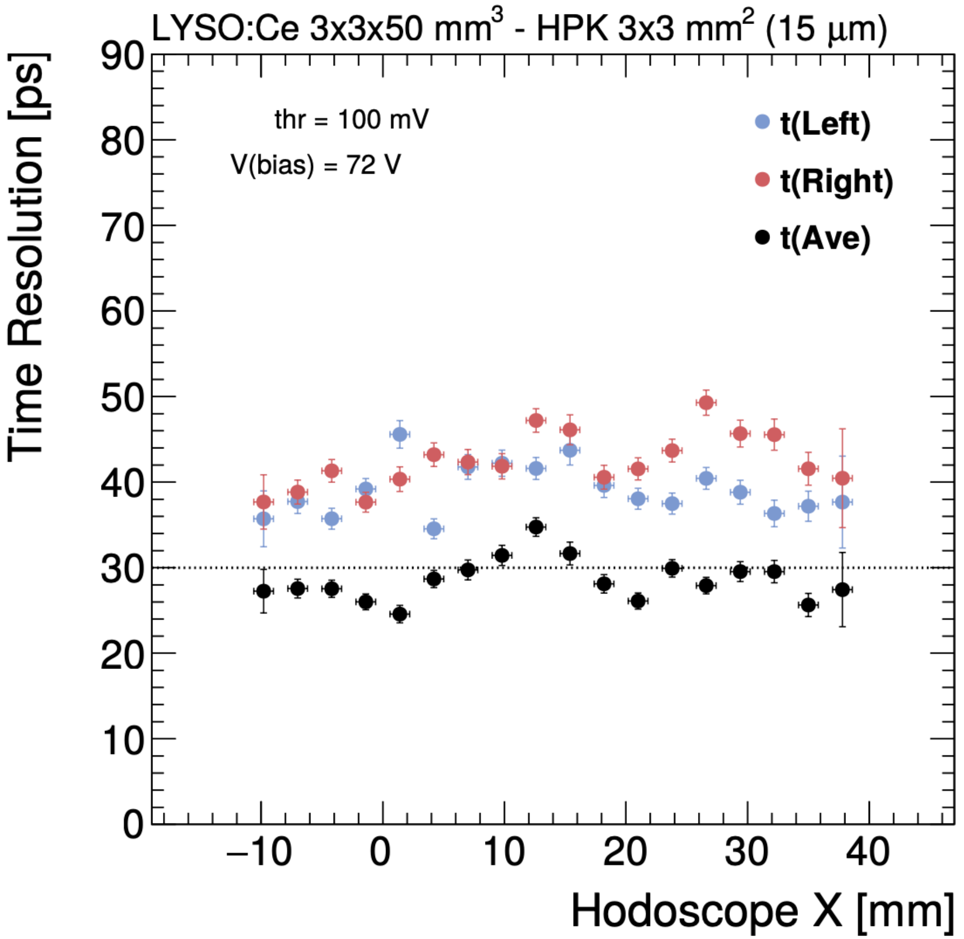
$t_{bar} = ½ [t_{left} + t_{right}]$

LYSO bars with double end readout:

- Improve timing resolution by a factor of $\sqrt{2}$ than single-end

Sensor Module (LYSO + SiPM & TEC)





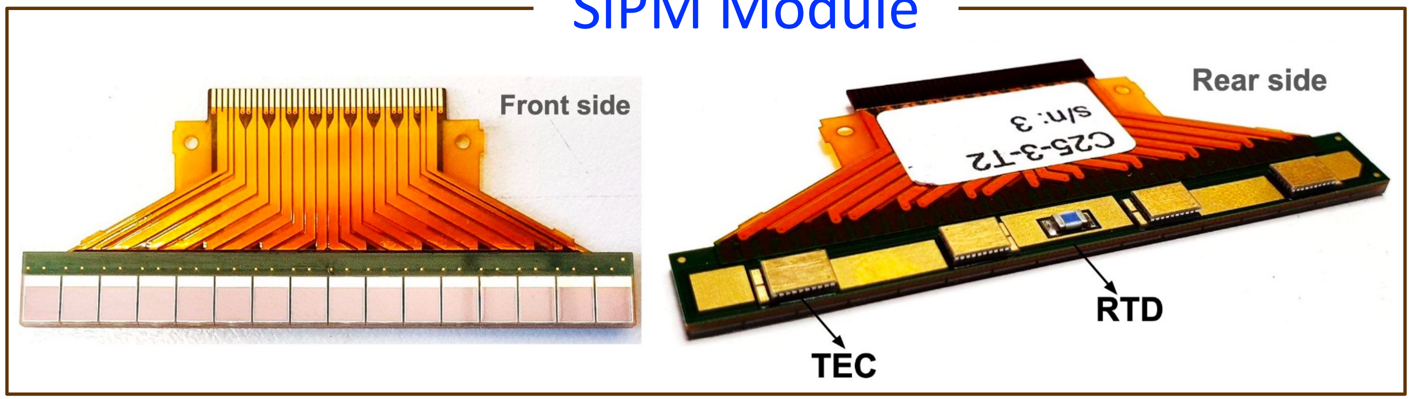
BTL Performance Optimization

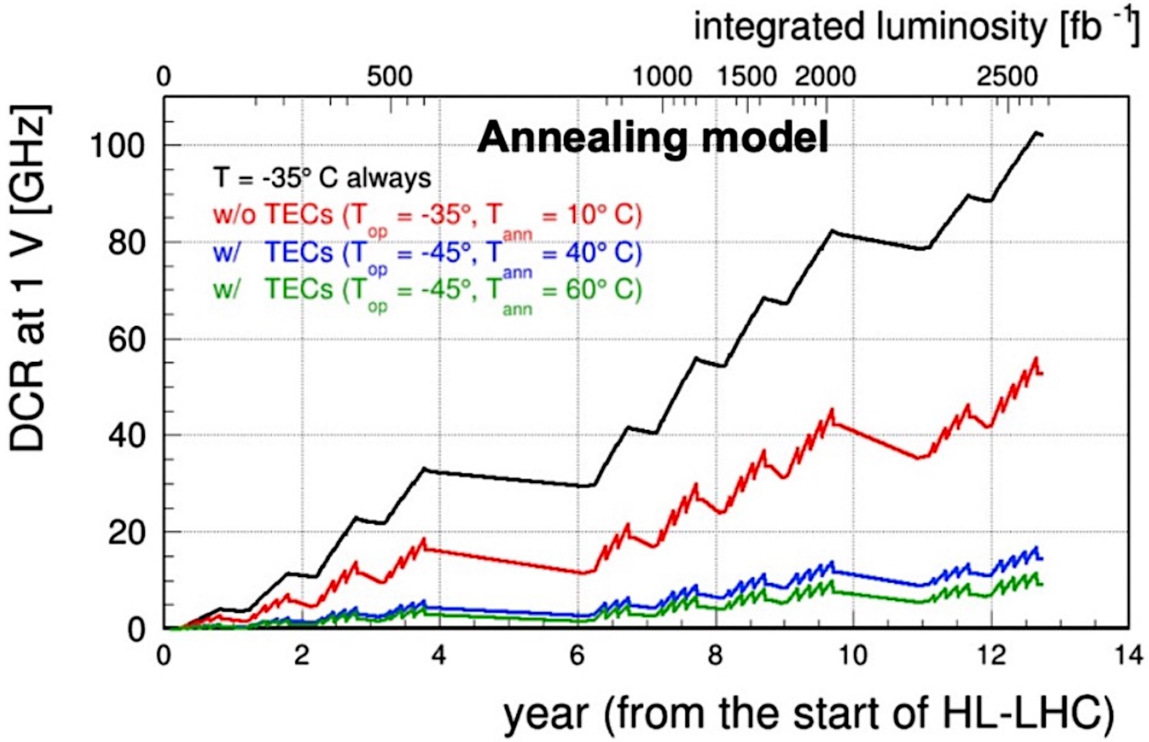
- A dark count in the SiPM corresponds to a single cell firing due to a thermally generated electron
- The dark count rate (DCR)
  - Proportional to the active area of the SiPM
    - **Lowering $V_{\text{over voltage}}$** and **optimizing S/N ratio**

      ~ factor 2 less DCR
  - Decreasing at lower temperatures by about a factor two every 7–10 ◦C
    - Further lowering SiPM's temperature to **-45°C** using **Thermoelectric coolers (TEC)**

      ~ factor 2-3 less DCR
  - Increasing with radiation damage
    - **Annealing** at room **+65 °C** during LHC shutdown and technical stops ~ factor 2 less DCR
    - **Noise filtering** with signal processing technique DLED in TOFHIR ~ factor 2 less DCR

SiPM Module

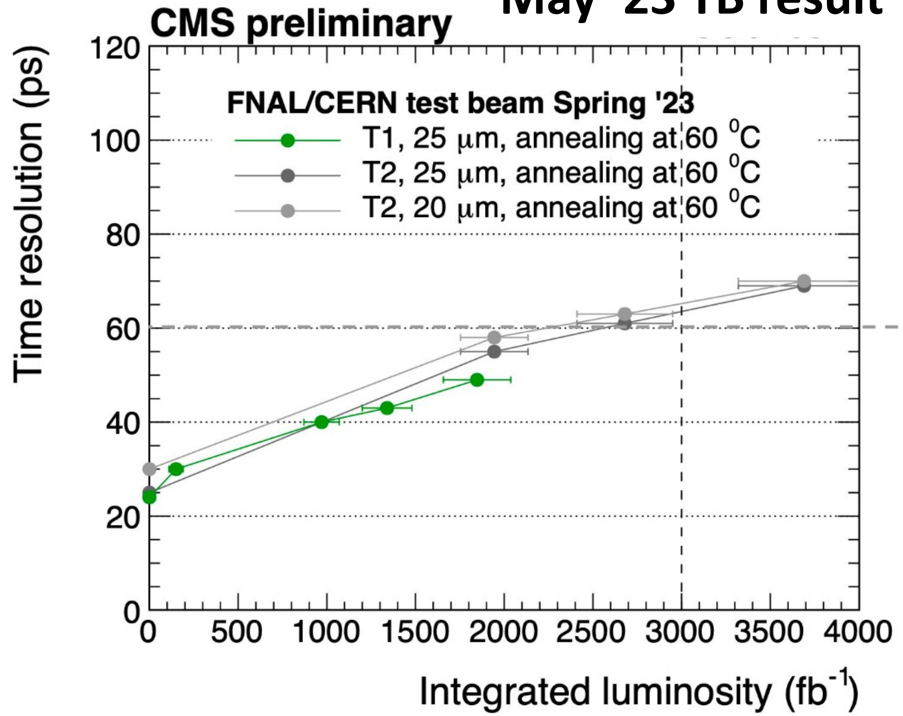




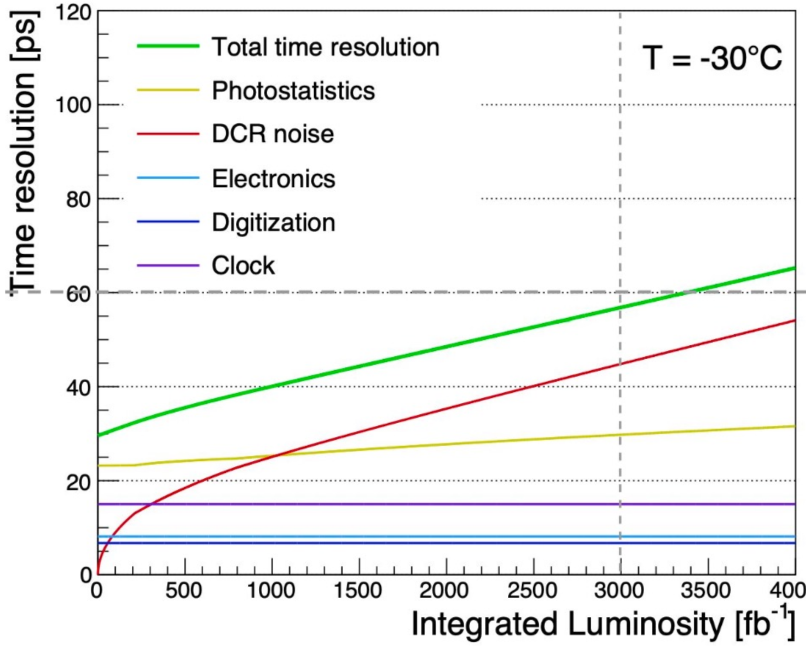
The BTL prototyping phase is completed

- **Changing configuration of BTL with respect to the TDR (Almost same performance!)**
  - Smart thermal management with TECs (additional cooling and annealing)
  - SiPM cell size choice : 25 µm for boosting signal
  - Thicker LYSO arrays for larger energy deposits
  - TOFHIR2C optimization for electronic noise reductions

May ‘23 TB result



CMS MTD TDR

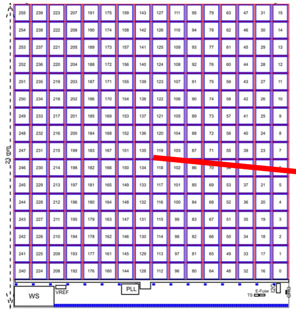


close to TDR performance

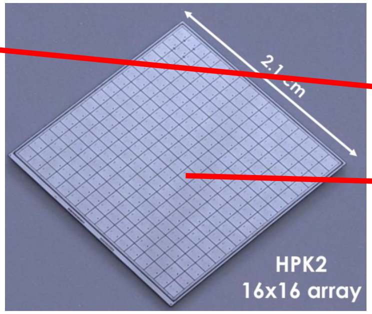
- Ready for starting procurement and the production & assembly phase

MTD Endcap Timing Layer (ETL)

- Two double- sided disks for each side
  - Maximize geometrical acceptance (85% per disk)
  - Coverage : $1.6 < |\eta| < 3.0$
  - Average of 1.8 hits per track
  - **Time resolution per track < 35 ps**
    - based on single hit resolution < 50 ps
- Low-Gain Avalanche Diode (LGAD) sensor bump bonded readout ASIC (ETROC)

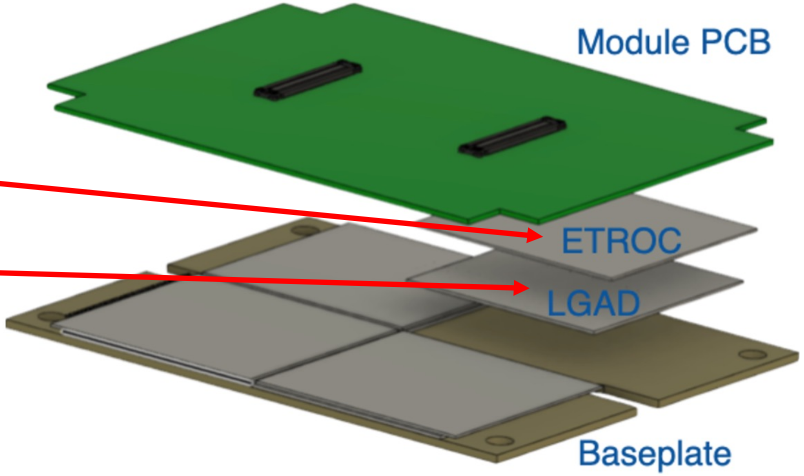


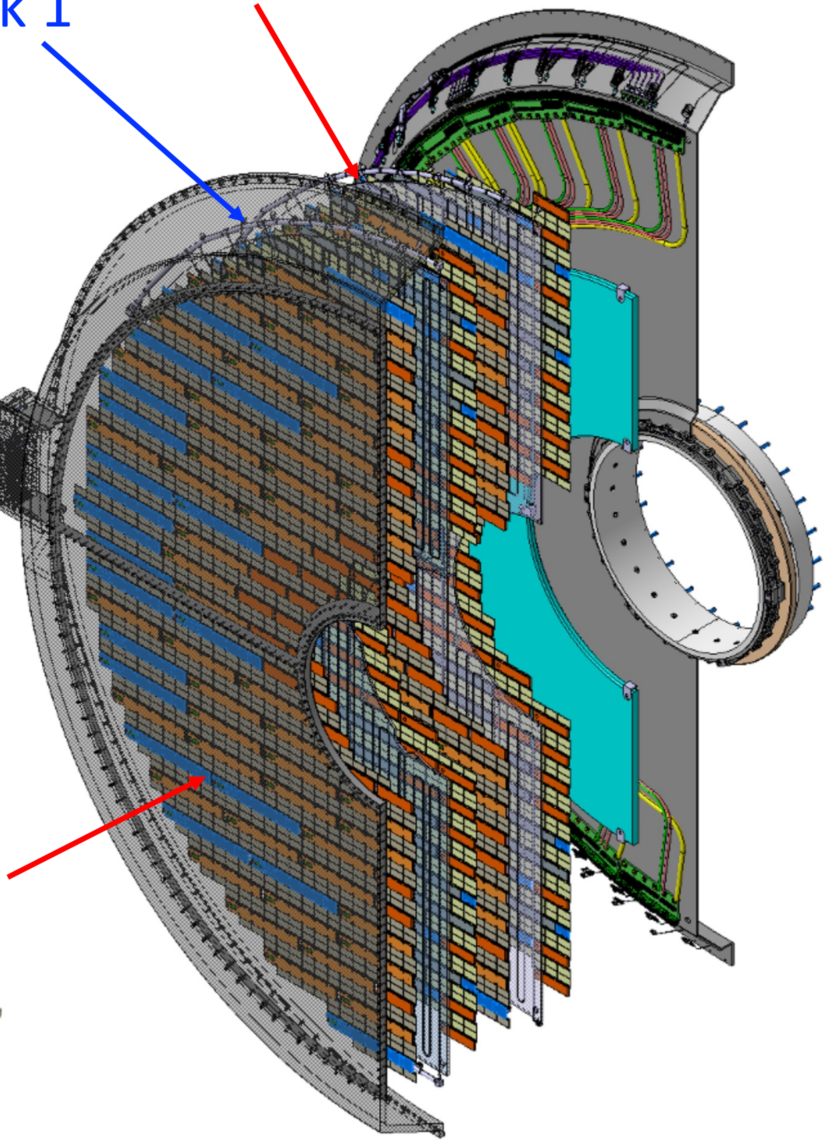
ETROC (ASIC)



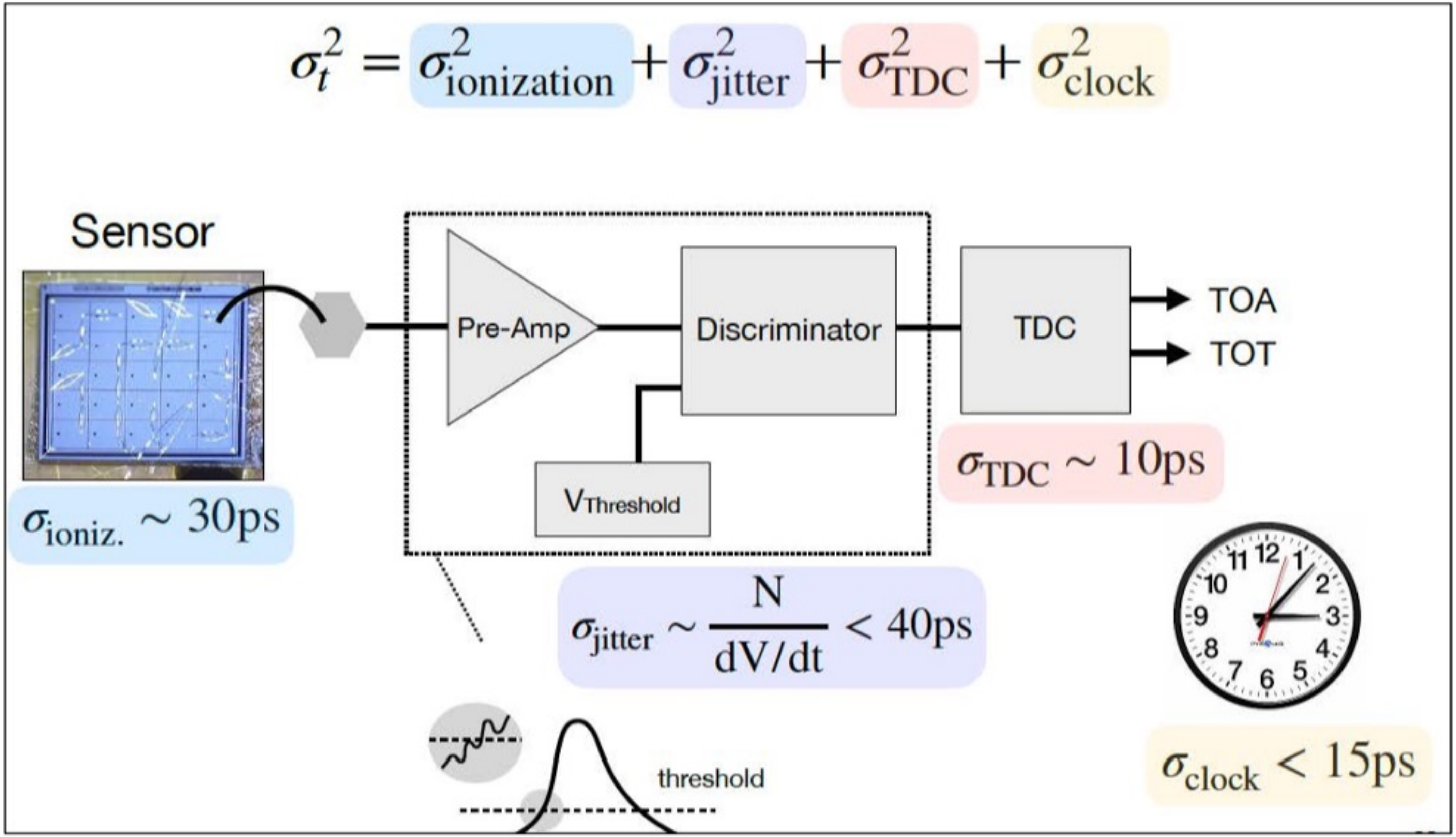
LGAD sensor

8000 modules (4 sensors each)





ETL - Timing Resolution



$$\sigma_t^2 = \sigma_{\mathrm{ionization}}^2 + \sigma_{\mathrm{jitter}}^2 + \sigma_{\mathrm{TDC}}^2 + \sigma_{\mathrm{clock}}^2$$

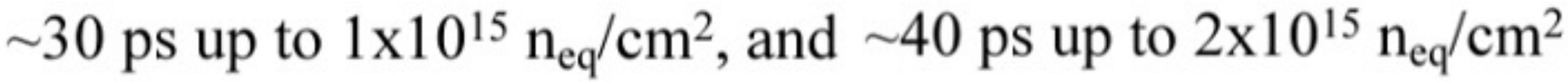
$\sigma_{\mathrm{ioniz.}} \sim 30\mathrm{ps}$

$\sigma_{\mathrm{TDC}} \sim 10\mathrm{ps}$

$\sigma_{\mathrm{jitter}} \sim \frac{\mathrm{N}}{\mathrm{dV/dt}} < 40\mathrm{ps}$

$\sigma_{\mathrm{clock}} < 15\mathrm{ps}$

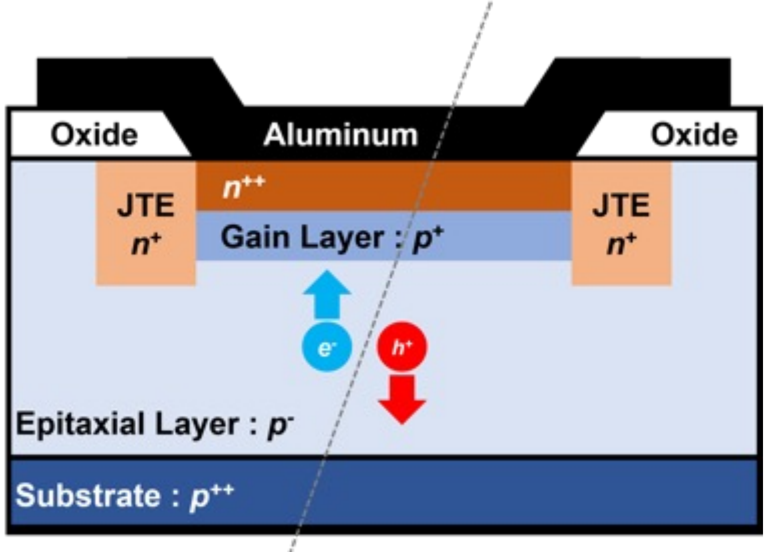
ETL - Timing Resolution

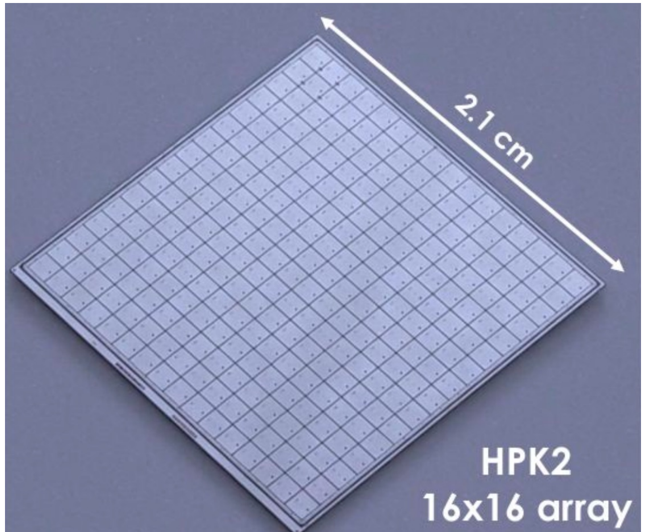
- $\sigma_{ionization}$: Random variation in particle energy deposition, determining the amplitude and the shape of the signal
  - 
    ~30 ps up to $1\text{x}10^{15}$ n_{eq}/cm^2, and ~40 ps up to $2\text{x}10^{15}$ n_{eq}/cm^2
- σ_{jitter} : Mostly due to electronics noise and depends on the amplifier slew rate (dV/dt)
  - jitter <40 ps before irradiation.
  - No degrading in ETROC0 performance observed up to 100 Mrad
- σ_{TDC} : Effect of the TDC binning
- σ_{clock} : Contribution from clock distribution

Low Gain Avalanche Diode (LGAD) sensors

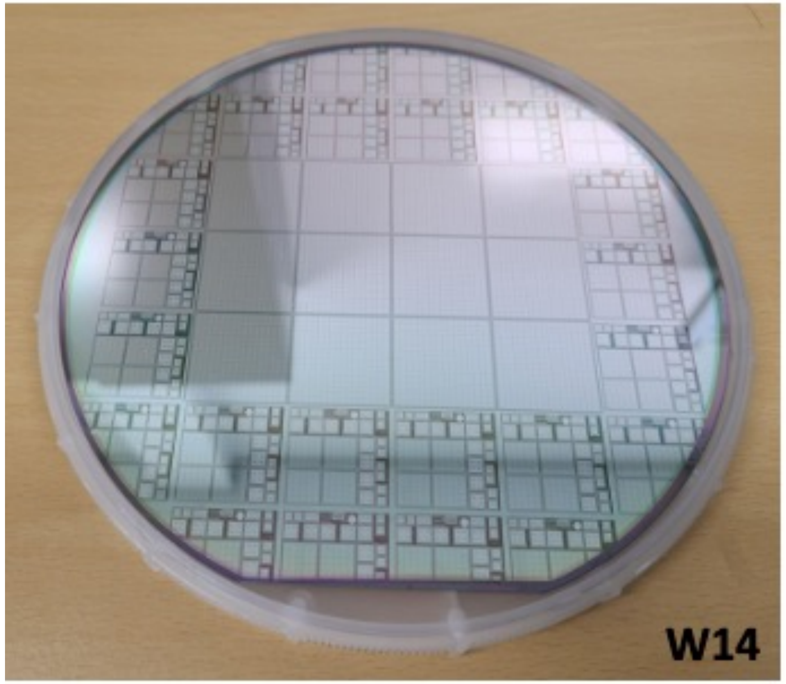
- LGAD characteristics (16x16 pixel matrix, 1.3x1.3 mm^2 pixel size)
  - Precision position reconstruction and timing resolution
  - Highly improved radiation tolerance
  - Moderate gain factor (10-30) to maximize S/N ratio -> Large signals with low noise
  - Thin implanted gain layer of overall thickness of 35–50 µm

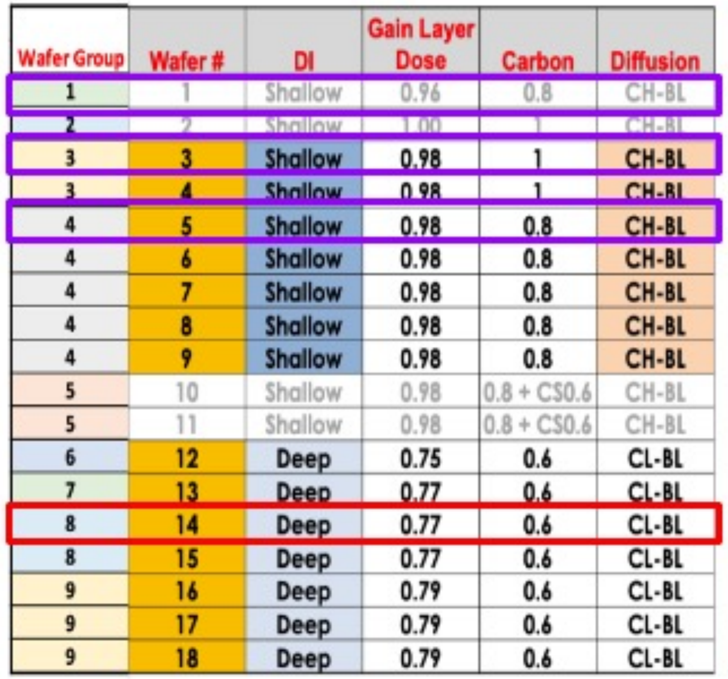
    : Thickness (50 µm) trade-off between signal size and time jitter of primary ionization
  - Gain uniformity (>8 fC of charge)
- The additional Gain layer: highly boron-doped thin layer at the n-p junction
  - Generates the high field necessary to achieve charge multiplication.



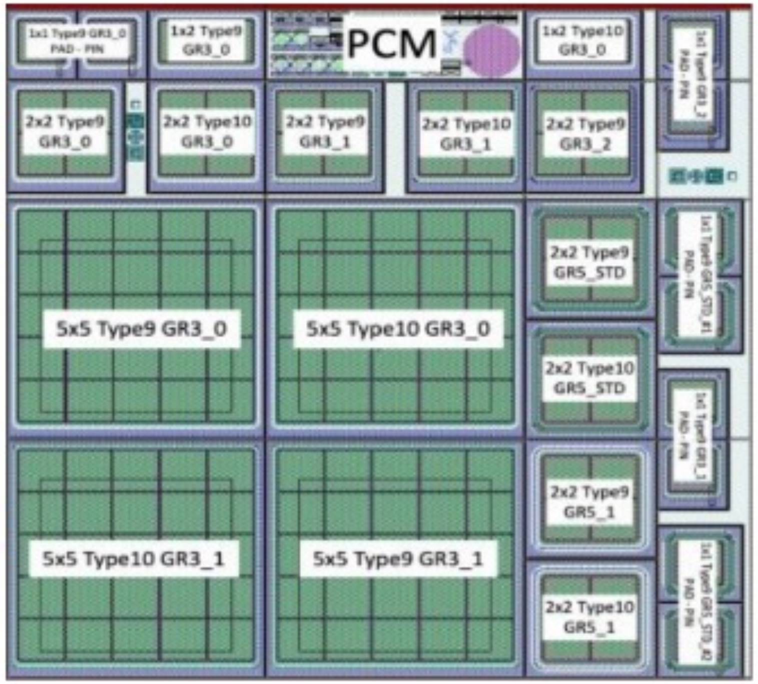


UFSD4 (FBK, Italy) wafers test in Korea



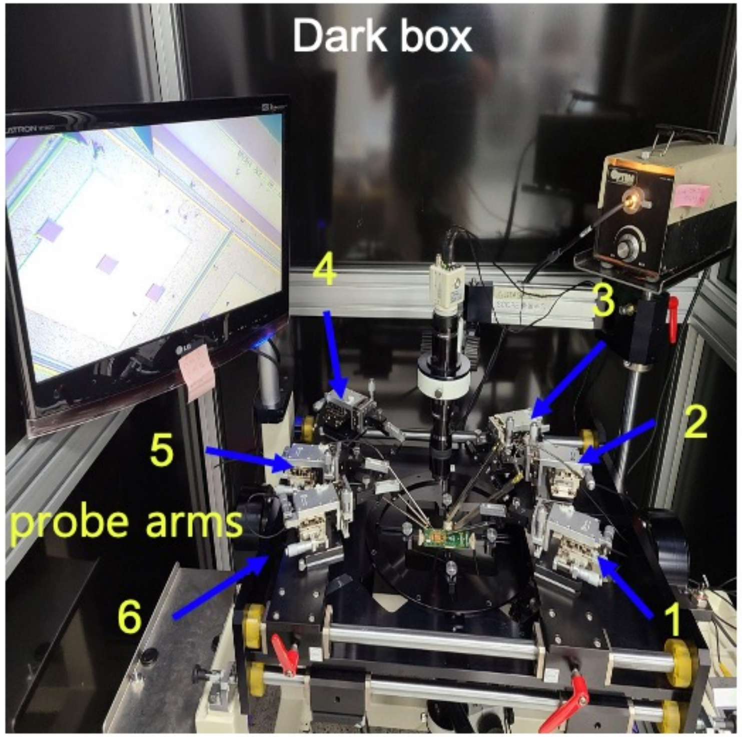


Wafer Group	Wafer #	DI	Gain Layer Dose	Carbon	Diffusion
1	1	Shallow	0.96	0.8	CH-BL
2	2	Shallow	1.00	1	CH-BL
3	3	Shallow	0.98	1	CH-BL
3	4	Shallow	0.98	1	CH-BL
4	5	Shallow	0.98	0.8	CH-BL
4	6	Shallow	0.98	0.8	CH-BL
4	7	Shallow	0.98	0.8	CH-BL
4	8	Shallow	0.98	0.8	CH-BL
4	9	Shallow	0.98	0.8	CH-BL
5	10	Shallow	0.98	0.8 + CS0.6	CH-BL
5	11	Shallow	0.98	0.8 + CS0.6	CH-BL
6	12	Deep	0.75	0.6	CL-BL
7	13	Deep	0.77	0.6	CL-BL
8	14	Deep	0.77	0.6	CL-BL
8	15	Deep	0.77	0.6	CL-BL
9	16	Deep	0.79	0.6	CL-BL
9	17	Deep	0.79	0.6	CL-BL
9	18	Deep	0.79	0.6	CL-BL

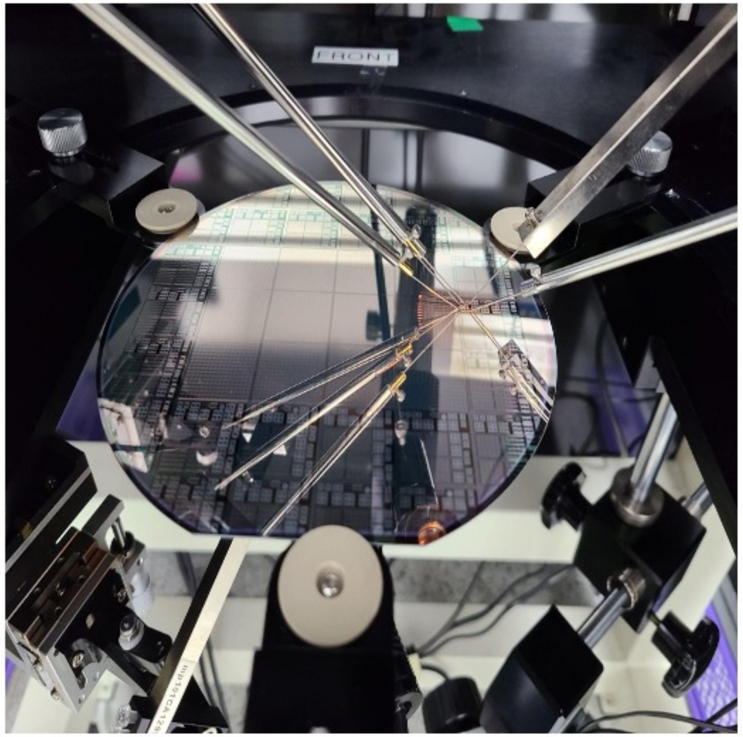


- The **Red box** represents the UFSD4 wafer #14 (W14), which has undergone wafer-level testing at KNU
- The **Purple box** represents three wafers which are shipped to CERN today for ETROC2 testing
- New 16 wafers (UFSD-K1), will be available for testing in a few weeks

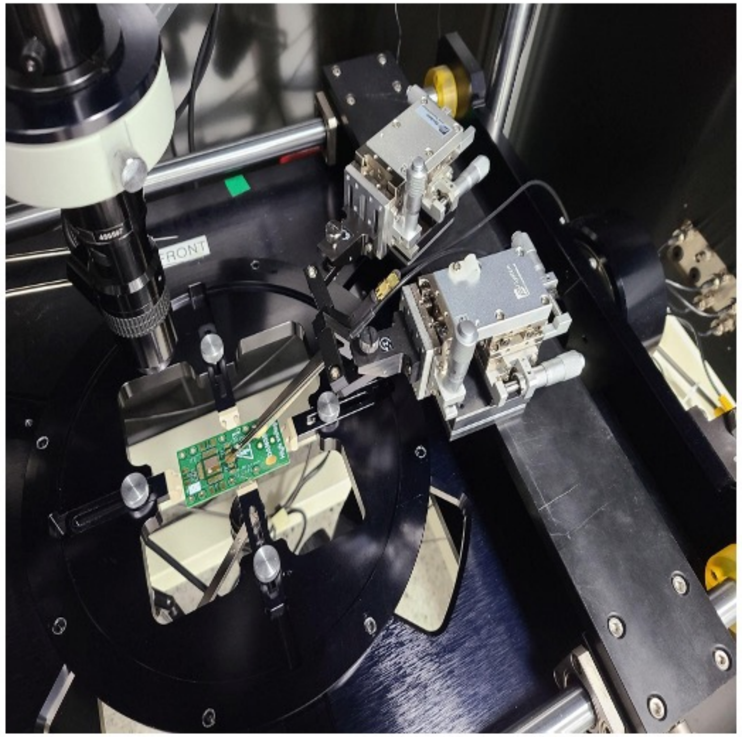
Probe station setup for wafer-level and sensor-level tests



- Overview



- wafer tray



- sensor tray

➢ There are 6 probe arms that use magnets to connect with the station (1 for signal read-out, 1 for bias voltage supplying, and 4 for grounding)

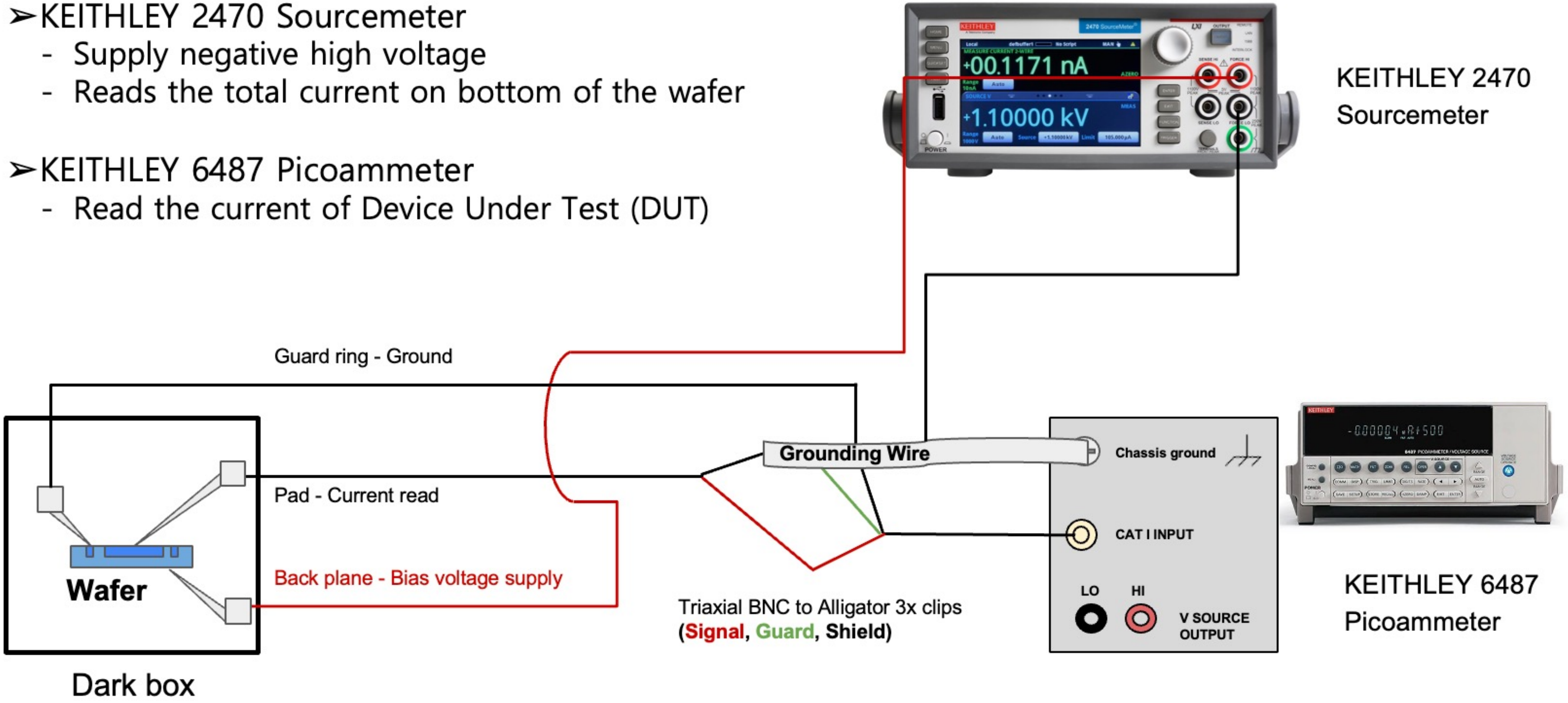
➢ Two types of tray available for wafer-level and sensor-level tests

➢ KCMS currently has plan to prepare a **probe card** and **switching matrix for 16x16 sensors**

Test setup for I-V measurements at KNU

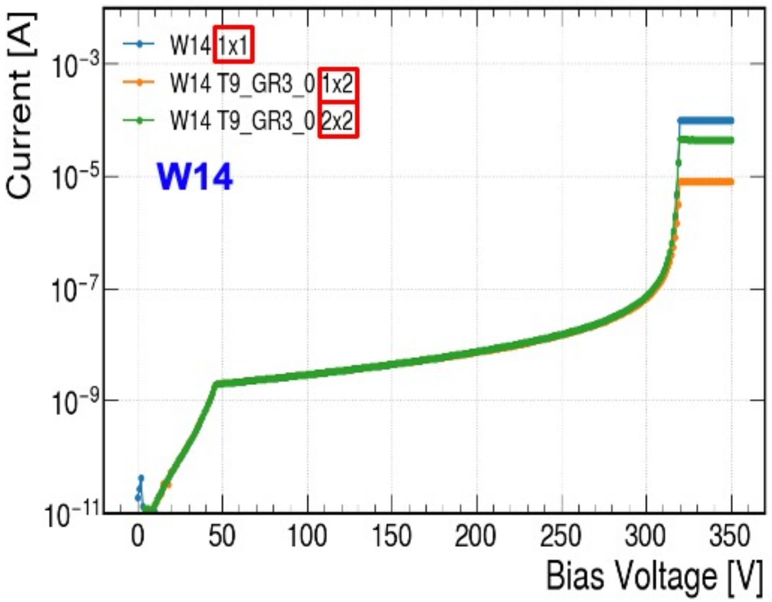
- ➢KEITHLEY 2470 Sourcemeter
  - Supply negative high voltage
  - Reads the total current on bottom of the wafer

- ➢KEITHLEY 6487 Picoammeter
  - Read the current of Device Under Test (DUT)

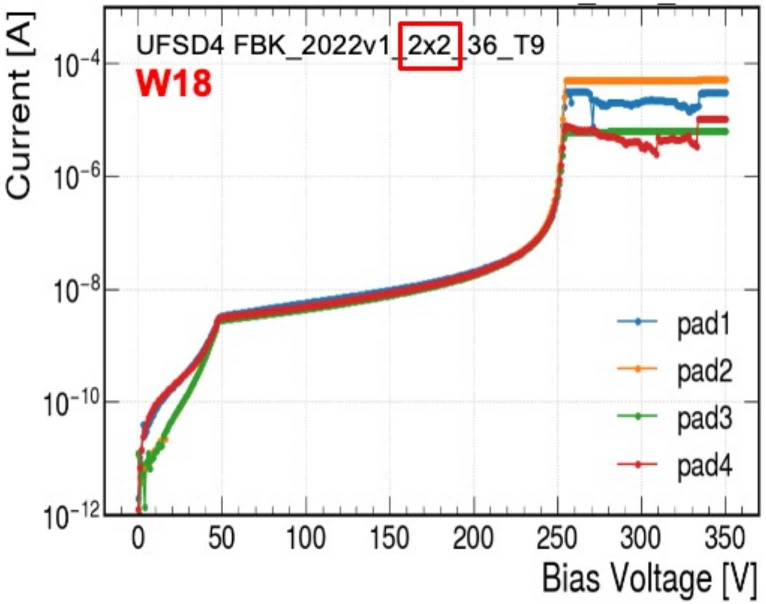


I-V measurement of 1x1, 1x2, 2x2 sensors (FBK UFSD4 W14) at KNU

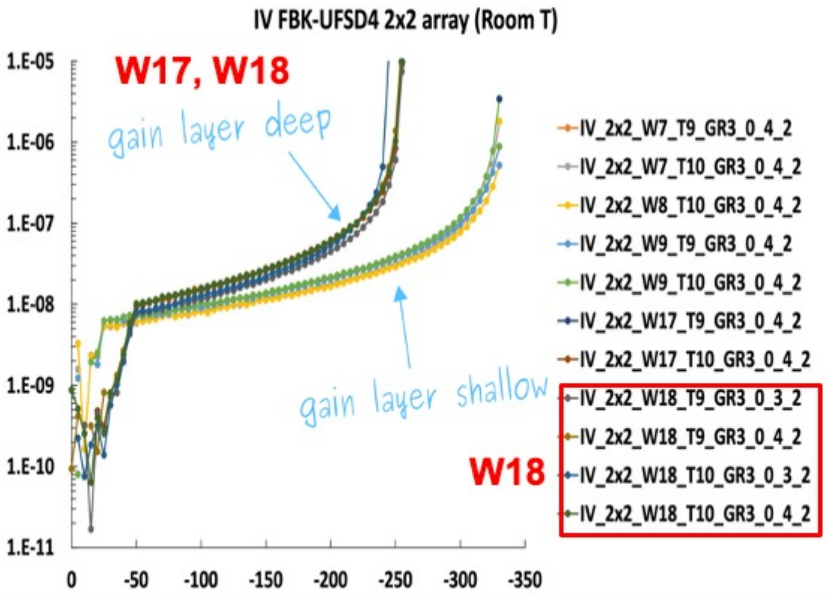
KNU (wafer-level)



KNU (sensor-level)



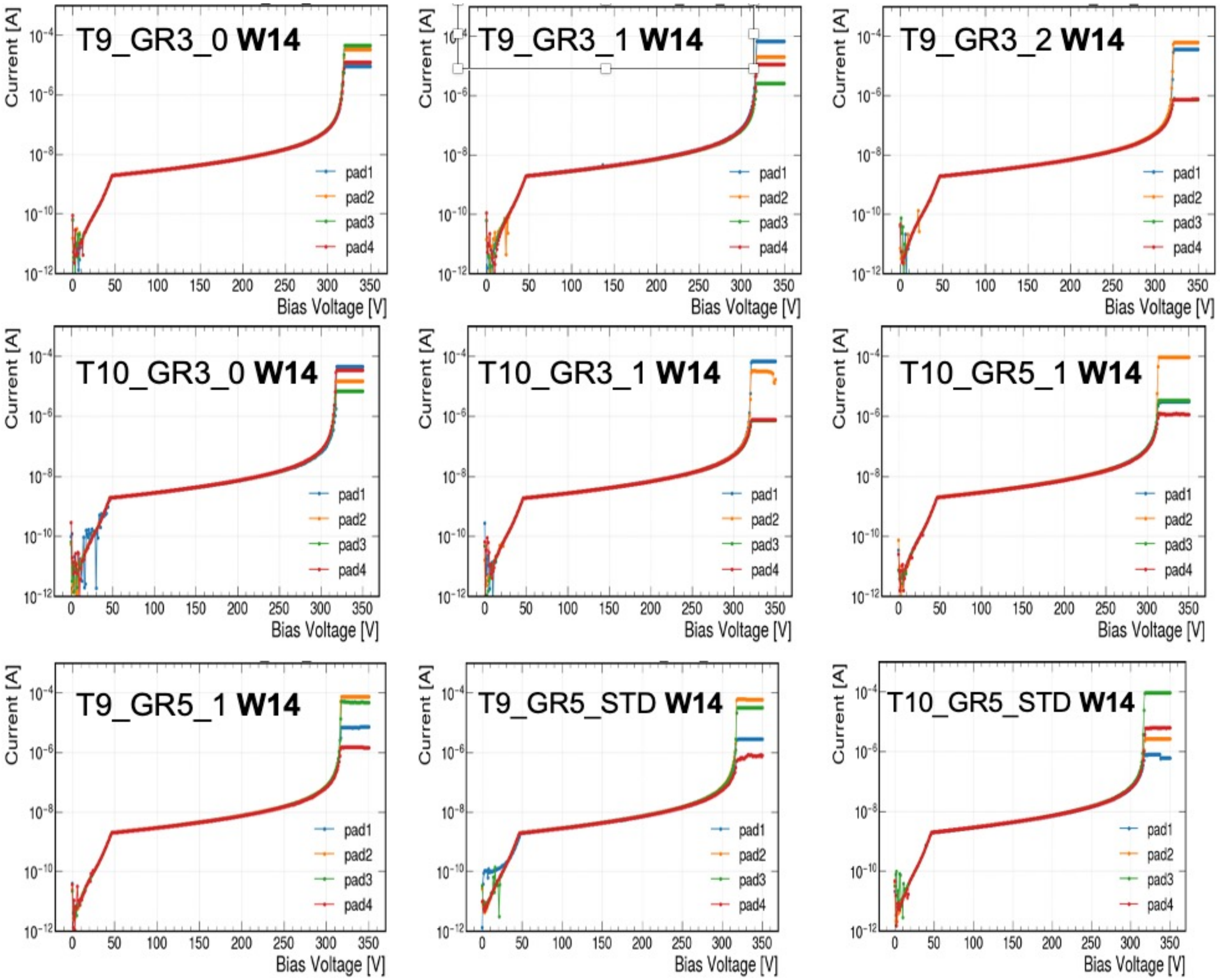
Torino



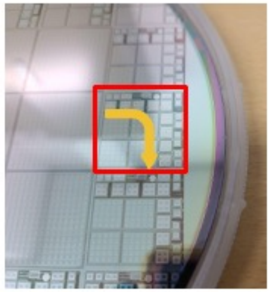
- ❑ Bias Voltage applied from 0 V to -350 V (**Δ**V = 1 V)
- ❑ Room temperature
- ❑ **Breakdown Voltage**
  - ○ V_{BD} ~ 320 V in W14 and V_{BD} ~ 250 V in W18
  - ○ The breakdown voltages do not depend on the sensor structures in the W14

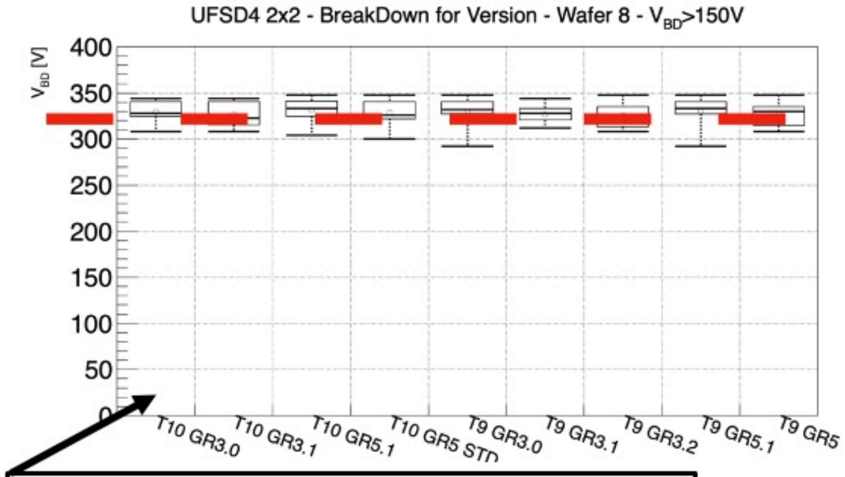
From Matias Senger's talk,
https://indico.cern.ch/event/1161512/

I-V measurement of 2x2 sensors in wafer level (UFSD4 W14) at KNU



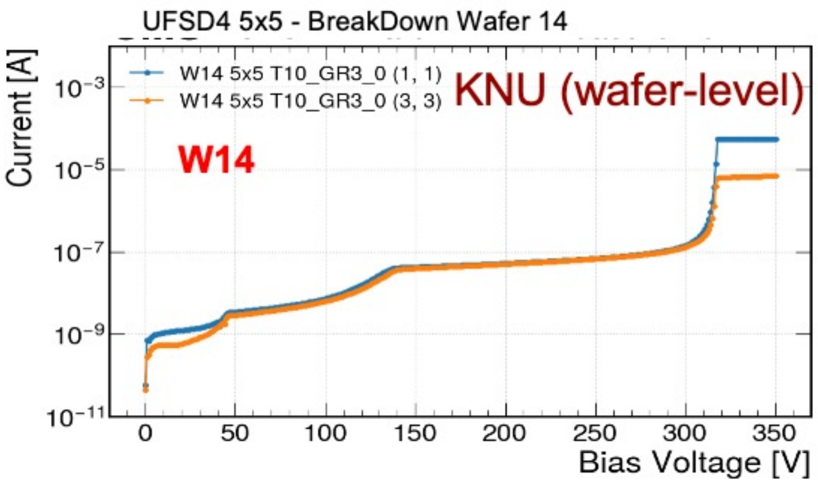
- Bias Voltage applied from 0 V to -350 V (**Δ**V = 1 V)
- Room temperature
- **Breakdown Voltage**
  - ○ V_{BD} ~ 320 V
  - The breakdown voltages are consistent in 2x2 sensors

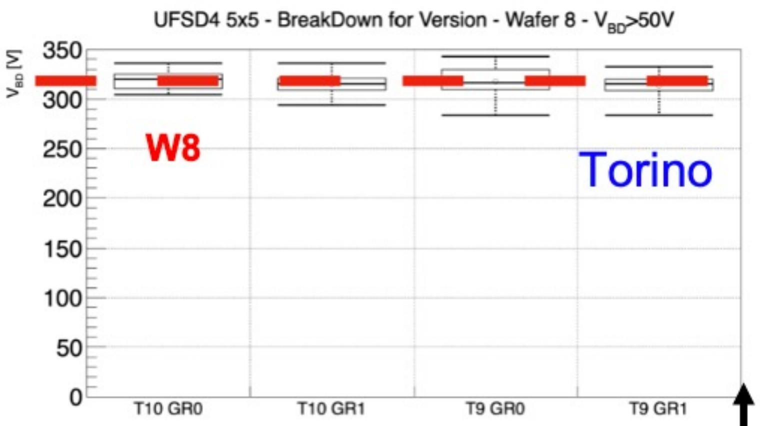


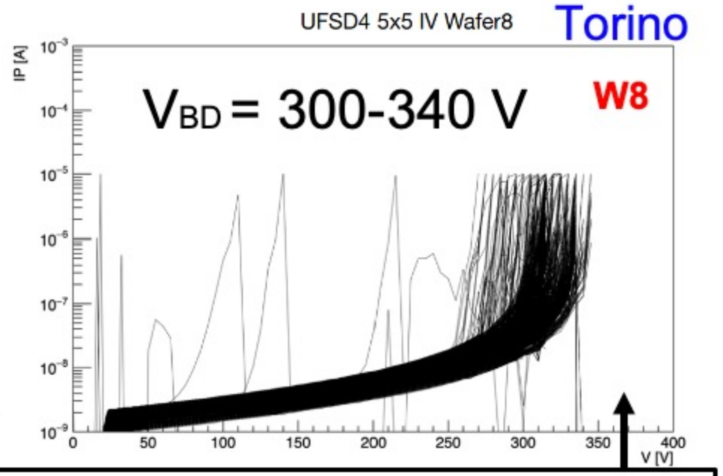


From Marta Tornago's talk,
https://indico.cern.ch/event/1141394/

I-V measurement of 5x5 sensor (UFSD4 W14) at KNU







From Marta Tornago's tal,
https://indico.cern.ch/event/1141394/

Differences in wafer design and measurement

- Torino, UFSD4 wafer 8 is in the same Wafer Group
  Shallow | Gain Layer Dose: 0.98 | Carbon: 0.8 | Diffusion: CH-BL
- KNU, The wafer we have (W14) is in Wafer Group 8
  Deep | Gain Layer Dose: 0.77 | Carbon: 0.6 | Diffusion: CL-BL

➢I-V parameters at KNU

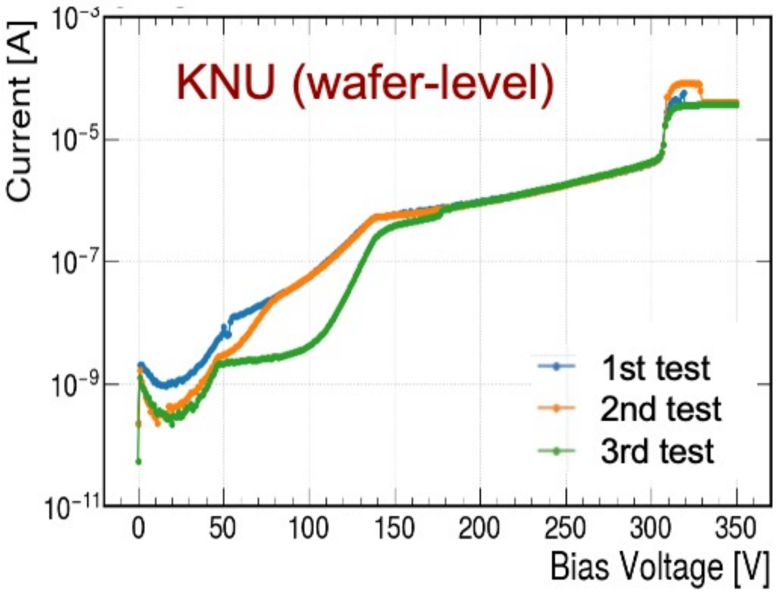
- Main Diode: Signal read out
- GR: Ground
- Near Pads: Ground
- BackSide: Connected HV
- Temperature: Room temp
- Compliance: 25 uA

➢I-V parameters 5x5 at Torino

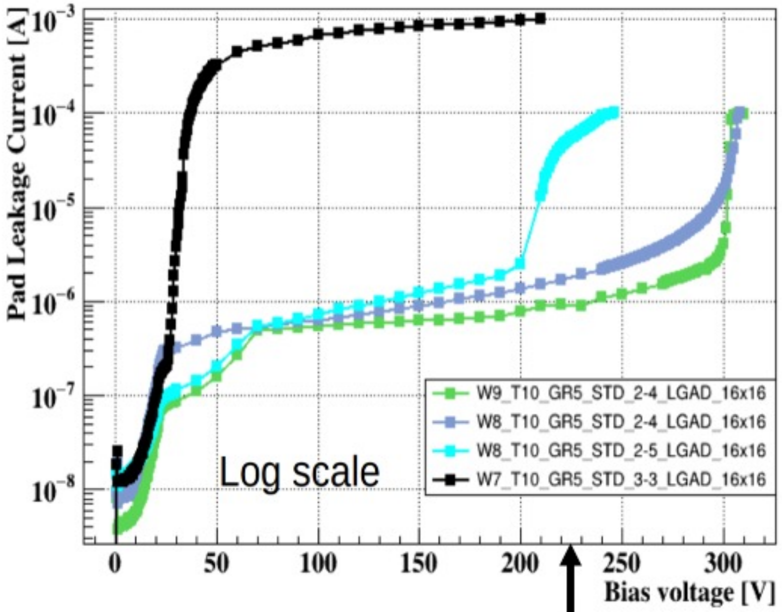
- Main Diode: Signal read out
- GR: Ground
- BackSide: Connected HV
- Compliance: 10 uA
- Measured by **Probe card**

I-V measurement of 16x16 sensors (UFSD4 W14) in wafer level at KNU

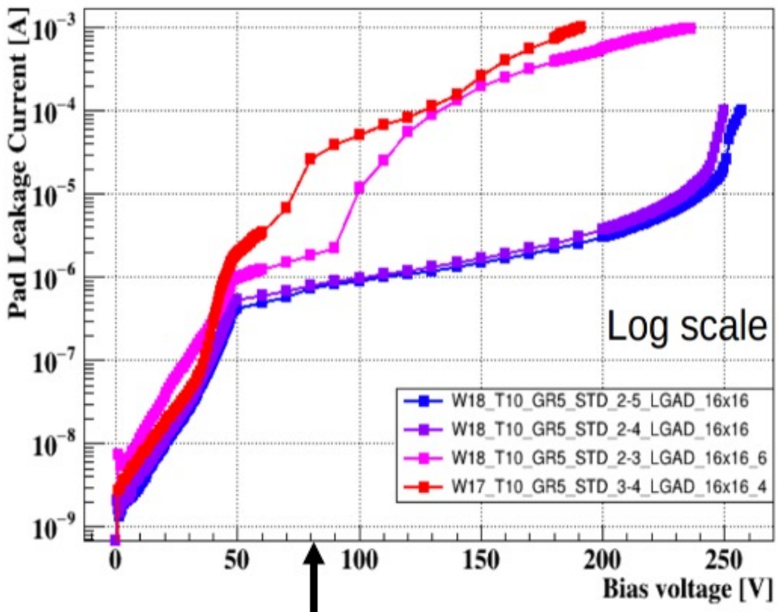
W14, Deep gain layer,
Carbon 0.6, Boron 0.77



W7, 8 & 9, Shallow Junction
Carbon 0.8, Boron 0.98
CSIC

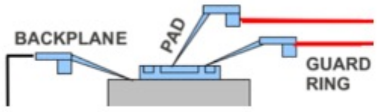


W17 & 18, Deep Junction,
Carbon 0.6, Boron 0.79
CSIC



- ❑ Bias Voltage applied from 0 V to -350 V (ΔV = 1 V)
- ❑ Room temperature
- ❑ **Breakdown Voltage**
  - ○ V_{BD} ~ 310 V
- ❑ The leakage current in 16x16 sensors measurement fluctuates following the grounding and iteration

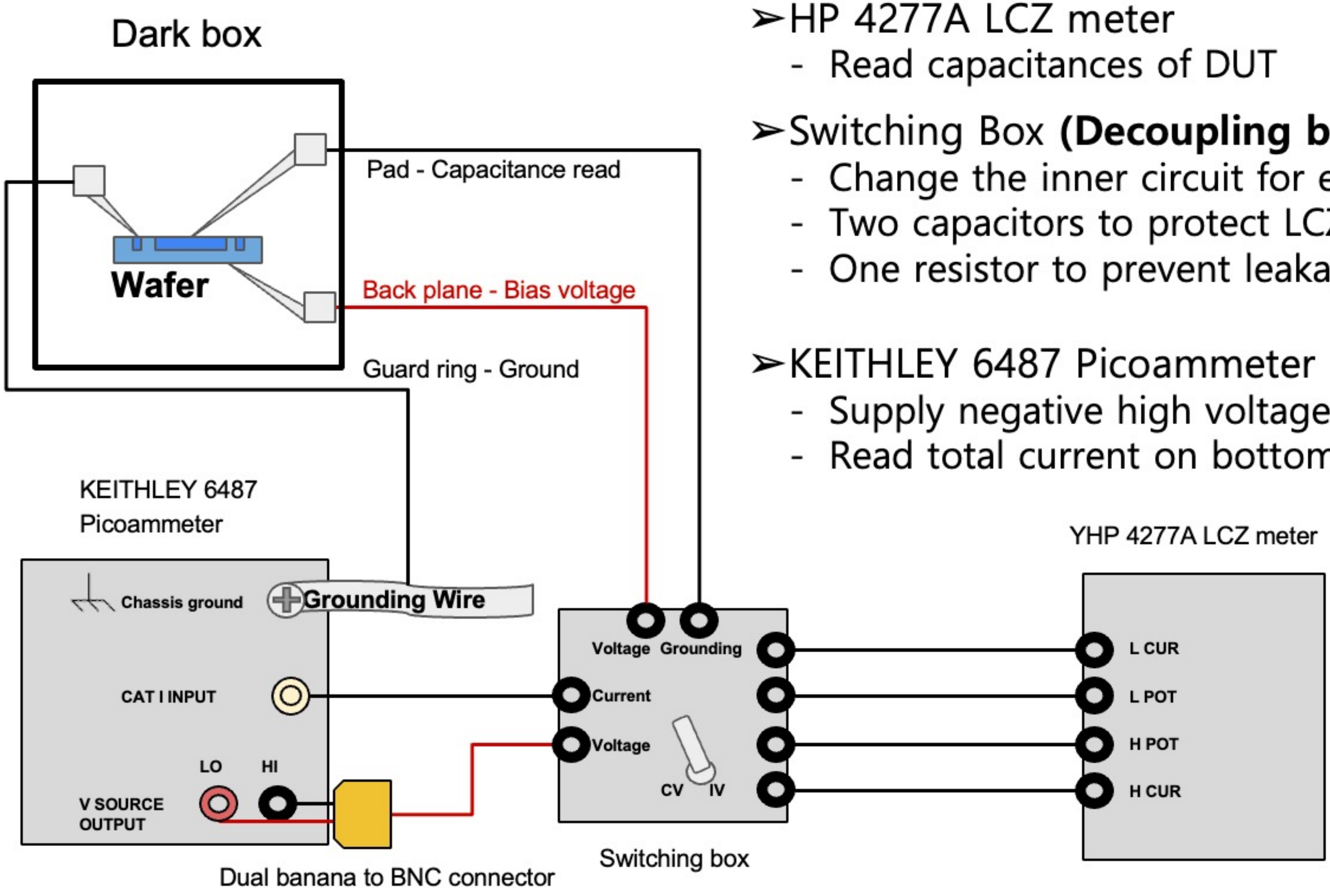
From Efren Navarrete Ramos's talk,
https://indico.cern.ch/event/1161512/



CSIC setup

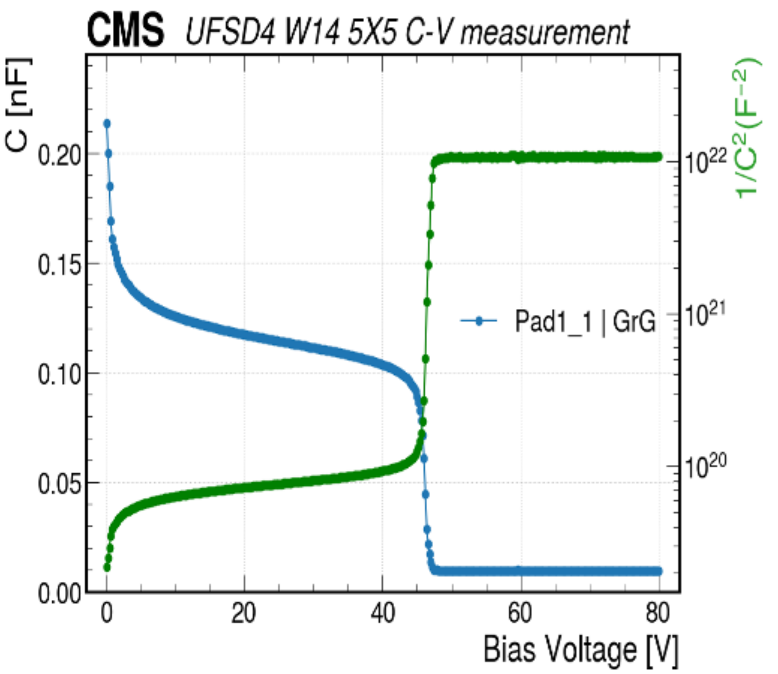
➢I-V parameters 16x16 at CSIC
- Main Diode: Connected HV
- GR: Not contacted
- BackSide: Ground
- Temperature: Room temp
- Compliance: 100 uA & 1 mA

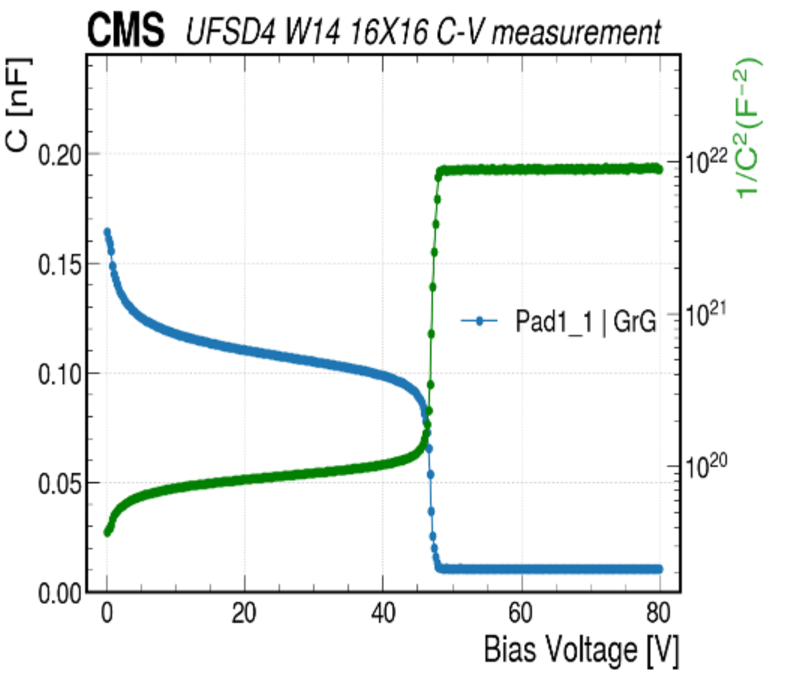
Setup for C-V measurement at KNU

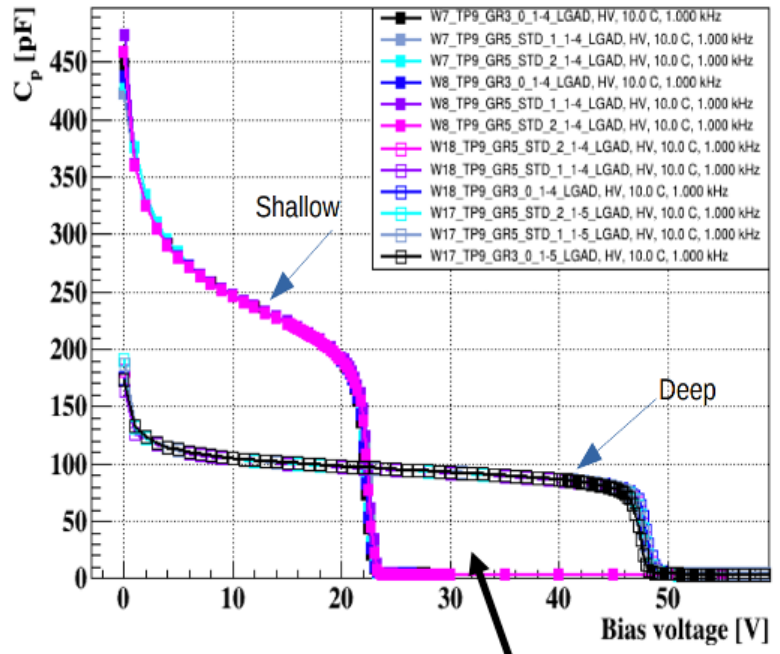


- ➢HP 4277A LCZ meter
  - Read capacitances of DUT
- ➢Switching Box **(Decoupling box)**
  - Change the inner circuit for each measurement
  - Two capacitors to protect LCZ meter from leakage current
  - One resistor to prevent leakage current to Picoammeter
- ➢KEITHLEY 6487 Picoammeter
  - Supply negative high voltage
  - Read total current on bottom of the wafer

C-V measurement of the UFSD4 W14 1x1, 1x2, and 2x2 sensors at KNU







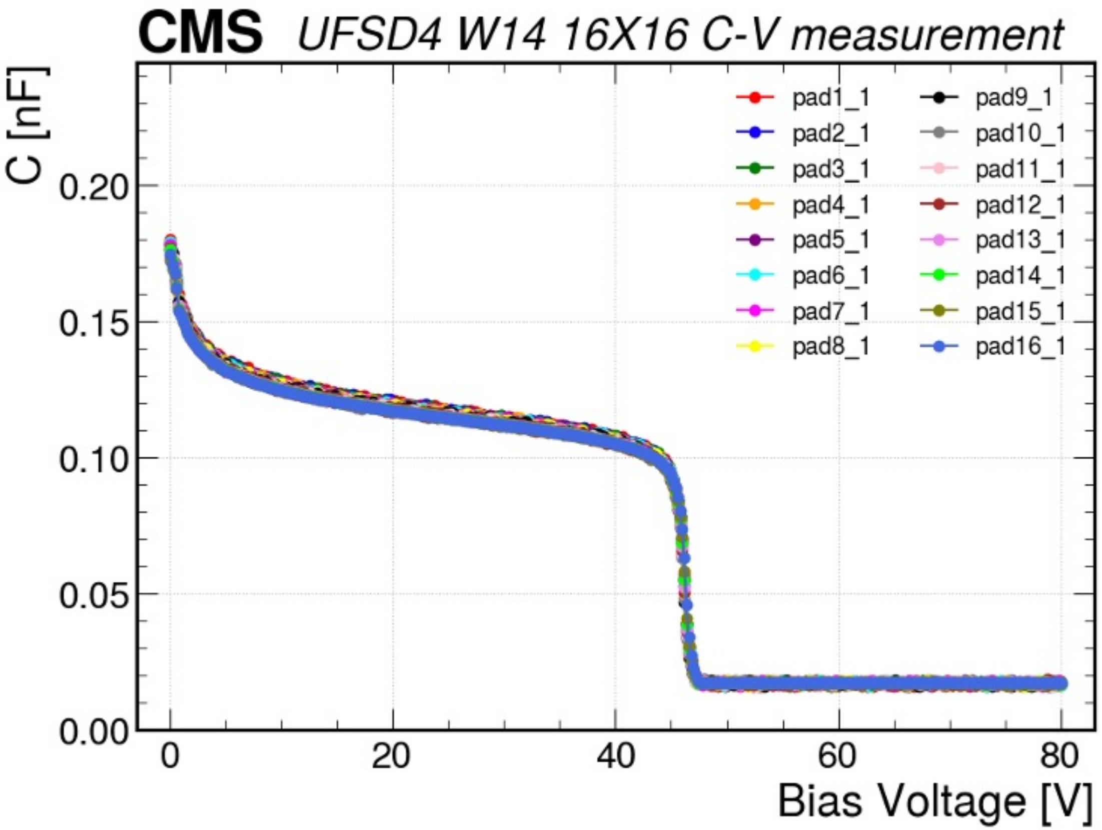
From Efren Navarrete Ramos's talk, https://indico.cern.ch/event/1161512/

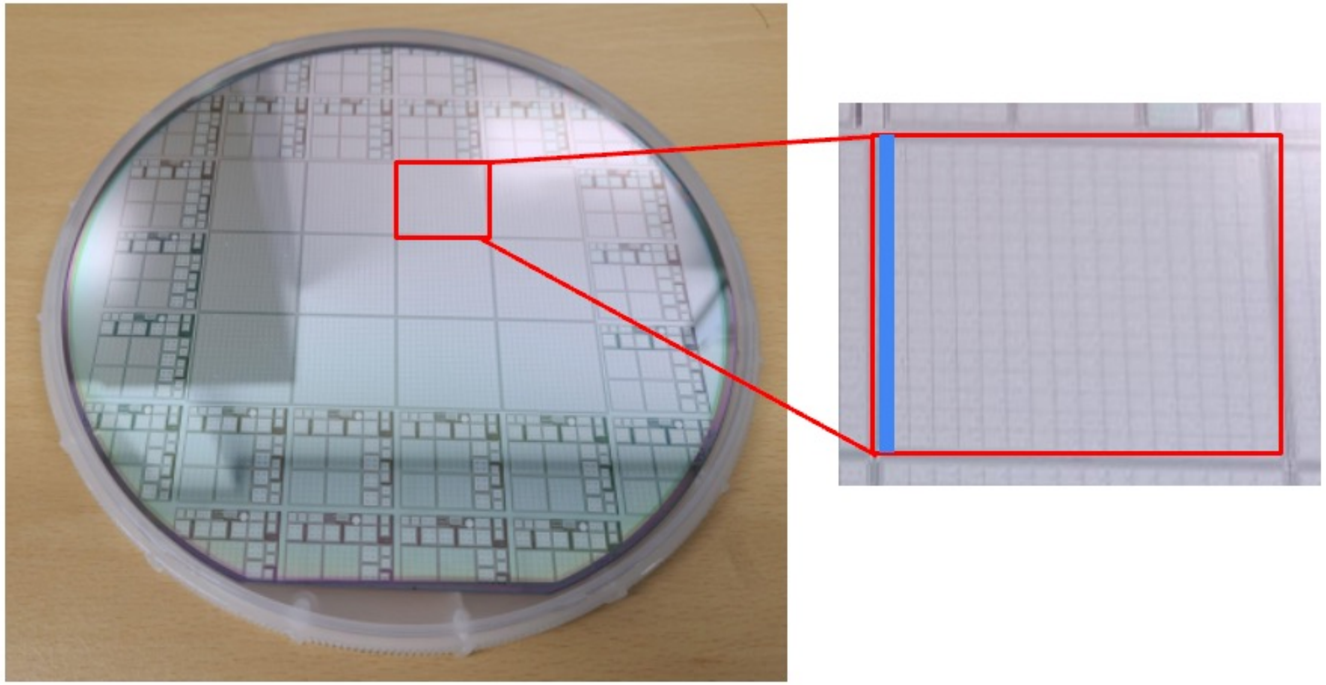
- ❑ Bias Voltage applied from 0 V to -80 V (ΔV = 0.2 V)
- ❑ AC frequency (10 kHz)
- ❑ Room temperature
- ❑ **Depletion Voltage**
  - ○ Gain layer depletion Voltage ~ 44 V
  - ○ Full depletion Voltage ~ 47 V

➢**C-V parameters at CSIC**

- Main Diode: HV
- GR: Connected HV
- BackSide: Ground
- Temperature: 10 ℃
- Frequency: 1 KHz

Gain layer uniformity studies with a column in 16x16 array at KNU

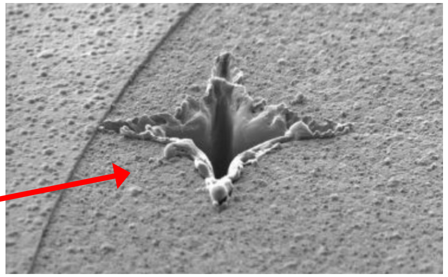


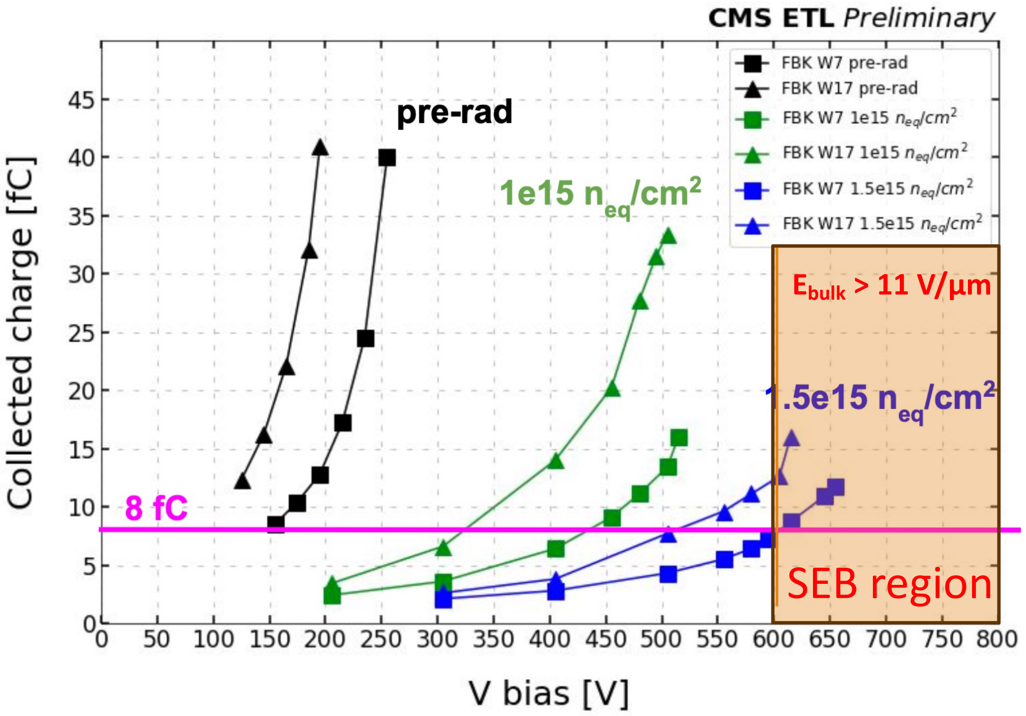


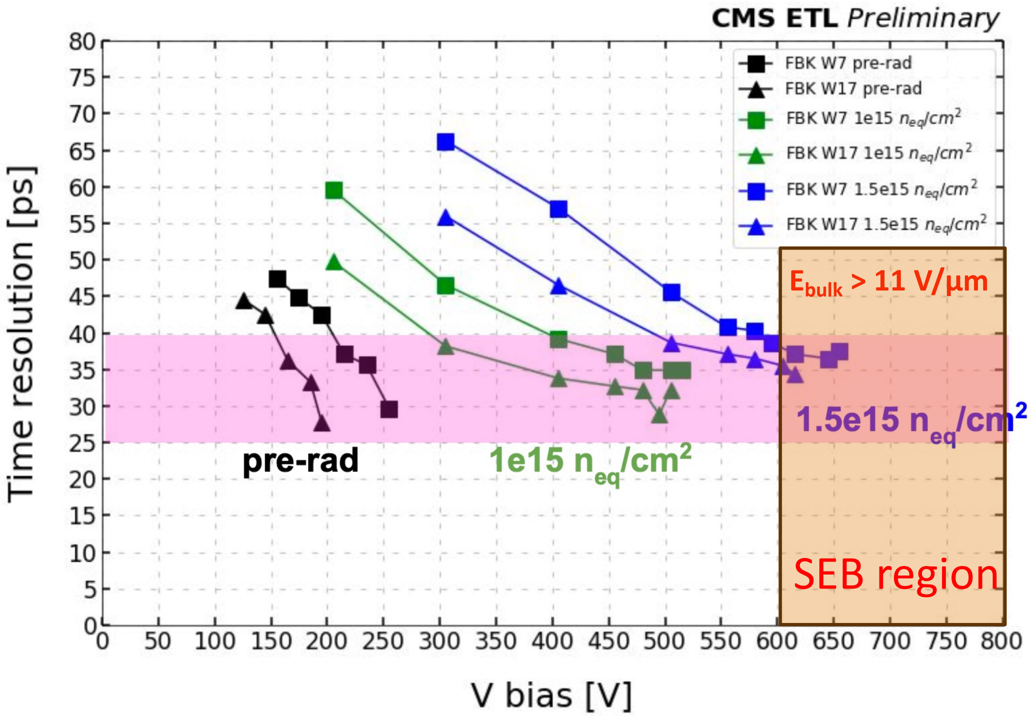
- Measurements performed on 16x16 T10_GR5_STD at KNU to extrapolate the uniformity of the gain layer
- C-V measurement are performed on 16 pads within one column
- Subsequent measurement will be conducted on pads near the center and pads within other reticles

Performance tests for LGAD sensors

- **Completed Market Survey for the procurement of the final LGADs Prototype.**
  - Qualified 4 vendors for production of the final LGAD sensors
- **Irradiated FBK sensors measured with a beta-source (Sr90) setup**
  - Collected charge and time resolution was satisfied with requirements
  - Fully recover performance by increasing the bias voltage
- Single Event Burn-out (SEB) observed for $E_{bulk} > 11$ V/µm

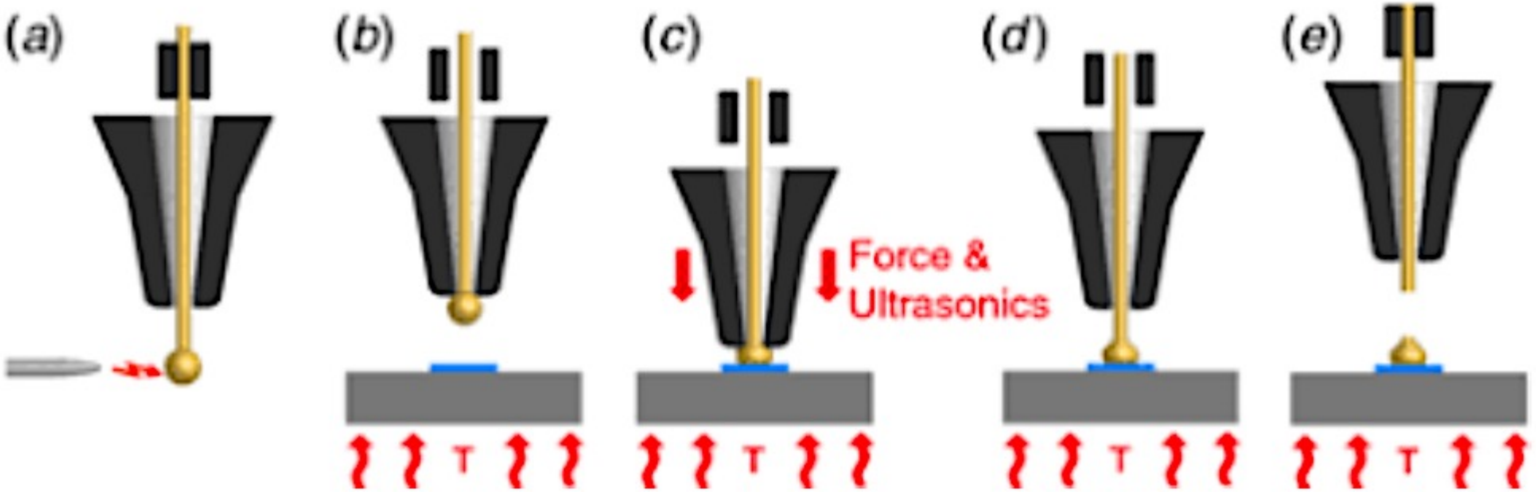


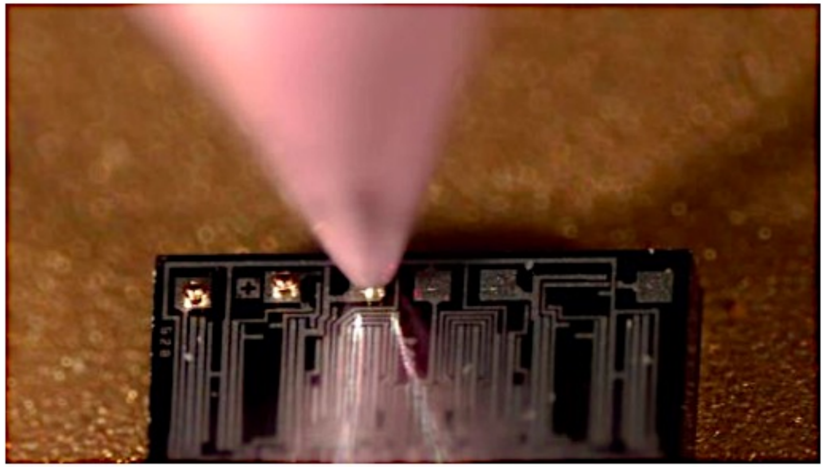




Bumping & Flip Chip Bonding

Ball Stud Bump Bonding Process

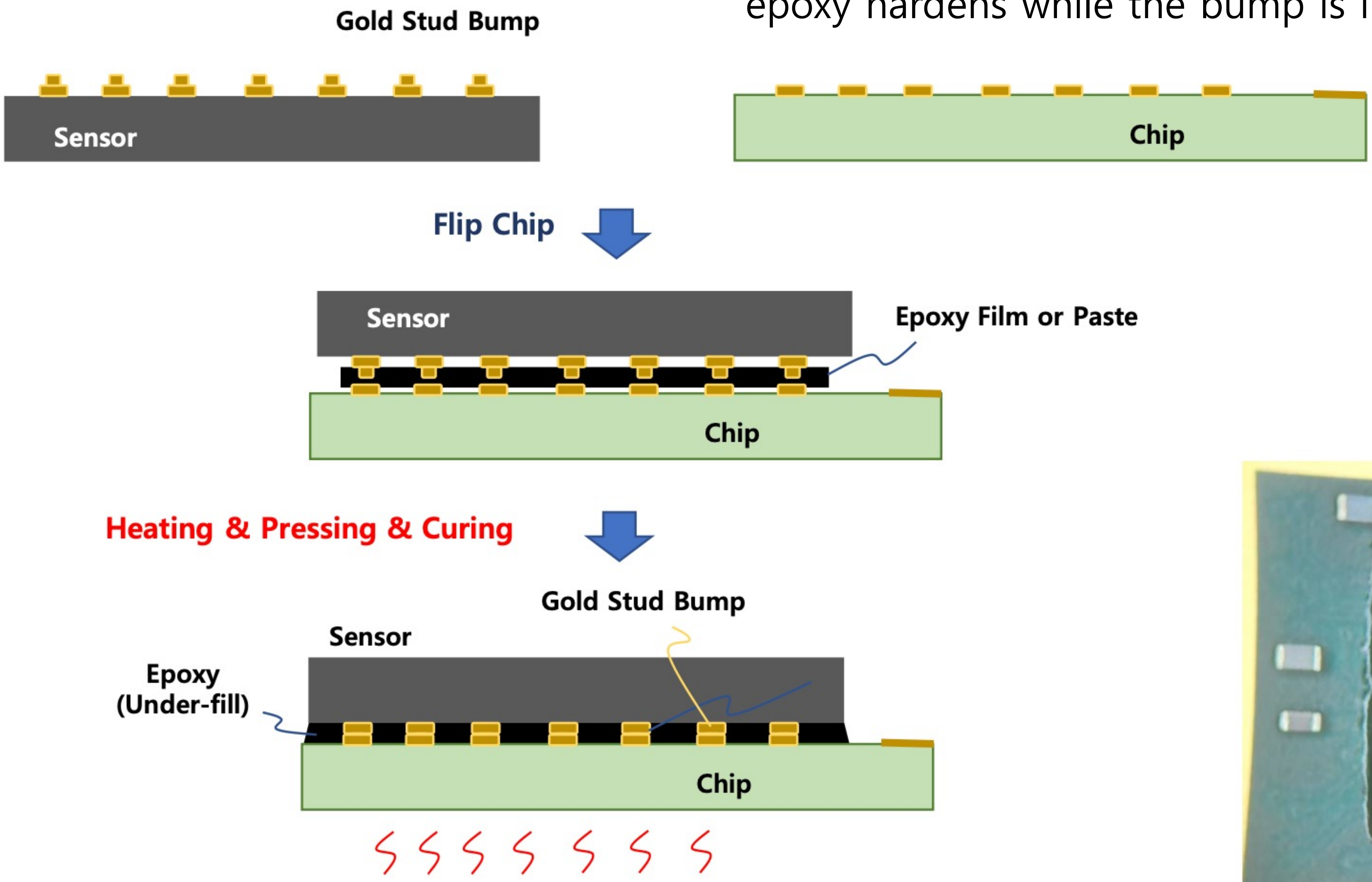


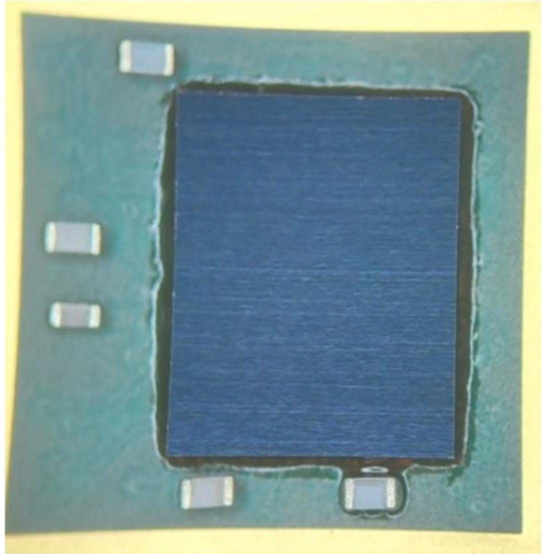


Bumping & Flip Chip Bonding

Flip Chip Bonding: option 1

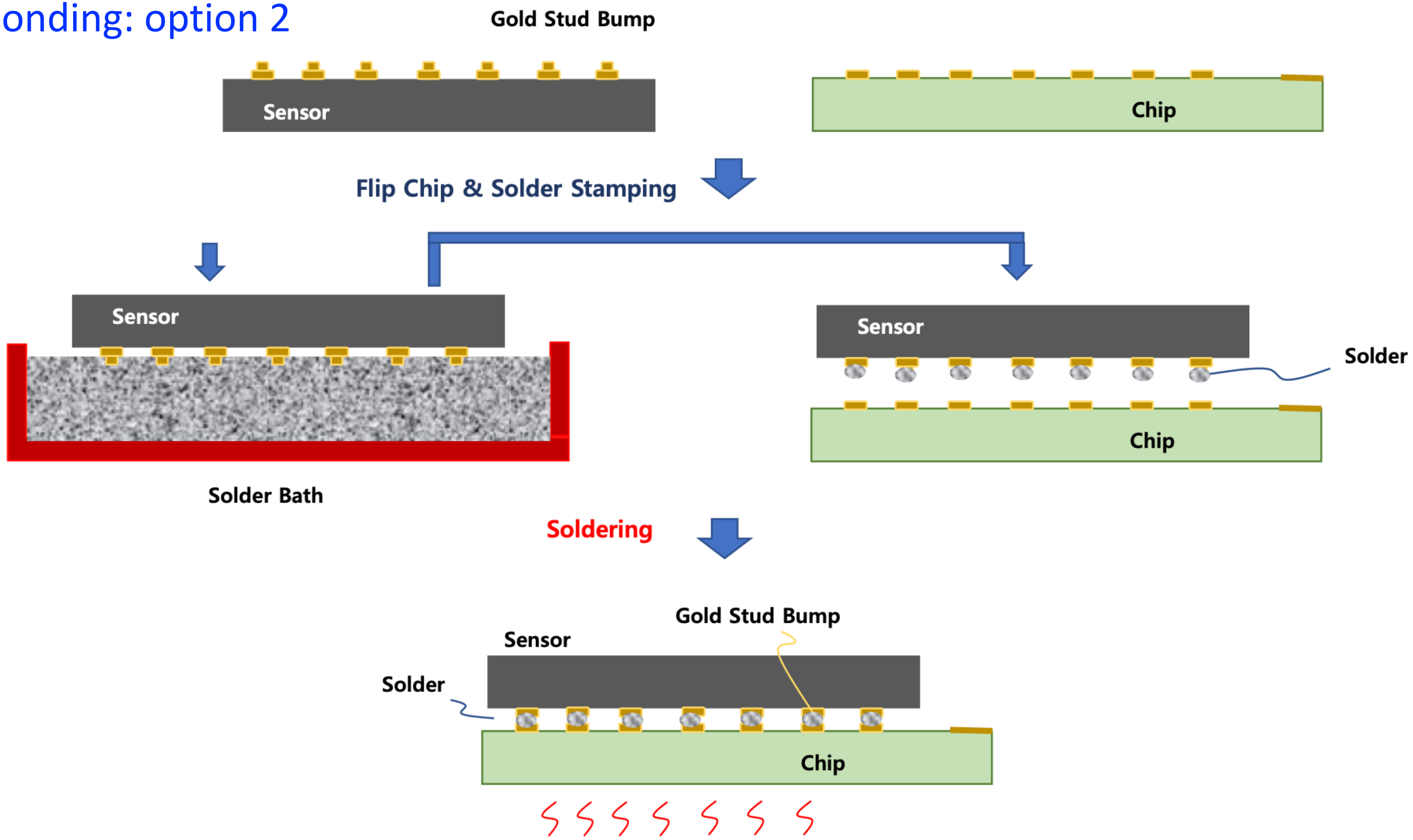
- Making a Gold Stud Bump on the chip and flipped it to join.
- At this time, the sensor and the chip are fixed as the under-fill epoxy hardens while the bump is in contact.



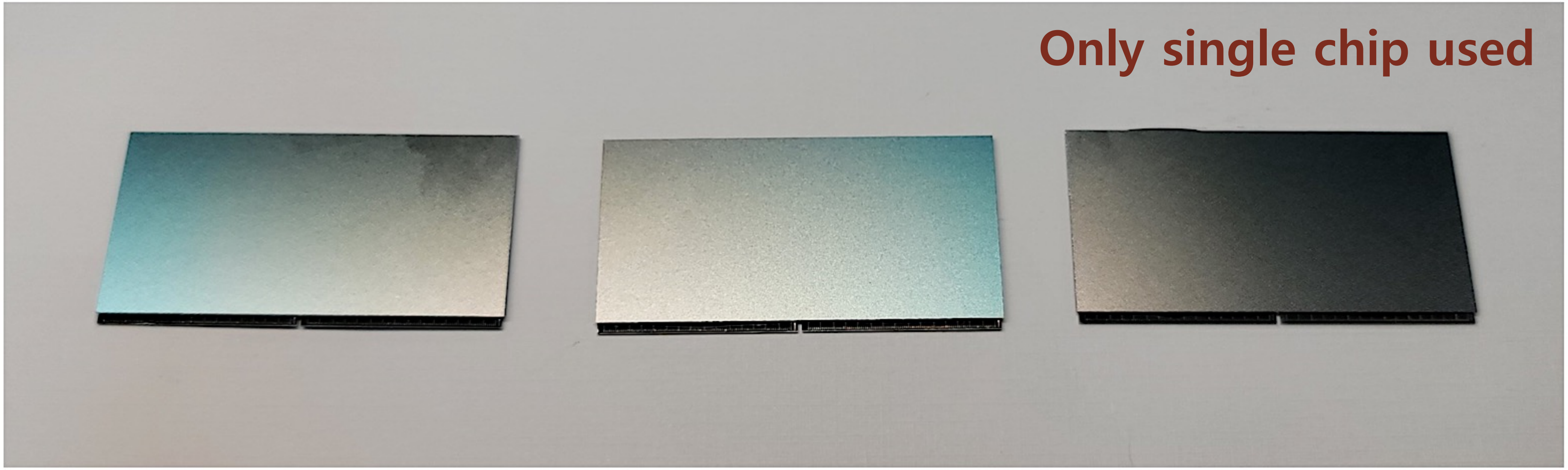


Bumping & Flip Chip Bonding

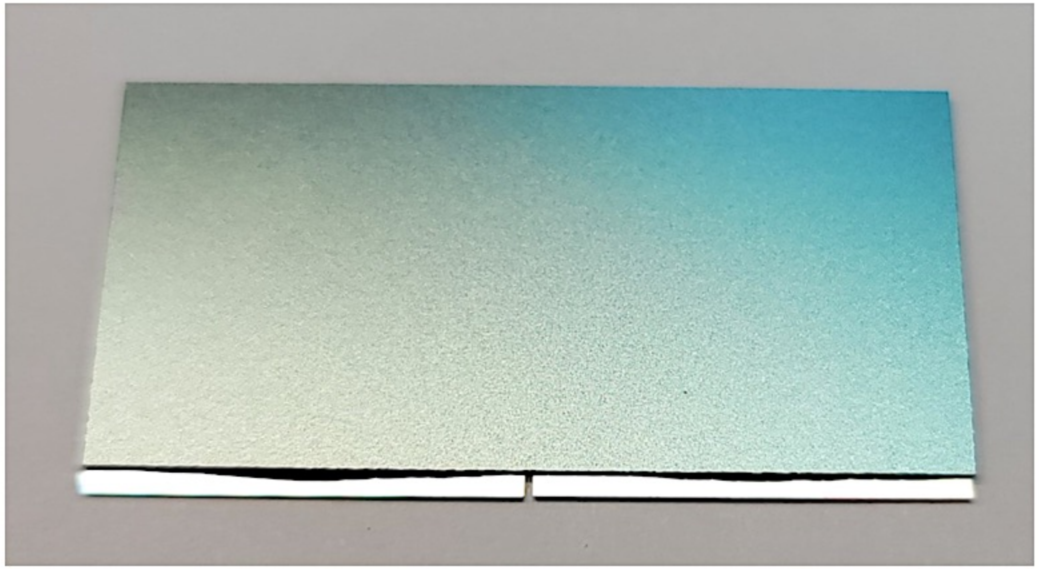
Flip Chip Bonding: option 2

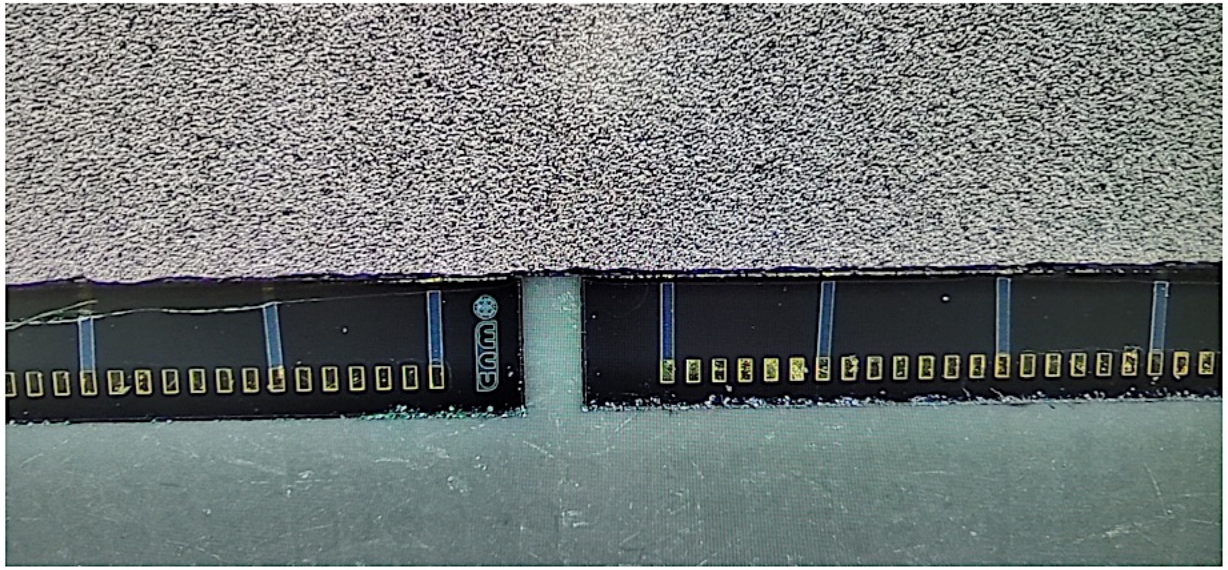


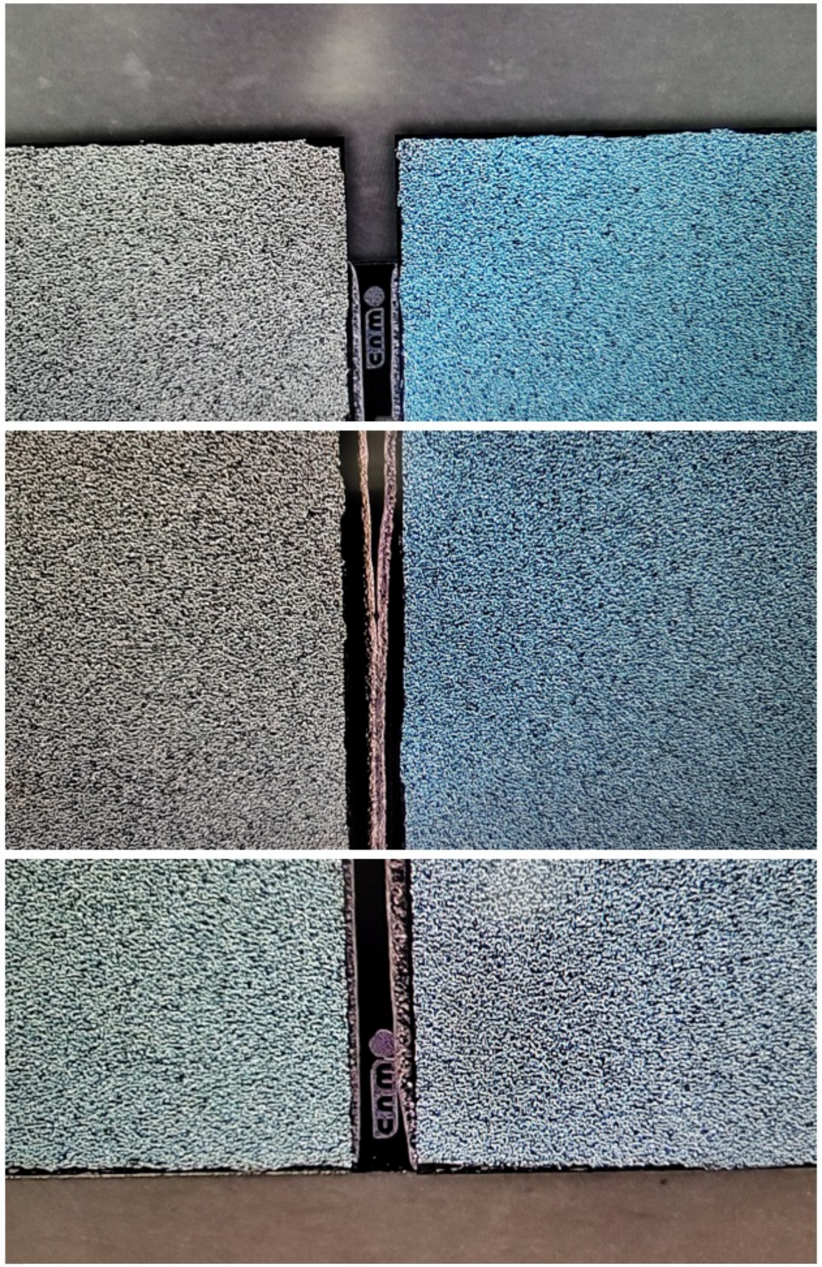
Bump-bonded dummy chip and sensor by the process (Option 1)



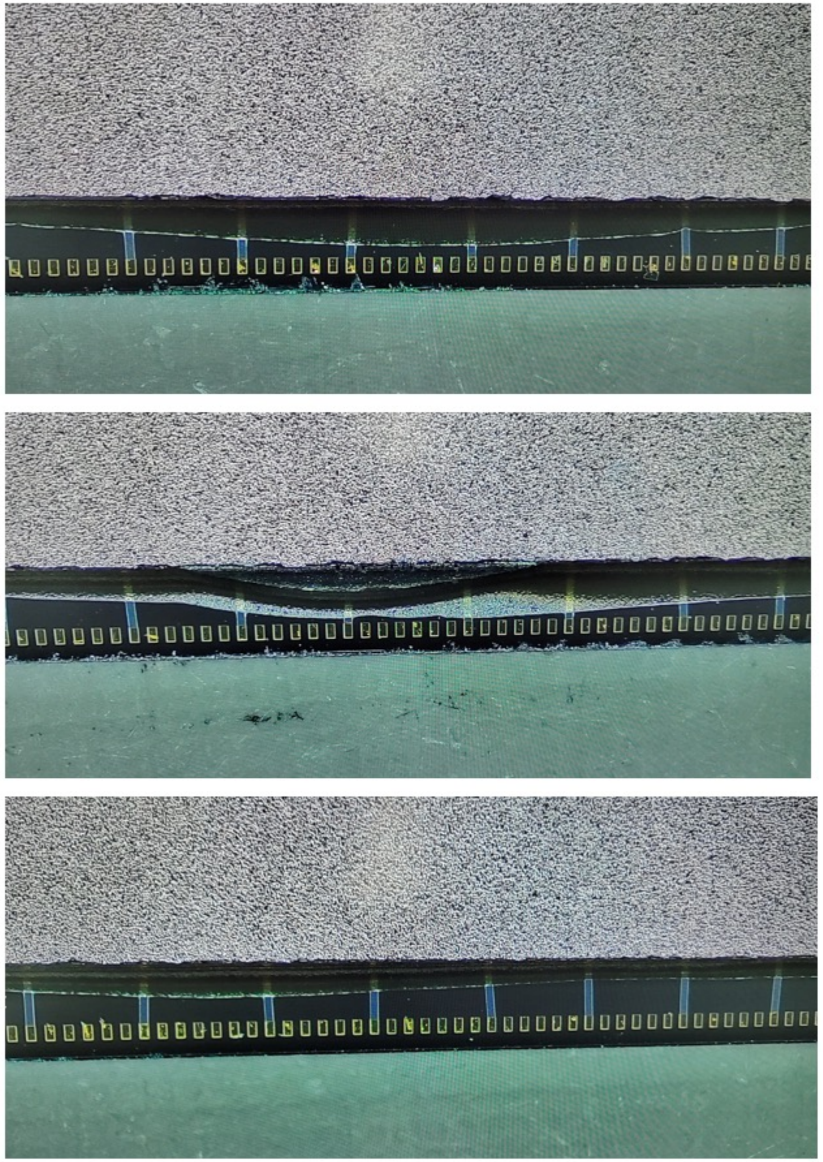
Only single chip used







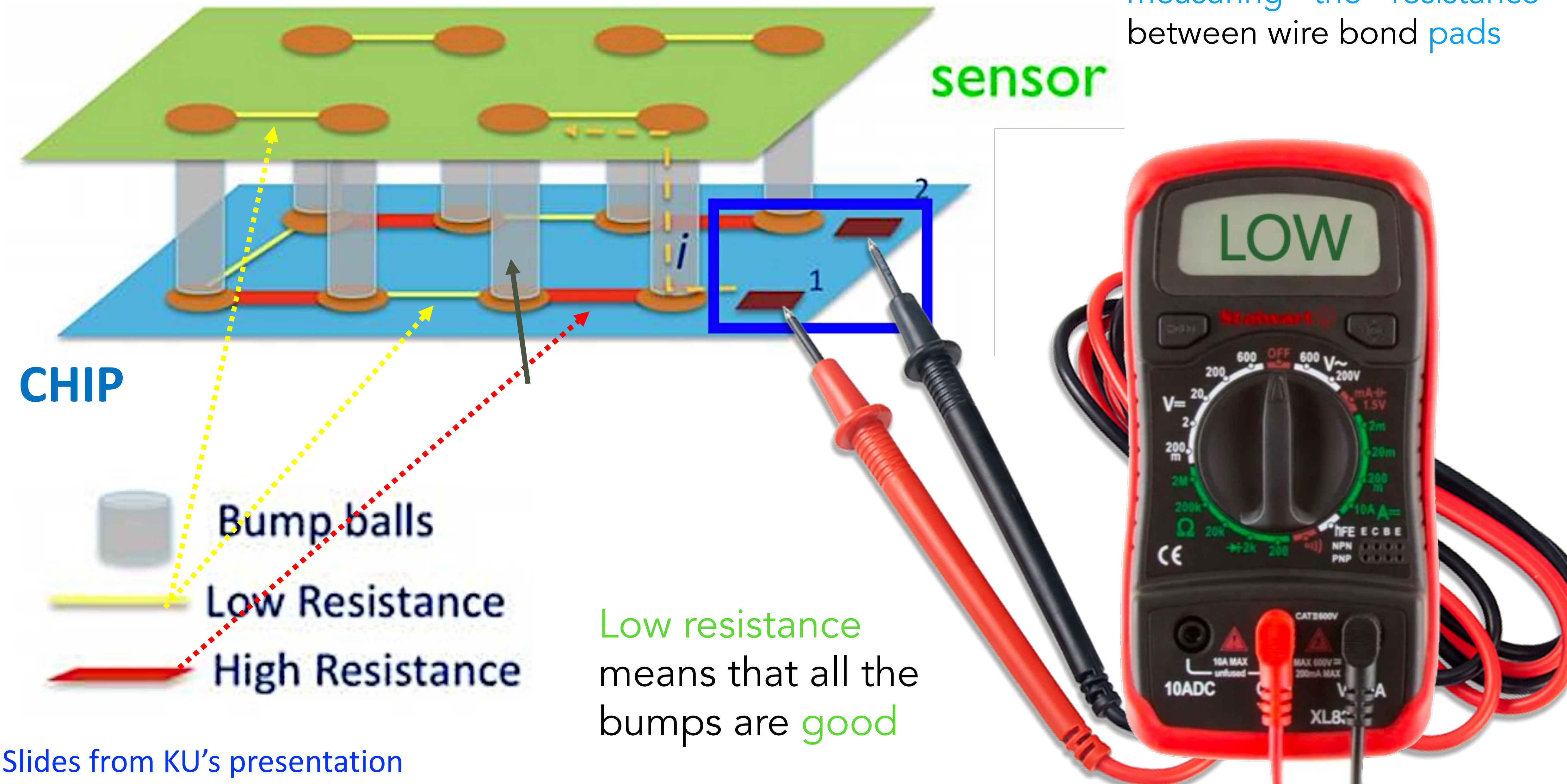
Interference between single chips : OK



Contamination of wire bonding pad : OK

Concept of electrical tests

determine the number of bumps per serpentine by measuring the resistance between wire bond pads



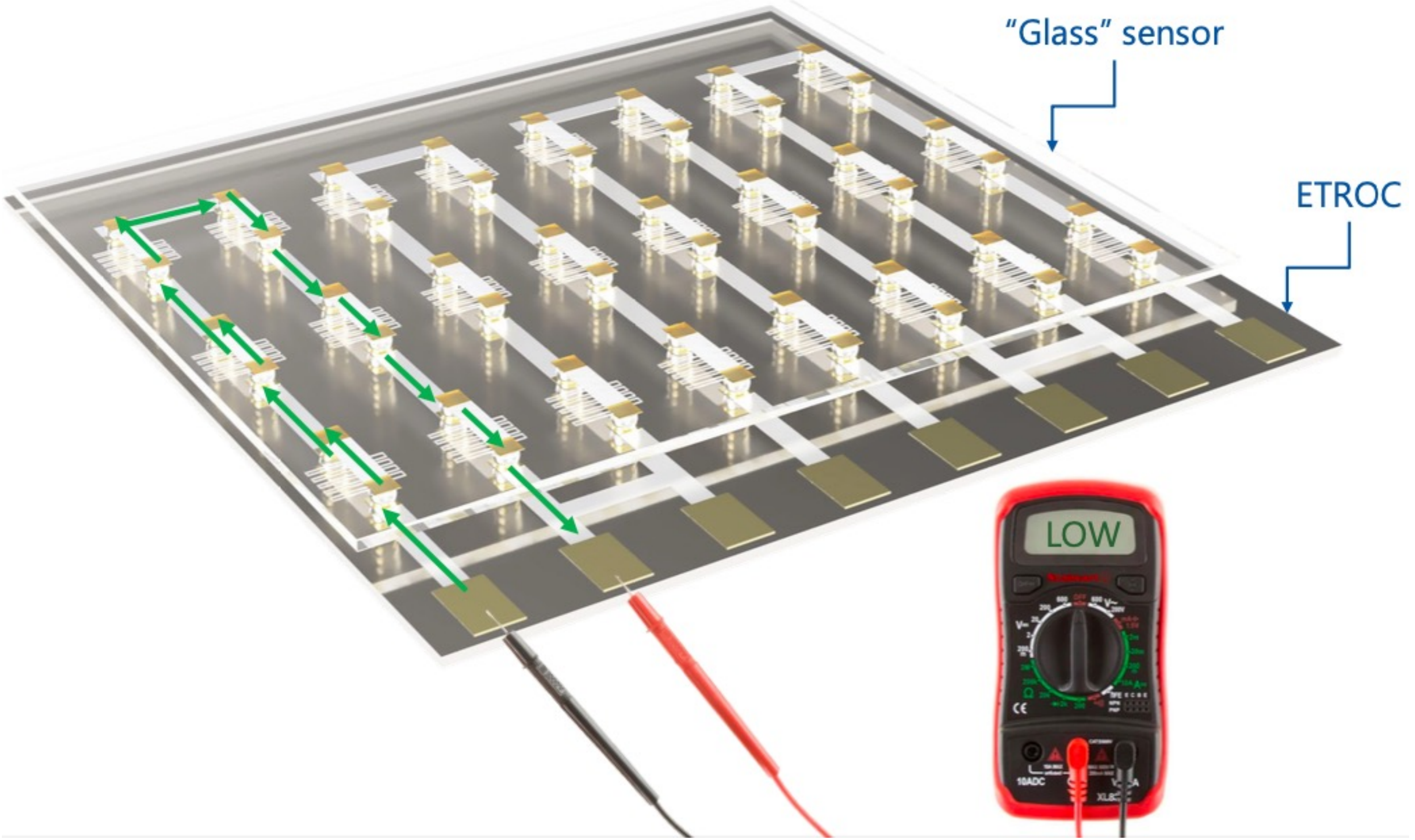
Low resistance means that all the bumps are good

Slides from KU’s presentation

Electrical tests (Good Bumps)

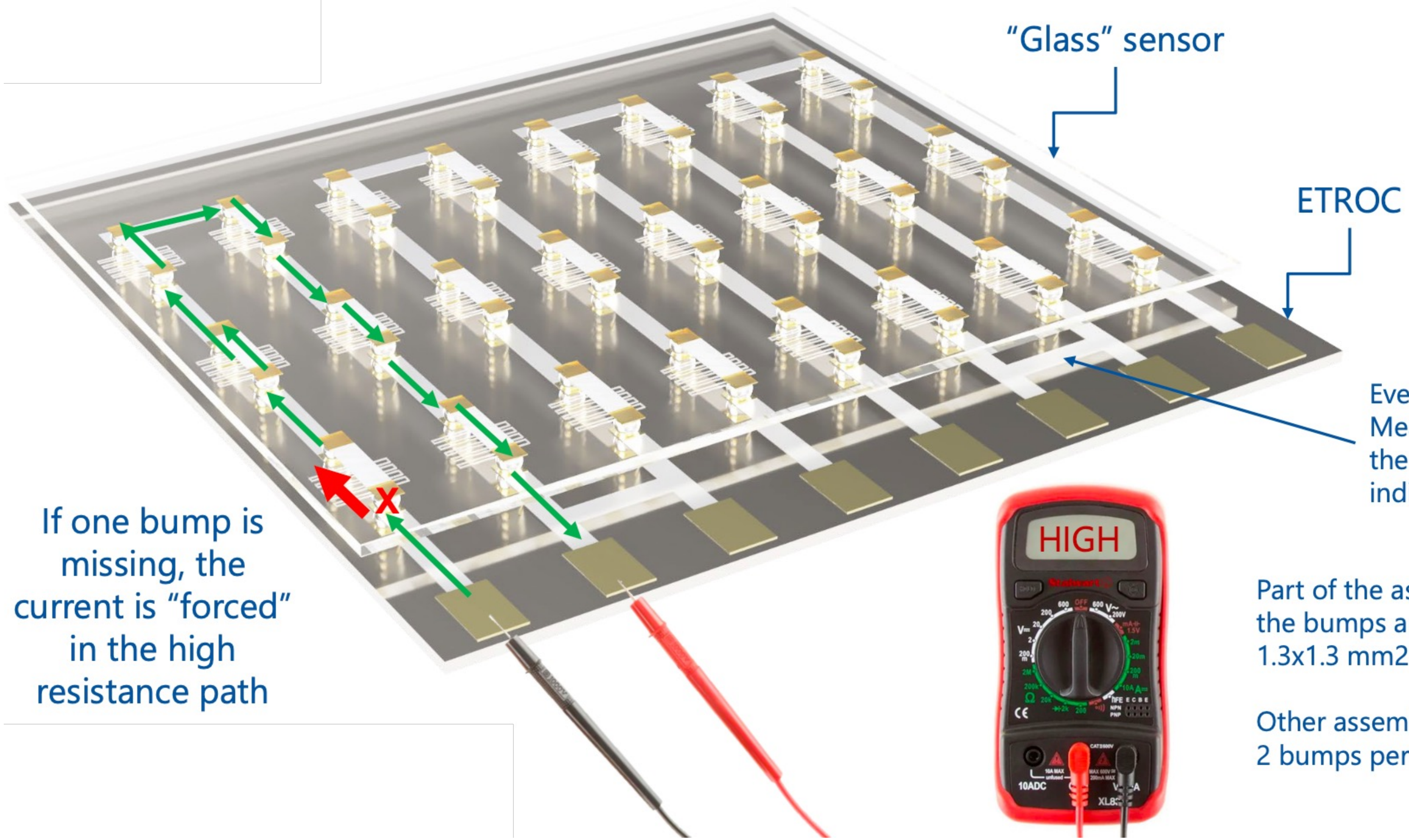
Slides from KU’s presentation

Dummy Assemblies they are designed to study bump bonding performance and yeld



Electrical tests (Bad Bumps)

Slides from KU’s presentation



If one bump is missing, the current is “forced” in the high resistance path

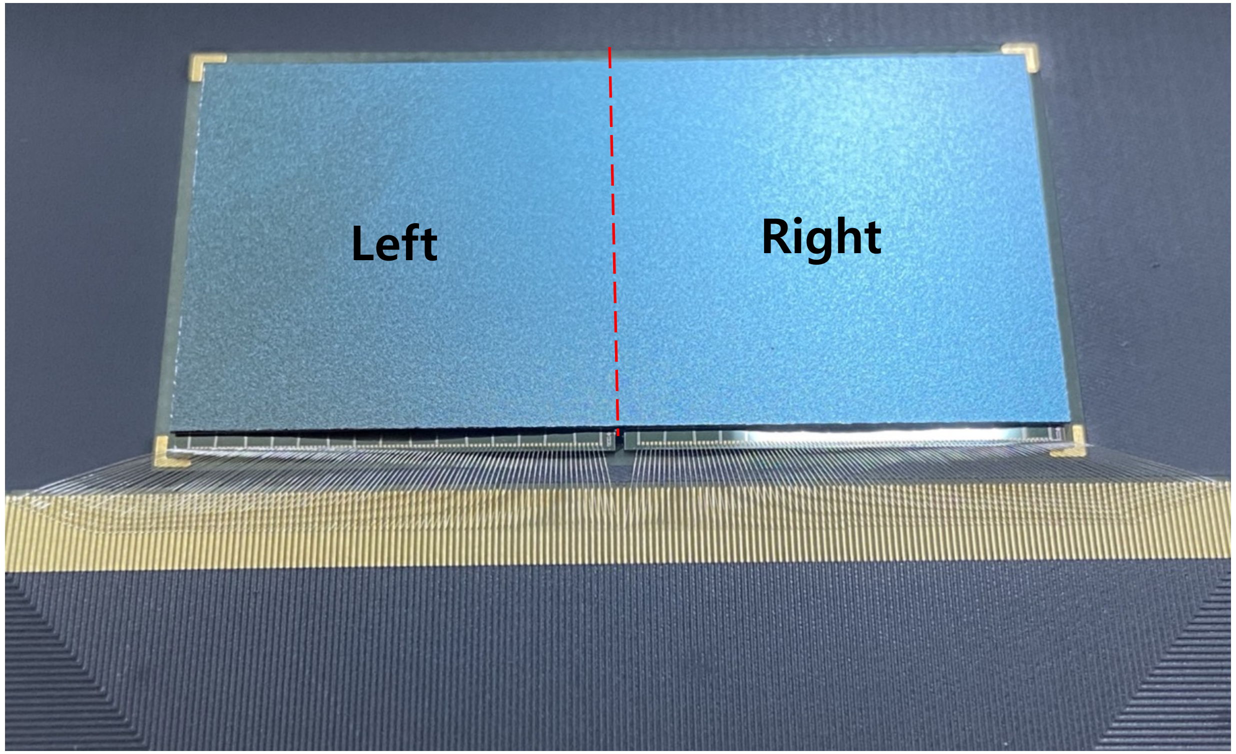
Every other pad there is a “short”: Measuring the resistance between the first and the last pad will give an indication of all the missing bump

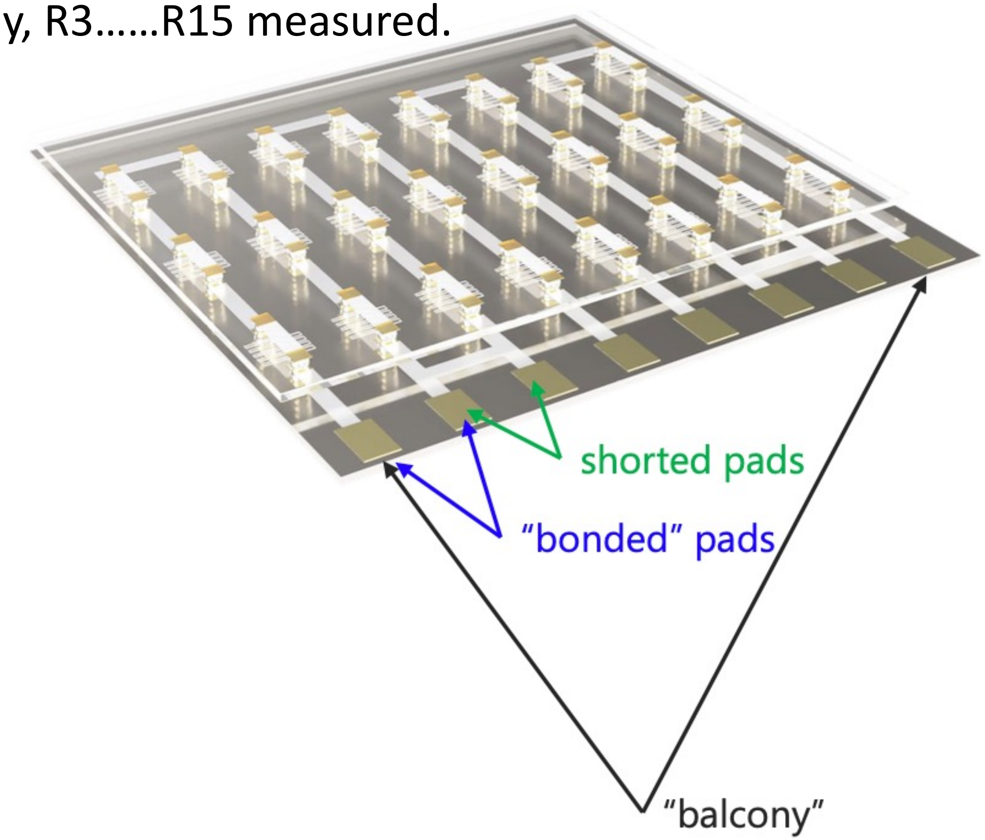
Part of the assemblies are “SINGLE BUMP”: the bumps are placed to simulate 1 bump per 1.3x1.3 mm2 pixel

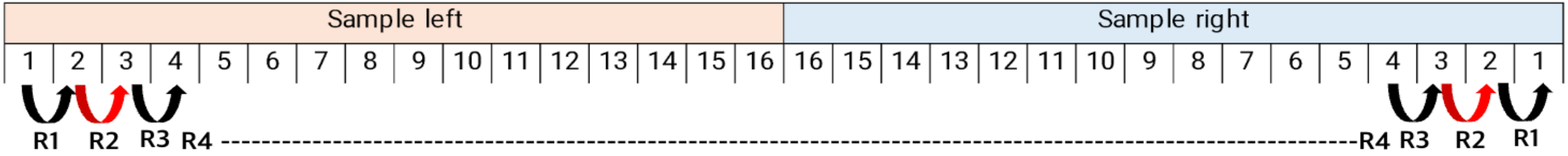
Other assemblies are “DOUBLE BUMPS”: 2 bumps per pixel

Electrical tests on Bump-bonding sensors

- Only pads capable of measuring resistance are selected and measured (16x16 bonded sensors (3 sets))
- Measurement method: (from R1 to R15)
  - 1st pad-2nd pad resistance measurement (R1)
  - 2nd pad-3rd pad resistance measurement (R2), in the same way, R3……R15 measured.
- Resistance measurements are made using a multi-meter.





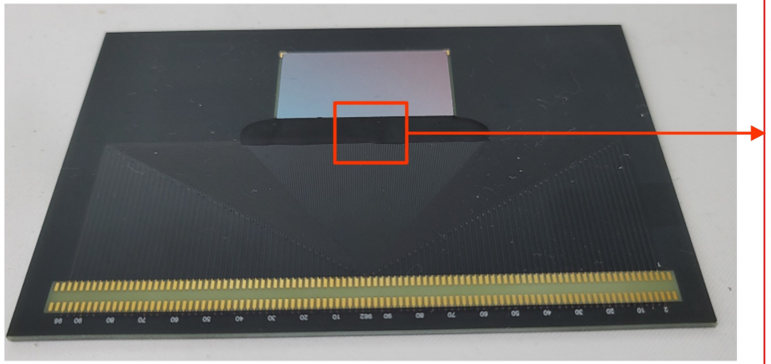


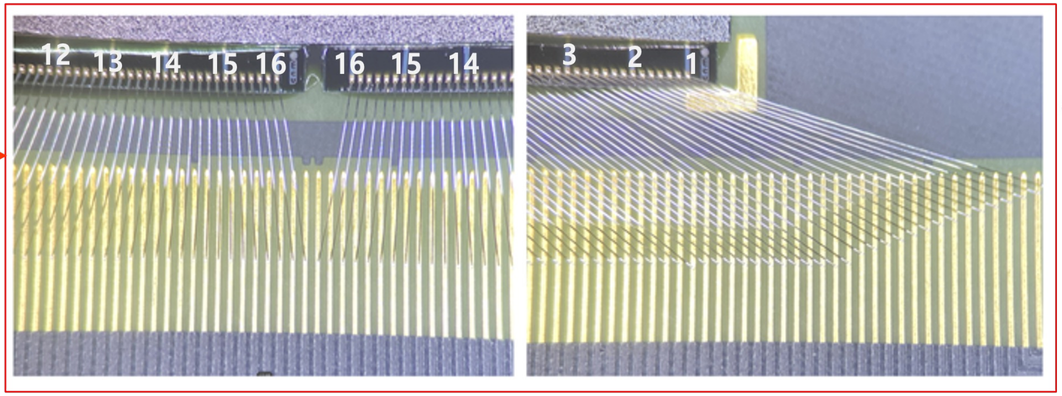
Sample left																Sample right															
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

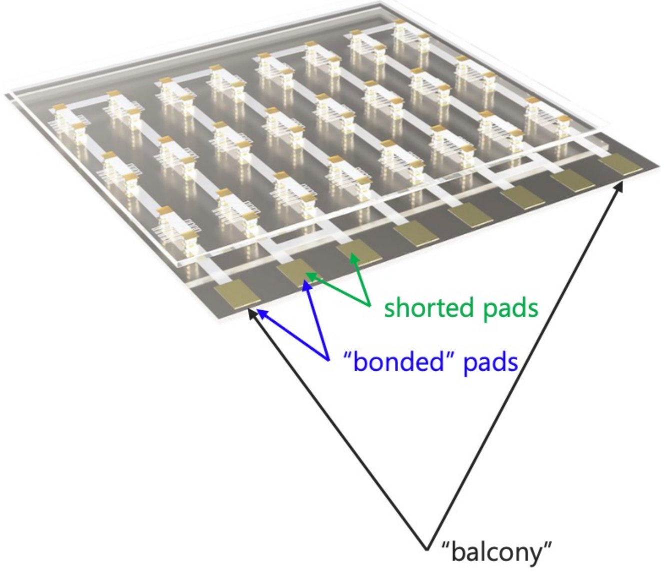
R1 R2 R3 R4 --R4 R3 R2 R1

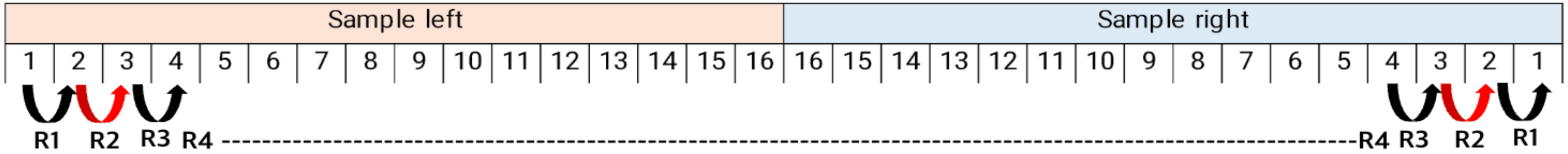
Electrical tests on Bump-bonding sensors

MEMSPACK
MEMS.IOT.Sensor





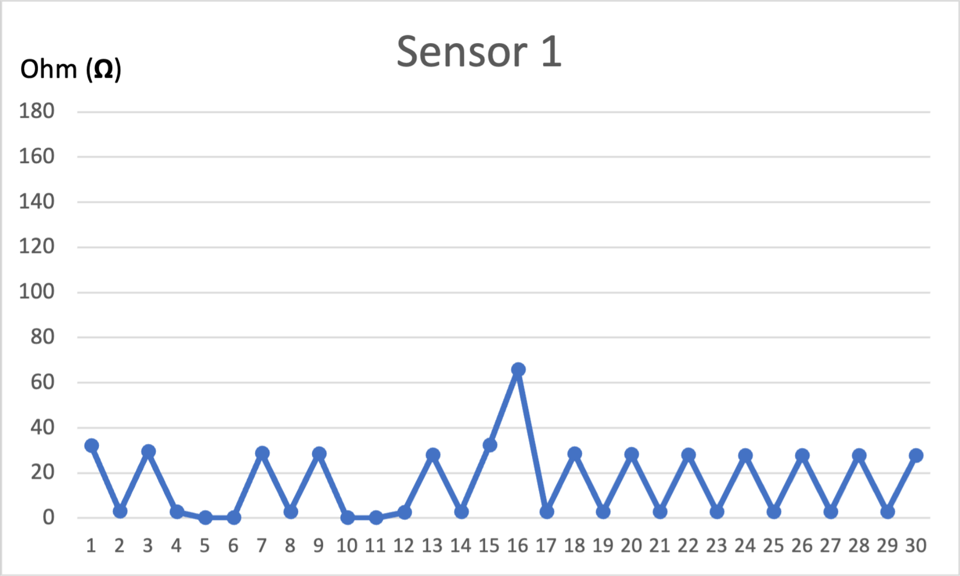


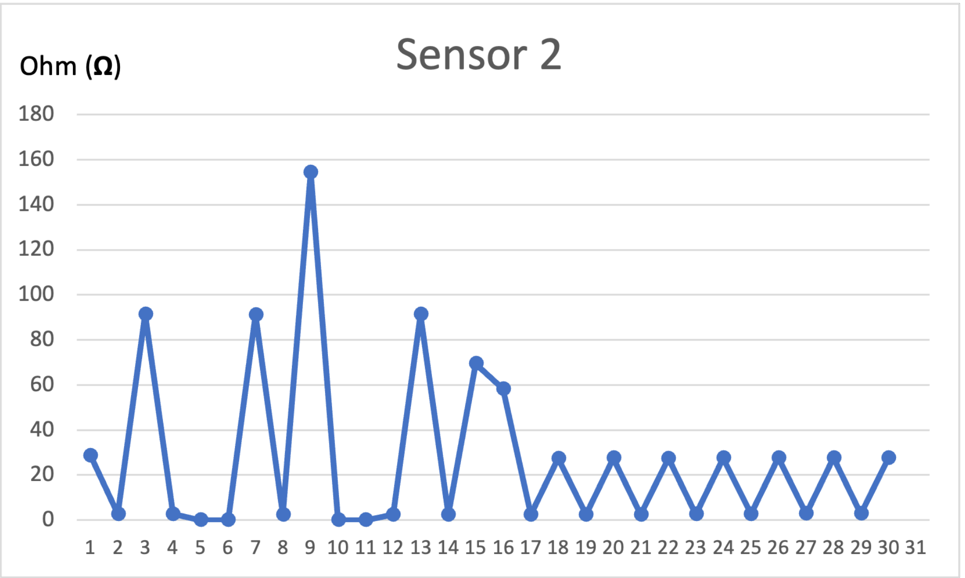


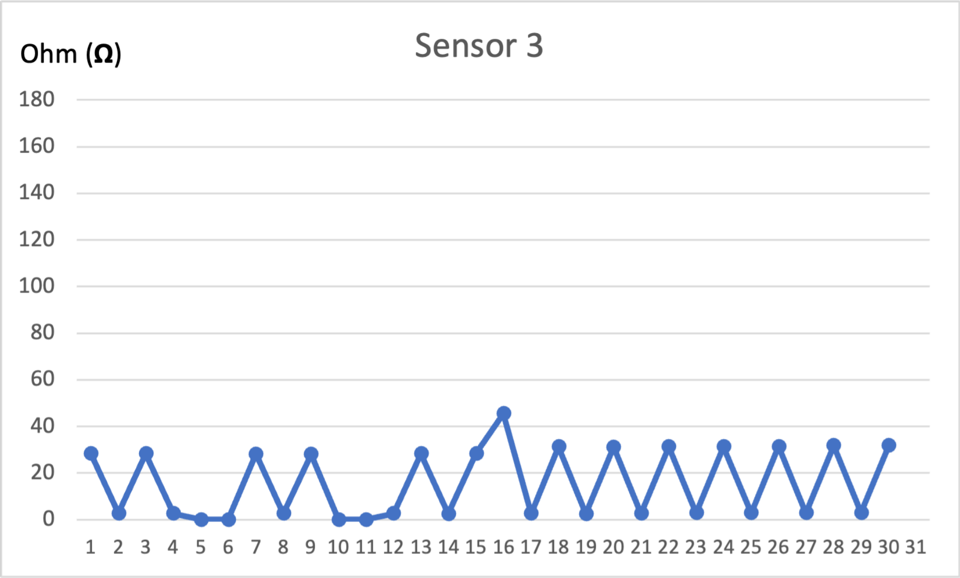
Ω	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
S1	31.9	2.9	29.4	2.7	X	X	28.7	2.7	28.4	X	X	2.5	28.0	2.7	32.2	65.6	2.6	28.4	2.7	28.1	2.7	28.0	2.7	27.7	2.7	27.7	2.8	27.7	2.7	27.7
S2	28.6	2.7	91.4	2.7	X	X	91.1	2.5	154.4	X	X	2.4	91.3	2.5	69.4	58.3	2.4	27.4	2.4	27.5	2.5	27.4	2.6	27.5	2.7	27.6	2.8	27.7	2.8	27.7
S3	28.3	2.7	28.3	2.6	X	X	28.1	2.6	28.0	X	X	2.6	28.3	2.4	28.4	45.5	2.6	31.3	2.5	31.1	2.6	31.2	2.8	31.2	2.8	31.4	2.8	31.7	2.9	31.7

- Checked most uniform values measured in odd number (several tens ohm) and even number (several tens ohm).
- The "x" mark is a pad that cannot be measured, left sample identified in the same position.

Distribution of resistances from bonding points



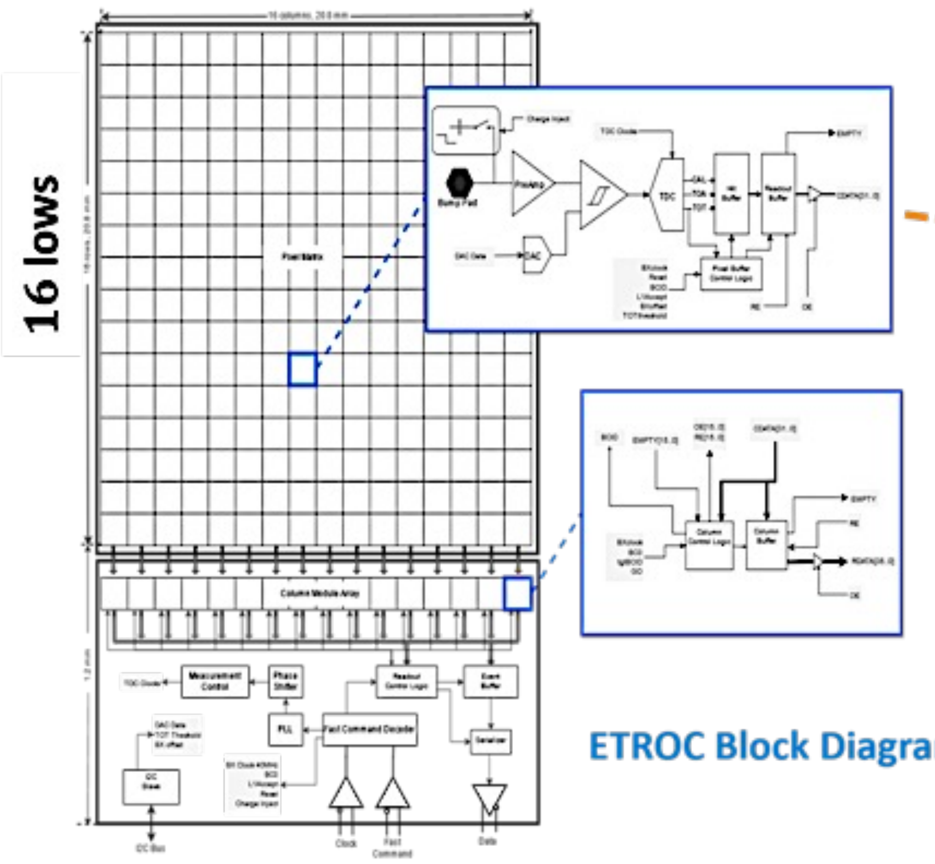




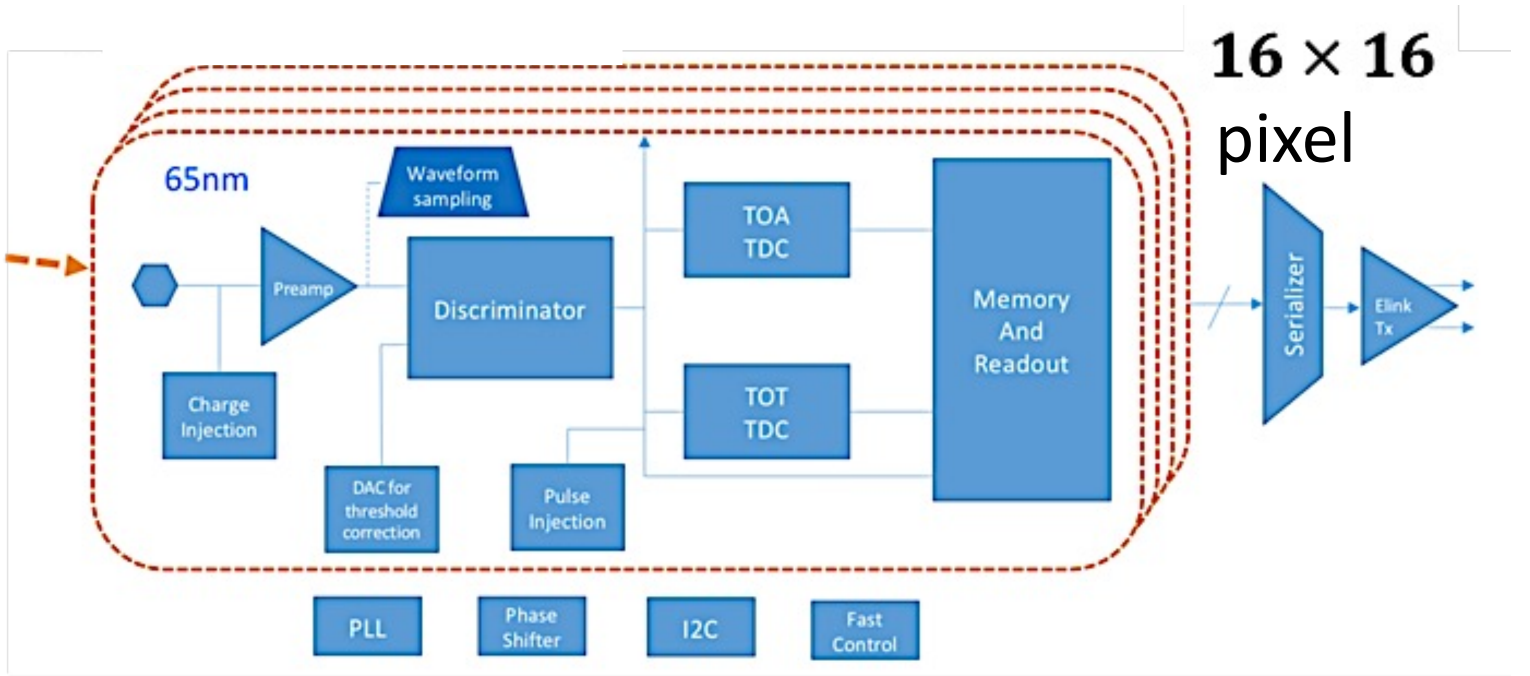
Almost uniform distributions as expected
: Maximum fluctuation 156 Ω

Plan to participate another bump-bonding tests with real LGAD and ETROC2 chip.

Endcap Timing Layer ReadOut Chip (ETROC)



ETROC Block Diagram

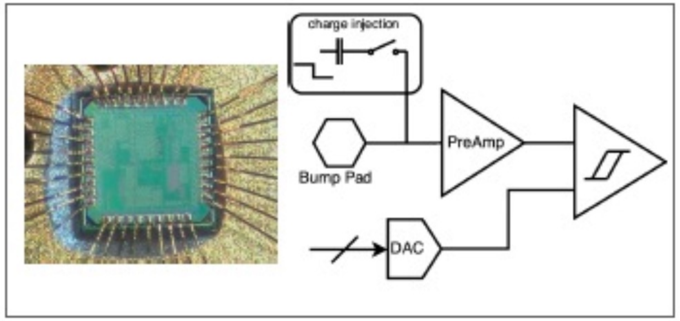


- ❑ Total ETROC size: 16 X 16 pixel cell
  - One pixel cell size: 1.3mm X 1.3mm to match the LGAD sensor pixel size
- ❑ Targeting signal charge (1MIP): 6 - 20 fC
- ❑ TDC (time-to-digital converter) range
  - ~5 ns TOA (time of arrival)
  - ~10 ns TOT (time over threshold)

ETROC Development Plan

2018

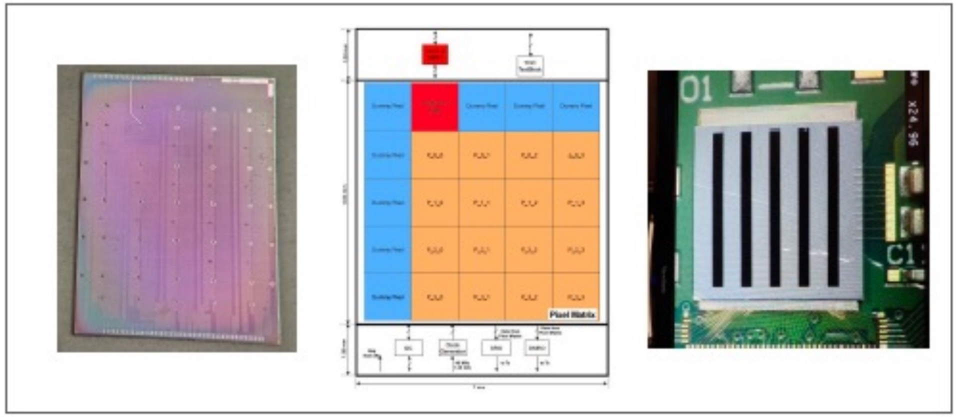
ETROC0 (1x1)



- Analog front-end only
- Wire-bonded with LGAD sensor reached ~33 ps time resolution per hit with preamp. waveforms
- Passed 100 Mrad TID

2020

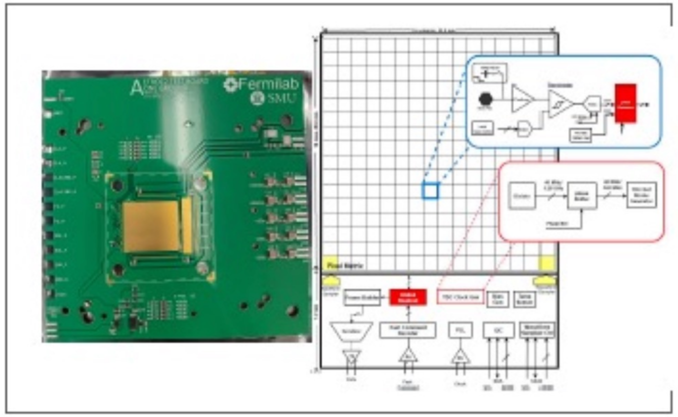
ETROC1 (4x4)



- Added low-power TDC and 4x4 H-tree for clock distribution
- Bump-bonded with LGAD sensor reached ~42 ps time resolution per hit with TDC data

2023

ETROC2 (16x16)

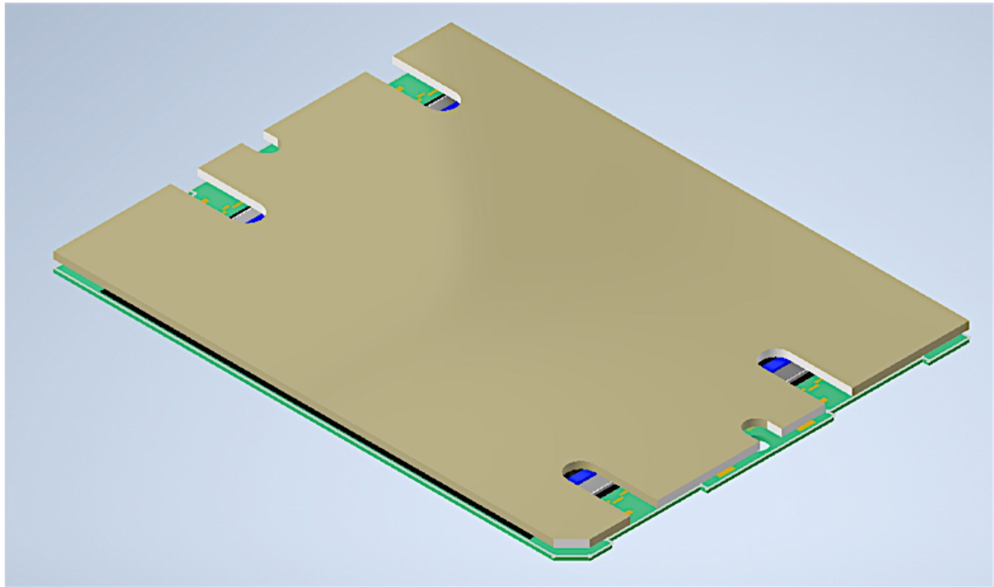


- First full-size chip (16x16) with all desired functionalities included
- All analog blocks silicon-proven; all digital blocks were verified in FPGA emulator

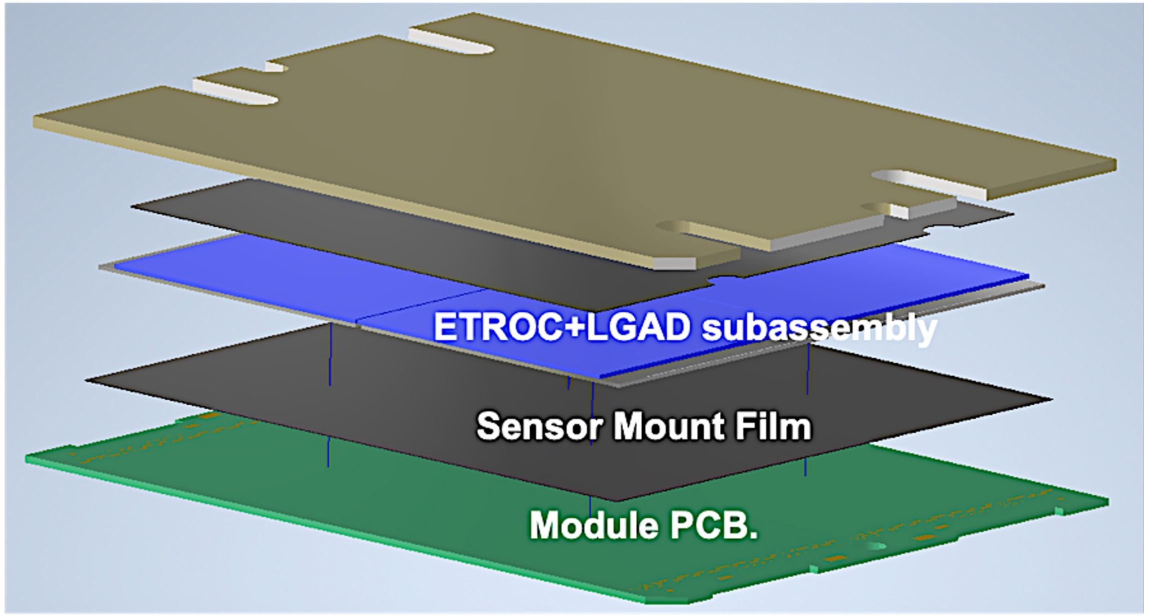
- ❑ **ETROC3 : Final chip**
  - The same functionalities as ETROC2, with improvements based on what will be learned from extensive ETROC2 testing
  - Submission scheduled for 2024

ETL Module design overview

- ❑ Module design overview



PCB + subassembly

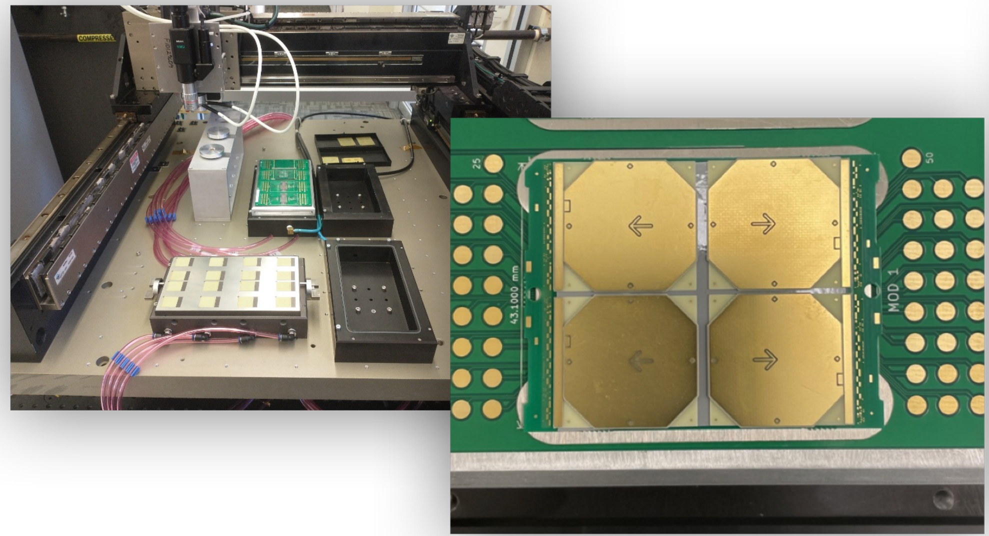


Basic scheme of a module

- ❑ Module PCB
  - Printed circuit board that serves as the power and readout interface for the module
- ❑ 4x ETROC+LGAD subassembly
  - 2x2 arrangement of bump-bonded assemblies
  - Each of a 16x16 pixel LGAD sensor and an “ETROC” readout chip

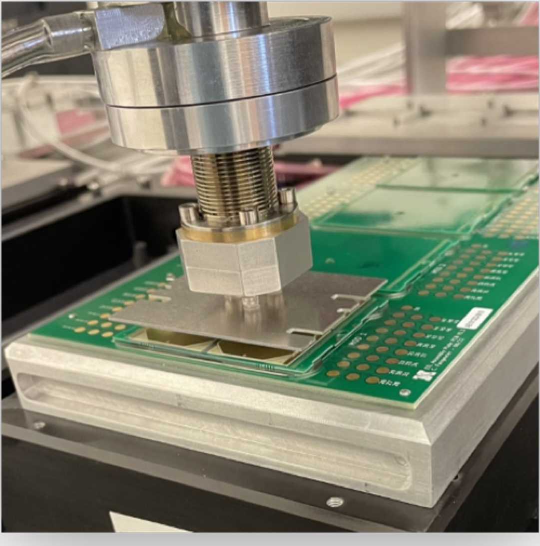
Assembling the ETL Modules

- The ETL detector will need ~8 thousand modules
- Each module will be made of 4 LGAD sensors and ETROCs
- An automated robotic gantry will be used for precision placement at the 10 micron level
- All modules will then be assembled into disks at CERN



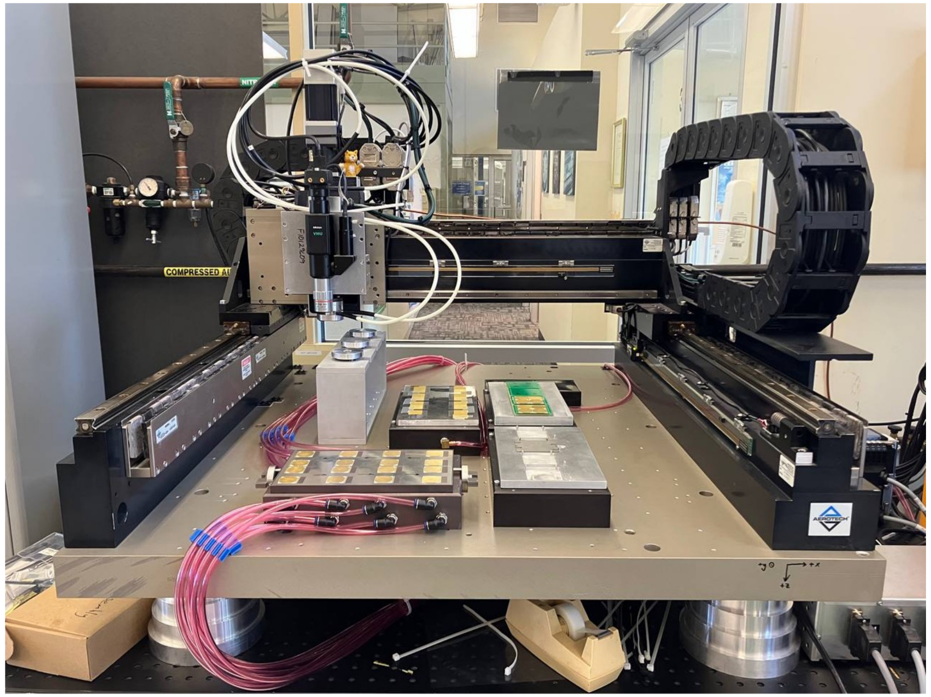
Pick & place sensor + PCB

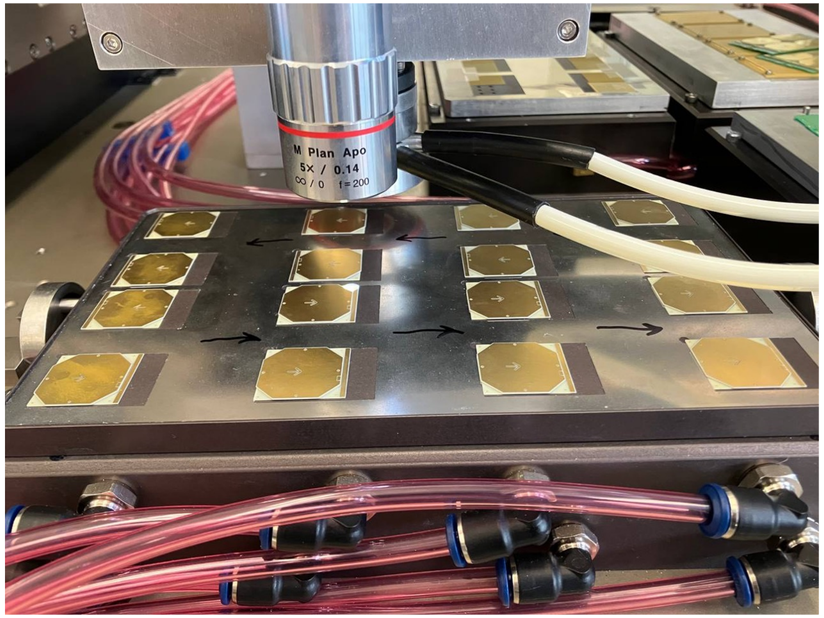
Wirebond and encapsulating

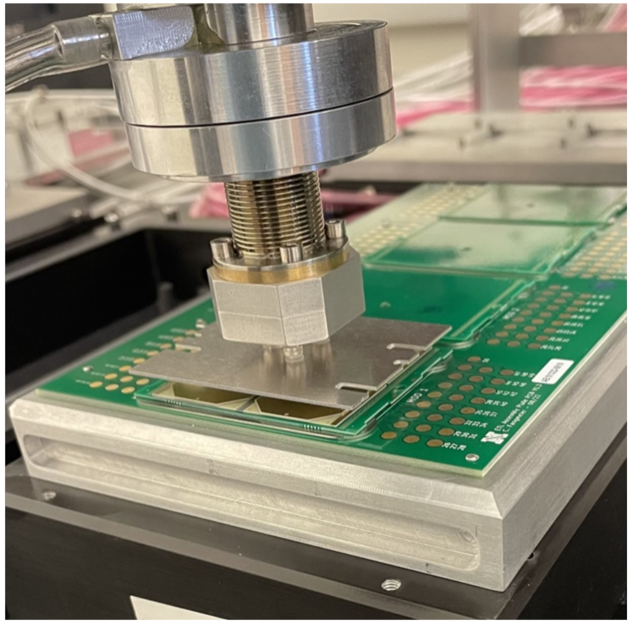


Apply film to baseplate, pick and place, and cure film

ETL Module assembly with Gantry

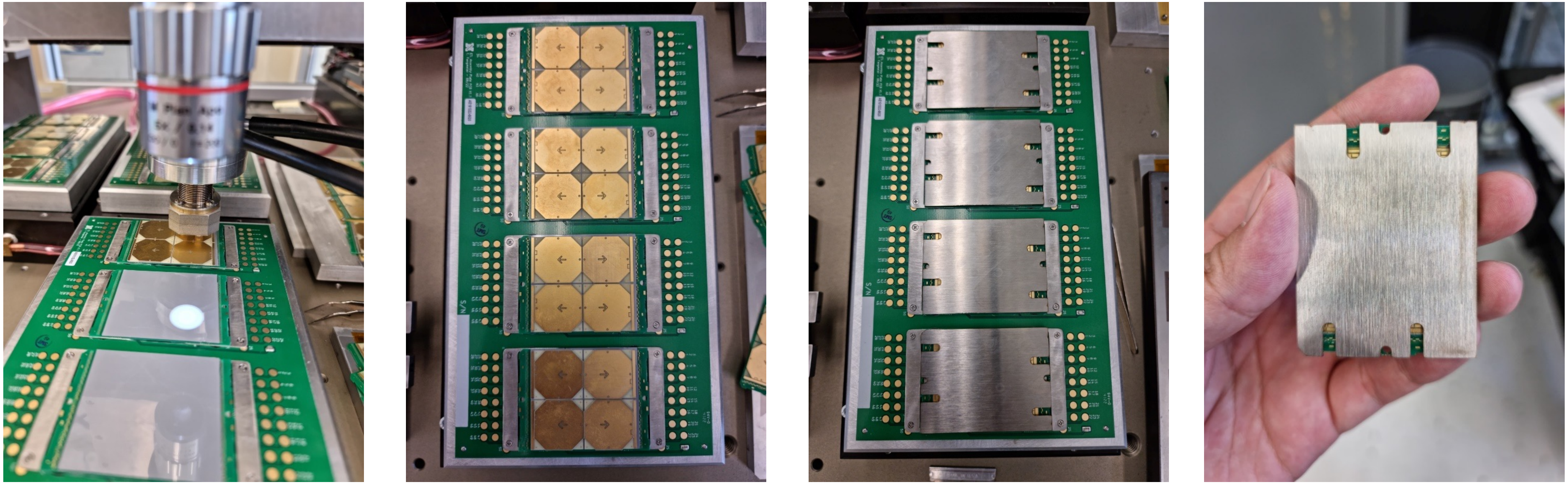






- Aerotech 3+1 axis gantries were used for ETL module assembly.
- Based on a vacuum pump
  - Modules PCBs and sensors are securely fixed.
  - Vacuum arm is used for picking and moving sub-assembly.
- The robot arm rail is moved using magnetic force, enabling precise operations at the 10μm level
- The camera measures and automatically corrects the position, rotation, and tilt of the sensors
- Checking production capacity of 100 modules per week

Gantry Based Throughput



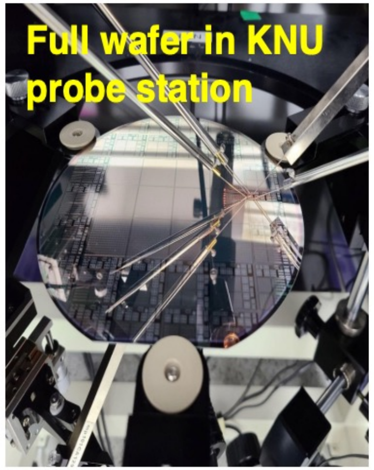
- Preparation of the full assembly process is complete and good to go
- 50% throughput demonstration with mockup components ongoing at assembly sites
- Robotic gantry is showing good subassembly alignment below the 100 μm limit

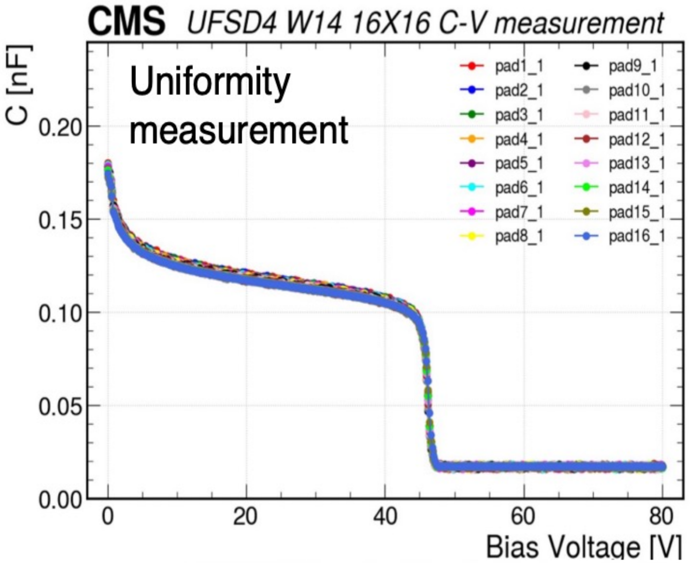

FID129CD9
FID129CD8
Mitutoyo
VMU
Code No. 378-505
Model VMU-V
Serial No. 001819
Mitutoyo Corporation
M Plan Apo
5X / 0.14
∞ / 0

Current Korea CMS Activities and Future plan

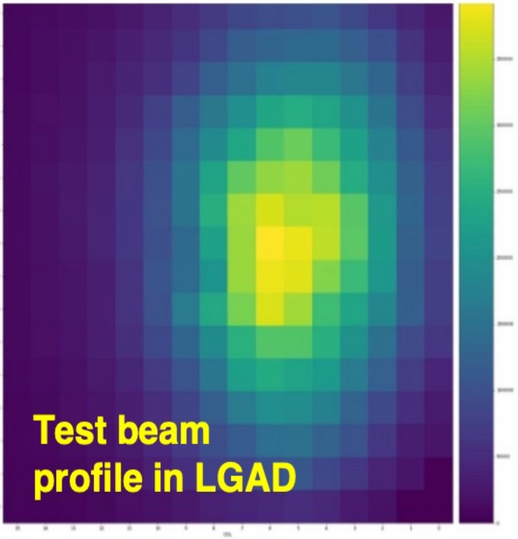
- **KCMS responsible for the delivery of one layer of ETL sensors!**
  - **25% of the total endcap coverage**

- **Significant contributions to prototyping towards production:**
  - **LGADs prototyping and validation**:
    - Detailed testing of prototype LGADs informed vendor qualification
    - Probe station measurements to verify quality and uniformity of full-size wafers
  - **ETROC2 testing**
    - Active in ETROC testing, including test beam campaigns for validation of the performance of the LGADs + ETROC chain
  - **Wafer processing:**
    - Exploring wafer processing with one of the qualified LGADs vendors for wafer thinning, dicing, and surface preparation at Korean companies for the production phase
  - **Bump-bonding:**
    - Exploring options with Korean companies for LGAD-to-ETROC bump-bonding during production

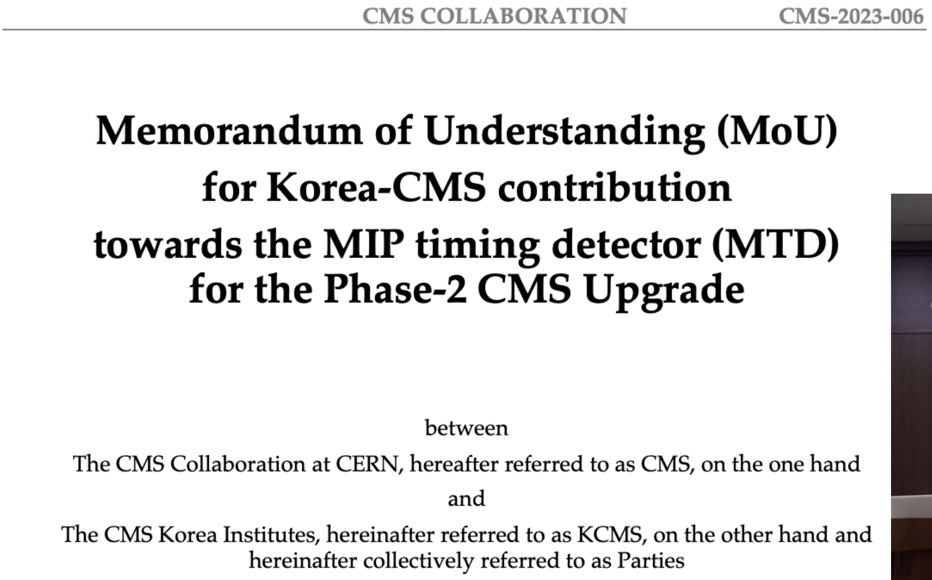

Full wafer in KNU probe station




LGAD+ETROC2 test board


Test beam profile in LGAD

CERN-Korea CMS Sign-up Ceremony for the MTD project



CMS COLLABORATION CMS-2023-006

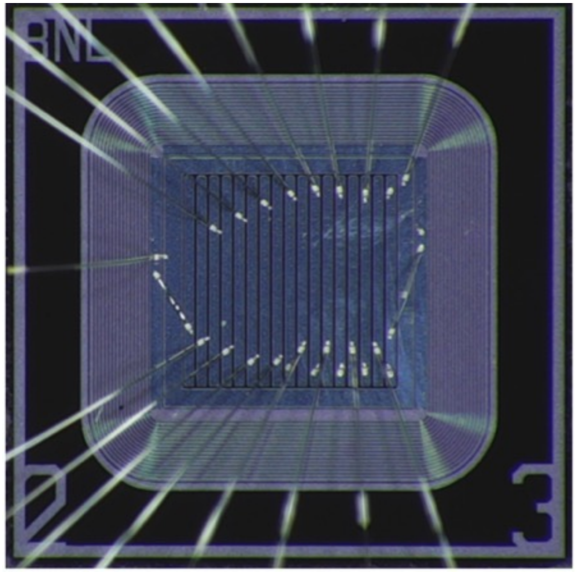
Memorandum of Understanding (MoU)
for Korea-CMS contribution
towards the MIP timing detector (MTD)
for the Phase-2 CMS Upgrade

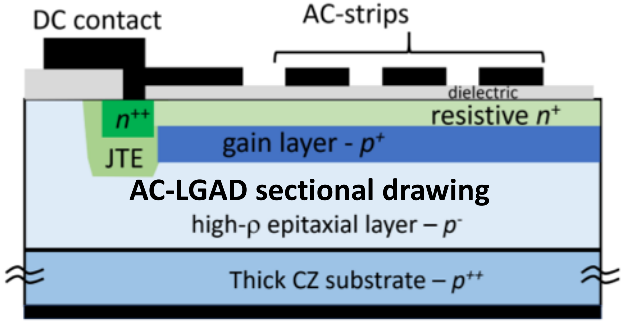
between
The CMS Collaboration at CERN, hereafter referred to as CMS, on the one hand
and
The CMS Korea Institutes, hereinafter referred to as KCMS, on the other hand and
hereinafter collectively referred to as Parties

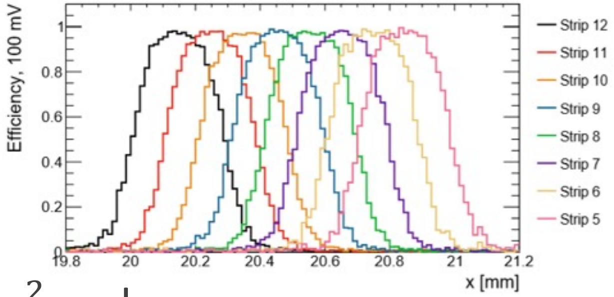
- ❑ **Korea CMS group** will contribute the **LGAD production (25%), bump bonding process, front-end ASICs and module structures**, etc.
- ❑ Total budget: **2.2M CHF** (equivalent to USD) supported by National Research Foundation of Korea (NRF)

Prototype next-generation LGAD sensor development

Prototype AC-LGAD Sensor



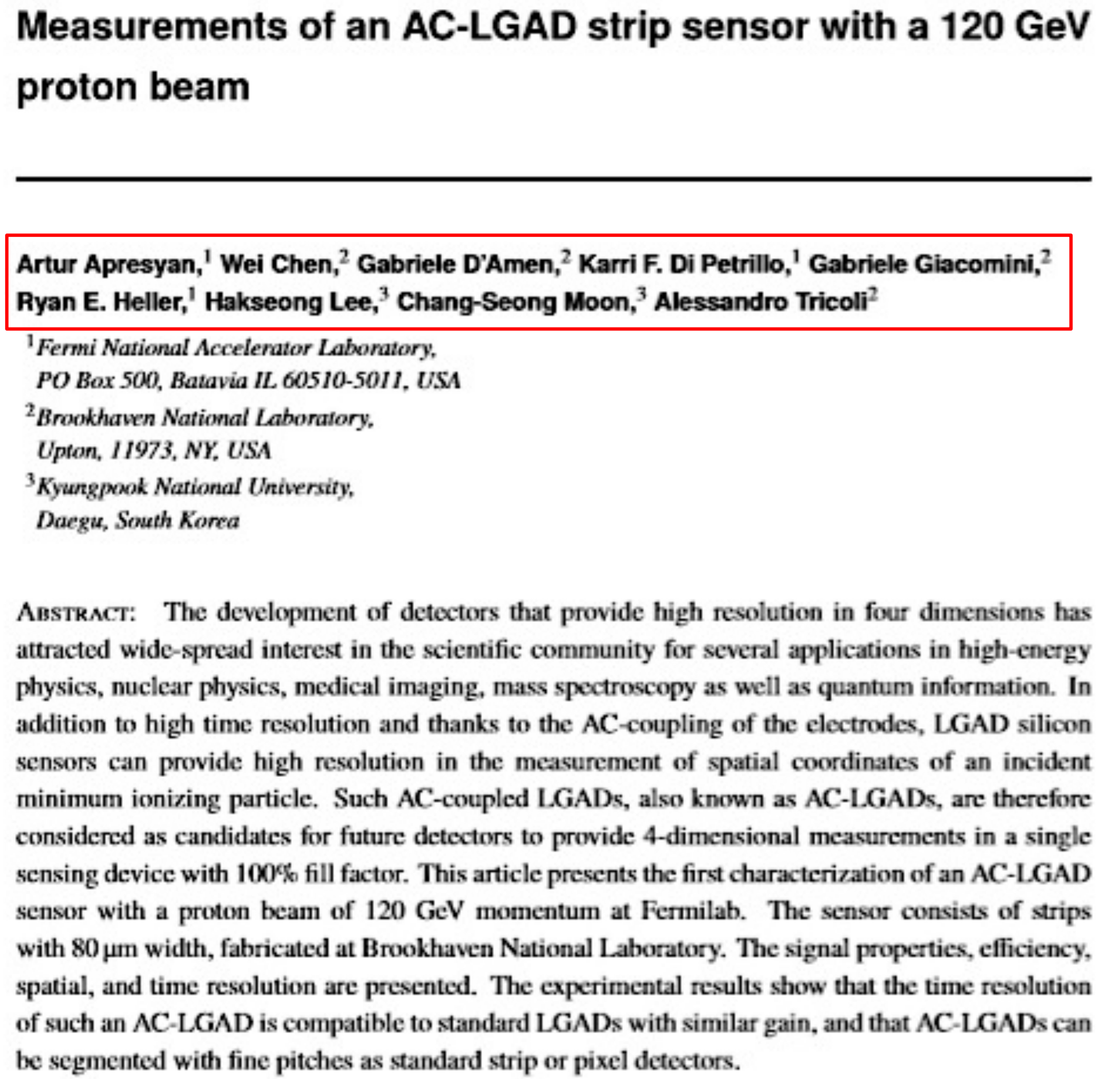




- ❑ CMS plan to use 1.3x1.3 mm^2 pads
  - ◦ 50-80 μm inactive region between pads
- ❑ AC LGAD have been developed to solve fill factor problem
  - ◦ DC pad surrounding 17 AC strip
  - ◦ 1.67 mm long with pitch of 100 μm
  - ◦ 50 μm thick substrate
- ❑ AC-LGAD can be used in future collider experiment
- ❑ AC-LGAD sensor test result was published in JINST
  - ◦ 2020 JINST 15 P09038

Research result publication

2020 JINST 15 P09038



Measurements of an AC-LGAD strip sensor with a 120 GeV proton beam

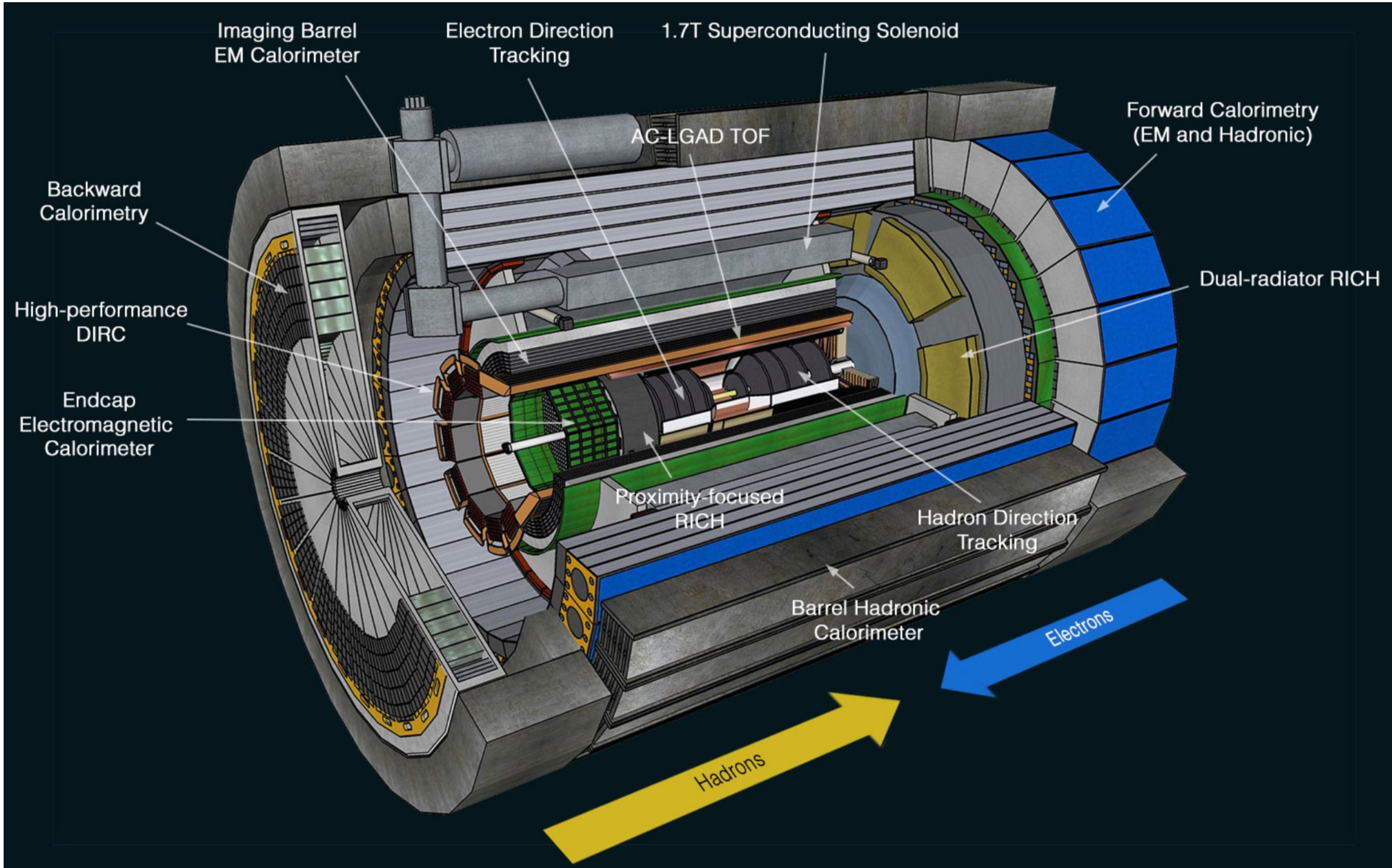
Artur Apresyan,[1] Wei Chen,[2] Gabriele D'Amen,[2] Karri F. Di Petrillo,[1] Gabriele Giacomini,[2] Ryan E. Heller,[1] Hakseong Lee,[3] Chang-Seong Moon,[3] Alessandro Tricoli[2]

[1] *Fermi National Accelerator Laboratory,*
PO Box 500, Batavia IL 60510-5011, USA
[2] *Brookhaven National Laboratory,*
Upton, 11973, NY, USA
[3] *Kyungpook National University,*
Daegu, South Korea

ABSTRACT: The development of detectors that provide high resolution in four dimensions has attracted wide-spread interest in the scientific community for several applications in high-energy physics, nuclear physics, medical imaging, mass spectroscopy as well as quantum information. In addition to high time resolution and thanks to the AC-coupling of the electrodes, LGAD silicon sensors can provide high resolution in the measurement of spatial coordinates of an incident minimum ionizing particle. Such AC-coupled LGADs, also known as AC-LGADs, are therefore considered as candidates for future detectors to provide 4-dimensional measurements in a single sensing device with 100% fill factor. This article presents the first characterization of an AC-LGAD sensor with a proton beam of 120 GeV momentum at Fermilab. The sensor consists of strips with 80 μm width, fabricated at Brookhaven National Laboratory. The signal properties, efficiency, spatial, and time resolution are presented. The experimental results show that the time resolution of such an AC-LGAD is compatible to standard LGADs with similar gain, and that AC-LGADs can be segmented with fine pitches as standard strip or pixel detectors.

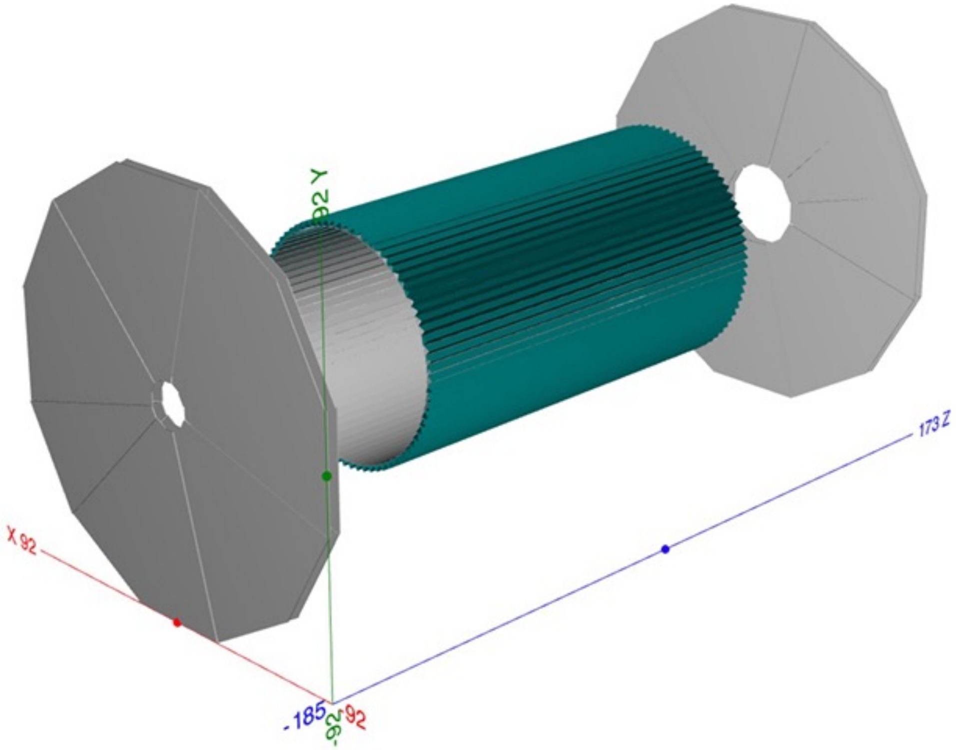
AC-LGADs for Electron Ion Collider

- AC-LGAD based Time of Flight (TOF) can provide the Particle ID for every particle in EIC.
  - based on 30 ps timing resolution
  - Ideally coarse pitch (500 μm, 1-2 cm strips) for sparse readout
  - TOF can be used tracking layer (~20 μm resolution)



AC-LGADs for Electron Ion Collider

AC-LGAD TOF Detectors for EIC – eRD112



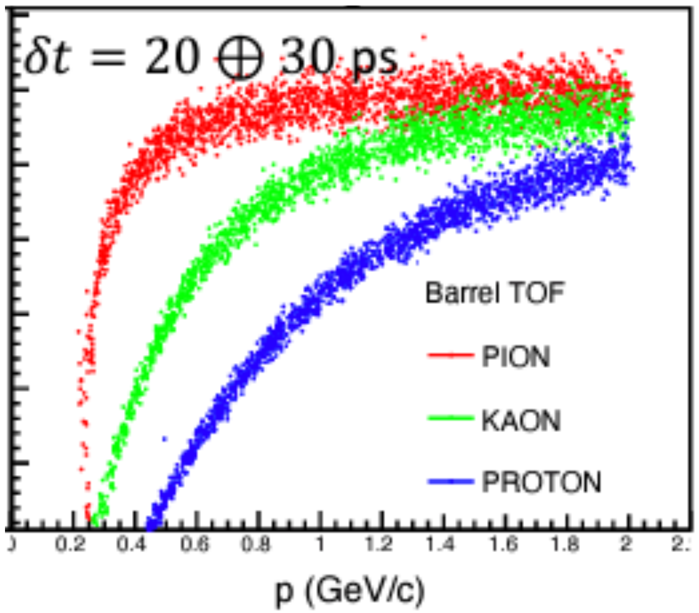
Barrel TOF
Single layer with 30 ps resolution and $2\%X_0$ material budget per layer

Forward TOF
Double layer with 25 ps resolution and $5\%X_0$ material budget per layer

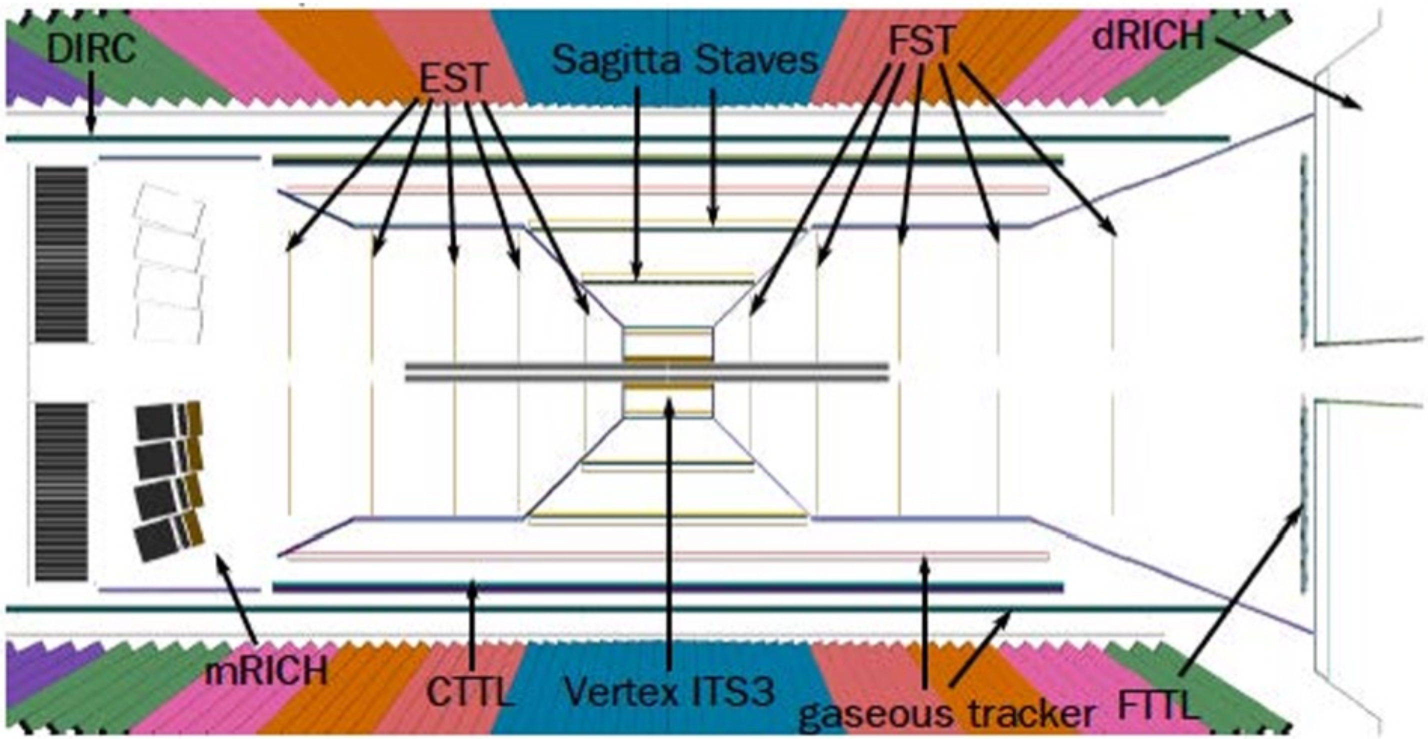
Backward TOF
Double layer with 25 ps resolution and $5\%X_0$ material budget per layer

START Time
20 ps resolution

Barrel TOF simulation (eta=0)



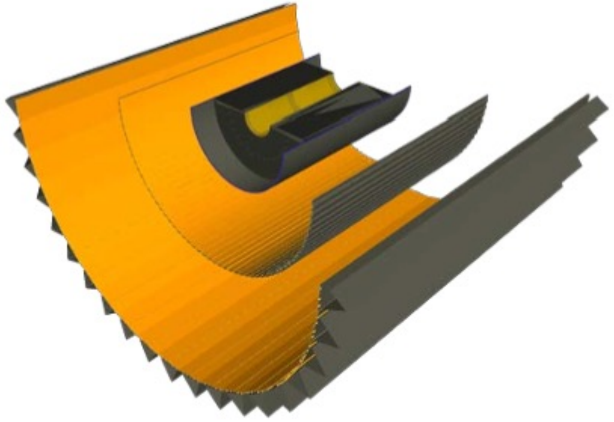
ePIC: Tracking and Vertexing

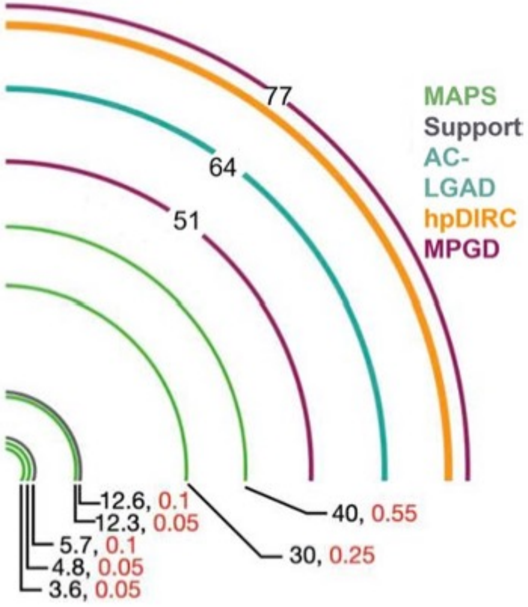


Technology mix

- **MAPS based Si-detectors**:
  $\sigma = 3\,\mu m \quad X/X_0 \sim 0.05 - 0.55\%/\text{layer}$
- **Gaseous tracker**:
  $\sigma = 150\,\mu m \quad X/X_0 \sim 0.2\%/\text{layer}$
- **AC-LGADs**:
  $\sigma = 30\,\mu\text{m},\ X/X_0 \sim$ 1-4 % /layer

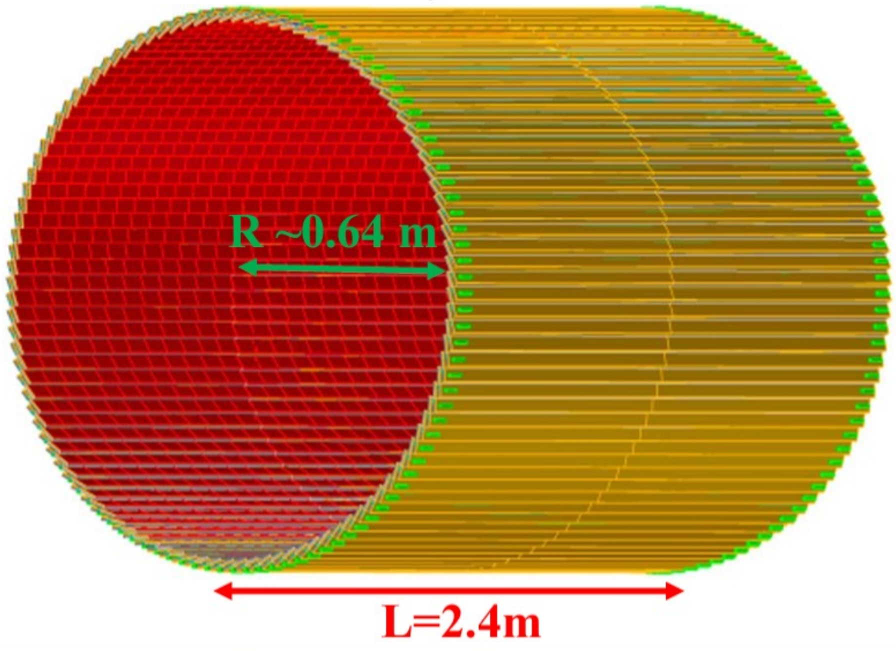
- **mid-rapidity:**
  Ultra thin MAPS based Si-detectors, gaseous detectors & AC-LGADs
- **Forward and Backward:**
  MAPS based Silicon discs & AC-LGADs
- Outer layers placed to provide seeds for tracking & ideal track points before/after PID detectors
- New Magnet with BABAR dimensions B = 1.7-2T



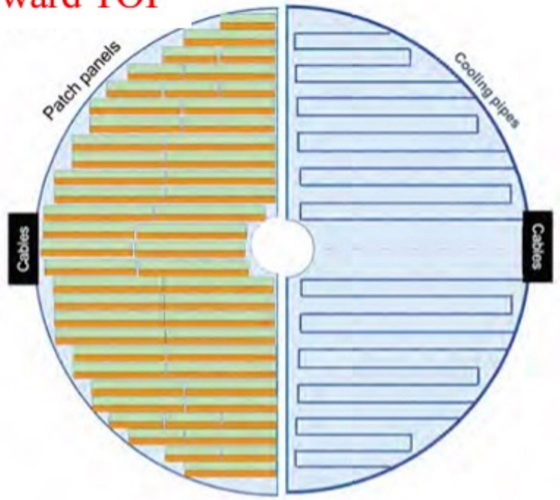


AC-LGAD Detectors for ePIC

ePIC Barrel TOF (~1% X_0)



Forward TOF



Roman Pots

	Area (m^2)	Channel size (mm^2)	# of Channels	Timing Resolution	Spatial resolution	Material budget
Barrel TOF	10.9	0.5*10	2M	30 ps	30 μm in $r \cdot \varphi$	0.01 X0
Forward TOF	2.22	0.5*0.5	6 M	25 ps	30 μm in x and y	0.08 X0
B0 tracker	0.07	0.5*0.5	0.3M	30 ps	20 μm in x and y	0.05 X0
RPs/OMD	0.14/0.08	0.5*0.5	0.6M/0.3M	30 ps	140 μm in x and y	no strict req.

Requirements on timing and spatial resolutions and material budget are still being evaluated and are subject to change as the design matures, and we will continue to explore common designs for these detectors where possible to reduce cost and risk.

Summary

- ❑ **The CMS MIP Timing Detector will measure precision timing of charged particles produced inside CMS.**
  - Provides significant pileup mitigation, furthering the experiment’s mission in the HL-LHC era.
  - Brings new capabilities to CMS that could help to search new phenomena in the HL-LHC.
- ❑ **BTL will be instrumented with LYSO crystals + SiPMs, read-out by the TOFHIR**
  - Beginning of life performance (30-40 ps) within requirements
  - End-of-life performance (~ 60 ps) close to requirements
  - The BTL prototyping phase is completed and now entering production phase
- ❑ **ETL will be instrumented with LGADs read out by the ETROC**
  - Performance at beginning and end of life within requirements (single hit resolution < 50 ps)
  - LGAD market survey done → Will enter a tender process soon.
  - Full-scale 16x16 ETROC2 arrived and Initial system test with bare ETROC2 in progress.
- ❑ **Common MTD DAQ system is being developed together for the ETL and BTL.**
- ❑ **Mechanical engineering of the full detector system is preparing.**