



# **SOFT ERROR RATE TEST METHODOLOGY FOR ADVANCE PROCESS NODES UNDER NEUTRON BEAM AT CHIPIR**

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# AGENDA

- Motivation
- Previous Experiments, New Design
- Experimental Setup
- The Math
- Results
- Issues/Future Work

# MOTIVATION

- FIT(Failures In Time) is a measurement of soft defects induced in silicon in the presence of high energy Neutron Particles found naturally.
- JEDEC Spec defines methodology and formulation for FIT rates.
- Nvidia Collects FIT data and does correlation to Foundry data.
- FIT rates help us determine
  - The amount of ECC logic to be added in a design.
  - Qualify
    - failure rate in the presence of bitcell interleaving for SRAMs.
    - process node and provide accurate FIT rates to our customers.
  - Find any design related issues causing skewed FIT rates for different data patterns.

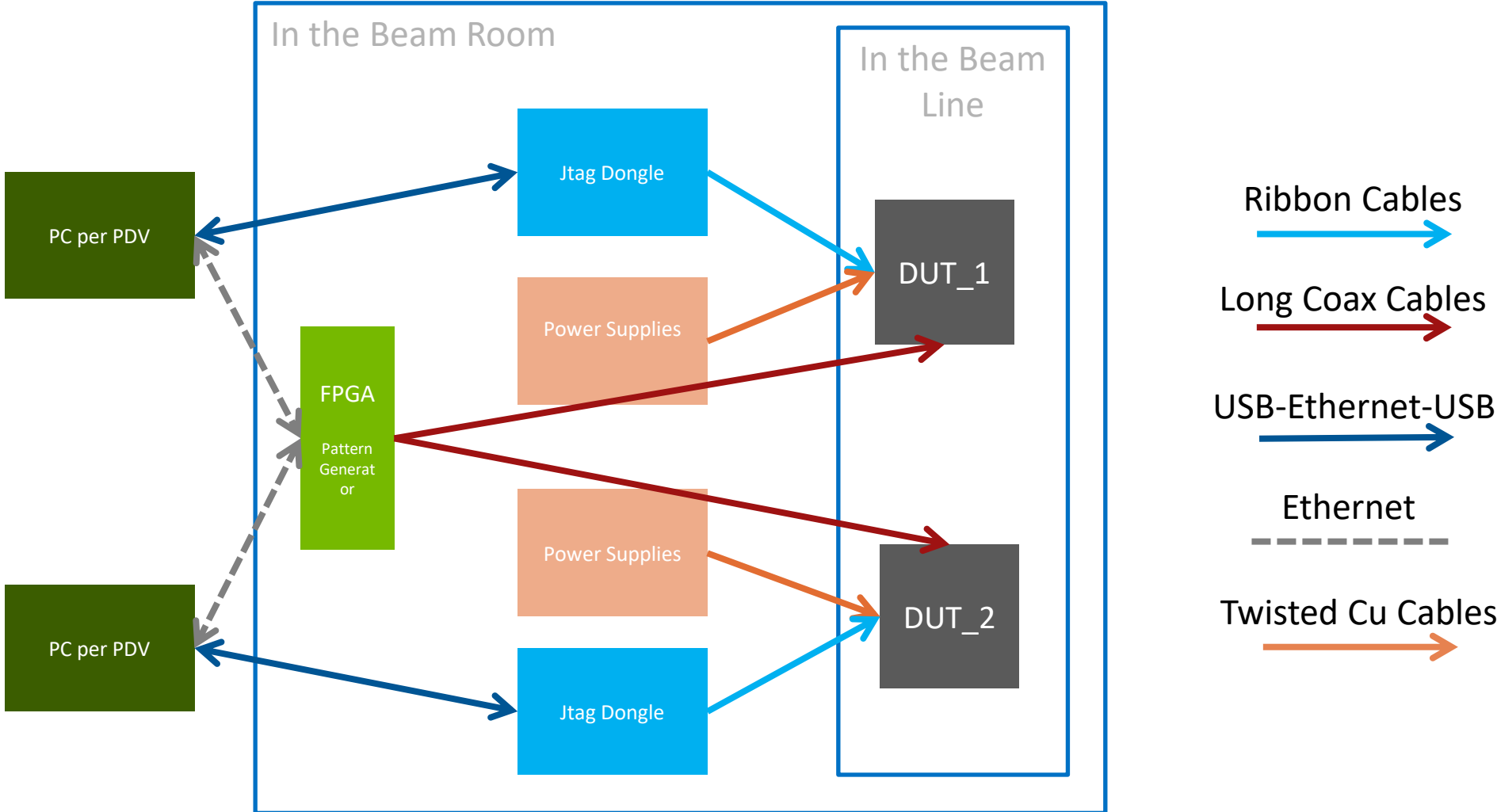
# DESIGN CHOICES

- ChipIR Beam –
  - Mimics energy spectrum of Neutron particles in the environment
  - Flux is  $1e^9$  X of Environment
- Full PC with GPU in Beam Line –
  - Complex setups
  - excessive Flux causes peripheral components to fail
- Process Design Vehicles (PDVs) –
  - Has dedicated hardware to find FIT rate
  - Works at very high flux
  - FIT for both SRAM and Logic Storage elements (Flops)
  - Similar design across process nodes

# EXPERIMENTAL SETUP

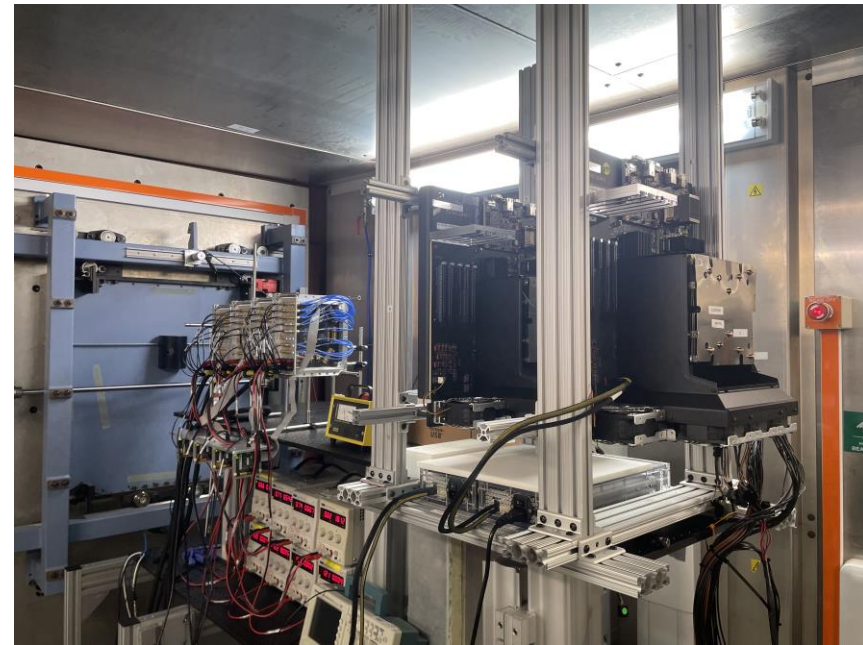
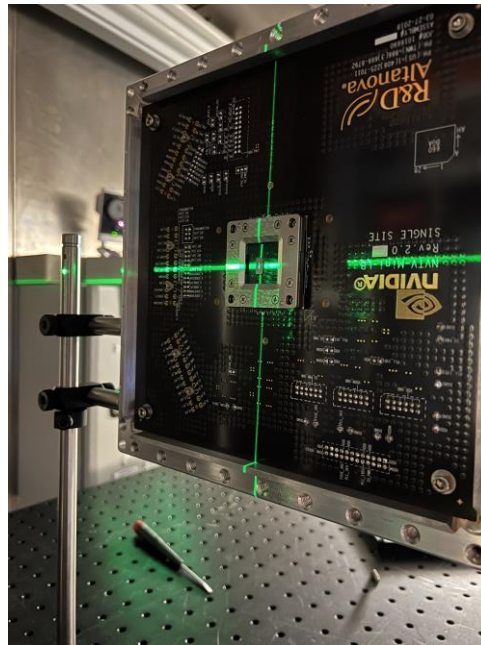
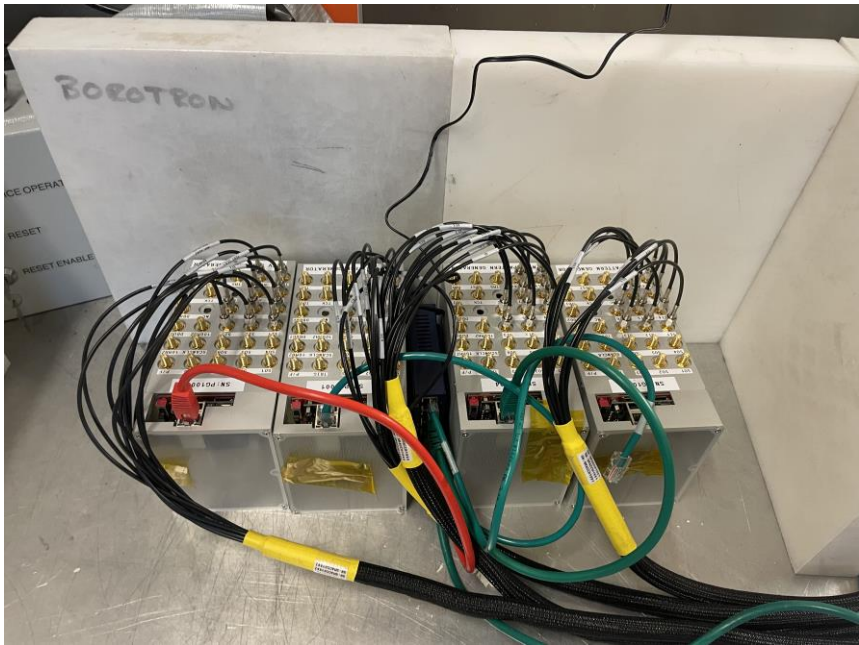
- 1) Load the scan chains with Data Pattern D (scan enable high, clk and SI on for 15K cycles)
- 2) Load the Srams with Data Pattern M (SE=0, free running clk)
- 3) Soak the die for 5 Minutes
- 4) Unload the Mbist failure count data
  - 1) If fails observed, then bitmap and collect all the bit fails – Single bit and Multi bit
- 5) Unload the Scan Chain XOR Counters –
- 6) Repeat Steps 1-5 for
  - 1) D=0000,1111,0101,1010
  - 2) M=WR-0,WR-1,W/R-Checkerboard, W/R-Inverse Checkerboard
- 7) Repeat Step 6 for 600-700 Minutes across multiple Voltages

# EXPERIMENT SETUP





- 4 load boards hooked up with 4 Pattern Generators
- We are able to test 4 die in parallel
- All the Pattern Generators were placed in a Cadmium box along with added shielding to avoid secondary thermal Neutrons
- Other than the DUT, no active components exist in the beam line



# THE MATH

**FIT: Failures In Time (caused by soft errors)** - Unit-of-measure for Soft Error Rate (SER) - 1 FIT == 1 Failure per 1 Billion Hours

$$\text{FITs/Mbit} = (\text{Total \# Events}) \times \left( \frac{1}{\text{Total \# n/cm}^2} \right) \times \left( 13 \text{ n/cm}^2 \times \text{hr} \right) \times \left( 10^9 / \text{Billion} \right) \times \left( 1 / \# \text{Mbit} \right)$$

└──────────────────┘

Total # of measured events\*

└──────────────────┘

Total # neutrons during exposure

└──────────────────┘

n flux at New York City

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per billion hrs conversion

└──────────────────┘

per Mbit conversion

\*# events instead of # bits corrupted- 1 event can cause more than 1 bit to flip

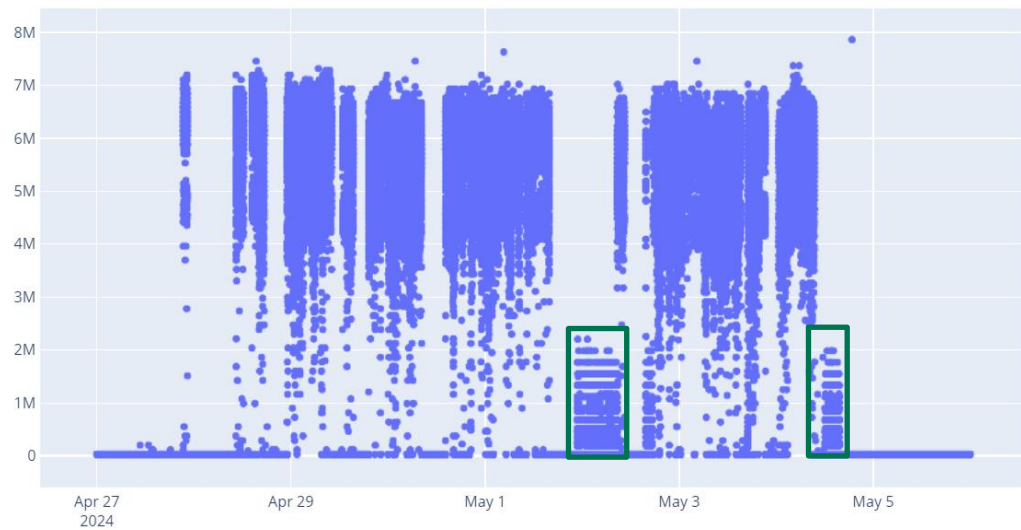
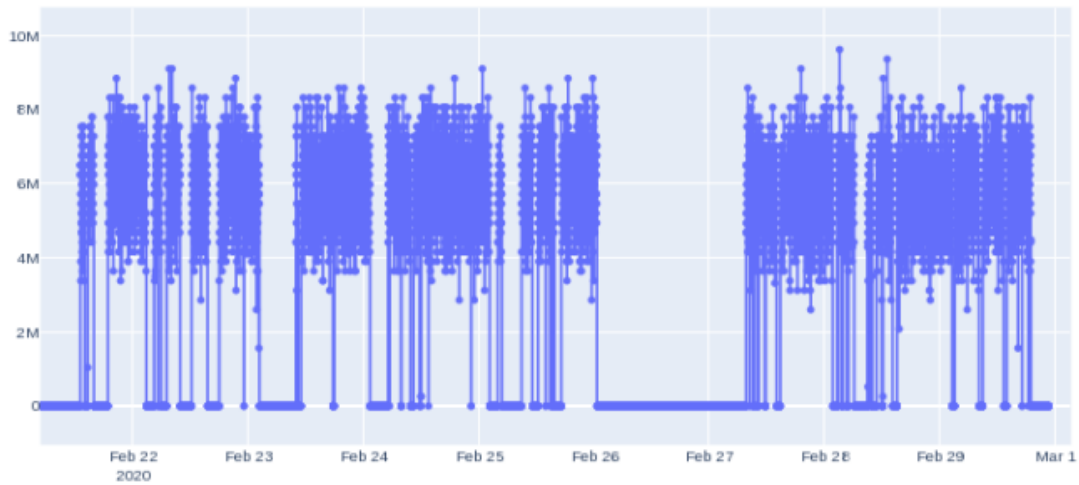
Flux = Delta Fluence/Delta Time (3s at chipIR)

Delta Fluence –

- New Sensor = count \* 2.63e5 (for spectrum > 10MeV) – New Sensor at chipIR since 2022
- New Sensor = count \* 2.63e5 \* 1.84 (for Full spectrum)



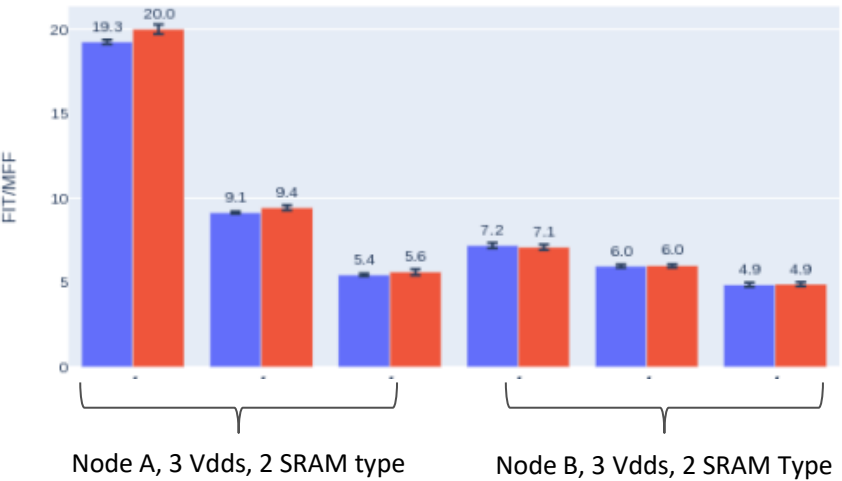
# FLUX LOG AT CHIP-IR 2020 AND 2024



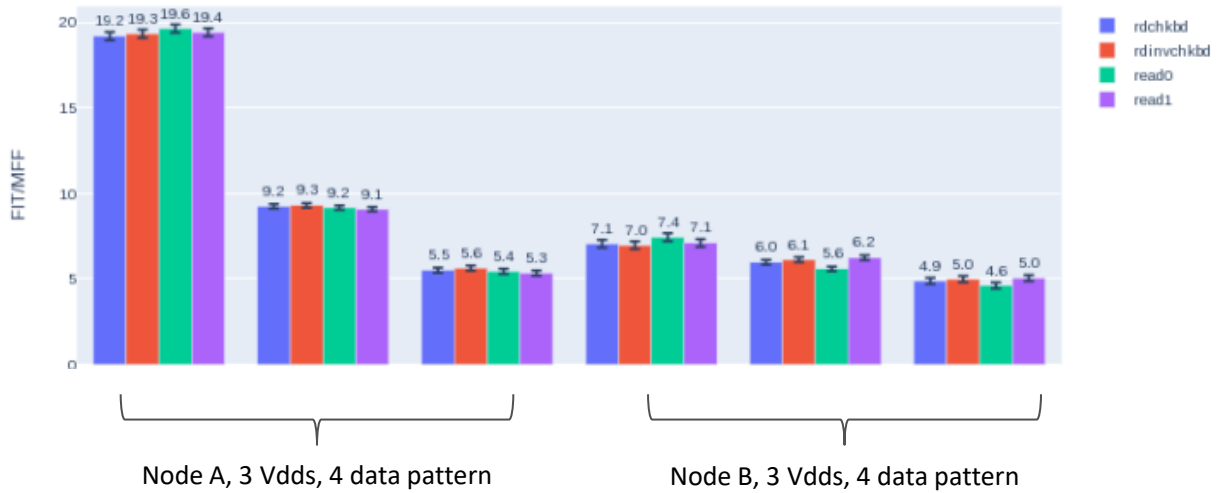
Used the new 10x attenuator in this time window

# FIT RATE DATA - SRAM

Fit across different ramtypes



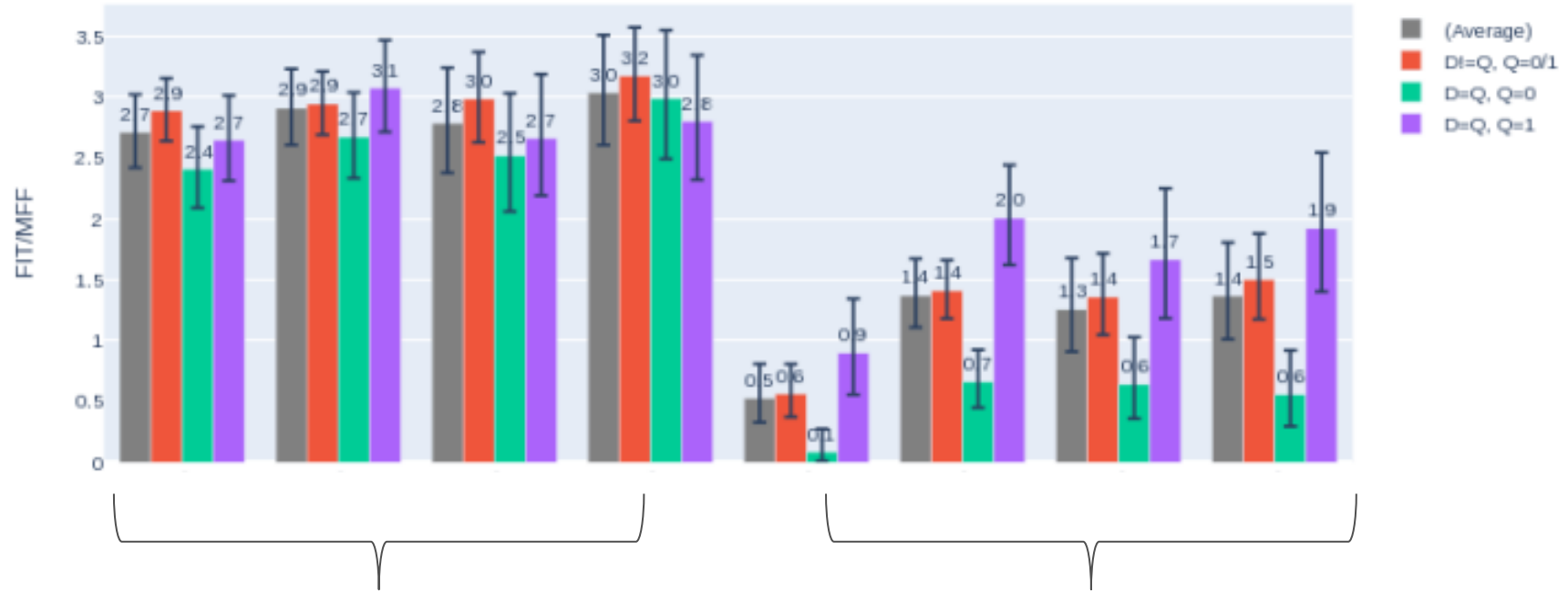
Fit across different data patterns



Fit Rates across voltage and nodes and SRAM type

Fit Rates across voltage and nodes and Data Pattern

# FIT RATE DATA - FLOPS



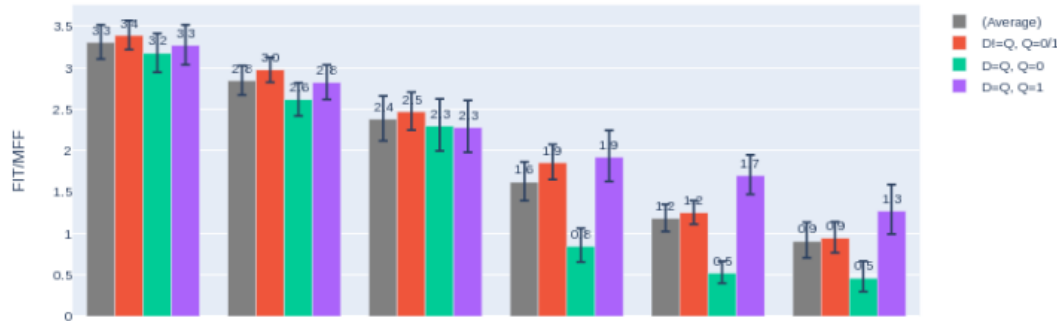
Node A, 4 gate types, 3 Data Pattern

Node B, , 4 gate types, 3 Data Pattern

Fit Rates across Different Gate Types

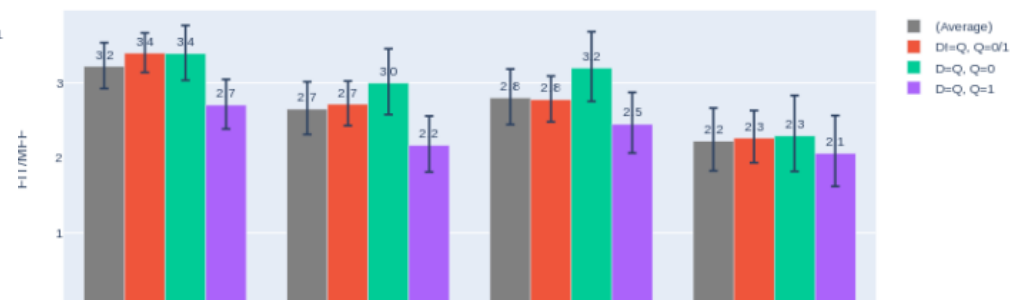
# FIT RATE DATA – FLOPS – MASTER VS SLAVE

Flip-Flop FIT/MFF across all macros at stage = slave



Clk was held low during the 5 minutes soak period

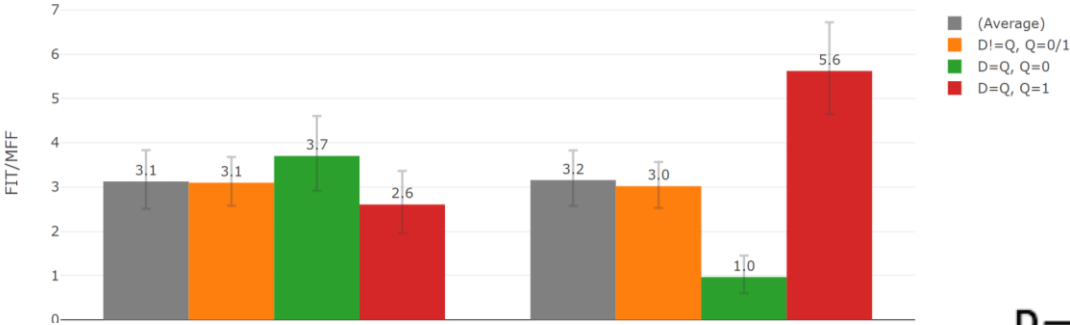
Flip-Flop FIT/MFF across all macros at stage = master



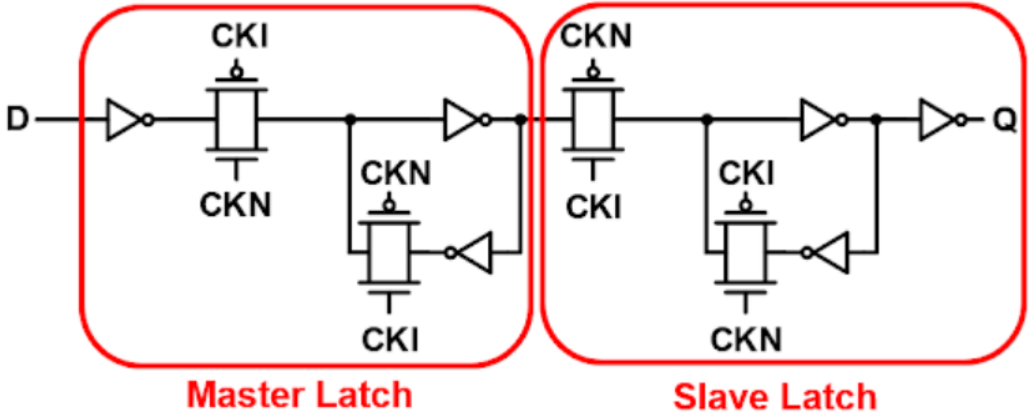
Clk was held high during the 5 minutes soak period

- Over the past 7 years, we have made 3 trip and collected data across 8 different PDVs.
- Results are consistent from trip to trip based on control experiments.
- Results match the expected data very closely
- Beam up time is very high

# FIT RATE DATA FLOPS



Fit rate for NodeA and Node B with different data patterns for flops.



- FIT rate for Node B for pattern 0000 is much lower than the other data pattern
- Root Cause - Node B flop design had a larger feed fwd inverter and a parasitic pmos device on the feedback pulldown path

# ISSUES/ENHANCEMENTS

- With 10X attenuators on
  - Flux reduced by 10x
  - Expected FIT was 10x lower.
  - We see much higher FIT numbers.
- With lower geometries, we need better ways to characterize lower energy spectrum
- Is it possible to selectively choose the desired energy spectrum Neutrons?

# CLOSING REMARKS

- ChipIR provides an excellent infrastructure to evaluate FIT rates for all our advance nodes processes.
- The facility is well equipped with all the tools and equipment needed for a successful trip.
- Beam is very consistent and has a high availability factor.
- Our dedicated PDVs provide with very accurate FIT data across various parameters with extremely low error bars.
- The staff at chipIR (Maria, Carlo and Chris) are phenomenal to work with.

