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Talk 5: Soft Error Rate Test Methodology For Advance Process Nodes Under Neutron Beam At ChipIR

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Abstract:

Soft Error Rate (SER) testing is crucial for evaluating the robustness of advanced process nodes offered by various foundries, particularly those caused by high-energy neutron particles. We derive the Failure In Time (FIT) numbers using a test setup specifically designed to comply with the JEDEC Spec JESD89-3B. This setup is tailored to assess the SER sensitivity of SRAM bit cells (both 6T and 8T, along with various peripheral physical designs) and Flip-Flops using different pattern backgrounds. ChipIR provides an ideal environment for our testing, offering flexible chip placement options and a consistent beam with uniform flux and fluence.
Over the past seven years, we have conducted experiments on eight different test vehicles across three different trips. The results have been consistently reliable, with extremely small error bars. These test vehicles have dedicated hardware built-in to collect SER data, enabling us to determine highly accurate FIT numbers. Additionally, our hardware allows us to pinpoint the physical location of each bit cell failure and differentiate between Single Event Upset (SEU) and Multi Event Upset (MBU) FIT rates.

Presenter: GUPTA (NVIDIA), Puneet

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