Progress with PRs – newly merged

- PR [#796](#) (AV) – MERGED (approved SR)
  - Add fbridgesequence_nomultichannel function, needed by SR in channel array PR
  - Can be merged independently of the channel array PR (and I suggest we do)

- PR [#809](#) (AV) – MERGED (approved OM and SR)
  - Add support for ROCRAND on AMD GPU (as suggested by SR)
  - Implemented via the HIPRAND API (drop-in replacement for CURAND)
    - Implemented: random numbers on GPU device
    - Not yet implemented (WIP in HIPRAND): random number on CPU host, random number ordering

- PR [#813](#) (OM) – MERGED (approved AV)
  - Moved handling of a few files (counters.cc etc) from patchMad.sh to 'proper' plugin
  - AV: this was ok for .MAD but added unnecessary files in .SA, added an ugly hack to fix that
  - OM: implemented a better fix than AV's ugly hack

- PR [#816](#) (OM) – MERGED (approved SR and AV)
  - Fix default runcard for GPU mode

Progress with PRs – almost ready or WIP

- PR #819 (NN, latest SYCL branch) – READY TO MERGE?
  - Latest changes to epochX/sycl (this does not affect the cudacpp directory)

- PR #625 (AV, fixes for SUSY) – ~ALMOST READY (need CODEGEN)
  - SUSY gg_tt ok in C++ (both HRDCOD=0 and =1) and partially ok in CUDA (HRDCOD=0)
    - Various fixes, e.g. fixed visibility of mdl_I51x11 parameter and copied it to GPU constant memory
  - SUSY gg_tt NOT (yet?) OK in CUDA HRDCOD=1 builds
    - constexpr sin/cos/atan functions exist in gcc C++ but not in nvcc – add them from gcc headers?
  - My proposal: add CODEGEN, clean up a bit, merge as is without constexpr trig functions
  - I will then also look at SMEFT again and see if these SUSY fixes also fix SMEFT...

- PR #798 (AV, based on Jorgen's #775) – ~ALMOST READY (must fix new conflicts)
  - Separate build targets for CUDA and C++ (and must now add HIP)
  - This was complete and ready to merge before recent merges
    - Now there are a few ~easy conflicts to fix (HIP, HIPRAND, gXXX.cu all changed makefiles)

- Issue #765 (SR's new_interface_wrap branch, no PR yet) – WIP?
  - From scalar channel ID to array of channel IDs
  - Will use AV's fbridgesequence_multichannel in PR #796
  - Eventually need also Olivier's mg5amcnlo gpucpp_wrap (not yet in gpucpp): complete?

Also missing before the release (non-exhaustive list?)

- Wait for Nathan's Intel GPU support? ([#805](#))
  - Would also need the full manual tests on Intel GPUs (or even better an Intel GPU CI)

- Process-specific issues on AMD GPUs: segfault in gq_ttq ([#806](#))
  - I suggest we release without waiting for this and we fix it later

- Update the separate plugin repo (issue [#661](#)) or recreate it with the full history
  - mg5amcnlo_cudacpp exists with the full history but is stuck to Aug 30
  - As discussed two weeks ago: I will prepare scripts to copy commits to/from madgraph4gpu

- Try to fix EFT before the release?
  - As discussed, SUSY is now in a much better state, the fixes may improve EFTs too

- See also the May 2023 summary (issue [#671](#)): not up to date but still relevant
  - The issues that are still open remain desirable, though not strictly necessary?
  - Many issues mentioned there have been fixed/completed
  - Only a few new issues have appeared (e.g. channel id array)

- Am I missing some very big thing not mentioned above?