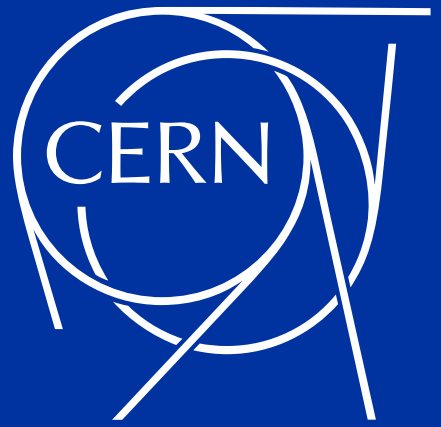

Implications of the BISv2 design for the LBDS

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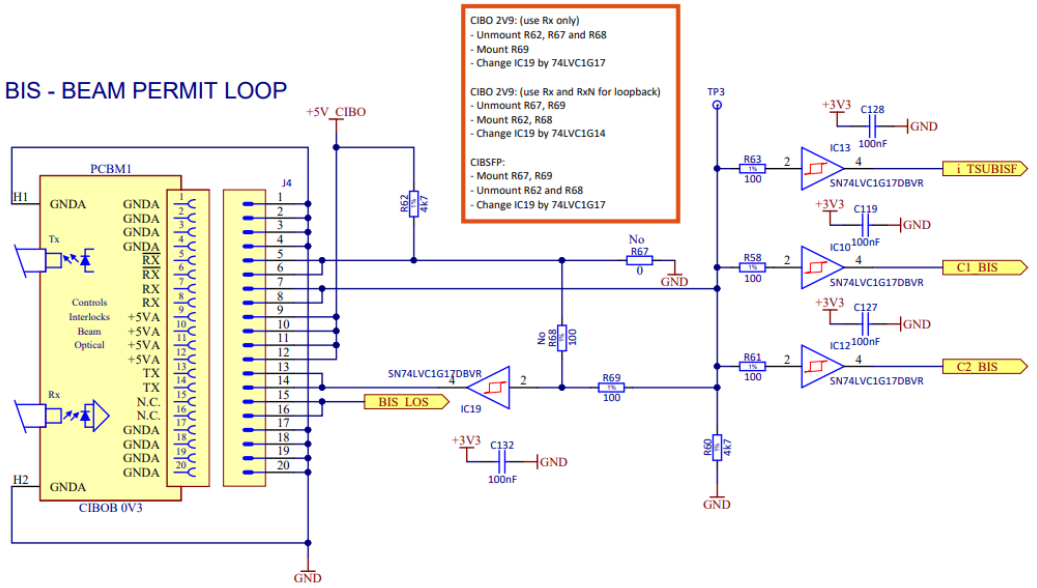
242nd Machine Protection Panel Meeting (LHC), 15th of December 2023

Impacts for SY/ABT

- **BIS V2 renovation impacts two SY/ABT cards**
  - Trigger Synchronization Unit (TSU)
    - TSU is a safety critical element of the LBDS.
    - Used to centralize beam dup requests from BIS, BETS, LBDS Slow Control (SCSS), BLM, Early Dump (SBDS).
    - BIS is the major client of the TSU systems.
    - Synchronizes beam dumps with the beam abort gap using beam revolution frequency (BRF) + delay.
    - BRF is internally regenerated and surveyed in case of loss/fault.
  - Fast Inhibit Board (FIB)
    - Inhibits/gates signals (mostly prepulses) depending on client state.
    - On SPS MKE4 and MKE6 connected to Extraction BIS.
    - On LHC MKI2 and MKI8 connected to Injection BIS.

TSU actual BIS interface

- The actual operational TSU use CIBO cards
  - Interface is compatible with CIBSFP (running on BIS V2 testbench for ~2 years).
  - The BIS signal passes through TSU with feedback to output.
  - Reliable for SY/ABT, but causes issue with TE/MPE as not enough diagnostics on fibres.
- TSU has only RX to FPGA/CPLD and feedback. RXn is not connected to logic, sadly…
- Interface possibly replaceable by CIBIR but:
  - No line status to CPLDs/FPGA (Permit Fault).
  - Might not be safe enough if only BIS state is transmitted.
    - i.e. CLK stop on CIBAB
    - Will trigger dump via second TSU
    - In case the 2 CIBAB fail, retrigger line will trigger an asynchronous dump.
    - **=> reliability study…**

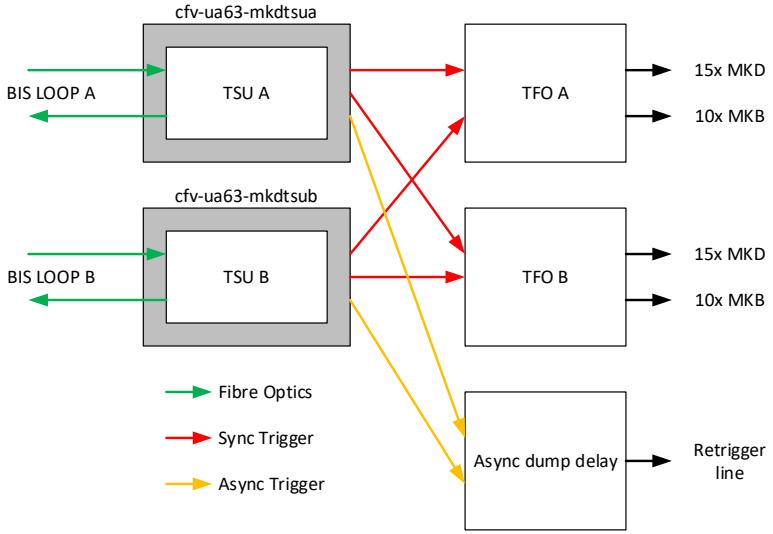


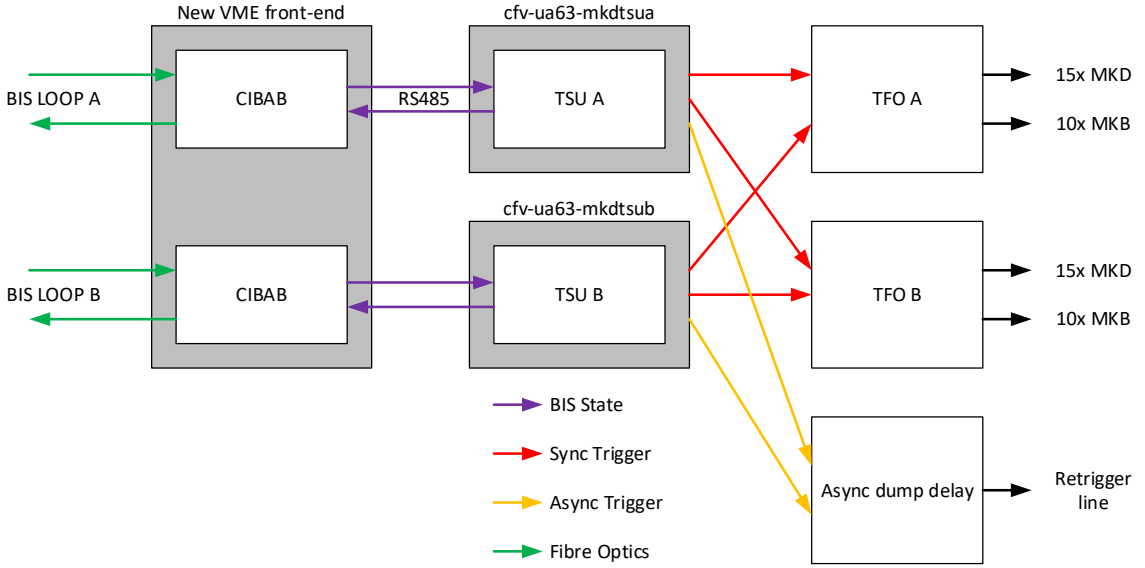
To FPGA

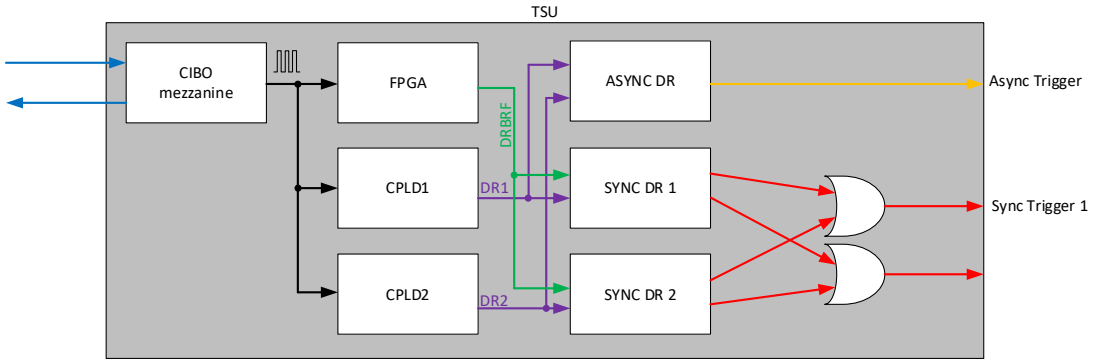
To CLD1

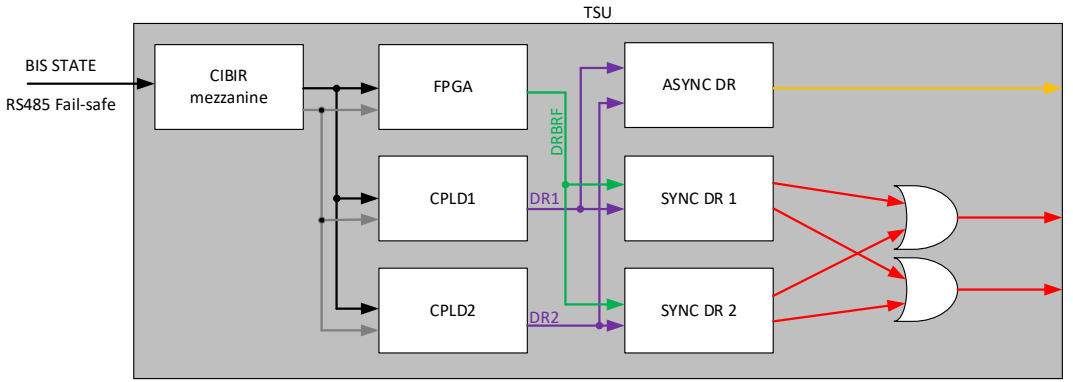
To CLD2

BIS-TSU actual vs Post-LS3







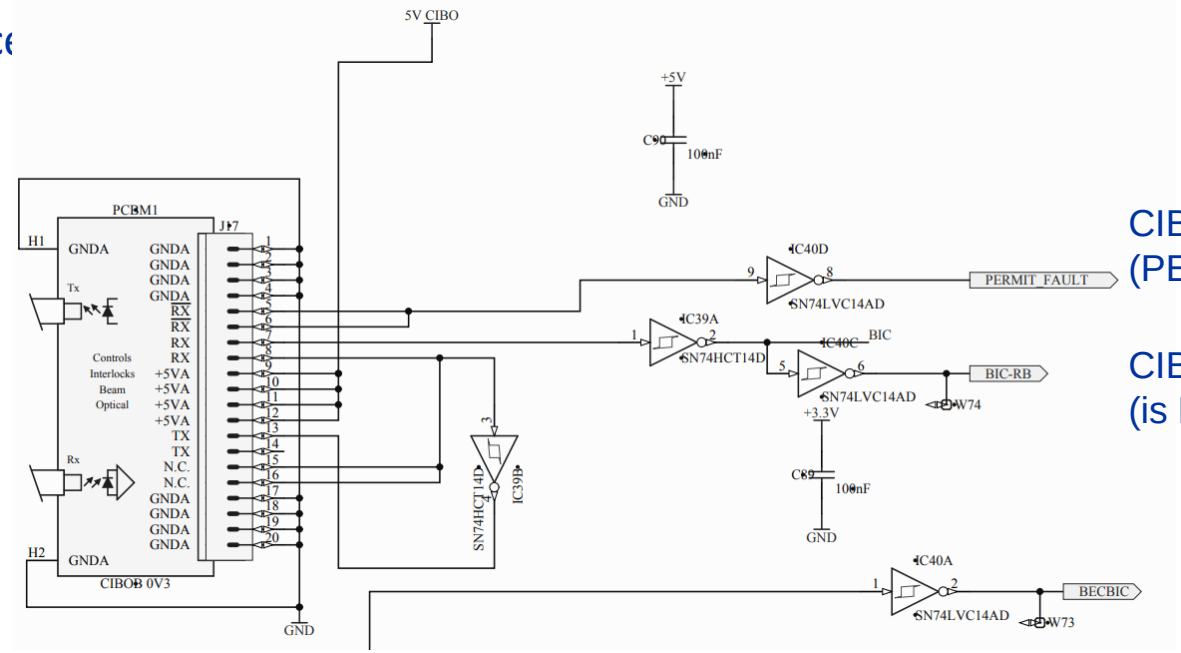


Impacts for TSU

- Change BIS frequency decoding in TSU by CIBAB BIS state (x2). SY/ABT get rid of BIS frequencies check.
- BIS state only cannot indicate on which BIS loop which TSU is connected to (tests?).
- Interface between CIBAB and TSU:
  - Initially questioning the safety of a simple state from CIBAB to TSU (true /false).
  - SY/ABT and TE/MPE agreed on a robust Fail-Safe RS485 bipolar signaling with line status (CIBIR-like).
  - A reliability study must still be performed, ideally by TE/MPE as requester for changes.
- Two scenarios:
  - Renovation of TSU:
    - We can integrate CIBIR circuit or interface onto TSU.
  - No renovation of TSU:
    - Not possible to use CIBIR, because not all signals are routed to FPGA on actual card.
    - Only one signal to FPGA and CLPLDs -> not safe enough with simple state.
    - Find another solution (watchdog frequency, serial bus or other).

Impacts for FIB

- FIB cards can be connected to BIS.
  - One FIB per BIS loop.
  - Uses CIBO cards to interface to BIS.
- FIB cards are compatible already with CIBIR interfaces. Check Permit Fault signal in CIBIR mode already implemented.
- If we implement CIBIR interfac

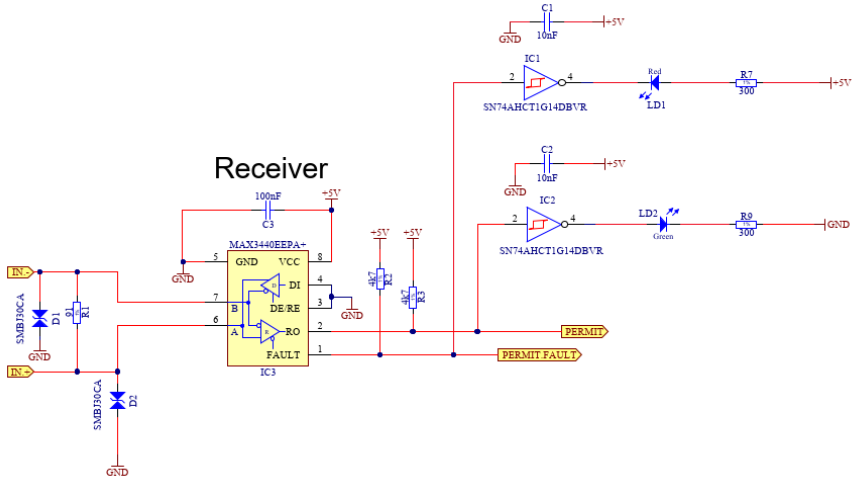


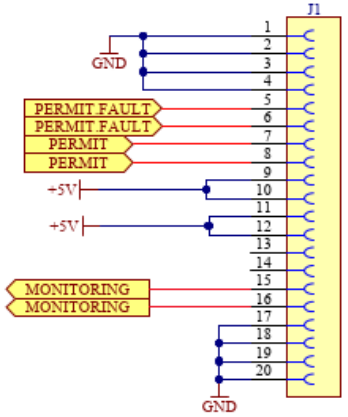
CIBO RXn to FPGA
(PERMIT on CIBIR)

CIBO RX to FPGA
(is PERMIT_FAULT on CIBIR)

Advantages of CIBIR-like interface

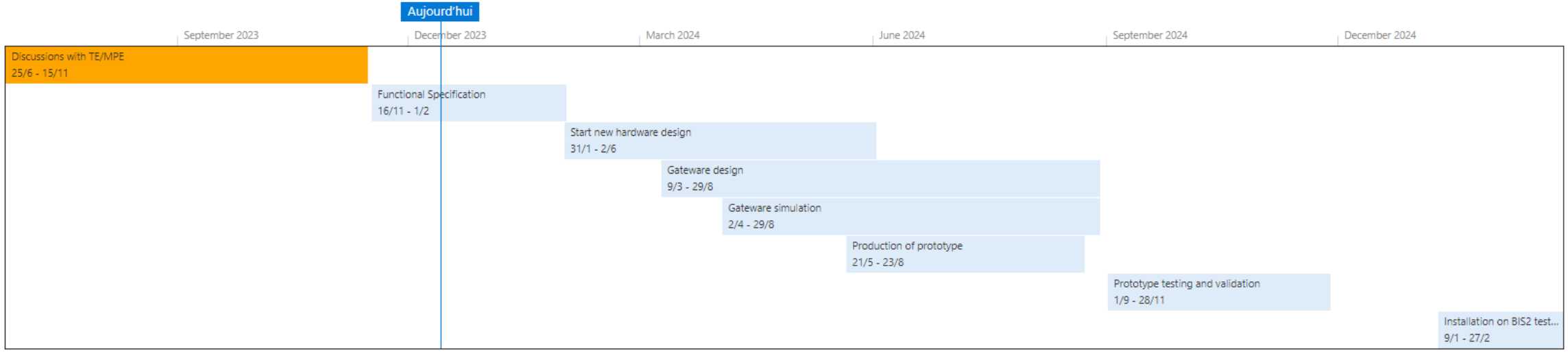
- Use of MAX3440 Fail-Safe RS-485 transceivers.
- Status of the transmission line
  - Gives indication of cable presence and signals quality, TSU can interlock on hardware issue.
- CIBIR receiver to transmitter as feedback status for CIBAB.
  - CIBAB can check that signal is correctly transmitted to TSU. Interlock?
- CIBIR circuit can be directly added to TSU.
- Or we can keep flexibility by keeping mezzanine-like interface.
  - Interface must be compatible with : CIBO, CIBIR, CIBSFP

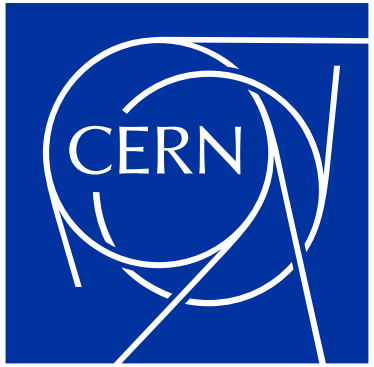




Timeline

- Prototype of new TSU system to be started ASAP and ready by end of 2024.
- First tests CIBAB – TSU by Q3 2024.
- BIS V2 hardware and testbench to be ready by Q4 2024.
- Installation on BIS V2 testbench (UA63) planned for YETS 24-25.
- Validation on BIS V2 testbench during RUN4.
- Deployment of new HW and GW during LS3.





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References

TSU main board:

- https://edms.cern.ch/item/EDA-02715-V3-1/0

TSU Mezzanine card:

- https://edms.cern.ch/item/EDA-02716-V3-0/0

TSU Interface:

- https://edms.cern.ch/item/EDA-02713-V3-0/0

TSU Backplane:

- https://edms.cern.ch/item/EDA-02714-V1-0/0

FIB card:

- Fast Inhibit B (FI/B) schematics AED-00086-V6 | Document 1385128 (v.6) (cern.ch)