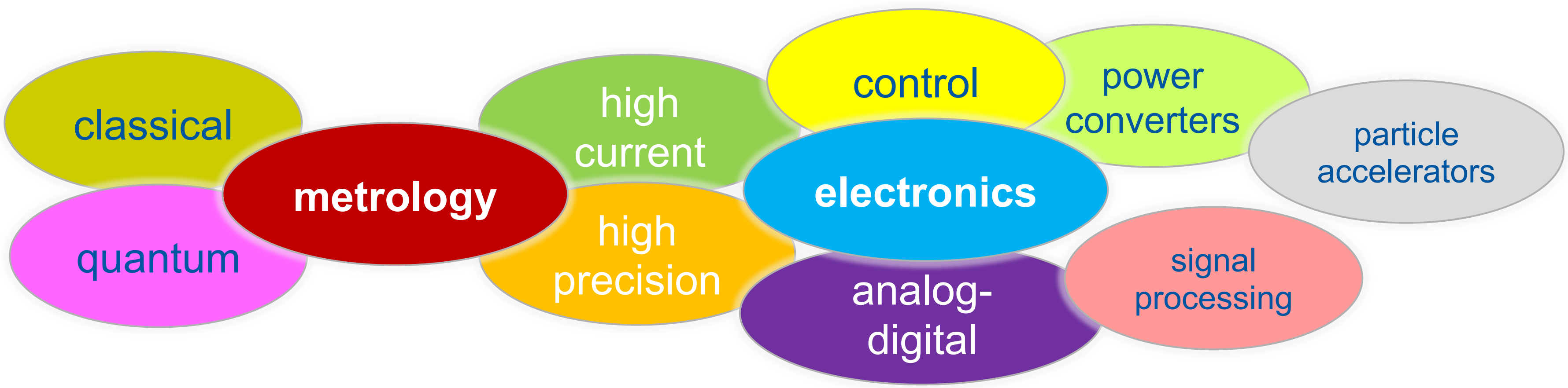
# Metrology and digitization for the highest accuracy class power converters in High Luminosity LHC

**High Performance Digitizer and DC Metrology Seminar**
Slovak University of Technology, Bratislava, Slovakia

# Overview

- PART I
  - Introduction
  - Development of high-performance digitizers at CERN
- PART II
  - HL-LHC Accuracy Class 0. HPM7177
  - Proving digitizer performance



# About me

**Education**

2004-2008 BSc – Technical University of Sofia

2008-2010 MSc – Tampere University of Technology

2023- PhD – Slovak University of Technology

**Employment**

2009-2011 Tampere University of Technology, Finland

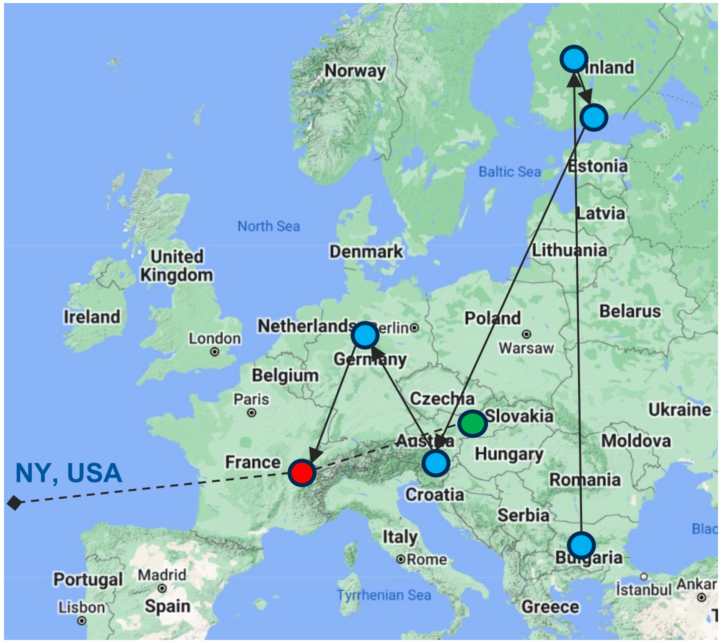
2011-2014 VTT – Espoo, Finland

2014-2015 CISC Semiconductor – Klagenfurt, Austria

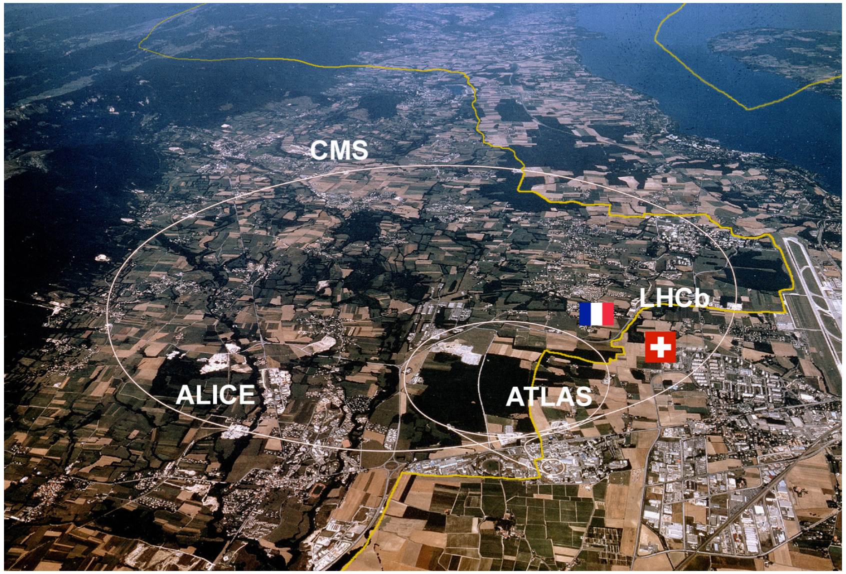
2015-2016 PTB – Braunschweig, Germany

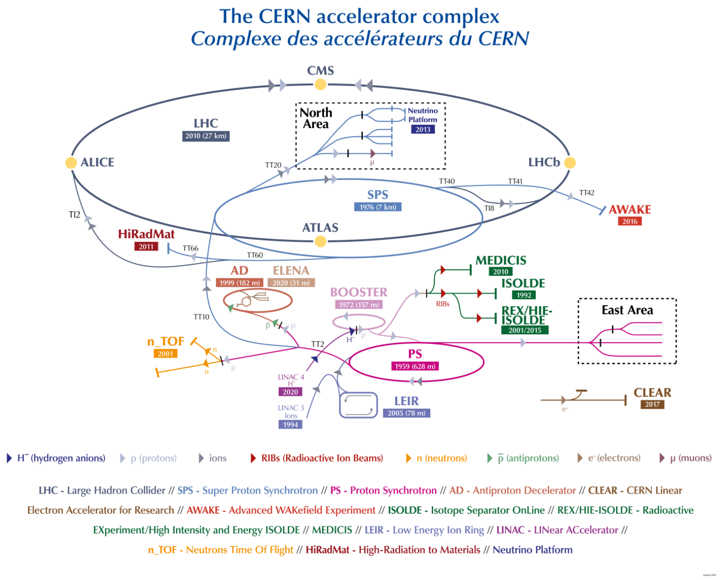
2017- CERN – Geneva, Switzerland

2018- AIP Publishing – Melville, NY, USA



# Introduction to CERN




- 23 Member states
- 10 Associate member states
- 4 Observers
- Many co-operation agreements

# EPC group, HPM section

## EPC group mandate

**Design, development, procurement, construction, installation, operation and maintenance of electrical power systems for all accelerators, transfer lines, experimental areas and tests facilities at CERN**

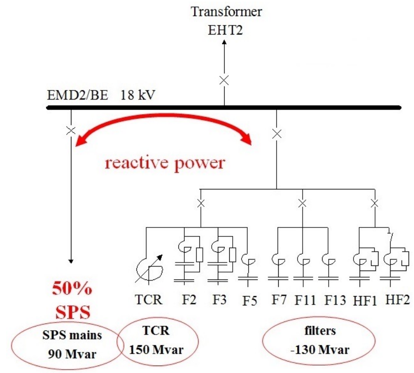
## Sections

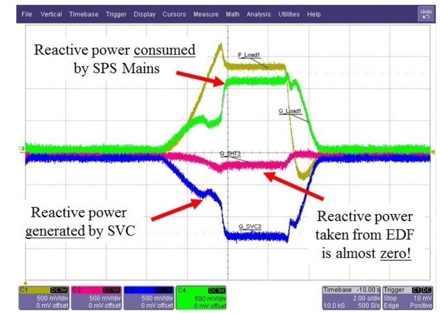
- Converter Controls Electronics (CCE)
- Converter Controls Software (CCS)
- Fast Pulsed Converters (FPC)
- High Power Converters (HPC)
- Medium Power Converters (MPC)
- Low Power Converters (LPC)
- Operation and Maintenance Support (OMS)
- **High Precision Measurements (HPM)**

## HPM section mandate

- Maintain/support operation of all DCCTs in the LHC and injector chain
- Maintain/support operation of all ADCs of the FGC control platform
- Provide high precision current measurement and digitizing solutions for ongoing and future projects
- Provide high voltage measurement solutions for ongoing and future projects
- Provide a consultancy service for the group on measurement and control & regulation issues
- Provide a calibration service for high-precision equipment in the group
- Operate and improve the DCCT and Standards Laboratory
- Follow the state of the art in high-precision measurements

# Some examples of EPC equipment


Static VAR Compensator (SVC) – at LHC P2, P4, P6, P8

**RPTE** – LHC main dipoles
13 kA / 190 V, 2-quadrant

**RPMB**
600 A / 10 V
4-quadrant

**RPLA** 60 A / 8 V, 4-quadrant

# Some examples of HPM equipment

DCCT chassis

5x PBC rack

Current calibrator (CDC)

HL-LHC Class 0 DCCT test rack

Mobile current calibrator in the LHC tunnel

20 kA DCCT test bed

# Some terms and definitions

- **ADC** – Analog-to-Digital Converter - integrated circuit or discrete realization
- **Digitizer** – a complete system that contains an ADC plus supporting circuits and sub-systems
- **DCCT** – Direct Current Current Transformer – magnetically-coupled current transducer based on zero flux detection
  - DCCT head – magnetics + windings + shielding
  - DCCT chassis – electronic system (modulator, detector, power amplifier, controller, etc.)
  - Burden – precision resistor that converts the secondary DCCT current to voltage
- **FGC** – Function Generator Controller – a digital control platform used for power converters at CERN
- **Reference**
  - Reference signal in the digital control loop
  - Voltage reference (integrated circuit)
  - Reference device or instrument (DCCT, voltage standard, current standard, etc.)
- **Circuit** – magnet + power converter *(accelerator jargon)*
- **ppm** – part per million

# How much (or how little) is 1 ppm?

- 1% of 1% of 1%, or 1‰ of 1‰ => $^{o}/_{ooooo}$

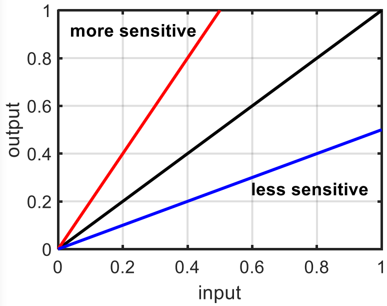
- **10 µV of 10 V** — 10 V - typical voltage standard
- **13 mA of 13 kA** — 13 kA - LHC main dipole magnet current

- **10 cm of 100 km** — a golf hole 100 km from here (e.g. near Brno)
- **150 km of 1 AU** — from here to Budapest / from here to the Sun

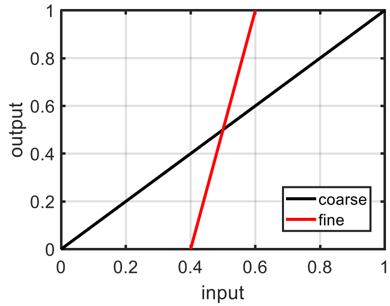
- **120 dB** — the *total* dynamic range of human vision and hearing *(with adaptation)*
- **$M_L$ 3 / $M_L$ 7** — barely felt / *very* destructive earthquake (1 ton / 1 Mton TNT)

# The need for high dynamic range

- Some natural or artificial signals have intrinsically high **dynamic range.** For example:
  - magnetic fields in the Solar system: from $5\times10^{-11}$ T (interplanetary space) to $1.4\times10^{-3}$ T (near Jupiter)
  - ionization chamber-based beam loss monitors: $I_{out}$ from $10^{-10}$ A to $10^{-3}$ A
- Workarounds are often used to match such signals to measurement systems

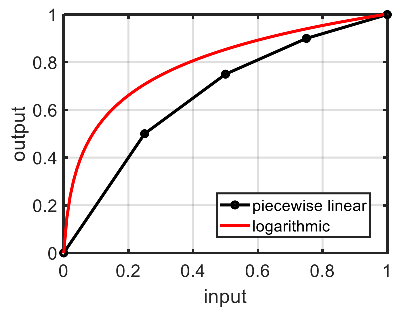



Multiple ranges

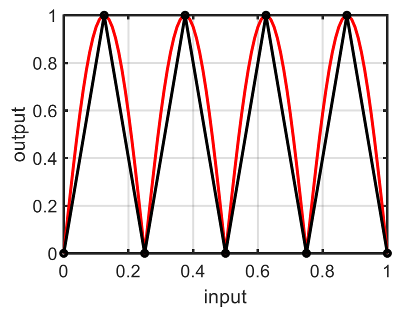



Sub-ranging, compensation

**Linear**



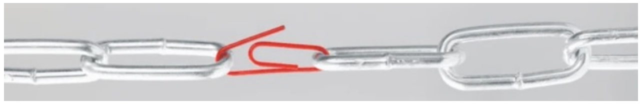

monotonic



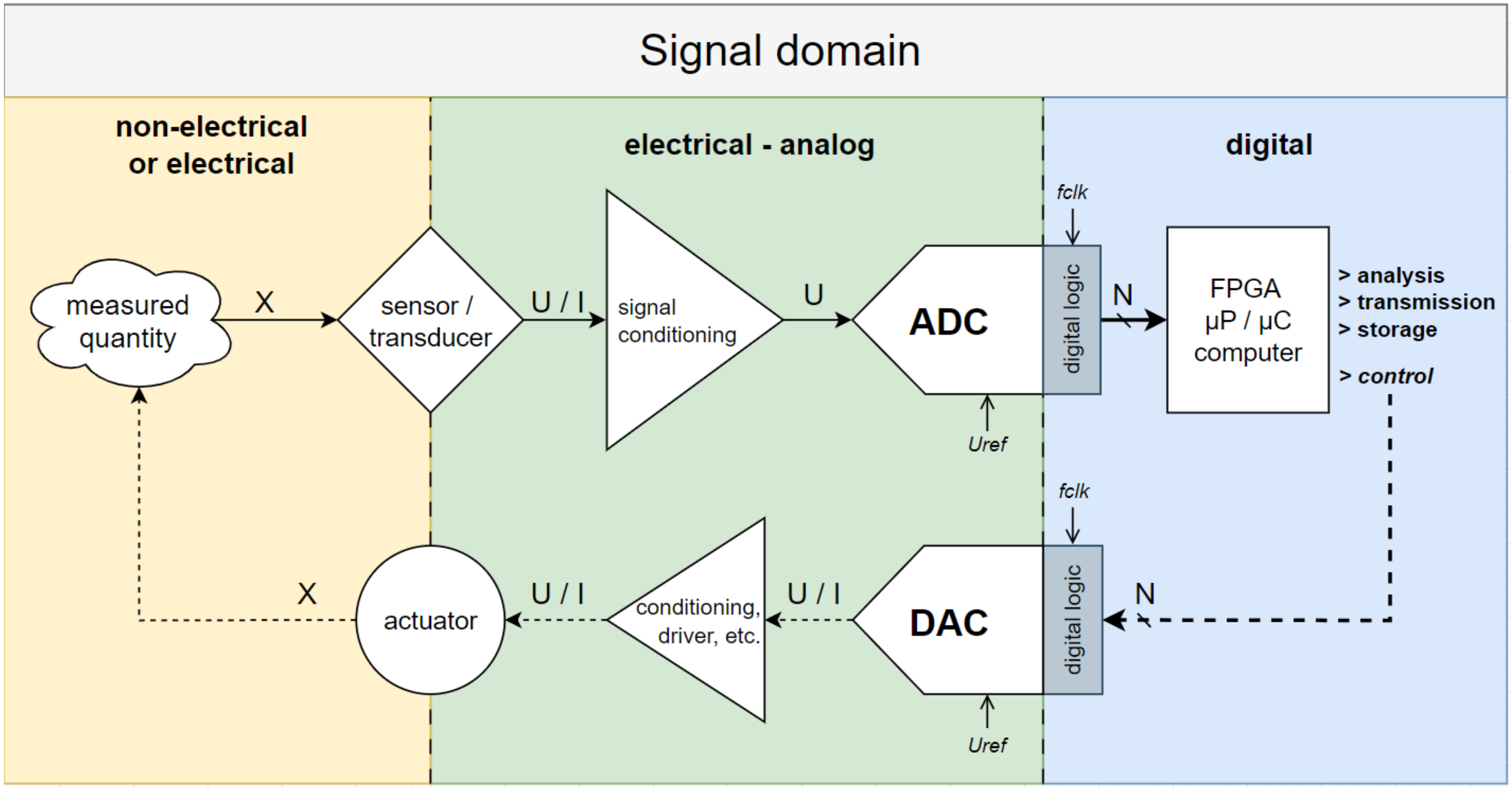

non-monotonic (folding)

**Non-linear**

- In some cases, these techniques are not practical, e.g. in high-precision control applications
- Therefore, a highly linear **signal chain** having high dynamic range is needed



# Signal chain for high precision control




**Limitations:**

- Physics
- Sensor technology

**Analog signal processing**

- Many limitations (physical, technical)
- Sensitive to disturbances
- Needs calibration
- “Expensive” in terms of system resources

**Digital signal processing**

- Scalable, flexible, reliable, stable
- Immune to disturbances
- “Cheap” in terms of system resources
- Needs interface to the outside “real world”

# The cost of analog performance

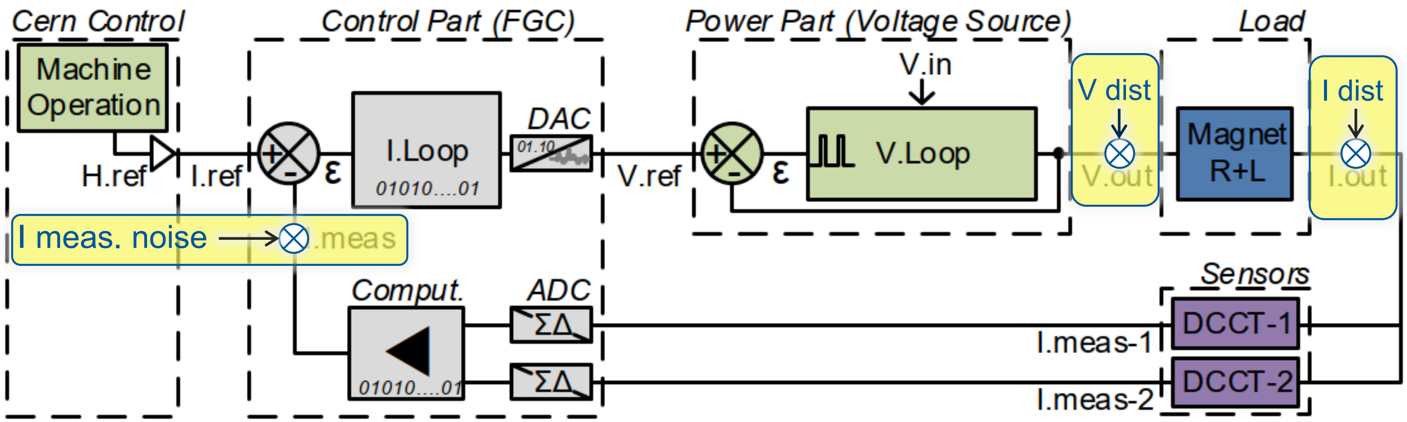
- Technical and physical limitations:
  - Supply voltages
  - Noise

    } *dynamic range* (Supply voltages, Noise)
  - Bandwidth, slew rate, settling
  - Causality: only real-time signal processing
- Non-ideality of components
  - non-linearity, temperature dependence, limited voltage/current/power ranges, aging, hysteresis/memory effects, excess noise, parasitics, …
- High impact of component and material obsolescence
- Niche, specialized, shrinking segment of electronics → limited expertise and tools

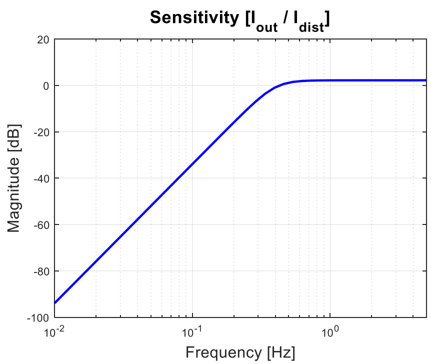
*"Traditional analog signal processing carries with it a certain hopelessness with respect to noise. As analog processing complexity grows, additive noise sources grow in number, and system performance fades away."*

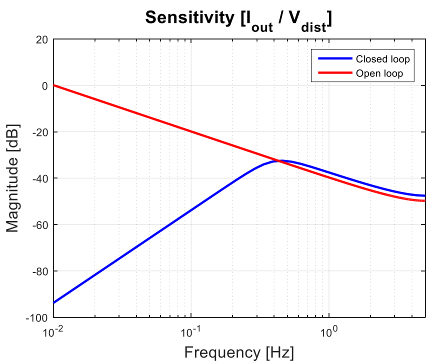
Eric Swanson [1]

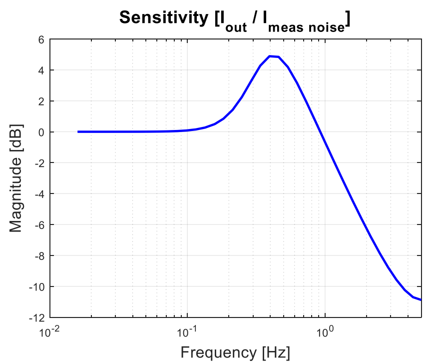
# High precision magnet powering




Example : circuit RPTE.UA83.RB.A78 – LHC 13 kA




**Disturbance in magnet current**
- High suppression << 1Hz
- No suppression > 1 Hz

**Voltage disturbance (PC)**
- High suppression << 1Hz
- LPF action of magnet > 0.5 Hz

**Noise in current measurement**
- No suppression < 0.1 Hz
- **Amplification** of noise 0.1 – 1 Hz
- Suppression > 1 Hz

# Metrology lab vs accelerator tunnel

## Metrology laboratory

A. good EM environment
B. stable environmental conditions (T, RH)
C. easy access → frequent calibrations possible
D. ample time to measure


“Copper room”, Kopfermann-Bau, PTB-Braunschweig

## LHC tunnel

A. not the best EM environment *(noisy neighbours)*
B. temperature variations due to machine operation, some seasonal variation of humidity
C. difficult access → limited calibration capabilities
D. precision measurements needed for real-time control → low and *constant* latency needed

Service area near one of the LHC access points, CERN

# Unique challenges

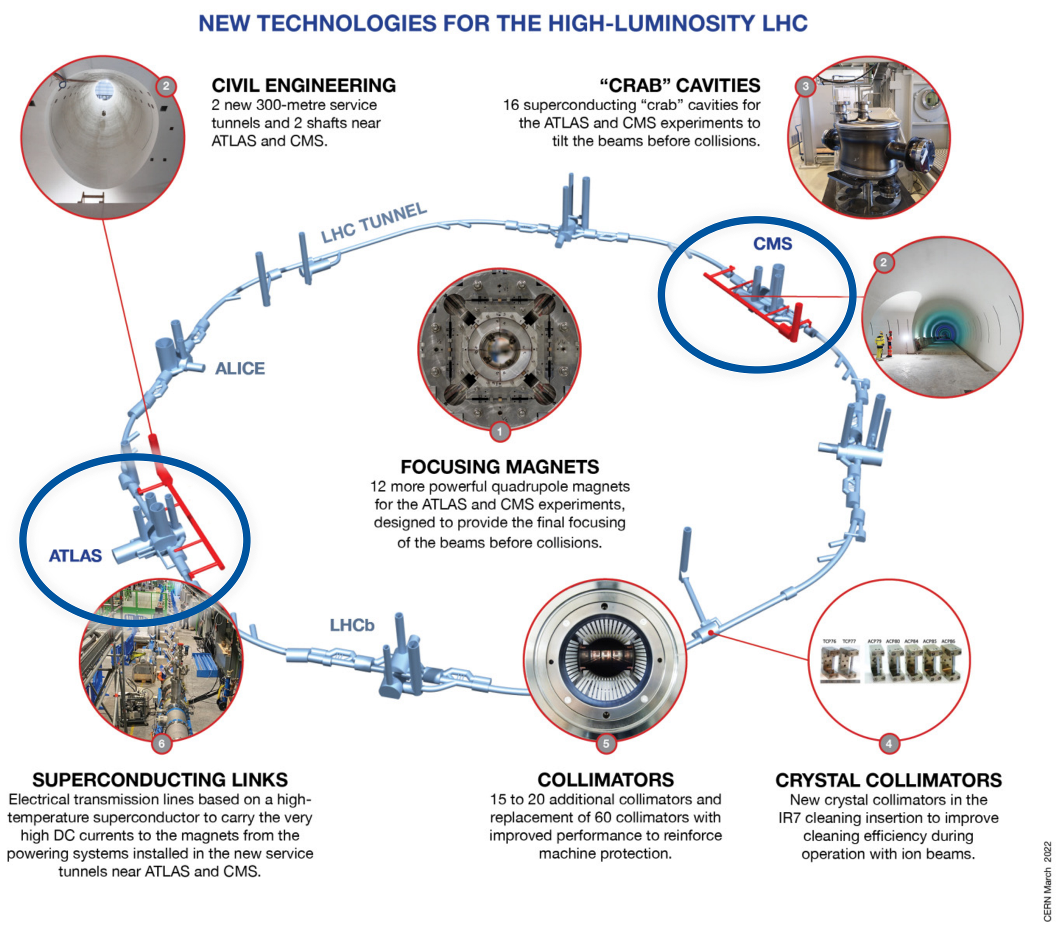
- **Environment**
  - Underground tunnel → limited space
  - Impact of surrounding equipment (EMC, thermal)
  - Some (*lower-precision*) measurement devices are close to the beamline → exposure to ionizing radiation
- **Reliability**
  - Many of the circuits are critical for machine operation. A single non-operational device could stop the entire LHC operation
  - Power converters and magnets are protected against disturbances, but there could still be negative impact (least of all a beam dump)
- **Maintainability**
  - Difficult access (time, effort, cost, operational constraints)
  - Large number of devices spread over a considerable area
  - Independent operation and tracking: common reference setpoint (digital) sent by CERN Control Center, but each measurement device relies on its own local electrical voltage reference

# Solutions

maintainability and reliability environment

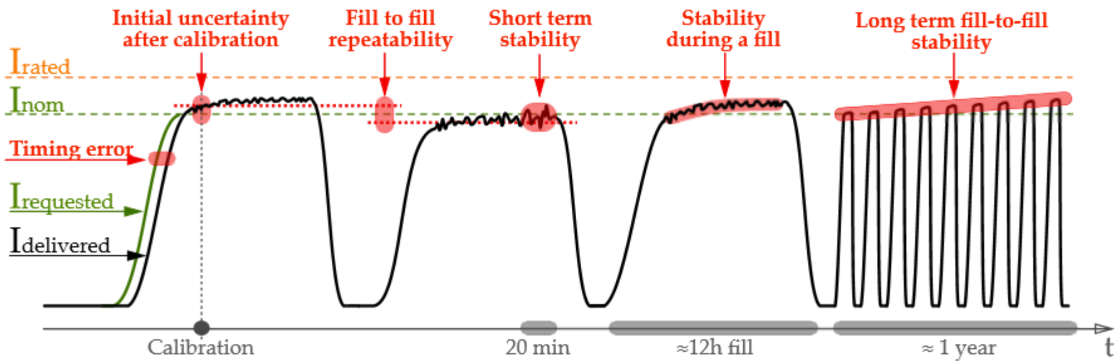
- **Improvement of the local environment**
  - Temperature-controlled racks for the highest accuracy systems
  - Uninterruptible power supply (UPS) – in case of power cuts and network disturbances
- **EMC robustness**
  - Shielding (system, rack, module, sub-module levels), differential transmission of analog signals, optical fiber for digital interface, etc.
- **Redundancy**
  - Inspired by nature
  - Some performance improvement when both channels operate ($\sqrt{2}$ lower noise)
  - *“First rule in government spending: Why build one, when you can have two at twice the price?”* Carl Sagan, Contact (1985)
- **Remote diagnostic and calibration tools**
  - For identifying faults, possible performance degradation, or post-mortem analysis
  - Fixed and mobile infrastructure for in-situ calibration; self-calibration in some devices
- **Field support and management of spare units**
  - “Hot” spares in the tunnel – already calibrated and thermally settled, ready for quick replacement
  - In the lab (above ground) – device support for >20 years. Mitigation of obsolescence (hardware, software, knowledge)

# High Luminosity LHC




- Major upgrade of the LHC [3]
- Target: ~10 times higher luminosity for ATLAS and CMS
- Installation and commissioning in 2026-2028
- Planned to run from 2029 till 2041
- New $Nb_3Sn$ Inner Triplet magnets *(focusing at interaction points)* for ATLAS (P1) and CMS (P5)
- New power converters + need for high**er** precision measurements

# HL-LHC Requirements




| Circuit Name | Irated [A] | PC class |
|---|---|---|
| RB | 13000 | 1 |
| RQ(D/F) | 13000 | 1 |
| RQX | 18000 | 0 |
| RTQX1 | 2000 | 2 |
| RTQXA1 | 120 | 4 |
| RTQX3 | 2000 | 2 |
| RCBX | 2000 | 2 |
| RQSX | 200 | 3 |
| RC(S/0)X | 120 | 4 |
| RC(D/T)X | 120 | 4 |
| RD(1/2) | 13000 | 0 |
| RCBRD | 600 | 3 |
| RQ(4/5) | 6000 | 2 |
| RCBY | 120 | 4 |
| RQ6 | 6000 | 2 |
| RCBC | 120 | 4 |
| RTB8 | 300 | 3 |

New inner triplets

New separation/ recombination dipoles

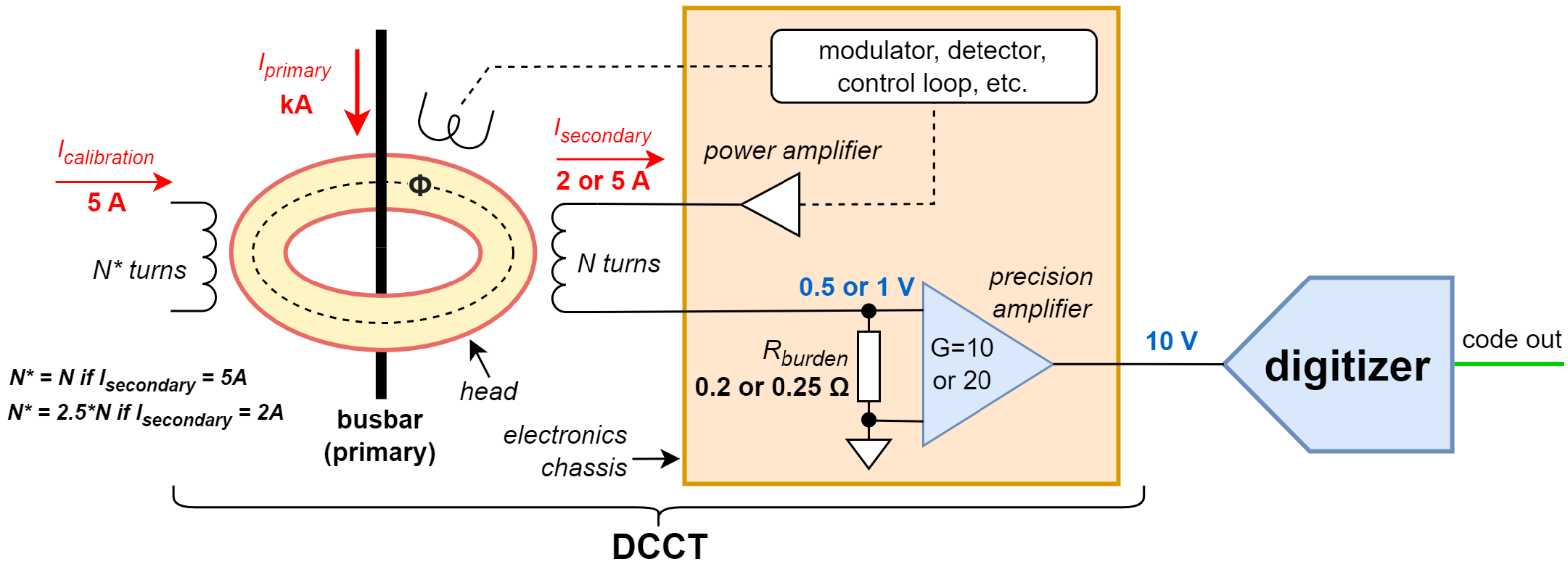
| | PC REQUIREMENTS SUMMARY - ACCURACY CLASSES | | | | |
|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 |
| Resolution [ppm] | 0.5 | 0.5 | 1.0 | 1.0 | 1.0 |
| Initial uncertainty after cal [2xrms ppm] normal | 2.0 | 2.0 | 3.0 | 7.0 | 10.0 |
| Linearity [ppm] [max abs ppm] uniform | 2.0 | 2.0 | 5.0 | 8.0 | 9.0 |
| Stability during a fill (12h) [max abs ppm] uniform | 0.7 | 1.9 | 5.0 | 8.0 | 9.5 |
| Short term stability (20min) [2xrms ppm] normal | 0.2 | 0.4 | 1.2 | 2.0 | 5.0 |
| Noise (<500Hz) [2xrms ppm] normal | 3.0 | 5.0 | 7.0 | 15.0 | 19.0 |
| Fill to fill repeatability [2xrms ppm] normal | 0.4 | 0.8 | 2.6 | 4.0 | 5.0 |
| Long term fill to fill stability [max abs ppm] uniform | 8.0 | 8.0 | 19.0 | 40.0 | 45.0 |
| Temperature coefficient [max abs ppm/C] uniform | 1.0 | 1.2 | 2.5 | 5.5 | 6.5 |
| 12h Delta T for HL-LHC [max C] constant | 0.5 | 1.0 | 5.0 | 5.0 | 5.0 |
| 1 y Delta T for HL-LHC [max C] constant | 0.5 | 1.0 | 5.0 | 5.0 | 5.0 |

isothermal

TC, ΔT

New highest PC accuracy class

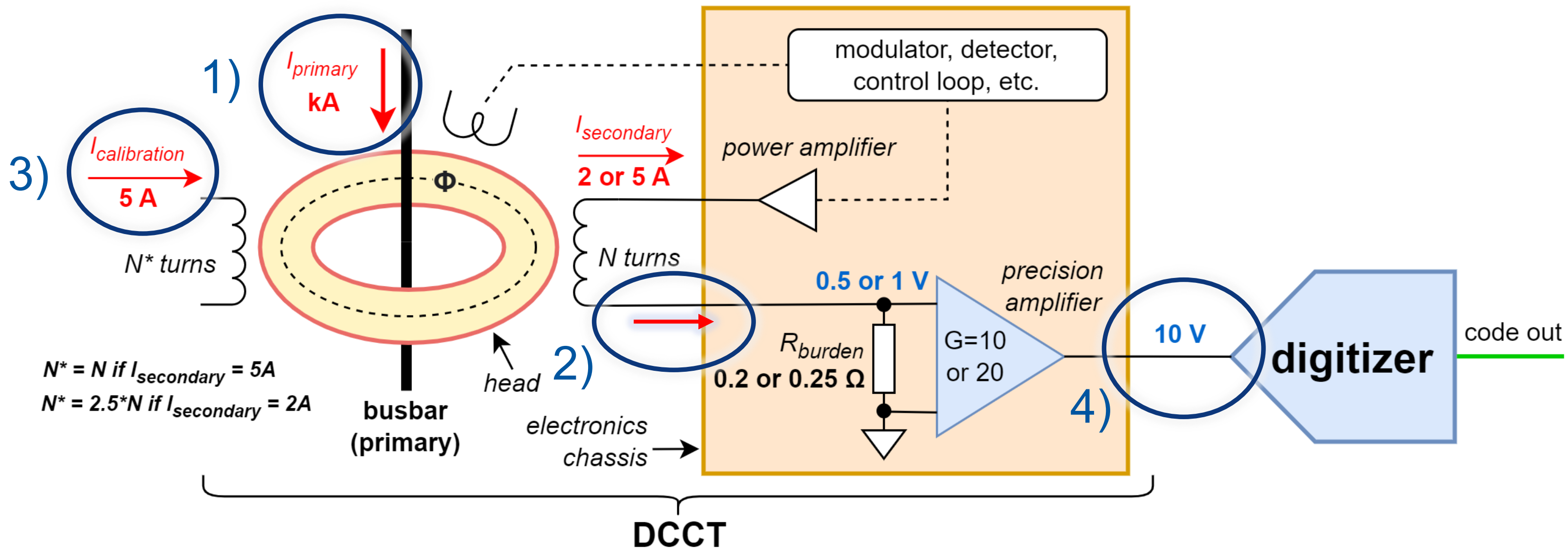
# The complete measurement chain




| Accuracy class | Circuits * | $I_{primary}$ (kA) | $I_{secondary}$ (A) | N turns | $R_{burden}$ (Ω) |
|---|---|---|---|---|---|
| LHC Class 1 | main dipoles, main quadrupoles | 13 | 5 | 2600 | 0.2 |
| LHC Class 1 & 2 | inner triplets, insertion quads, separation/recombination dipoles | 4 / 5 / 6 / 7 | 2 | 2000 / 2500 / 3000 / 3500 | 0.25 |
| HL-LHC Class 0 | separation/recombination dipoles | 14 | 5 | 2800 | 0.2 |
| HL-LHC Class 0 | inner triplet quadrupoles | 18 | 5 | 3600 | 0.2 |

* all listed circuits are unipolar

# Measurement chain calibration




1) **Primary current** – fixed testbed; for testing, not calibration
2) **Secondary current** – test of $R_{burden}$ + precision amplifier (excluding DCCT head)
3) **Calibration winding** – 5 A from the CERN DCCT Current Calibrator: simulation of primary current, calibration of the entire DCCT
4) **Digitizer** – voltage calibration – 3 points (-10 V, 0 V, +10 V), using a 10 V standard

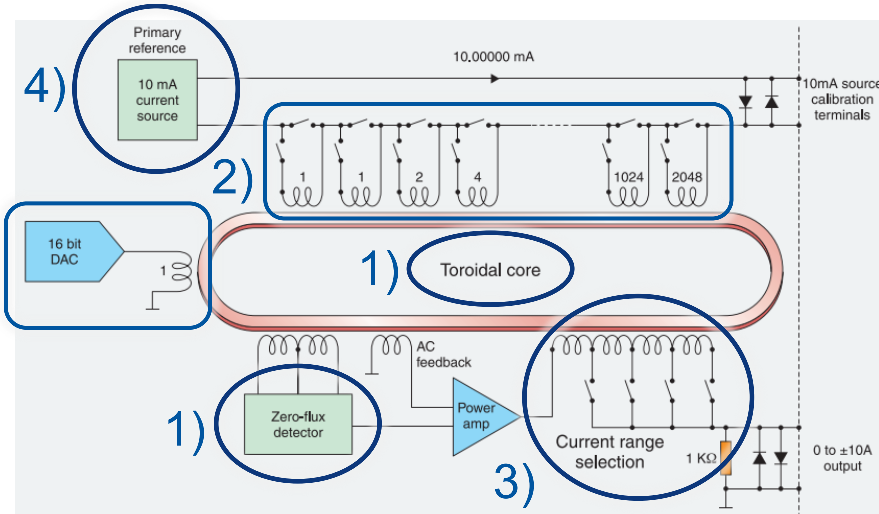
- Calibration is digital. Values are stored centrally in a database

# The CERN current calibrator

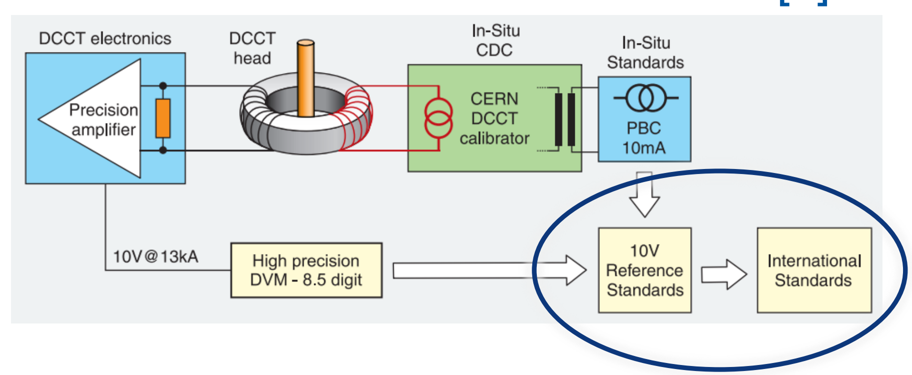
1) Principle: Zero Flux Detector, "inverse DCCT"
2) Resolution: >24 bits
   - coarse: binary-encoded windings (12 b)
   - fine: one-turn DAC (16 b)
3) Ranges: ±1 A, ±2.5 A, ±5 A, ±10 A
4) Current reference: 10 mA from PBC

- Part of the fixed calibration infrastructure for LHC, but also mobile
- Used for traceable DCCT calibration

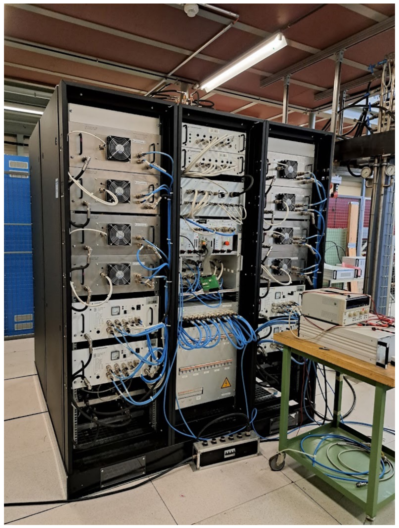
- Improved variant for HL-LHC Class 0 DCCT testing
  - hardware and controls upgrade
  - 50 mA reference (5x new PBCs) instead of 10 mA, for lower noise and higher stability *(submitted to CPEM-2024)*



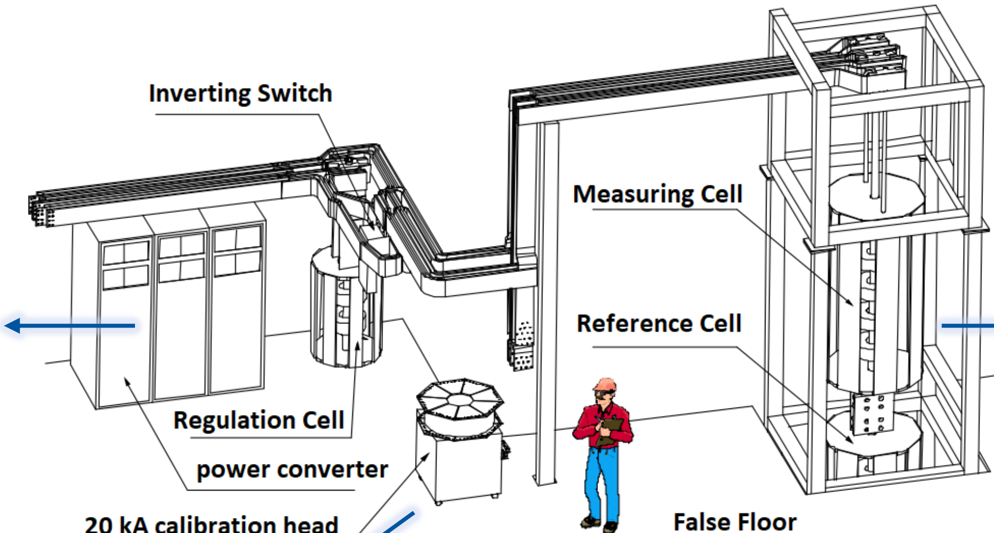

From [4]



# The upgraded 20 kA DCCT testbed



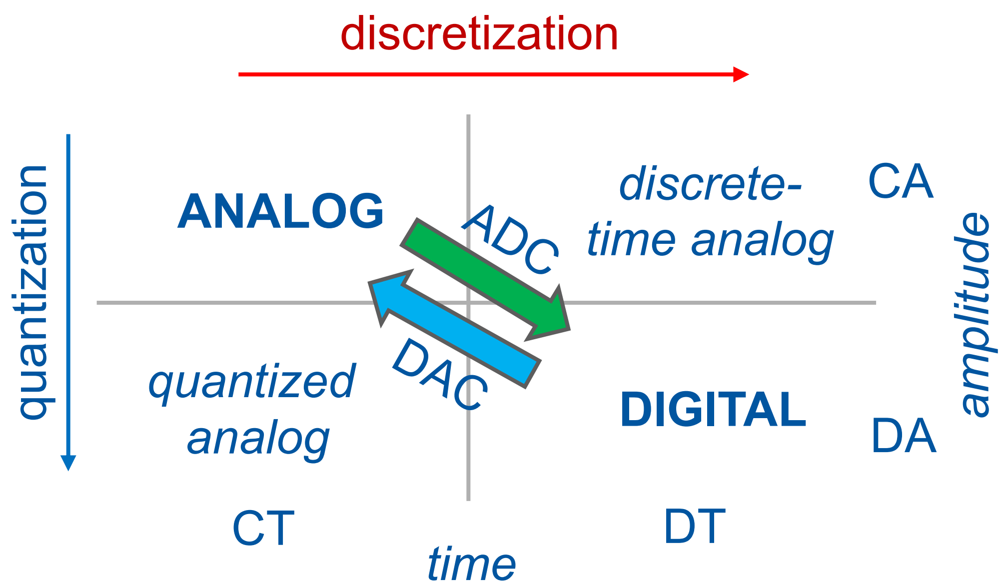
New 20 kA PC

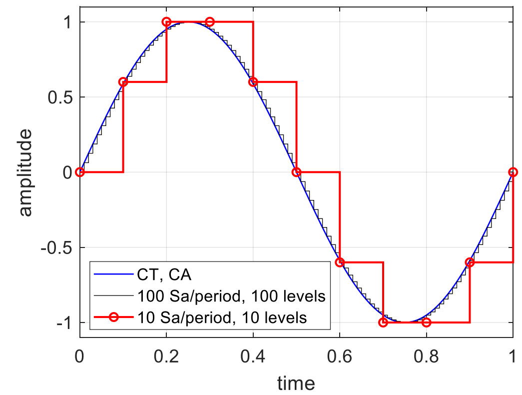


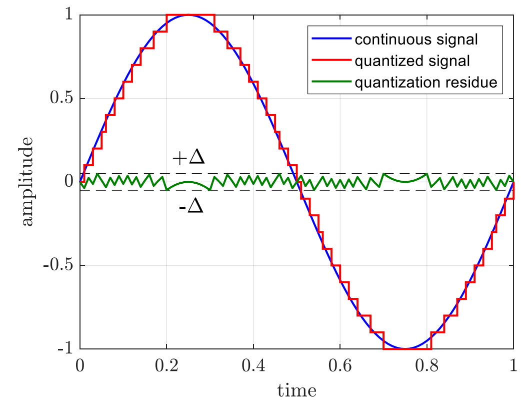


New electronics chassis for the 20 kA head

# Analog-to-digital conversion




## Discretization

$$x(t) \rightarrow x[nT_S]$$

**Shannon-Nyquist sampling theorem:**

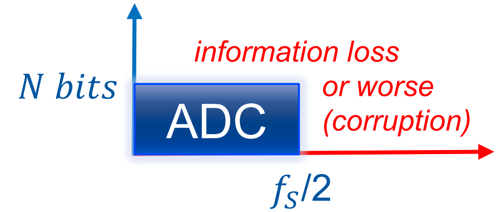
$$f_S > 2f_{\max(signal)}$$

## Quantization

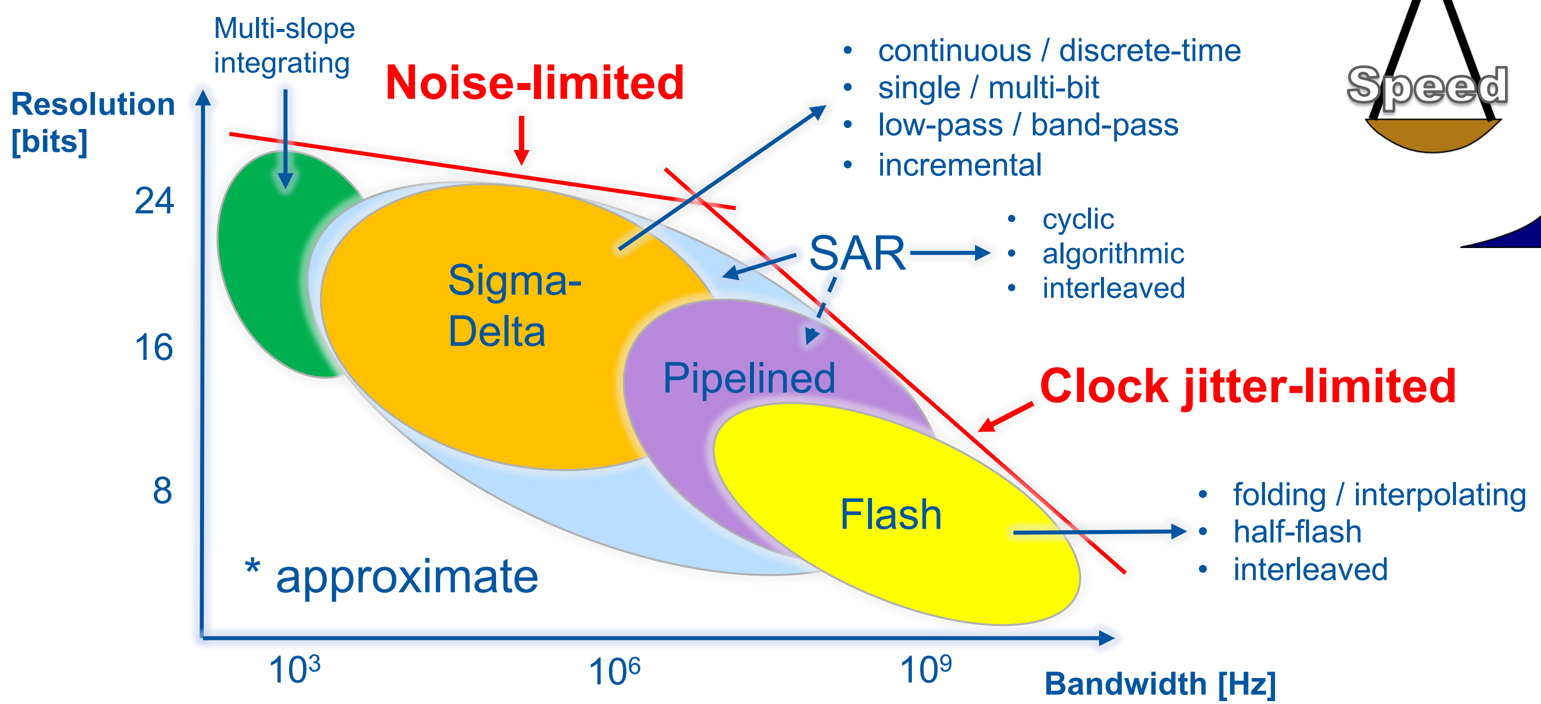
$$Q(x) = \Delta \left\lfloor \frac{x}{\Delta} + \frac{1}{2} \right\rfloor$$

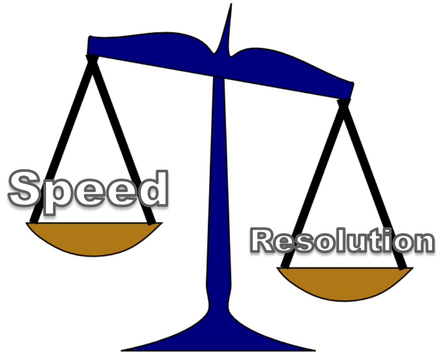
$$\sigma_q = \frac{\Delta}{\sqrt{12}}$$

*(a.k.a. "quantization noise")*

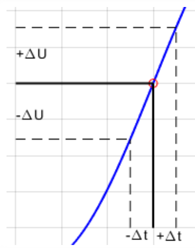


# ADC architectures



# ADC limitations




*Sampling and aperture jitter worst case: Nyquist sampling, middle of sine wave*

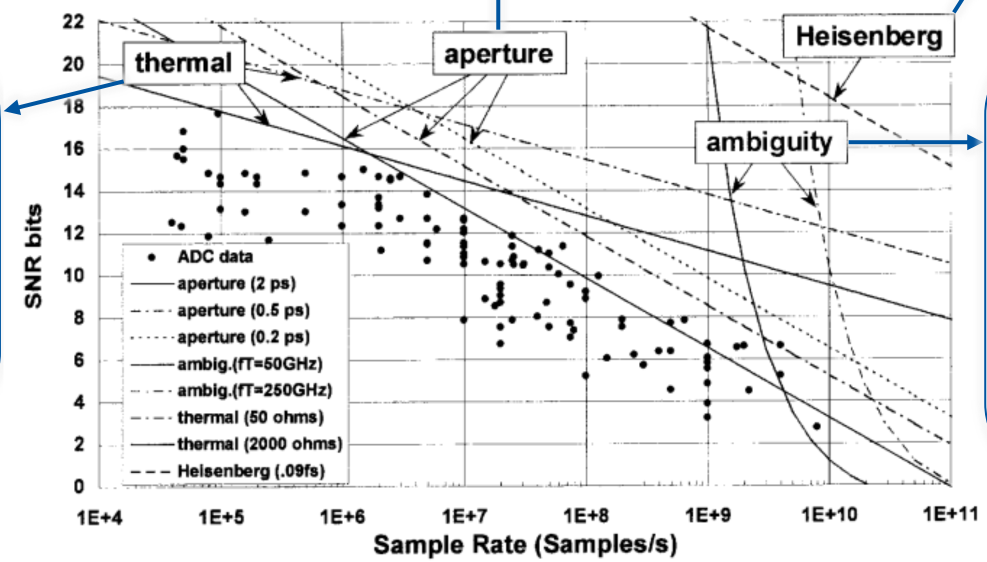
$$B_{\text{aperture}} = \log_2\left(\frac{2}{\sqrt{3}\pi f_{\text{samp}}\tau_a}\right) - 1$$

$$\Delta E \cdot \Delta t = \frac{1}{R}\left(\frac{LSB \cdot T}{4}\right)^2 \geq \hbar$$

uncertainty principle

$$B_{\text{thermal}} = \log_2\left(\frac{V_{FS}^2}{6kTR_{\text{eff}}f_{\text{samp}}}\right)^{1/2} - 1$$

In reality: multiple sources of white noise (thermal, shot noise, etc.) lumped together into a single input-referred ***effective noise resistance***




From Walden's 1999 ADC survey [2]

$$B_{\text{ambiguity}} = \frac{\pi f_T}{6.93 f_{\text{samp}}} - 1.1.$$

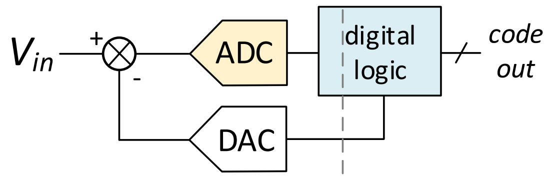
$f_T$ – transition frequency (transistor technology)

ambiguity – how fast a comparator responds to a ½ LSB step

**ALL practical limitations are in the analog domain**

# High resolution ADCs

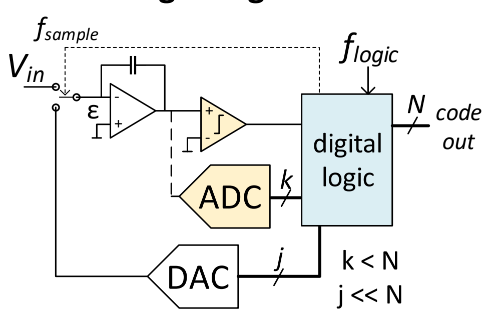
**analog → digital**




**basic structure**

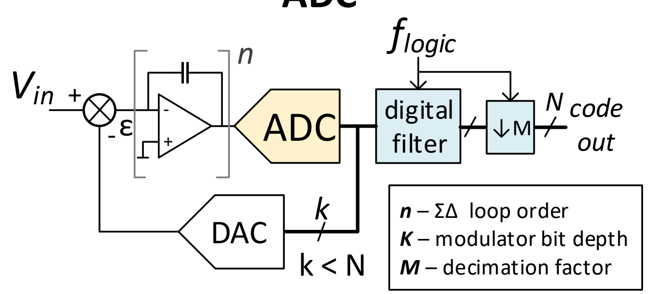
> **Common features**
>
> - closed-loop topology
> - low-resolution ADC (or comparator) in the loop
> - DAC in the feedback path
> - requires $f_{logic} >> f_{sample}$

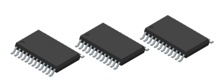
## Multislope integrating ADC




High-end DVMs

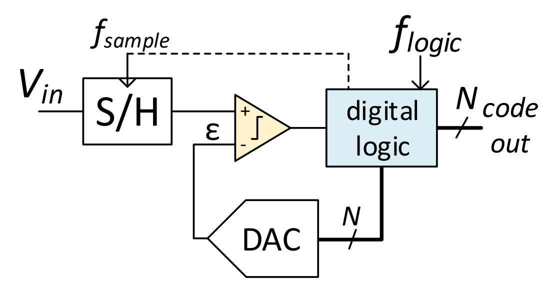
## Sigma-Delta ADC

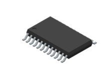


Very wide range of ICs

## SAR ADC



A few with N>20 bits

# The ideal digitizer

## Ideal ADC

- No excess noise (only quantization)
- No sampling jitter
- Perfectly linear, monotonic, no missing codes
- No drift (temperature, time, etc.)
- No latency
- Immediate step settling

## Ideal Digitizer

- Infinite $Z_{in}$
- Infinitely high power supply isolation
- **Ideal ADC**
- Perfectly stable and noiseless voltage reference
- Flexible operation

*“Swiss army knife”*

# What we really need in a digitizer

| Feature / parameter | Need comes from | Ballpark |
|---|---|---|
| Resolution | Capability for fine adjustment | >22 effective bits (near DC) |
| Monotonicity | Closed-loop control | >22 effective bits (near DC) |
| Broadband noise | Regulation performance (< 10 Hz),<br>resolving of tones above the noise floor (> 10 Hz) | a few ppm in 500 Hz<br>~$10^{-7}$ V $Hz^{-1/2}$ |
| Short-term and mid-term stability | Regulation performance (<< 10 Hz) | sub-ppm in minutes / hours ($10^{-6}$ to $10^{-1}$ Hz) |
| Temperature coefficient (TC) | Regulation performance (<< 10 Hz),<br>temperature variations due to machine operation | < ppm/°C |
| Long-term stability | Tracking of different magnets / powering sectors, frequency of calibration | few ppm/year |
| Linearity | Tracking of different magnets / powering sectors | ppm |
| Delay / latency | Real-time control | ~ms<br>constant ! |

# What we don’t really need

| Feature / parameter | Why not important |
| --- | --- |
| **Dynamic performance** (sampling jitter, aperture uncertainty, settling time, passband flatness, AC accuracy, etc.) | quasi-DC signal, slow control loop (~ Hz)<br>AC measurement only for small tones, no need for high accuracy |
| Fast sampling | ~kHz is enough |
| Low power dissipation | No practical limitations. A few W are negligible, compared to other systems. |
| **Functional flexibility** (measurement ranges, sampling rates, interfaces, very high $Z_{in}$, wide operating temperature range) | Not needed.<br>Only one fixed, well-defined application environment |

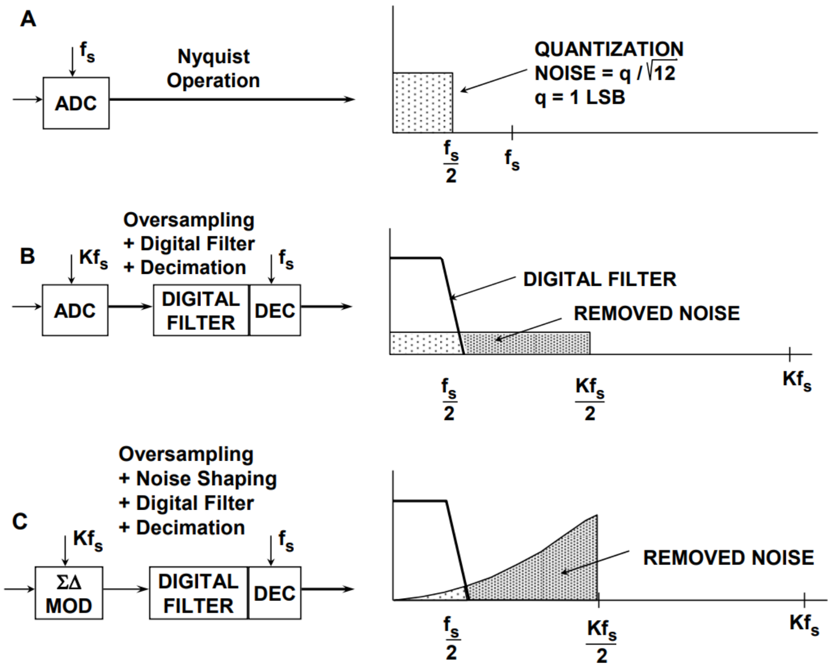
# Development of high-performance digitizers for power converters at CERN

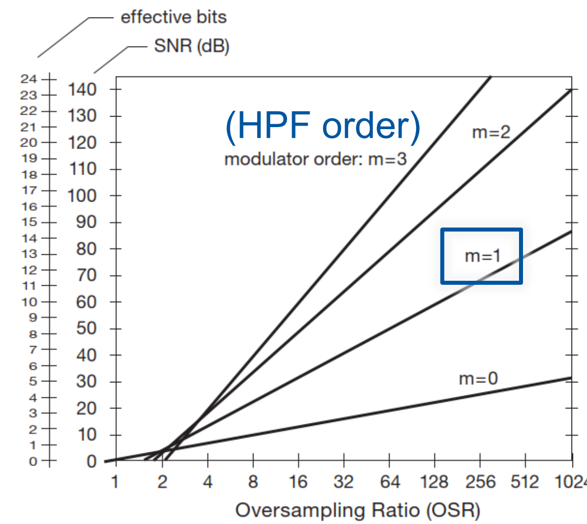
# DS22

- Designed and developed at CERN in the 1990s
- 3rd order Sigma-Delta ADC built of discrete parts (no ADC IC)
  - High precision Vishay foil resistors
  - LTZ1000A-based voltage reference
  - Temperature-stabilized using a Peltier element
- Improved gradually over the years
- Version 10.1 (2006) installed in LHC
- Accuracy Class 1: main dipoles, main quadrupoles, inner triplets – in total 24 circuits (48 digitizers) in operation
- Excellent reliability record so far

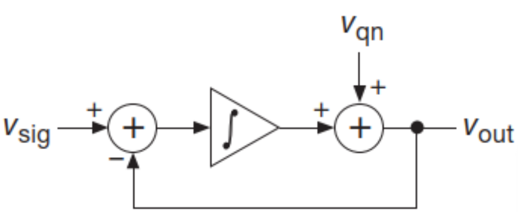
- Not compliant with HL-LHC Class 0 requirements for noise (low-frequency and broadband), as well as fill stability
- Contains obsolete components (e.g. 5 V CPLD)
- Has known problems (e.g. idle tones)
- Difficult to build and tune

# Sigma-Delta – frequency domain view



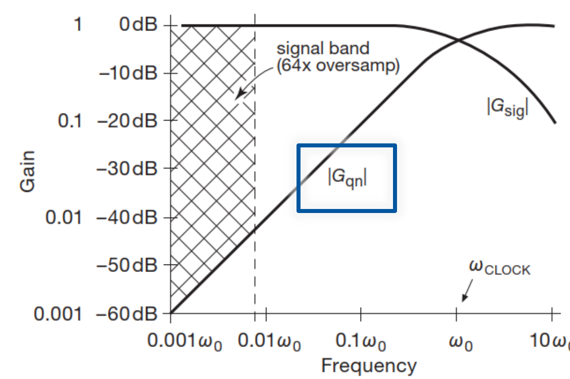

From: Analog Devices MT-022




linear model

$$|\mathbf{G}_{\mathrm{sig}}| \equiv \left|\frac{v_{\mathrm{out}}}{v_{\mathrm{sig}}}\right| = \frac{1}{\sqrt{1+(\omega/\omega_0)^2}}$$

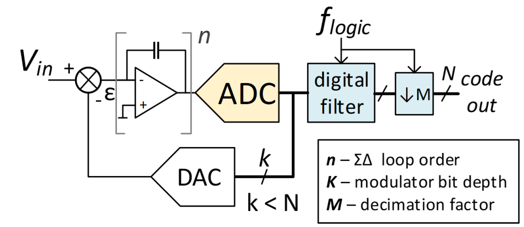
$$|\mathbf{G}_{\mathrm{qn}}| \equiv \left|\frac{v_{\mathrm{out}}}{v_{\mathrm{qn}}}\right| = \frac{\omega/\omega_0}{\sqrt{1+(\omega/\omega_0)^2}}$$ HPF



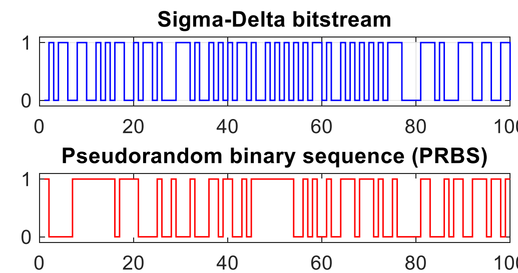

From [5]

# Sigma-Delta – time-domain view

- Integrators: the first one is a *summing node*; all integrators behave as distributed memory

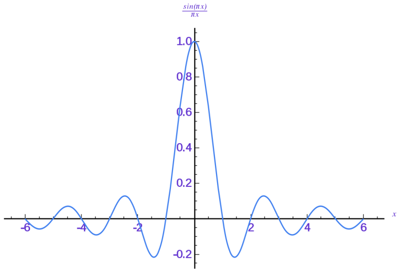



- SD modulator loop: the instantaneous error *ε* is not minimized (Each and every try is wrong, but over a longer time the *average of the error* is minimized)
- Quantization error is *larger* than the signal
- Modulator action – "noise shaping" can be seen as "being more active" (same mean value, more transitions)

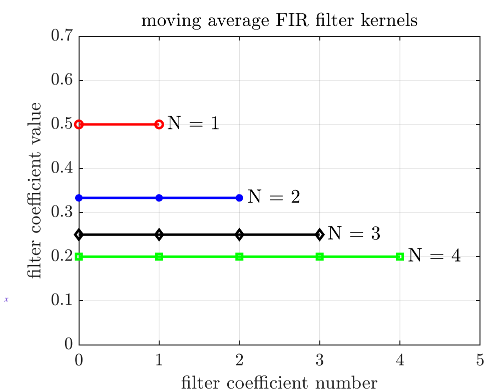



- Filter – not a simple **moving average**, where the number of digital code levels would be *(N + 3)*
- Typically, *sinc (sin(x)/x)* filters are used. They can be cascaded (*sinc$^n$*)
- zeros can be set for rejection at specific frequencies (50/60 Hz, N x $f_S$, etc.)
- ***N* >> OSR**
- Group delay = [(N-1)/2] x $T_S$ *(for linear-phase FIR filters*

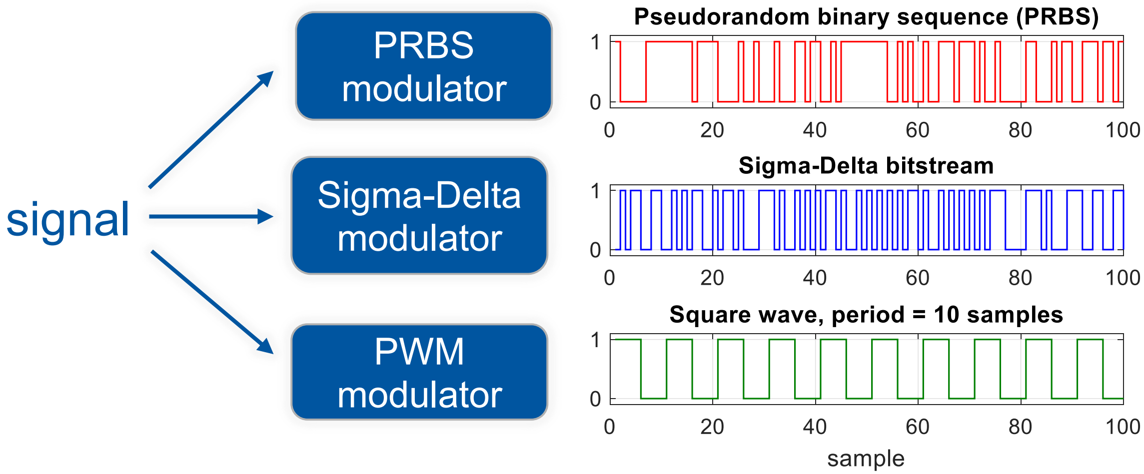
- One bit from the bitstream contributes to many bits in the filtered and decimated output

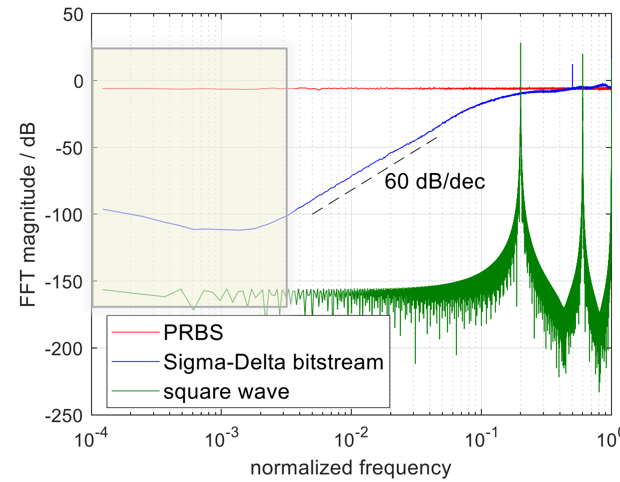



*sinc* filter kernel



# Still, why Sigma-Delta?




**Disadvantages of PWM:**

- Tradeoff in PWM frequency vs time resolution
- Typically, fine/coarse scheme needed for >12 bits
- Modulator is **less robust** against component non-ideality

“ Finally, it should be noted that $\Sigma\Delta$-encoders have many other virtues than the possibility of decoding their output democratically. One of their amazing advantages is their robustness: imperfections in the quantizer do not affect the rate of convergence in $\lambda$ given in (2), whereas the same imperfections would lead to a strictly positive lower bound on the error in a binary encoding procedure, regardless of $\lambda$ (see [2], [3]). ”

IEEE TRANSACTIONS ON INFORMATION THEORY, VOL. 48, NO. 6, JUNE 2002

**The Pros and Cons of Democracy**

A. R. Calderbank, *Fellow, IEEE*, and I. Daubechies, *Fellow, IEEE*

*Invited*

***Abstract*—We introduce the concept of “democracy,” in which the individual bits in a coarsely quantized representation of a signal are all given “equal weight” in the approximation to the original signal. We prove that such democratic representations cannot achieve the same accuracy as optimal nondemocratic schemes.**

***Index Terms*—Democratic decoding, sigma–delta quantization.**

# A quick information-theoretic view

- The goal: optimal (or at least efficient) encoding and decoding of information for reliable communication

  *"Just about everyone who transmits digital bits tries to send those bits as far as possible, as fast as possible, down the cheapest possible medium, until recovery of those bits becomes an analog problem"*

  Eric Swanson [1]

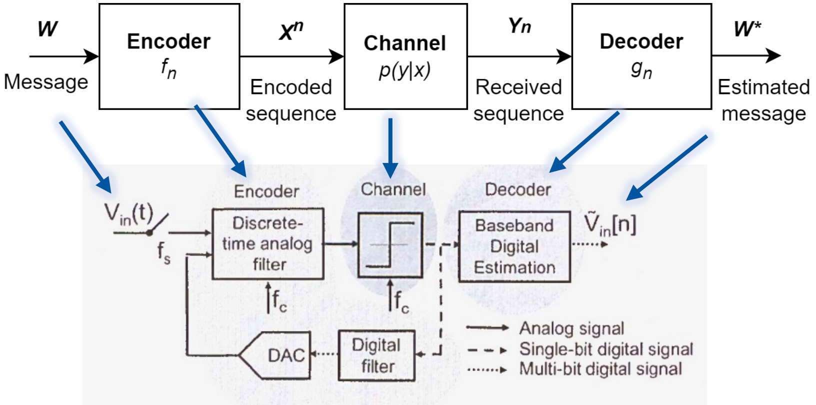
- Established by Nyquist, Hartley and **Shannon**
- Average information quantity: **entropy**

$$H = -\sum_i p_i \log_2 p_i$$

- Communication **channel capacity**:

$$C = B \log_2 \left(1 + \frac{S}{N}\right)$$

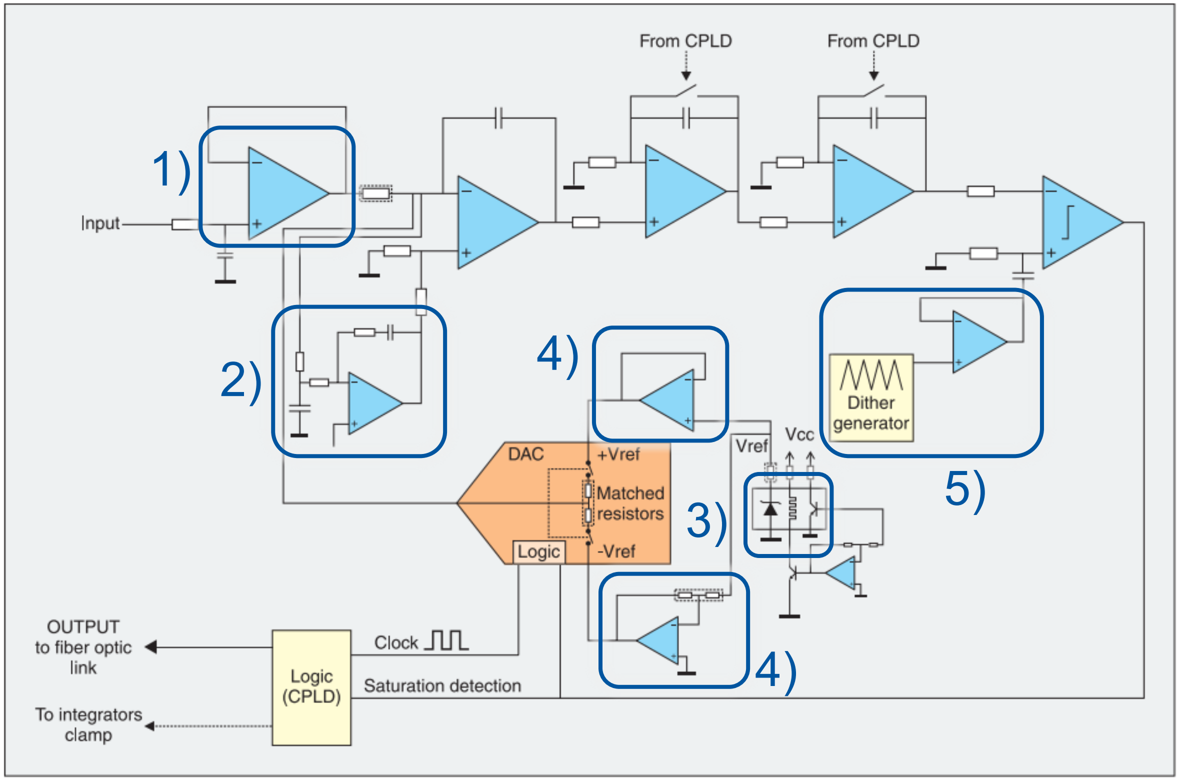
*Band-limited channel with white Gaussian noise*




From [6]

- Every modulation / encoding scheme exists between these two extremes, including Sigma-Delta
- Some schemes (e.g. Turbo codes) approach the Shannon limit. Others are optimal in terms of other criteria (error rate, robustness, complexity of implementation, etc.)
- Despite the different goals, there could be valuable clues coming from Information Theory regarding ADC operation, bottlenecks, and optimization at the system/architecture level

# From DS22 to DS24



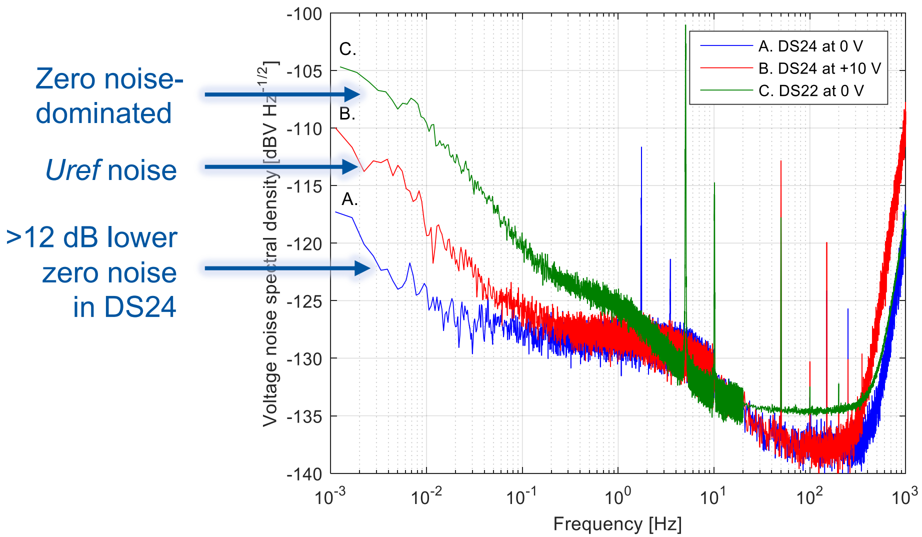

1) **Input buffer** → autozero amp
2) **DC stabilization of first integrator**
→ optimized circuit
3) **Voltage reference**
→ ADR1000 instead of LTZ1000
4) **Buffering and scaling of Uref**
→ autozero amps
5) **Dither signal generator**
→ PRBS instead of 480 kHz triangular wave

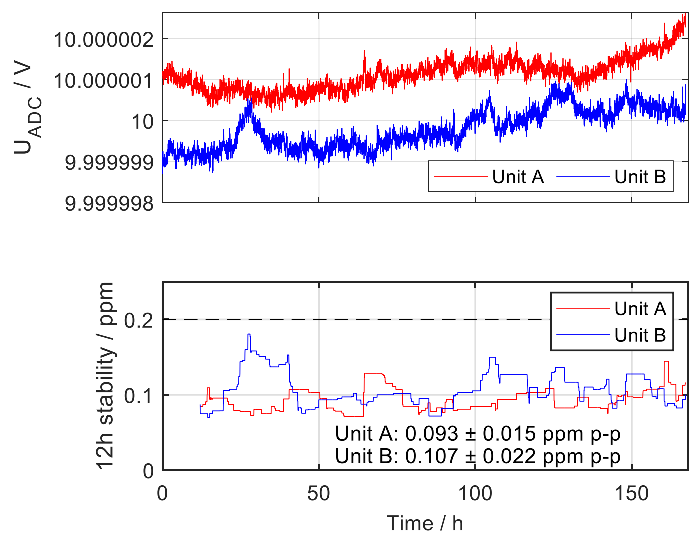
+ replacement of obsolete parts
+ new PCB layout
+ some improvements in mechanical design

analog problems → analog solutions

# DS22 to DS24 – improvements

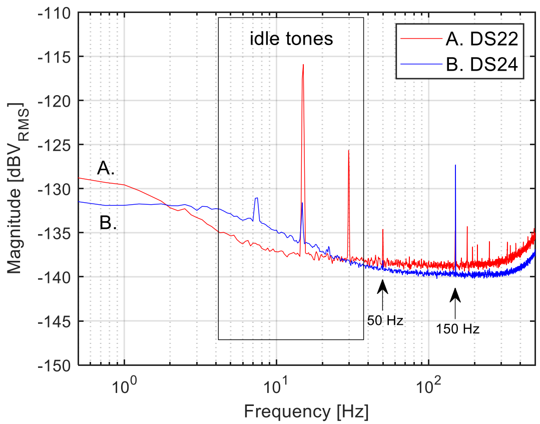
- LF noise improvement: >12 dB (hence DS2**4**)
- Mid-term isothermal stability also much better; Class 0 - compliant



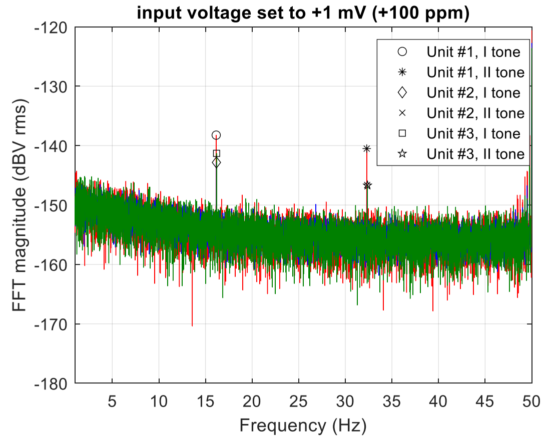




- Unfortunately, TC could not be improved significantly without a major redesign *(bottleneck: TC of DAC switches).* It remained on the ±0.2 ppm/°C level

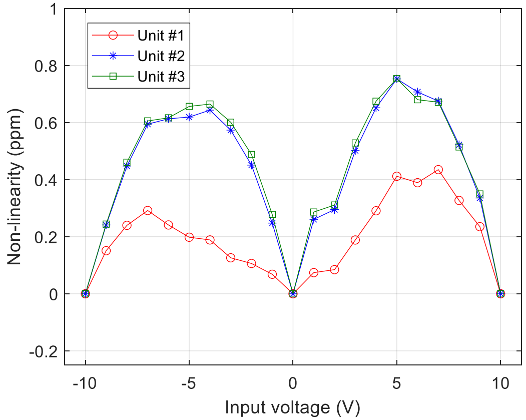
# DS22 to DS24 – improvements



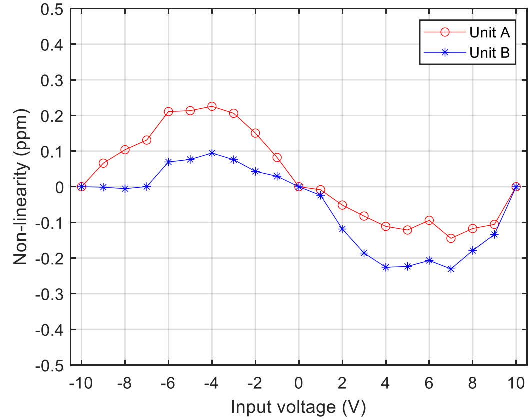

Idle tones: first try of PRBS dither
**>15 dB improvement over DS22**




Newest prototypes: even lower!




INL first try: similar to DS22




Newest prototypes: better!

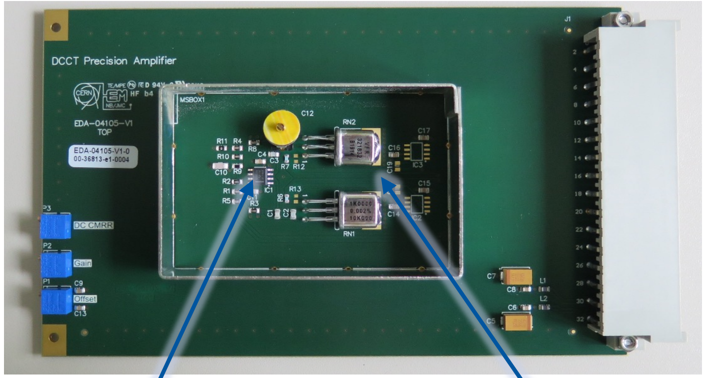
PCB layout improvements

→ impact of parasitics is dominant

😐

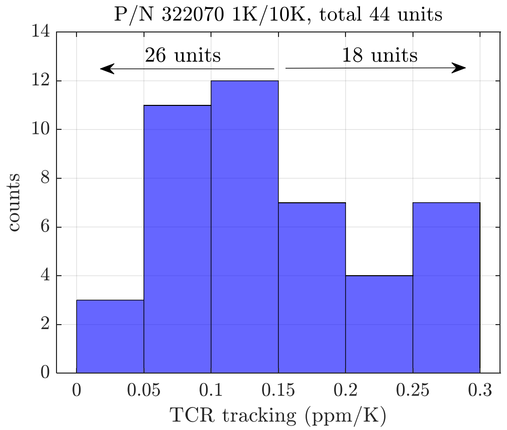
# LHC dipole circuit upgrade

- Beam optics studies suggested that the short-term stability of magnet powering for certain dipole circuits would impact on the tune stability in HL-LHC
- Full upgrade of the dipole circuits to Class 0 was deemed too complex/expensive
- A partial upgrade was proposed and accepted. It has two parts:
  - Replacement of DS22 with DS24 digitizers (full backward compatibility)
  - Replacement of the precision amplifier (G=10) in the DCCTs
- The upgrade targets mainly short-term stability/noise, but would also impact on mid-term stability

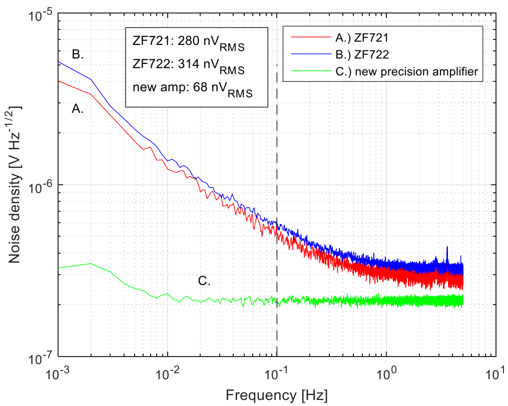



OPA189 auto-zero amp

VHD200 selected for lowest gain TC




~60% of units have TC tracking < 0.15 ppm/°C

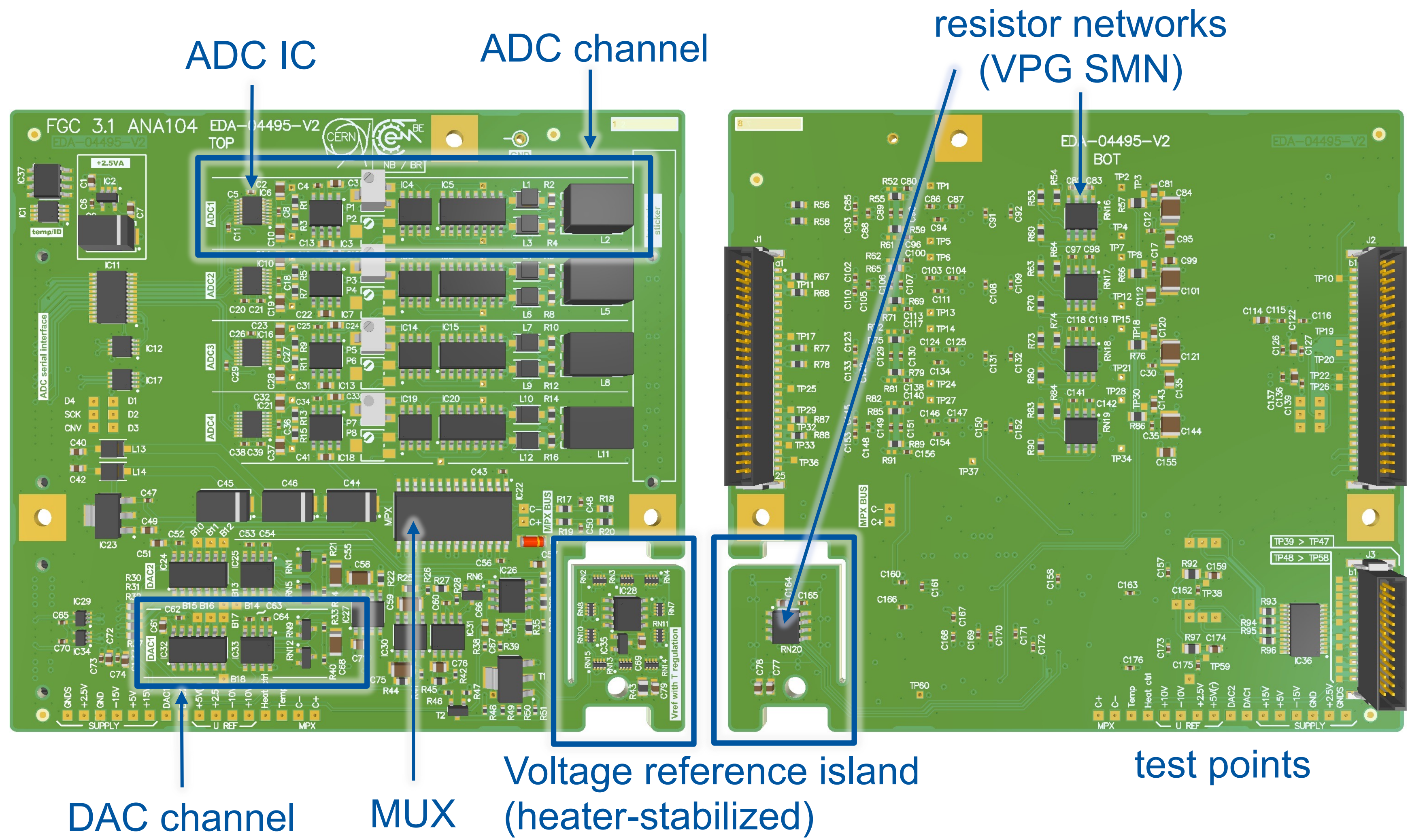



LF noise (0.001-0.1 Hz) improved >4x

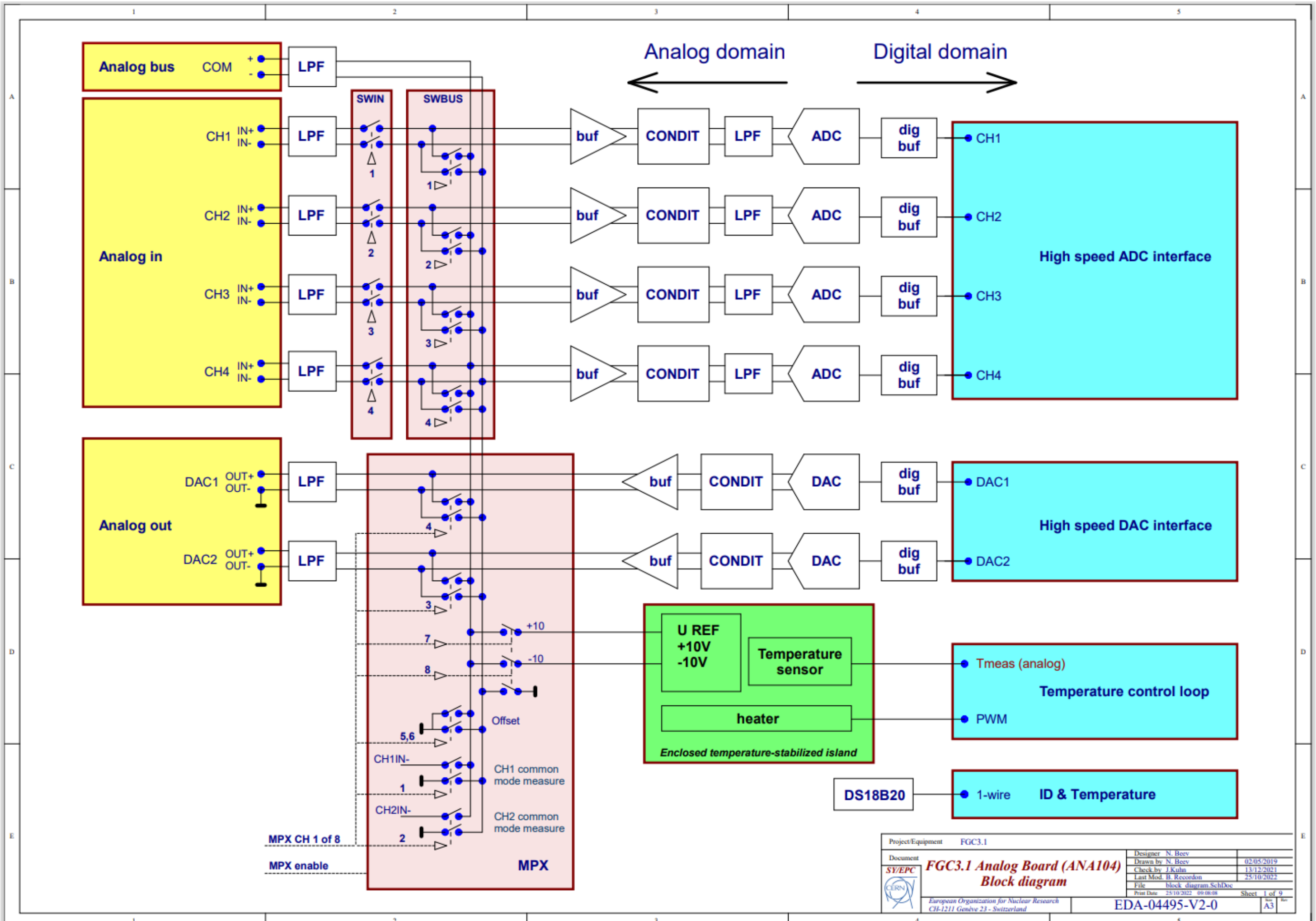
# Other (lower-precision) digitizers

- Many applications don’t need extreme precision
- However, high bandwidth is needed for pulsed and cycled applications (non-LHC – *injectors*)
- Need for multiple channels, analog outputs (DACs)
- Many boards / systems have been developed for use in magnet and RF powering at CERN:
  - FGC3 ANA101 – based on ADS1274 (4-channel $6^{th}$ order 1-bit Sigma-Delta)
  - FGCLite analog board – radiation-tolerant, based on ADS1271. Raw bitstream output, filter implemented in FPGA
  - PAM, PAMB *(for POPS, POPSB)* – also based on ADS1271 & ADS1274
  - FGC3 ANA103 / 104 – based on LTC2378-20 (20-bit SAR, 500 kSamples/s). Very widely used *(~1000 ANA104s arriving this year)*
  - HV “analog optical link” for Marxdiscap – LTC2378-18 on ADC side (floating at HV); 20-bit DAC (MAX5719) on the other end

# ANA104 - overview

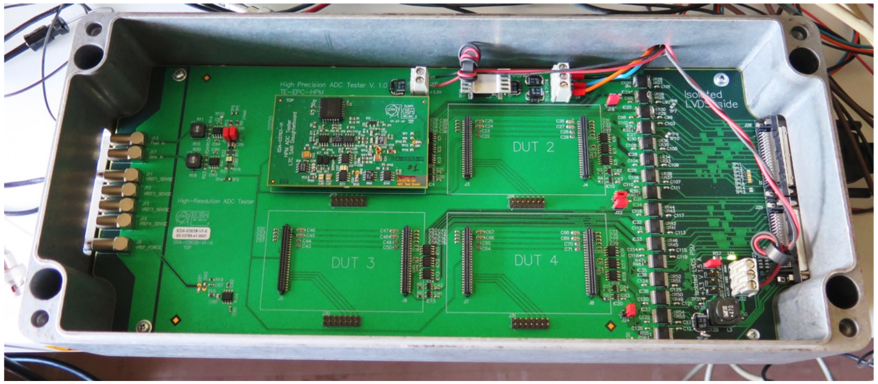


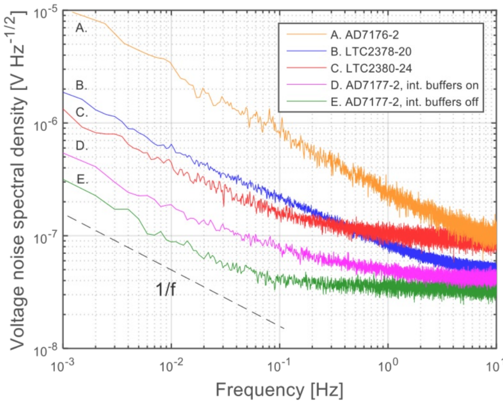
# ANA104 - block diagram



# Evaluation of commercial ADC ICs

- Started in 2007 as part of HL-LHC R&D for Accuracy Class 0
- Many candidates with nominal resolution ≥24 bits were screened (datasheet information)
- Results presented at I2MTC-2018 [7]
- Some selected units were tested in the lab




- Main finding: integrated ADCs had improved significantly: **the few best candidates beat DS22 in terms of noise**

# ADC resolution metrics

- **Nominal resolution** – number of bits at the ADC output interface for a single conversion
- **Digital code resolution** – $log_2$(*number of digital codes*) → Arbitrarily high

**Signal-to-Quantization Noise Ratio (SQNR) ***

$$SQNR\ [dB] = 10log_{10}\frac{P_{signal}}{P_{quant.\ noise}} = 6.02N + 1.76$$

↔

**Nominal resolution**

$$N[bits] = \frac{SQNR\ [dB] - 1.76}{6.02}$$

← **Ideal or low-resolution ADC**

**Signal-to-Noise Ratio (SNR) ***

$$SNR\ [dB] = 10log_{10}\frac{P_{signal}}{P_{quant.\ noise} + P_{excess\ noise}} \approx 10log_{10}\frac{P_{signal}}{P_{excess\ noise}}$$

→ To equivalent ideal ADC

**SNR bits**

$$SNR\ bits\ [bits] = \frac{SNR\ [dB] - 1.76}{6.02}$$

← **Practical high-resolution ADC**

**Signal-to-Noise and Distortion ratio (SINAD) ***

$$SINAD\ [dB] = 10log_{10}\frac{P_{signal}}{P_{noise}+P_{distortion}}$$

hard to measure > 18 bits

→

**Effective Number of Bits (ENOB)**

$$ENOB\ [bits] = \frac{SINAD[dB] - 1.76}{6.02}$$

"signal": full-scale pure sine wave

**0 V input**

**Effective Resolution (ER)**

$$ER\ [bits] = log_2\left(\frac{V_{FS(p-p)}}{V_{excess\ noise(RMS)}}\right)$$

**Noise-Free Code Resolution (NFCR)**

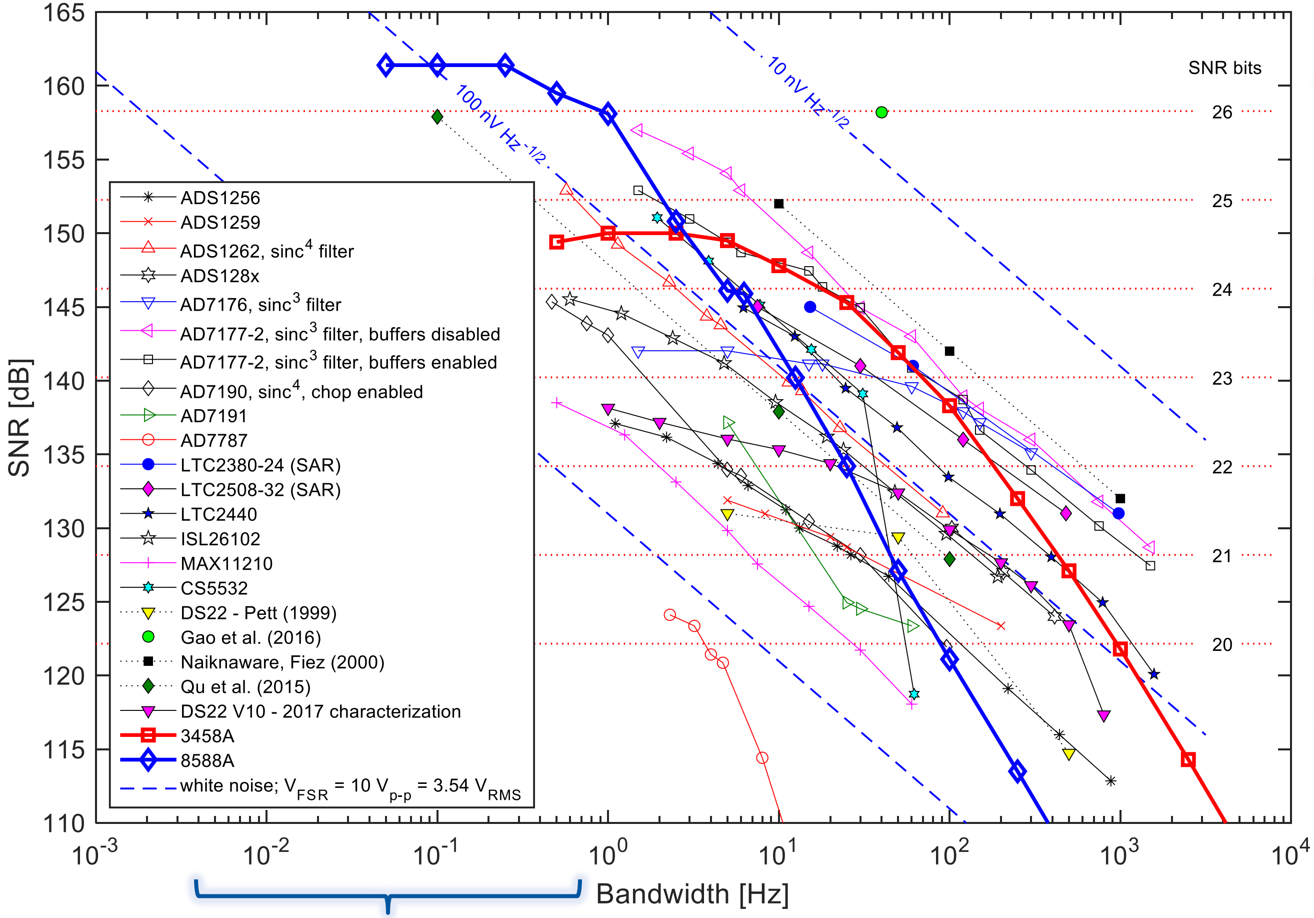
$$NFCR\ [bits] = log_2\left(\frac{V_{FS(p-p)}}{V_{excess\ noise(p-p)}}\right) = ER - 2.7\ bits^*$$

*1000 samples of noise with Gaussian PDF

---

| Nominal resolution | ER | NFCR | ENOB | DC-accurate bits (ΔT=10 °C; int. Uref) |
|---|---|---|---|---|
| 32 b | 26 b at 50 Samples/s | 23.3 b at 50 Samples/s | (<19 b at 1 kHz) | (<16 b) |

# Integrated ADCs - summary




Few having > 24 SNR bits

$$SNR\ bits = \frac{SNR\ [dB] - 1.76}{6.02}$$

Fairly big spread

Typically no information for sub-Hz

# Integrated ADCs - summary

| ADC | Type | Nominal resolution [bits] | Noise floor $[\mathrm{nV}/\sqrt{\mathrm{Hz}}]$ | Offset drift [ppb/°C] | Gain drift [ppm/°C] | INL (typ) [ppm] |
|---|---|---|---|---|---|---|
| **AD7177-2** | SD | 32 | **30** [a] | ±8 | ±0.4 | ±1 |
| **ADS1256** | SD | 24 | 120 | ±20 | ±0.8 | ±3 |
| **ADS1262** | SD | 32 | 110 | **±0.1** | 0.5 | 3 |
| **ADS1281** | SD | 32 | 110 | 6 | 0.4 | **0.6** |
| **AD7190** | SD | 24 | 280 [a] | **±0.5** | ±1 | ±5 |
| **LTC2440** | SD | 24 | 70 | ±2 | 0.2 | 5 |
| **CS5532** | SD | 24 | 70 | ±1 | ±2 | ±15 |
| **ISL26104** | SD | 24 | 120 | ±30 | ±0.1 | ±2 |
| **MAX11210** | SD | 24 | 250 [b] | 5 | **0.05** | ±10 |
| **LTC2508-32** | SAR | 32 | 50 | ±14 | **±0.05** | **±0.5** |
| **LTC2380-24** | SAR | 24 | **30** [b] | 9 | **0.05** | **0.5** |
| **AD7767** | SAR | 24 | 60 | 1.5 | 0.4 | 3 |

Estimated, assuming [a] BW = ODR/3; [b] BW = ODR/2

ODR = output data rate

↓ ppb (!) ↓ < ppm ↓ ≈1 ppm

This is a summary from 2017. Since then, some new parts with even better performance have appeared.
e.g. AD4630-24 – INL typical **±0.1 ppm (!), max ±0.9 ppm, gain drift ±0.025 ppm/°C**

# PART II

after a short break

# HL-LHC Accuracy Class 0

Stricter than LHC Class 1

| | Power converter | DCCT | ADC |
|---|---|---|---|
| Resolution [ppm] | 0.5 | - | 0.2 |
| Initial uncertainty after cal [2xrms ppm] | 2.0 | 1.0 | 1.0 |
| Linearity [ppm] [max abs ppm] | 2.0 | 1.0 | 1.0 |
| Stability during a fill (12h) [max abs ppm] | **0.7** | **0.5** | **0.3** |
| Short term stability (20min) [2xrms ppm] | 0.2 | 0.1 | 0.1 |
| Noise (<500Hz) [2xrms ppm] | **3.0** | **2.0** | **1.0** |
| Fill to fill repeatability [2xrms ppm] | **0.4** | **0.3** | **0.1** |
| Long term fill to fill stability [max abs ppm] | 8.0 | 4.0 | 4.0 |
| Temperature coefficient [max abs ppm/C] | **1.0** | **0.8** | **0.2** |

isothermal

$\Delta T = 0.5$ ºC

- Determined by operational experience from LHC and beam optics studies
- Improvement mostly needed in low-frequency noise and stability
- In particular, needed for K-modulation for the Inner Triplets
  *(K-modulation: a method to measure the focusing strength of quadrupole magnets)*
- Some requirements are easier to be met by the digitizer, hence the unequal splitting between DCCT and ADC

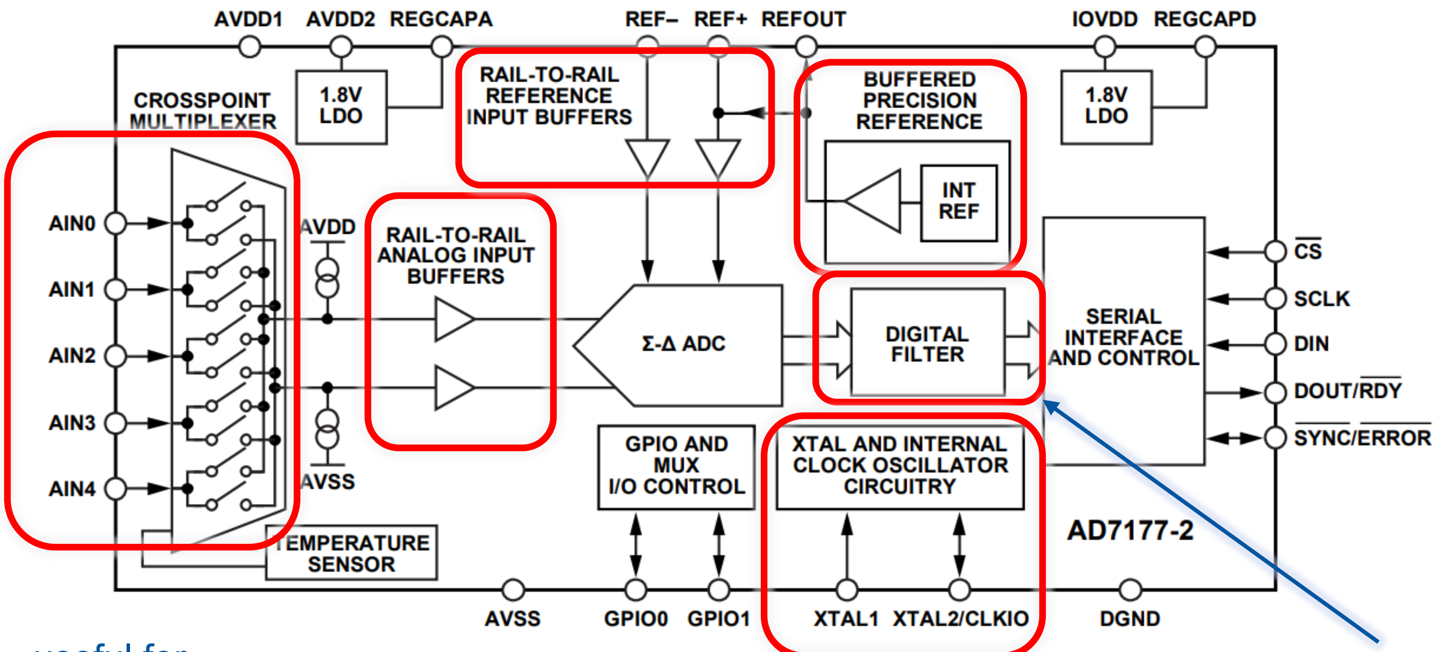
# HPM7177 – strategy and timeline

- In 2018/2019, it was decided to keep working on DS24, while in parallel developing a new digitizer based on a commercial IC
- Parts of the new digitizer were tested separately, before the first full prototypes were built in 2019
- Testing and characterization carried on through 2020-2021, with many difficulties related to COVID and component shortages
- The decision was eventually taken to use HPM7177 for HL-LHC Accuracy Class 0, and to produce DS24 units for replacement of DS22 only in the LHC main dipole circuits
- In 2022, two HPM7177 units were tested at PTB - Braunschweig
- Also in 2022, a contract was signed with Norcott Technologies Ltd. (Widnes, UK), following a tender for >100 units for HL-LHC
- In 2023-2024, the first series units were received, tested, and installed in SPS (mains consolidation) and in prototype power converters for HL-LHC

# AD7177-2 internals

Flexible buffering options
(better performance *without* buffers)

Internal reference: 2.5V, ±2 to ±5 /°C
(still useful for CM biasing)

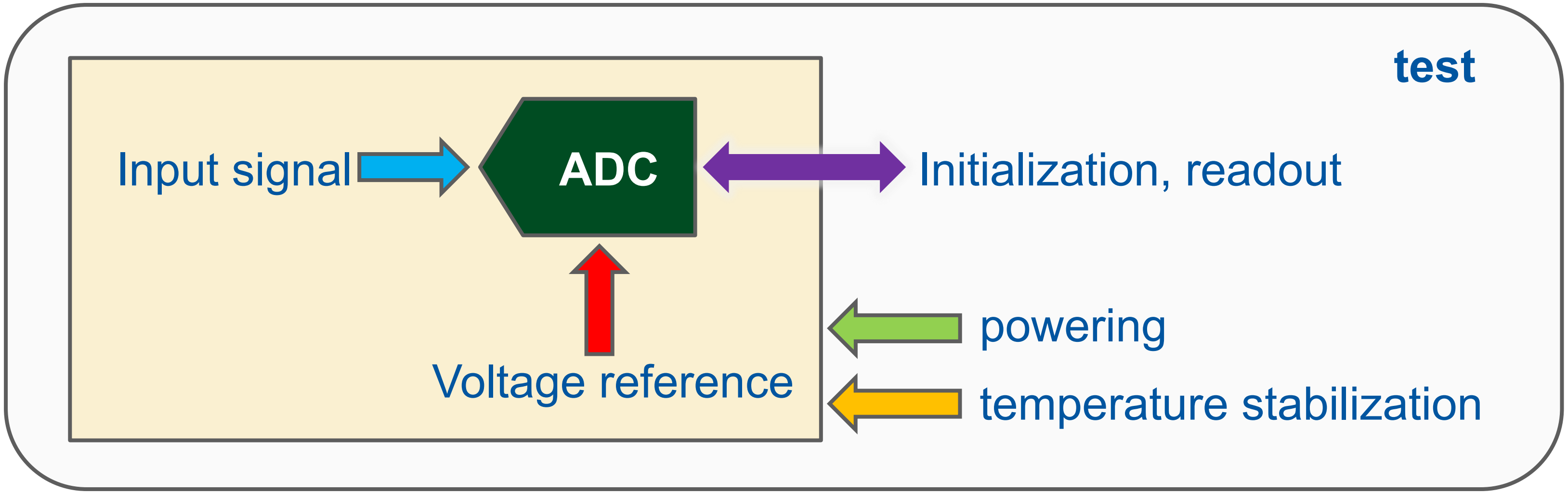



MUX – useful for
"internal short" test

External 16 MHz oscillator
– has impact on INL

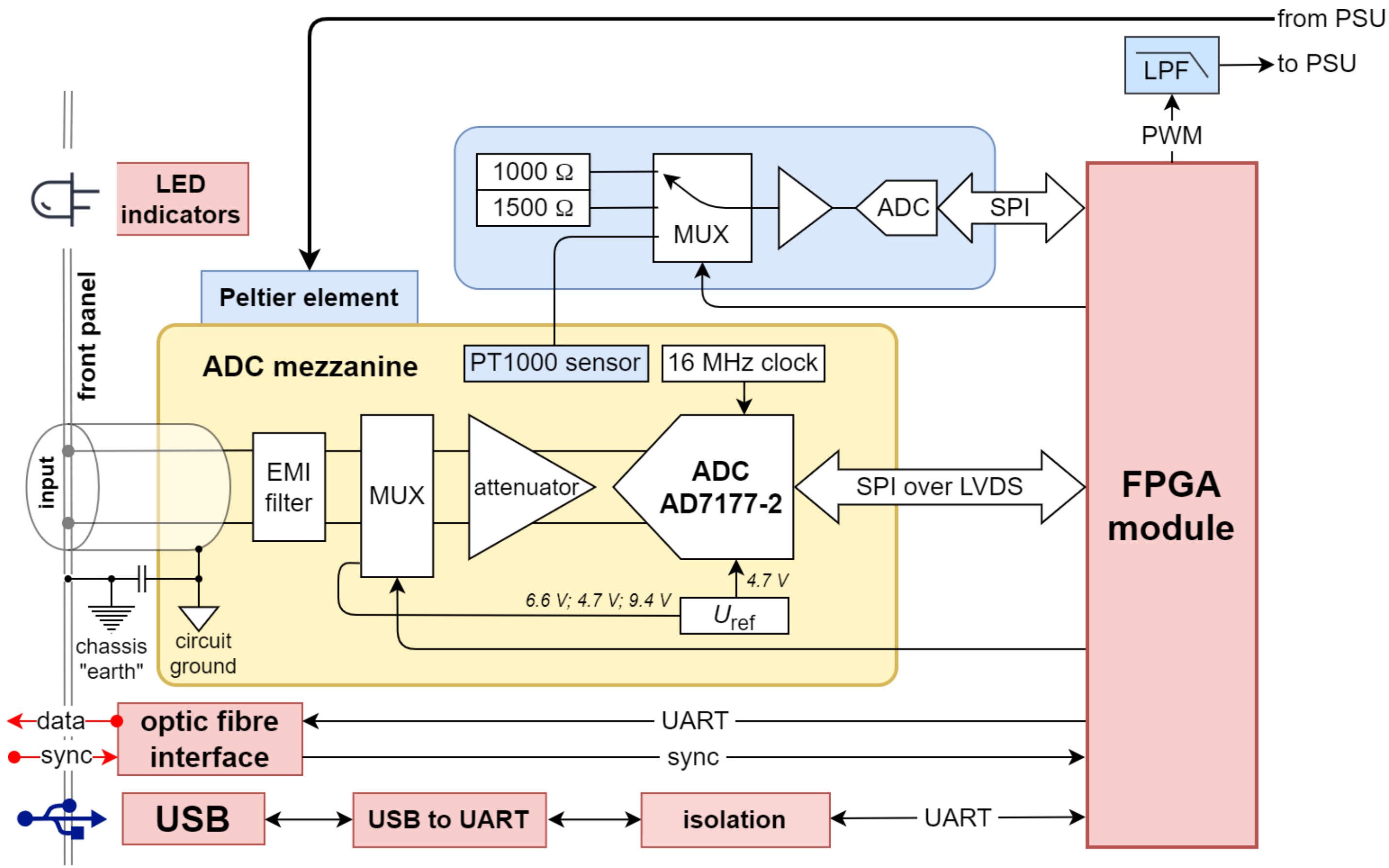
Digital filters + decimation
(reduced data rates)
we use the full 10 kSPS

# Building a digitizer around an ADC




- Matching of input range to ADC range (noise and stability critical, high CMRR)
- Matching of voltage reference to ADC (noise and stability critical)
- Low-noise, stable powering of ADC and analog circuits
- Digital logic – initialization and readout of ADC, control, diagnostics; interfacing with other systems
- Temperature stabilization – for TC << ppm/°C
- Built-in test features to facilitate production and laboratory tests

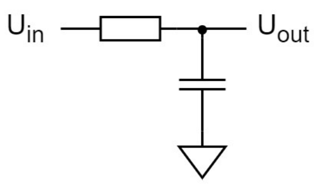
# HPM7177 block diagram



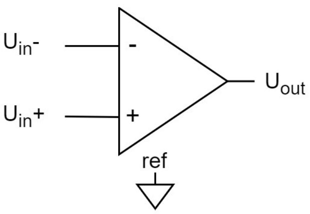

https://ohwr.org/project/opt-adc-10k-32b-1cha/wikis/home

# Fully differential circuits - basics

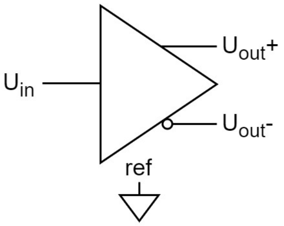
**Single-ended**
one input, one output, same reference point




**Differential**
two inputs **or** two outputs, same reference point

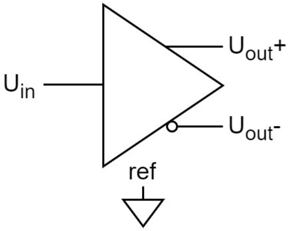



difference amplifier

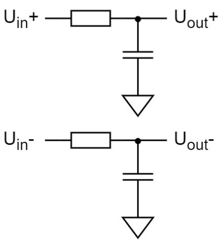



differential driver

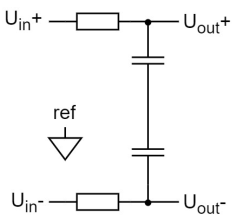
**Fully differential**
two inputs **AND** two outputs, (again) same reference point




fully differential amplifier (FDA)

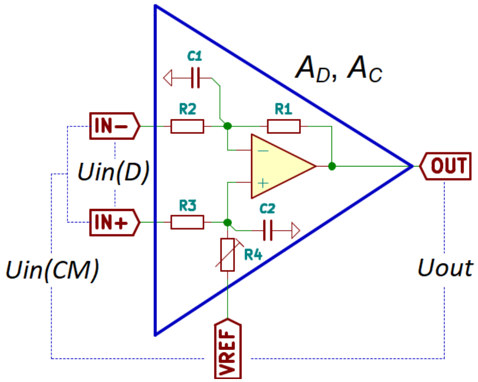



non-coupled FD filter

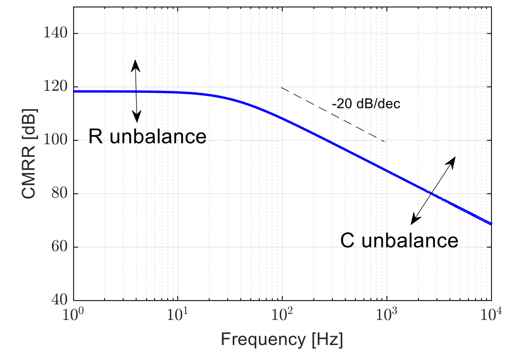



coupled FD filter

# The differential amplifier




$$U_{OUT} = A_D U_{in}(D) + A_C U_{in}(CM) + U_{ref}$$




**DC**

$$A_D = \frac{\frac{R1}{R1+R2} + \frac{R4}{R3+R4}}{2\frac{R2}{R1+R2}}$$

**Differential gain**
Can only be positive

$$A_C = \frac{\frac{R4}{R3+R4} - \frac{R1}{R1+R2}}{\frac{R2}{R1+R2}}$$

**Common-mode gain**
Can be positive, negative, **or zero**

**AC**

$$A_D(\omega) = \frac{\frac{\frac{R1}{1+j\omega R1C1}}{\frac{R1}{1+j\omega R1C1}+R2} + \frac{\frac{R4}{1+j\omega R4C2}}{R3+\frac{R4}{1+j\omega R4C2}}}{2\frac{R2}{\frac{R1}{1+j\omega R1C1}+R2}}$$

(LPF)

$$A_C(\omega) = \frac{\frac{\frac{R4}{1+j\omega R4C2}}{R3+\frac{R4}{1+j\omega R4C2}} - \frac{\frac{R1}{1+j\omega R1C1}}{\frac{R1}{1+j\omega R1C1}+R2}}{\frac{R2}{\frac{R1}{1+j\omega R1C1}+R2}}$$

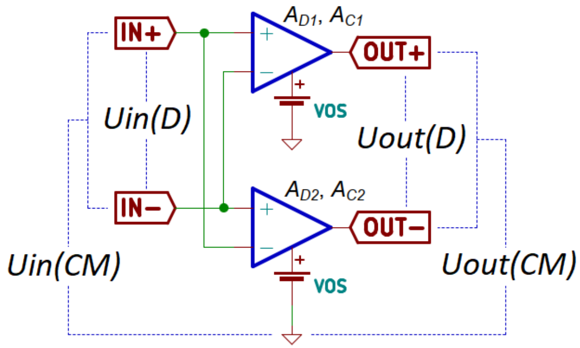
(HPF)

$$CMRR_{DA} = \frac{A_D}{A_C}$$

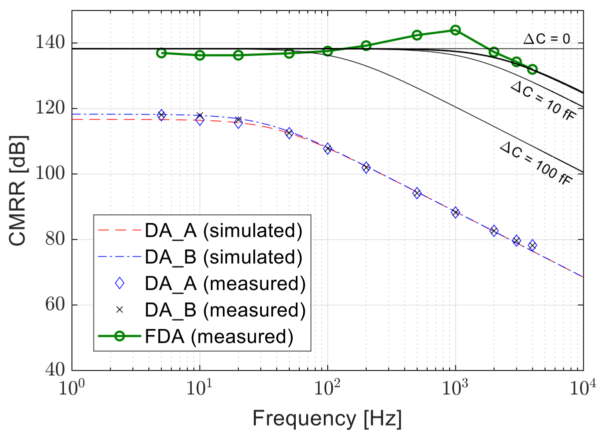
**Common-mode rejection ratio**
Can be anything (+ , -, ≈0, ∞) →
(not clear, with only magnitude given in dB)

**Different CMR behaviour at AC and DC:**
DC – matching of resistances; AC – matching of capacitances

# The fully differential amplifier




Built of two identical DAs




>130 dB from DC to 5 kHz,
ΔC between the two DAs < 10 fF
(a *really good* prototype)

$$\begin{bmatrix} U_{OUT}(D) \\ U_{OUT}(CM) \end{bmatrix} = \begin{bmatrix} A_{DD} & A_{CD} \\ A_{DC} & A_{CC} \end{bmatrix} \begin{bmatrix} U_{IN}(D) \\ U_{IN}(CM) \end{bmatrix} + \begin{bmatrix} U_{OS}(D) \\ U_{OCM} \end{bmatrix}$$

4 transfer functions

$$A_{DD} = A_{D1} + A_{D2}$$

**differential - differential**

$$A_{CD} = \frac{A_{D1} - A_{D2}}{2}$$

**CM - differential**

$$A_{DC} = A_{C1} - A_{C2}$$

**differential - CM**

$$A_{CC} = \frac{A_{C1} + A_{C2}}{2}$$

**CM - CM**

$$CMRR_{FDA} = \frac{A_{DD}}{A_{DC}}$$

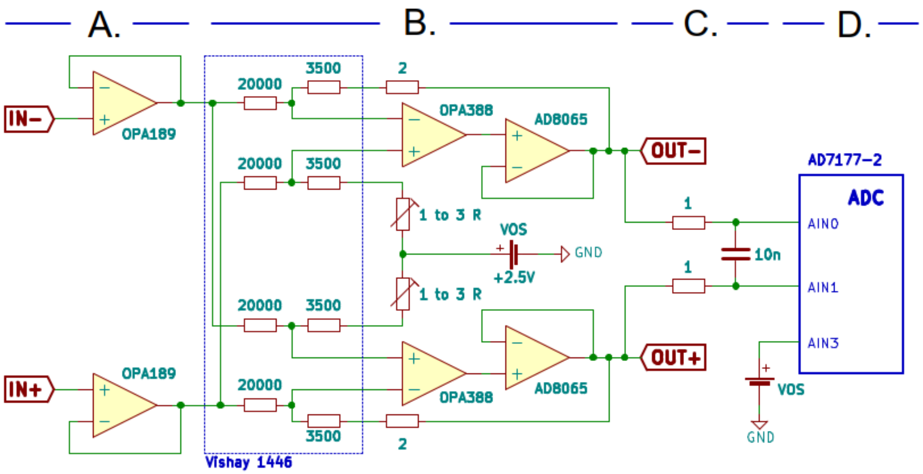
$CMRR_{FDA}$ depends on the ***difference*** between the two DAs → can be higher than their individual CMRRs

$$D = \frac{A_{DD}}{A_{CC}}$$

**Discrimination factor**

# A fully differential signal chain

- **Advantages**
  - 2x higher signal range for the same supply rails *(high-resolution integrated ADCs use this)*
  - More immune to interference (*if well balanced*), less sensitive to board-level stay currents
  - Possibility to achieve higher overall system CMRR
  - Possibility for cancellation of systematic errors
  - The natural way to go from differentially transmitted voltages to a differential ADC input
- **Disadvantages**
  - Higher circuit complexity, more components needed
  - Higher noise ($\sqrt{2}$ increase)




**A. Buffers** – non-coupled FD stage

**B. FDA** – coupled FD stage, trimmable DC CMRR, settable output DC CM voltage

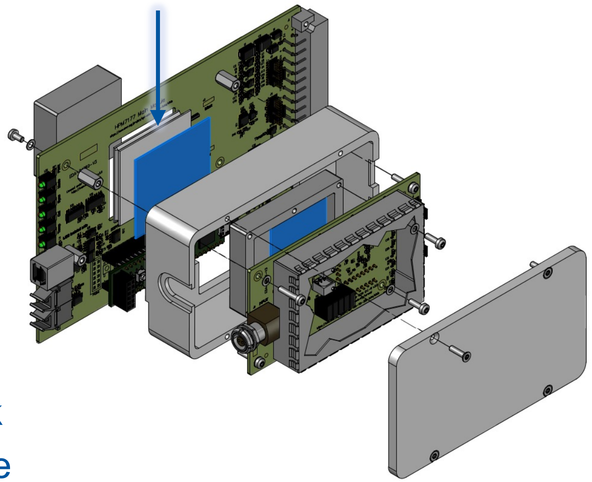
**C. Filter** – coupled FD stage

**D. ADC** – differential input, high CMRR *(requires DC bias of +2.5V)*

# Voltage reference system

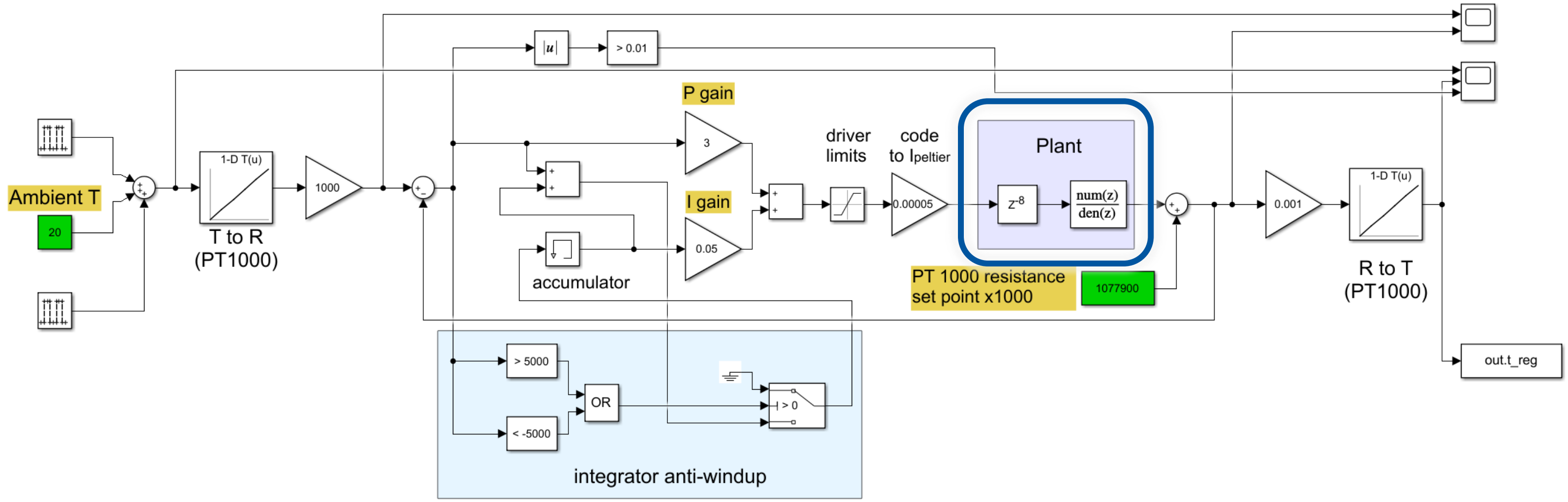
- Based on ADR1000 (more about it later)
- Burn-in performed on the ADR1000s (on-off cycling in oven)
- Fully standalone circuit, no controls
- Scaling from ≈7 V down to ≈ 5 V to be compatible with ADC – achieved using a “statistical” 1:1.41 divider made of six elements from an 8-element resistor network (the same as in the input FDA)
- The ratio was initially chosen for LTZ1000 ($U_z$ = 7.0 to 7.5 V), the $A_{VDD}$ of AD7177-2 was also increased to +5.2 V
- The ratio was kept the same for ADR1000 ($U_z$ ≈ 6.6 V), hence the lower derived voltages
- All DC voltages can be tested via the MUX, using a single external 10 V standard for absolute-value scaling:
  - Raw Zener voltage (≈ 6.6 V)
  - ADC reference (≈ 4.7 V)
  - ADC reference x 2 (≈ 9.4 V)
  - Additionally, the Zener + voltage divider current (in total ≈ 6.9 mA) is sensed using a 0.1 Ω resistor (node REF_GND)

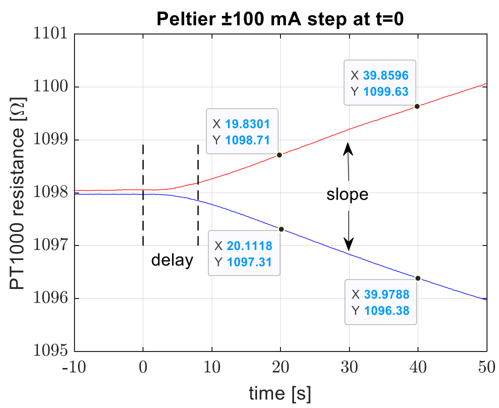
# Temperature stabilization



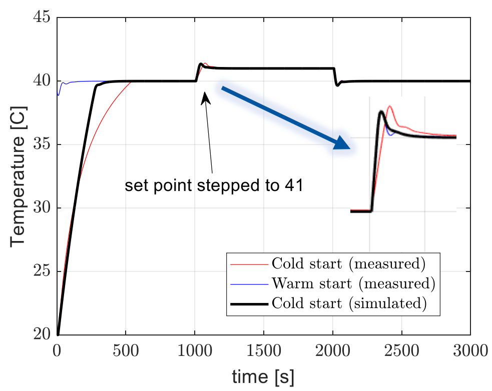

- **Sensor: PT1000**
  - Stable thin-film Platinum sensor in SMD package
  - On the ADC mezzanine, 4-wire connection to mainboard
  - Referenced to two fixed resistances: 1000 Ω and 1500 Ω → measurement range for temperature: 0 °C to 130 °C
  - Resolution ≈ mΩ/LSB → m°C/LSB
- **Actuator: Thermoelectric (Peltier) element**
  - Can heat or cool
  - One side connected to ADC mezzanine, the other to heat sink
  - Driven with DC current, which is generated in the PSU module
  - At $T_{set}$ = 40 °C, cross-over from heating to cooling happens around 30-32 °C (normal air flow)
- **Control algorithm**
  - Fairly plain and simple proportional-integral (PI) controller
  - Manually tuned (with some modelling help)
  - Implemented in Microblaze core firmware, using floating-point math
  - Control rate: 1 Hz
  - Mostly has to track changes in ambient temperature (self-heating is ≈ *constant*)
- **End result: TC at full scale < 0.05 ppm/°C (>16 tested units, ongoing campaign)**

# Temperature stabilization loop

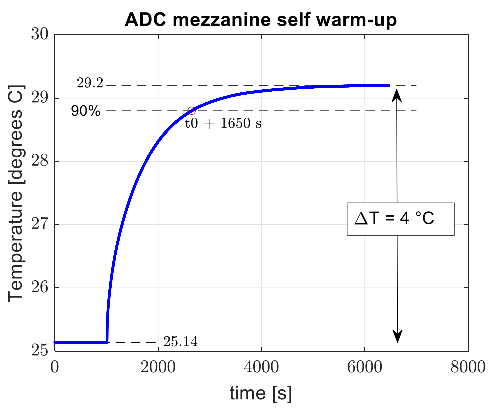



Parameters for simple plant model estimated from step measurement [8]

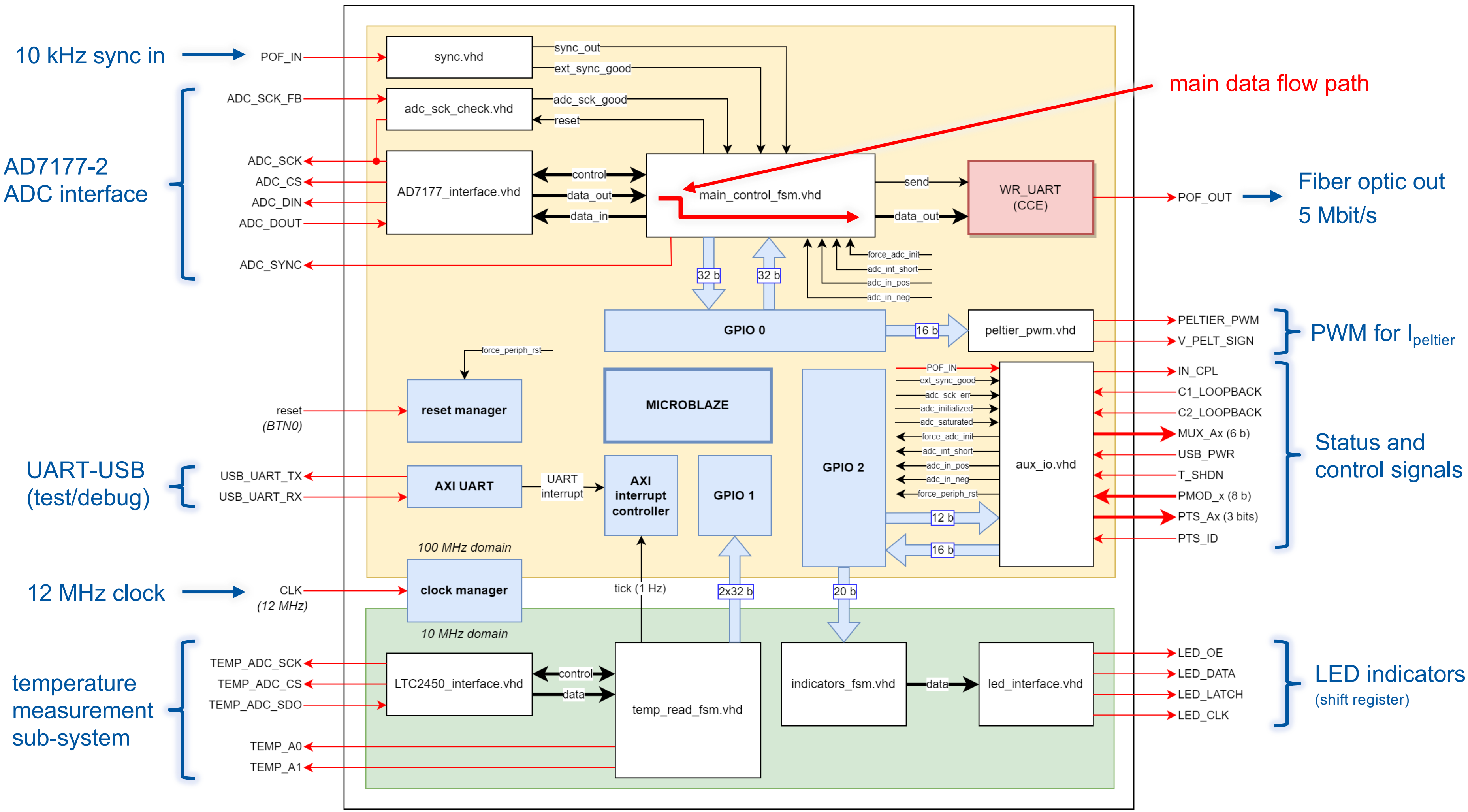



Models loop dynamics fairly well




Some effects (e.g. initial self-heating of mezzanine) are not modelled

# HPM7177 – FPGA design



# Component level

*“When art critics get together they talk about Form and Structure and Meaning. When artists get together they talk about where you can buy cheap turpentine.”*

**Pablo Picasso**

*“The practitioner will be aided in his task if he accepts two fundamental truths:*

1) *that no amount of wishful thinking will alter the laws of physics or the basic mathematical relationships that describe them, and*
2) *that **the most expensive way** to meet most system requirements, considering the value of the information converted over the life of the system, **is to select low-cost components** of inadequate stability and reliability.“*

**Bernard M. Gordon** [9]

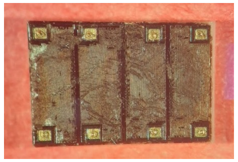
# Precision resistors

- Thin-film or metal foil
  - Mostly based on passivated NiCr films or NiCr-based alloys
  - Trimmable for highly precise absolute value, down to ±0.01%
  - Very low TC in foil resistors (but also non-linear and not very repeatable)
  - Packaging: SMD or THD (THD is more stress-resistant)
  - Packaging: plastic or hermetic (hermetic – resistant to humidity)
- To maintain precision and stability - should not be subjected to stress (mechanical, thermal, humidity, corrosive chemicals, ESD, etc.)
- It's better to operate well below the power rating, to avoid significant self-heating (self-heating → non-linearity, faster aging)
- Should be kept away from large thermal gradients and turbulent air flow

# Resistor networks

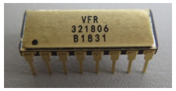
- Thin film or metal foil. Typically 2 to 8 elements per package
- Fabricated on the same substrate (A), or selected foil chips packaged together (B)
  - Case (A) – Inherent production matching, best for equal-value elements. TC and stability are usually dominated by **systematic effects**, so can be improved by proper element selection and interconnection (e.g. common centroid, interdigitation, etc.)
  - Case (B) – Matching by selection. TC is random, but the distribution is non-Gaussian (can be assumed rectangular)
  - In both cases, random mismatch can be improved by statistics (use of multiple elements)

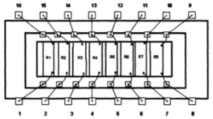
(A)

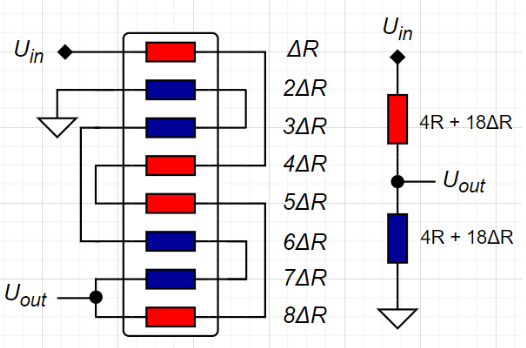
| RESISTANCE VALUES(1) | ABSOLUTE TCR (–55°C TO +125°C, +25°C REF.) (TYPICAL + MAX. SPREAD) | RESISTANCE RATIO | TCR TRACKING | TOLERANCE | |
|---|---|---|---|---|---|
| | | | MAX. | ABSOLUTE | MATCH |
| 100 Ω to1 kΩ<br>1 kΩ to 10 kΩ | ±0.2±2.8<br>±0.2±1.8 | R1/R2 = 1<br>1 <R1/R2 ≤10<br>10 <R1/R2 ≤100 | 0.5 ppm/°C<br>1.0 ppm/°C<br>2.0 ppm/°C | ±0.02%<br>±0.05%<br>±0.1% | 0.01%<br>0.02%<br>0.05% |

(B)

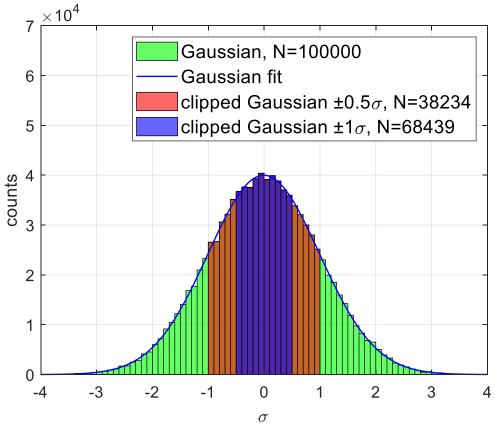


| RES# | PWR @70C (mW) | VALUE | ABS TOL. | RATIO TOLERANCE | ABS. TCR | TC TRACK +20 to +40°C | PINS |
|---|---|---|---|---|---|---|---|
| R1 | 100 | 20K | 0.01% | 0.01% between all | 5 ppm/ºC | 1 ppm/C between all | 1 - 16 |
| R2 | 100 | 3K5 | 0.01% | | 5 ppm/ºC | | 2 - 15 |
| R3 | 100 | 20K | 0.01% | | 5 ppm/ºC | | 3 - 14 |
| R4 | 100 | 3K5 | 0.01% | | 5 ppm/ºC | | 4 - 13 |
| R5 | 100 | 20K | 0.01% | | 5 ppm/ºC | | 5 - 12 |
| R6 | 100 | 3K5 | 0.01% | | 5 ppm/ºC | | 6 - 11 |
| R7 | 100 | 20K | 0.01% | | 5 ppm/ºC | | 7 - 10 |
| R8 | 100 | 3K5 | 0.01% | | 5 ppm/ºC | | 8 - 9 |



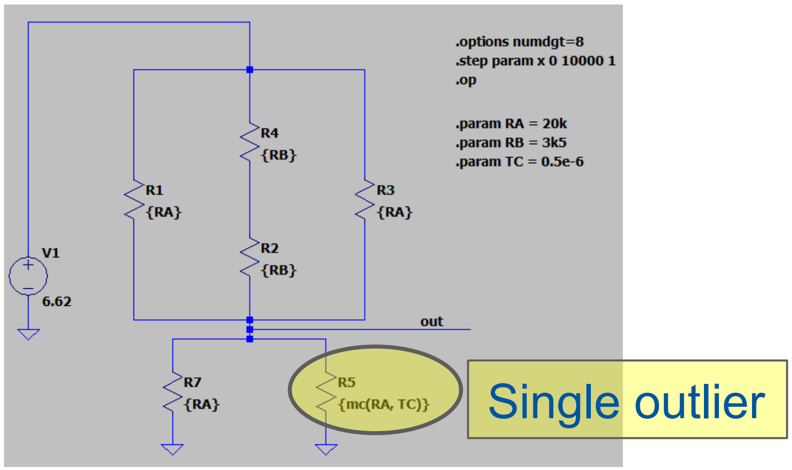

Common centroid layout cancels linear gradient *(just an example!)*

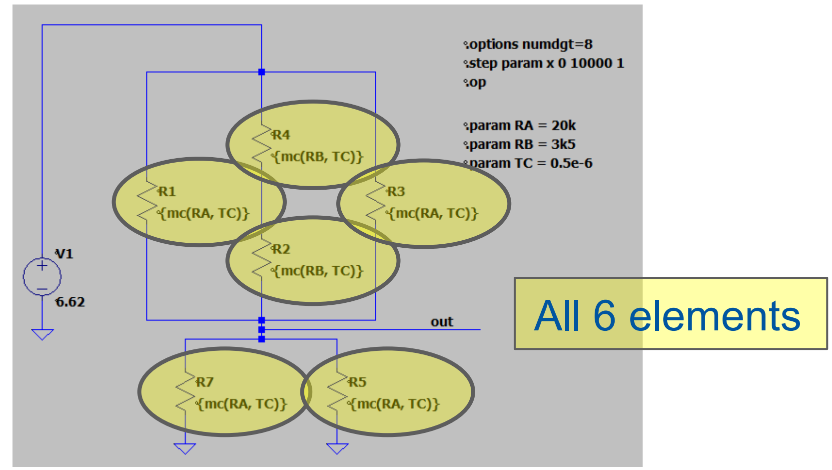


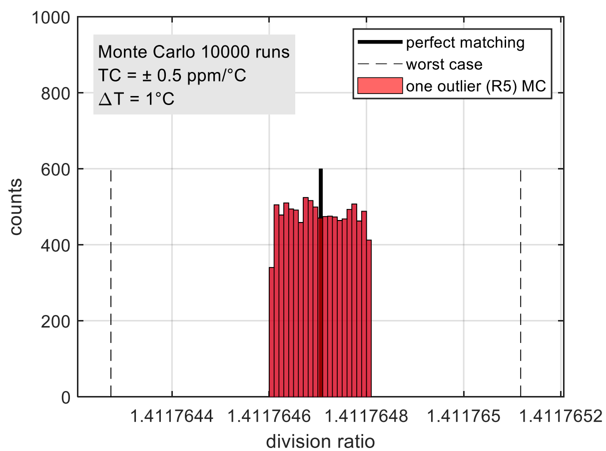

"Clipped Gaussian" distribution: stricter selection → more rectangular

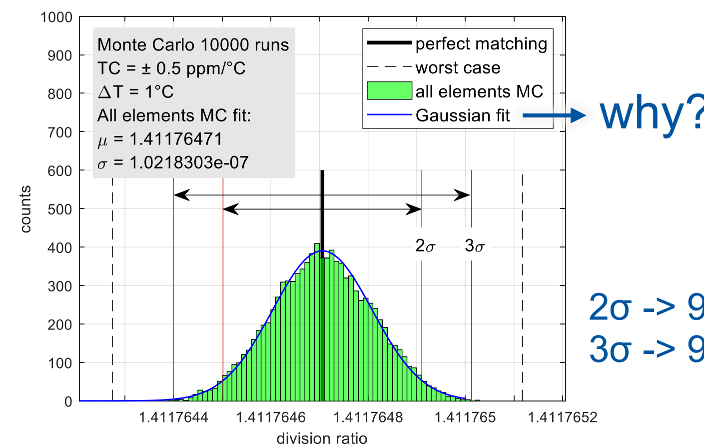
# Resistor networks and statistics

Example: 7 V / 5 V Voltage reference divider in HPM7177




2σ -> 95 %
3σ -> 99.7 %

# The Central Limit theorem

- $X_1, X_2 \ldots X_n$ – random variables with $\mu < \infty$ and $\sigma^2 < \infty$, *any* probability distribution
- Their normalized sum ($\mu=0, \sigma=1$) is:

$$Z_n = \frac{X_1 + X_2 + X_n - n\mu}{\sigma/\sqrt{n}}$$

- The limit of the cumulative distribution function (CDF) for large $n$ → standard normal CDF (**Gaussian**)

$$\lim_{n\to\infty} P(Z_n \le x) = \Phi(x), \quad x \in \mathbb{R} \qquad \Phi(x) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x} e^{-\frac{u^2}{2}} du$$

*“Under certain conditions, the sum of a large number of random variables is approximately normal”*

- An intuitive demonstration:


- Explains why the Gaussian distribution is so common (hence “normal”)
- Also relevant for uncertainty estimation – combined uncertainty can be considered normal, in case it is not dominated by uncertainties of type B (assumed rectangular), or type A based on just a few observations *(ISO GUM Annex G2)*

# Excess noise in resistors

- All resistors have **thermal** (Johnson / Nyquist) noise. It can be expressed as:

$$v_n = \sqrt{4k_BTR} \quad \left[\frac{V}{\sqrt{Hz}}\right]$$

(A) Voltage (Thevenin eq.)

$$i_n = \sqrt{\frac{4k_BT}{R}} \quad \left[\frac{A}{\sqrt{Hz}}\right]$$

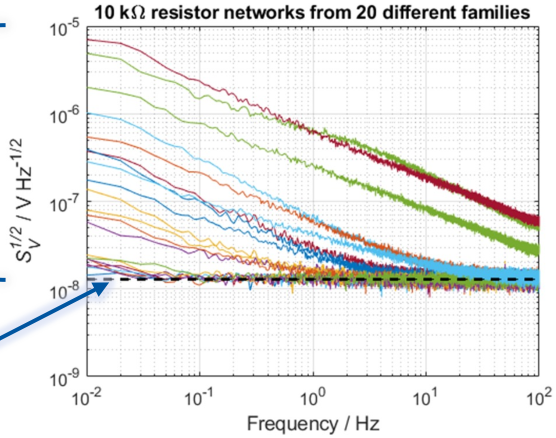
(B) Current (Norton eq.)

$$P_n = k_BT \quad \left[\frac{W}{Hz}\right]$$

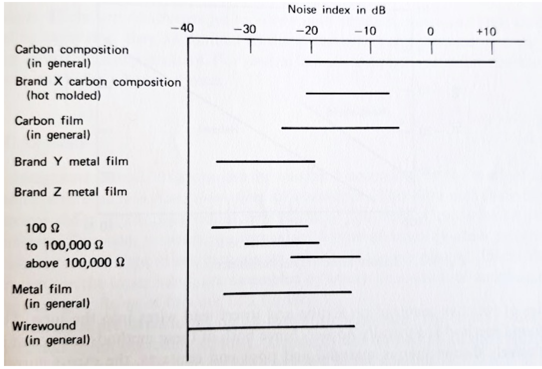
(C) power (matched load)

- It does not depend on the resistor type, construction, condition, etc. Its power *(C)* depends **only** on temperature. Voltage / current noise (A / B) depend on the resistance
- Fluctuations in resistance cause measurable **excess noise** when a resistor is biased
- Excess noise is a low-frequency phenomenon, typically *1/f* (equal power per *log(f)*) or *1/f*$^{\alpha}$
- Excess noise depends on many factors related to the resistor technology

4 decades spread
*(and these are not even "noisy" types!)*




thermal noise (theoretical)



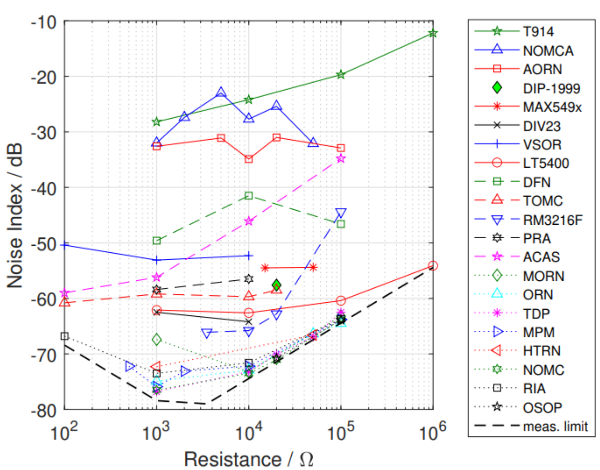

From [10]

# Excess noise in resistors

- Noise index

$$NI = 20log_{10}\left(\frac{V_{rms}[\mu V]}{V_{DC}[V]}\right) \quad [dB/decade]$$

  - Not always specified in datasheets
  - Standard method is good down to -40 dB
- An improved method and test setup were developed in 2021-2022
- Results presented at I2MTC-2022 [11]
- Many resistor networks were tested (thin film, metal foil, 100 Ω to 1 MΩ)




| NI [dB] | NiCr | | TaN | other |
|---|---|---|---|---|
| > -40 | | | NOMCA, AORN | T914 (*Tetrinox®*) |
| -40 to -60 | ACAS, PRA | DFN | DIP-1999, VSOR | MAX549x (*CrSi*) |
| < -60 | RM3216F, NOMC, MORN, OSOP, HTRN | TOMC, RIA, ORN, TDP, MPM | DIV23 | LT5400 (*CrSi*); metal foil: SMN / SMNZ, PRND, VHD |

substrate: Si, $Al_2O_3$, $Al_2O_3$ (foil)

- Foil resistors are very quiet
- Thin-film resistors on Si substrate are also good
- With ceramic substrates – it depends!

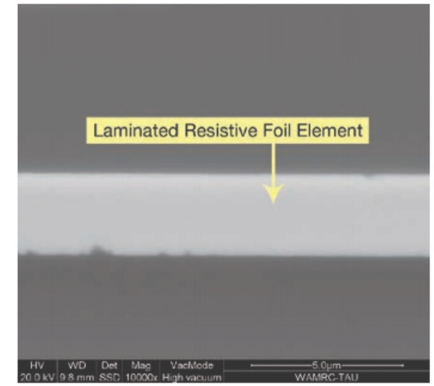



Figure 1. VSM0805 100R (X10,000)

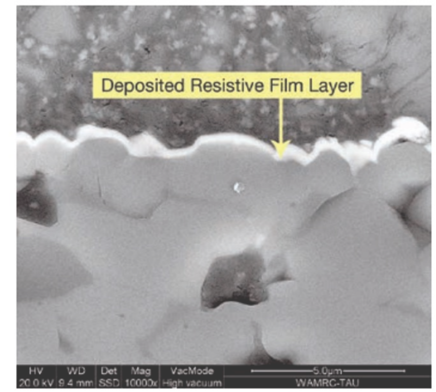



Figure 2. Thin film resistor 110R (X10,000)

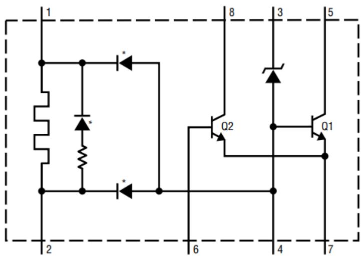
Foil vs thin film on $Al_2O_3$
From [12]

# Few words on capacitors

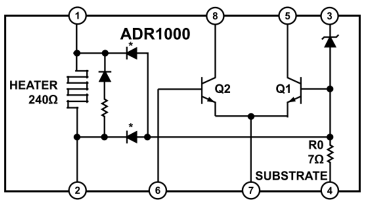
- For power supply decoupling: high-K ceramic capacitors are perfectly fine
- For anything in the signal path: **only** NP0/C0G ceramic capacitors should be used → cannot be very high-value
- In our application: fairly low dependence on capacitor non-ideality
  (capacitors used for filtering, op amp compensation)
- Most critical – filters at ADC signal and *Uref* input pins
- Just like precision resistors, should be kept away from air flow, stress, etc.

# Voltage reference ICs

- Lowest noise and best stability → buried Zener
- First HPM7177 prototypes: **LTZ1000**
  - ➢ Released in the 1980s
  - ➢ Two variants (LTZ1000 and LTZ1000A)
  - ➢ Used in high-end DVMs, voltage standards, calibrators
  - ➢ Considerable spread of parameters → selection
  - ➢ Burn-in helps with initial settling
- **ADR1000**
  - ➢ Pin-compatible with LTZ1000
  - ➢ Lower unit-to-unit spread, lower 1/f noise
  - ➢ Very low thermal (on-off) hysteresis
  - ➢ It was released just in time for the production of the HPM7177 series for HL-LHC
- Both require fairly complex external circuits
- Both need scaling down of the Zener voltage to the ADC $U_{ref}$ range (≈ 7 V to ≈ 5 V)
- *(ADR1001 has all supporting circuits built in plus scaling to 5 V, but was unavailable, and its performance is yet to be evaluated)*

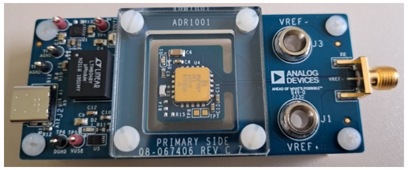



*SUBSTRATE DEVICES–DO NOT FORWARD BIAS




*SUBSTRATE TO NEPI DIODE.

NOTES
1. PIN 4 IS THE SUBSTRATE AND IS CONNECTED TO THE CASE.



# Other design aspects

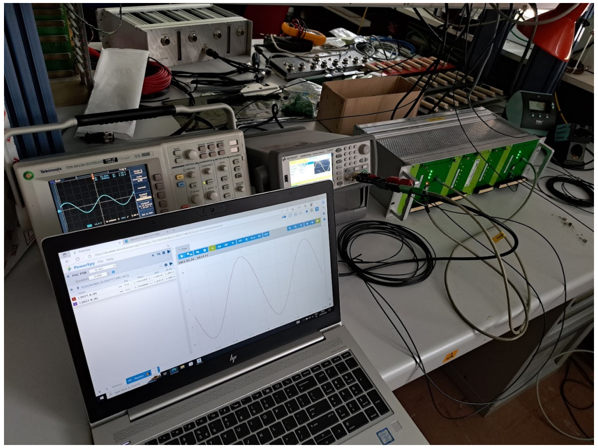
- Powering
  - Good filtering, multiple LDO-stabilized voltages
  - Separation of analog and digital supply rails
  - Additional local filtering on the ADC mezzanine
- Ground planes
  - Common ground planes on the mezzanine and on the mainboard
  - Functional layout separation into analog and digital areas
- Digital interfaces
  - Main ADC: SPI, converted to LVDS levels – to unload ADC digital outputs and to reduce parasitic coupling
  - Auxiliary ADC for T measurement: SPI (non-LVDS)
  - Test & debug: UART to USB using FT232, galvanic isolators
  - Fiber optic: UART @ 5 Mbit/s, IP reused from another project
  - Synchronization input – 10 kHz pulses, plastic optic fiber
  - Front panel LEDs – shift registers
  - Some simple control signals (MUX control, status flags, etc.)
  - 1-wire – for device identification and temperature monitoring

# Communication, integration, debug

- The crate with two HPM7177s interfaces to FGC using optical fibers
- **TX**: UART at 5 Mbit/s, reused from White Rabbit peripherals interface
- One data package sent per ADC sample (10 kSamples/s).
  In total 17 bytes per sample. Format:

| word #1 | word #2 | word #3 | word #4 | checksum |
|---|---|---|---|---|
| **ADC result** | **status** | **0** | **0** | **CRC** |
| 32 b | 32 b | 32 b | 32 b | 8 b |

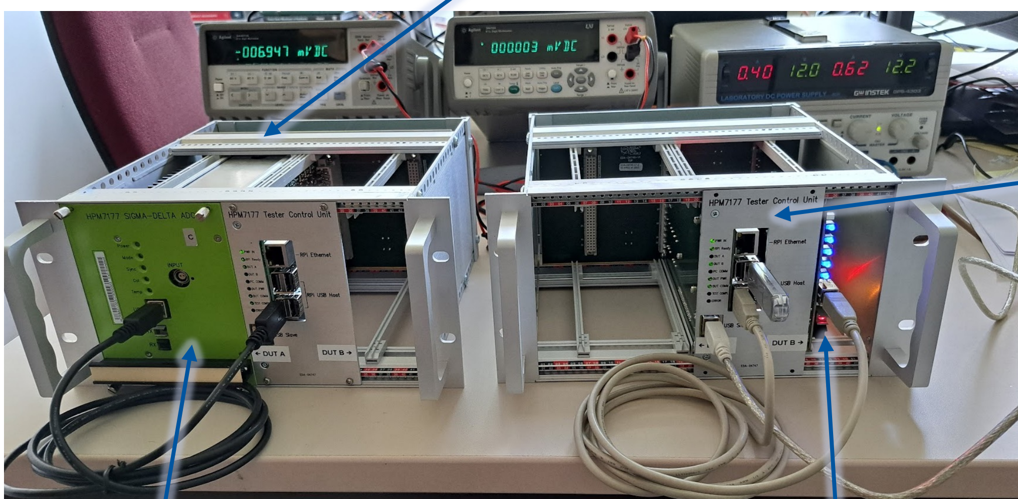
- Status word:
  - Status of ADC operation
  - Fault flags (ADC readout errors)
  - Synchronization - present or not
  - Status of temperature control loop, output of PI
- **RX**: 10 kHz synchronization pulses
- USB – extended debug information sent out once per second in text format

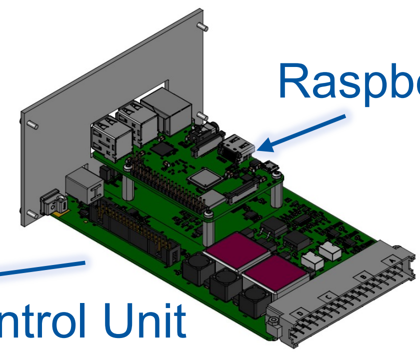


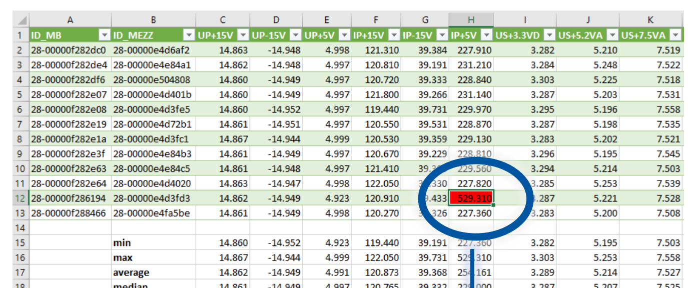
First demo of proper operation with FGC, ca May 2023

# Production testing

- Production tests (factory) and acceptance tests (CERN)
- Checks of basic functionality - voltages, currents, interfaces, sub-systems, etc. Estimated 95% coverage of hardware functions
- Also, basic precision check of mezzanine with external 10 V standard (at ~10s of ppm level, without T stabilization)



| | A | B | C | D | E | F | G | H | I | J | K |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ID_MB | ID_MEZZ | UP+15V | UP-15V | UP+5V | IP+15V | IP-15V | IP+5V | US+3.3VD | US+5.2VA | US+7.5VA |
| 2 | 28-00000f282dc0 | 28-00000e4d6af2 | 14.863 | -14.948 | 4.998 | 121.310 | 39.384 | 227.910 | 3.282 | 5.210 | 7.519 |
| 3 | 28-00000f282de4 | 28-00000e4e84a1 | 14.862 | -14.948 | 4.997 | 120.810 | 39.191 | 231.210 | 3.284 | 5.248 | 7.522 |
| 4 | 28-00000f282df6 | 28-00000e504808 | 14.860 | -14.949 | 4.997 | 120.720 | 39.333 | 228.840 | 3.303 | 5.225 | 7.518 |
| 5 | 28-00000f282e07 | 28-00000e4d401b | 14.860 | -14.949 | 4.997 | 121.800 | 39.266 | 231.140 | 3.287 | 5.203 | 7.531 |
| 6 | 28-00000f282e08 | 28-00000e4d3fe5 | 14.860 | -14.952 | 4.997 | 119.440 | 39.731 | 229.970 | 3.295 | 5.196 | 7.558 |
| 7 | 28-00000f282e19 | 28-00000e4d72b1 | 14.861 | -14.951 | 4.997 | 120.550 | 39.531 | 228.870 | 3.287 | 5.198 | 7.535 |
| 8 | 28-00000f282e1a | 28-00000e4d3fc1 | 14.867 | -14.944 | 4.999 | 120.530 | 39.359 | 229.130 | 3.283 | 5.202 | 7.521 |
| 9 | 28-00000f282e3f | 28-00000e4e84b3 | 14.861 | -14.949 | 4.997 | 120.670 | 39.229 | 228.810 | 3.296 | 5.195 | 7.545 |
| 10 | 28-00000f282e63 | 28-00000e4e84c5 | 14.861 | -14.948 | 4.997 | 121.410 | 39.3[illegible] | 229.560 | 3.294 | 5.214 | 7.503 |
| 11 | 28-00000f282e64 | 28-00000e4d4020 | 14.863 | -14.947 | 4.998 | 122.050 | [illegible].330 | 227.820 | 3.285 | 5.253 | 7.539 |
| 12 | 28-00000f286194 | 28-00000e4d3fd3 | 14.862 | -14.949 | 4.923 | 120.910 | [illegible].433 | 529.310 | [illegible].287 | 5.221 | 7.528 |
| 13 | 28-00000f288466 | 28-00000e4fa5be | 14.861 | -14.949 | 4.998 | 120.270 | [illegible].326 | 227.360 | [illegible].283 | 5.200 | 7.508 |
| 14 | | | | | | | | | | | |
| 15 | | **min** | 14.860 | -14.952 | 4.923 | 119.440 | 39.191 | 227.360 | 3.282 | 5.195 | 7.503 |
| 16 | | **max** | 14.867 | -14.944 | 4.999 | 122.050 | 39.731 | 529.310 | 3.303 | 5.253 | 7.558 |
| 17 | | **average** | 14.862 | -14.949 | 4.991 | 120.873 | 39.368 | 25[illegible].161 | 3.289 | 5.214 | 7.527 |
| 18 | | **median** | 14.861 | -14.949 | 4.997 | 120.765 | 39.332 | 22[illegible].000 | 3.287 | 5.207 | 7.525 |

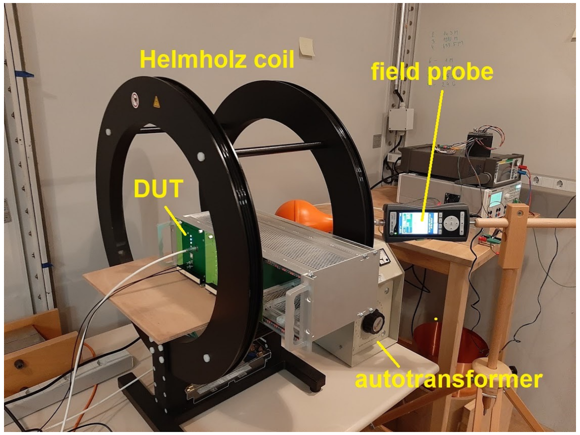
# EMC testing

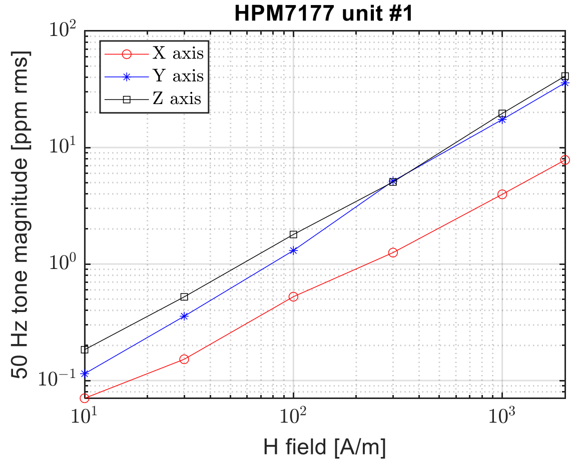
- As mentioned earlier, the EM environment can be a challenge
- Some typical EMC problems + common solutions:

| **Problem / offender** | **Solutions** |
|---|---|
| Magnetic fields | Keep loops small (internal / cables) |
| Ground loops | Floating PSU, differential transmission of signals, optical fibers |
| Electrical fast transients (burst) | Shielded cables, voltage clamps (TVS) |
| Susceptibility to conducted RF | Shielded cables, filtering, grounding |
| Susceptibility to radiated RF | Shielding, grounding |

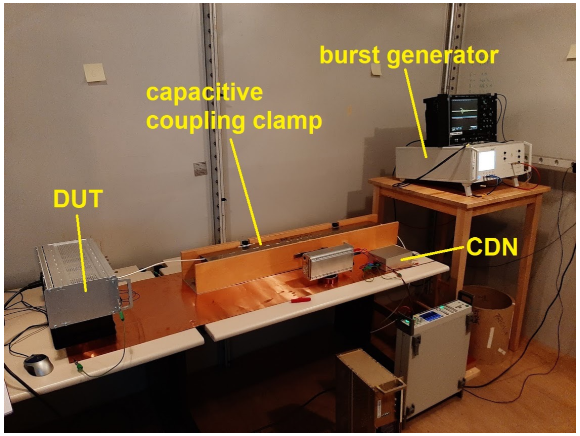
- Testing is indispensable for finding potential issues and solutions for them
- With high-precision devices, the aim is to ensure functionality and prevent permanent performance degradation related to EMI
- It is not realistic to maintain full DC accuracy during such aggressive tests
- Standards are a good starting point, but sometimes we have to go beyond

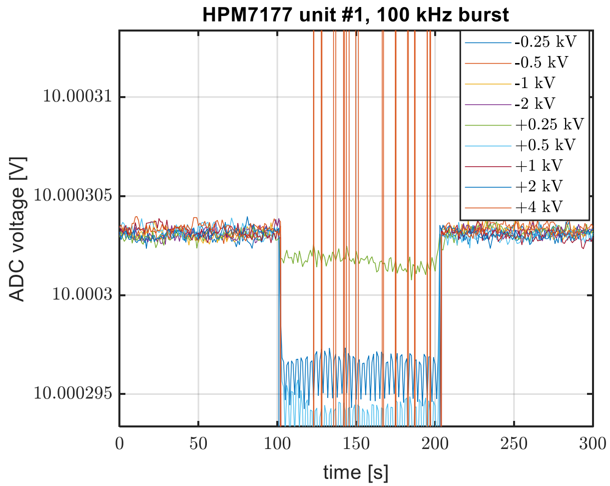
# EMC tests – LFMF and EFT

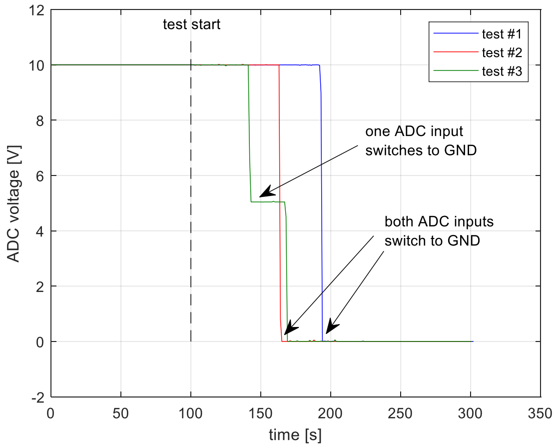



- No sensitivity to DC fields
- Low sensitivity at 50 Hz: max 35 ppm rms at 2000 A/m
- Not a very big dependence on orientation

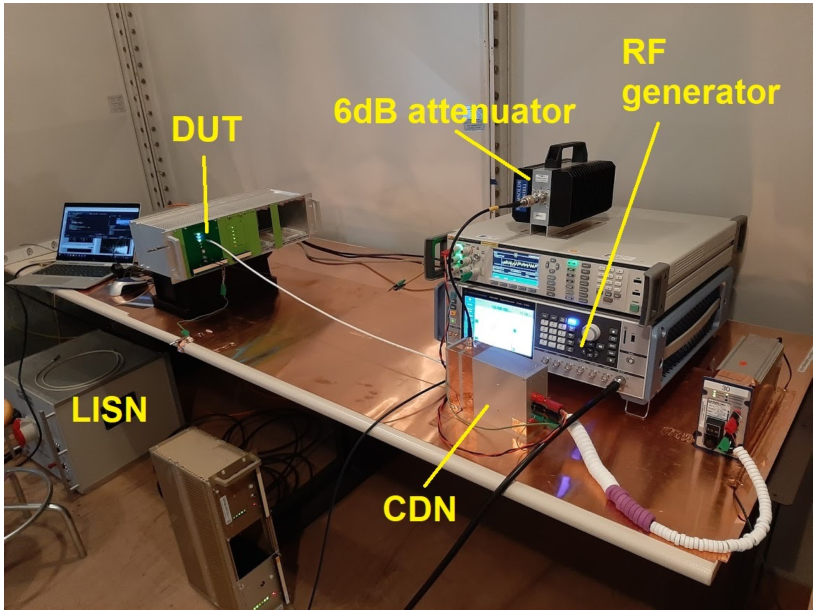


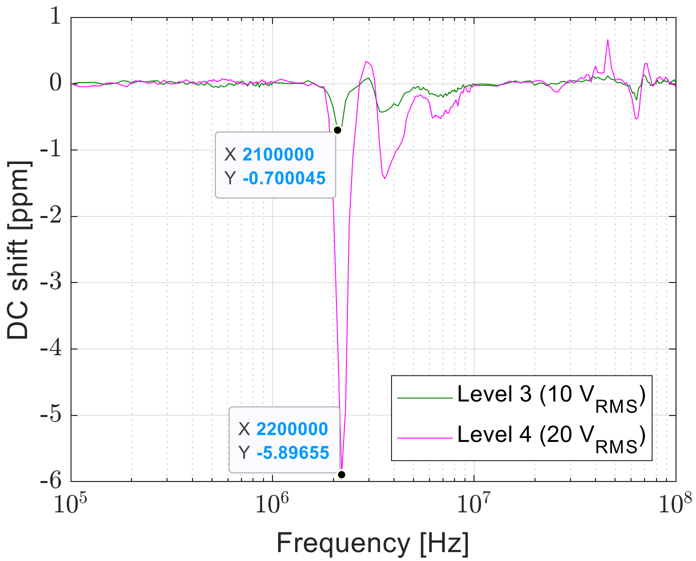



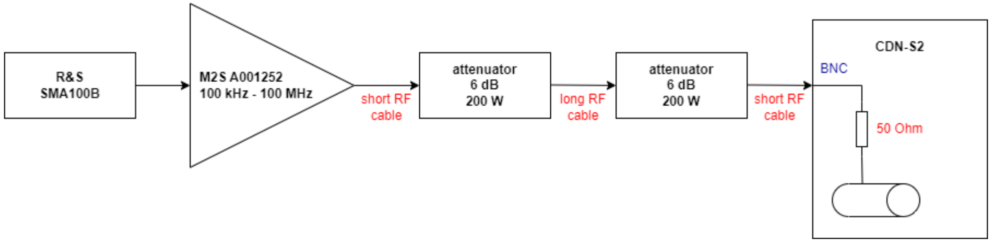



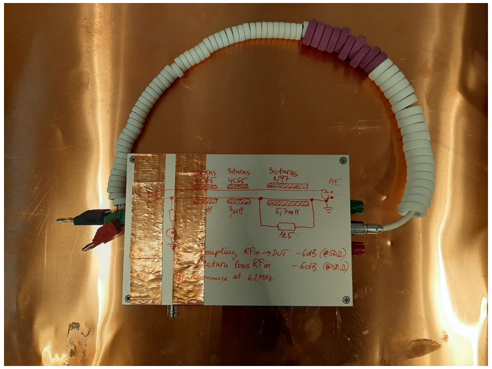

(reversible) fault at -4 kV → fixed in V3

# EMC tests – conducted RF



Difficult to achieve wide frequency span
with good flatness of RF power level!
Even more difficult to keep RF signals tame

# Summary: sources of error

| System | Element | Error sources | Mitigation solutions |
|---|---|---|---|
| **DCCT** | Head | External magnetic fields, return bar, centering | careful positioning |
| | Burden resistor | Settling, TC, PC, self-heating | TC compensation |
| | Precision amplifier | Offset / gain TC, noise, CMRR | auto-zero, CMRR trimming |
| **Digitizer** | ADC | Offset / gain TC, noise, non-linearity | auto-zero, active temperature stabilization, INL correction |
| | Frontend | Offset / gain TC, noise, CMRR | auto-zero, active temperature stabilization, CMRR trimming |
| | Voltage reference | TC, noise, aging | Auto-zero (for *Uref* scaling), active temperature stabilization, burn-in |
| **external** | cables | thermal EMFs | proper selection of cables and connectors |
| | cables | EMI | careful positioning, shielding, EMC-aware design |
| | environment | variations in temperature and humidity | active temperature stabilization |

systematic / random / mixed

# Measurement error strategy

- Main system-level goal: distribute the error, don't let any single source dominate
  - Ideal elements are not needed (remember the *chain*)
  - Statistics helps (remember the *central limit theorem*)
- Compensation/correction is only possible for known, systematic effects
- Testing is unavoidable and indispensable, especially to find subtle failure modes. Outliers are the first suspect.
- Specifically in our case:
  - the stability of the burden resistor is usually the performance bottleneck
  - providing a "better than expected" digitizer helps relieve the requirements for the DCCT, saving much effort and cost

# Error vs uncertainty

- **Measurement error -** the difference between a measured value of a quantity and its (generally unknown) true value
  - Systematic or random / static or dynamic / instrument or environment
- **Control error** – difference between the reference (setpoint) and the measured value
  - Goal of the controller – to minimize this error. It's usually negligible at DC
- **Measurement uncertainty** – an expression of **incomplete knowledge**
  *"non-negative parameter characterizing the dispersion of the quantity values being attributed to a measurand, based on the information used‘'*
  - Type A – based on statistical analysis of measurements
  - Type B – based on non-statistical methods (accuracy class, calibration certificate, prior knowledge)
- **In our context:**
  - Tests and characterization give the value of some performance parameter (e.g. noise or TC)
  - The uncertainty of this parameter is defined by the reference instruments (standards, DVMs, etc.), or the properties of the tested device, or both
  - The PC accuracy classes and ADC/DCCT guidelines are a broader target, but also a starting point for defining of strategies and drafting of specifications
  - We aim to guarantee that **all** devices of a given type fit into the target class, with a reasonable safety margin

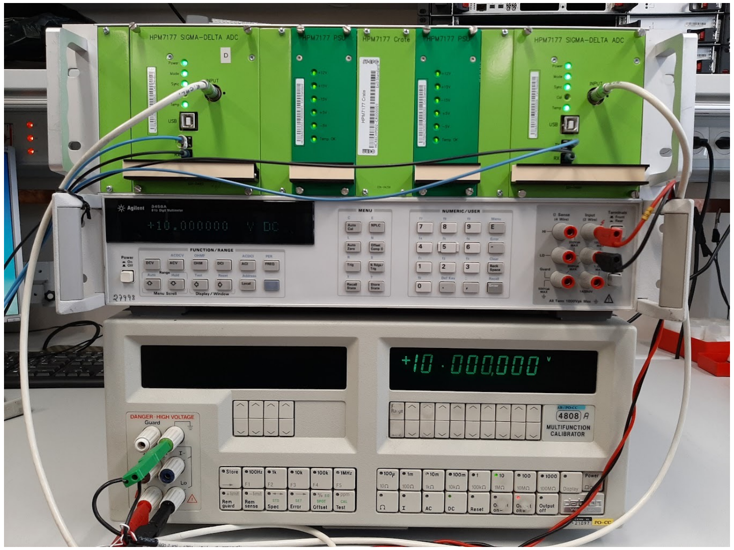
# Proving performance

*“Extraordinary claims require extraordinary evidence”*

Carl Sagan

# Limitations of classical equipment

- General principle: to characterize any device, *normally* you need another instrument with higher metrological performance
- e.g. voltage standard → DVM
- High-end DVMs and calibrators have certain limitations:
  - ➢ Trade-offs of performance vs flexibility
  - ➢ Different accuracy for different functions and ranges *(there is a "golden mean" / best range)*
  - ➢ Impact of usage history, power cycling, etc.
- Classical voltage standards are based on buried Zener references, thus:
  - ➢ They have non-negligible noise, especially *1/f*
  - ➢ They also drift - with time, temperature, stress / power cycling, etc. *(even atmospheric pressure!)*




- What if you don't have an instrument with significantly higher performance than your DUT? Do you just accept the high uncertainty?

# DVM best specifications

- HP/Agilent/Keysight 3458A (1988)


**Accuracy**[3] [ppm of reading (ppm of reading for Option 002) + ppm of range]

| Range | 24 hour[4] | 90 day[5] | 1 year[5] | 2 year[5] |
|---|---|---|---|---|
| 100 mV | 2.5 + 3 | 5.0 (3.5) + 3 | 9 (5) + 3 | 14 (10) + 3 |
| 1 V | 1.5 + 0.3 | 4.6 (3.1) + 0.3 | 8 (4) + 0.3 | 14 (10) + 0.3 |
| 10 V | 0.5 + 0.05 | 4.1 (2.6) + 0.05 | 8 (4) + 0.05 | 14 (10) + 0.05 |
| 100 V | 2.5 + 0.3 | 6.0 (4.5) + 0.3 | 10 (6) + 0.3 | 14 (10) + 0.3 |
| 1000 V[6] | 2.5 + 0.1 | 6.0 (4.5) + 0.1 | 10 (6) + 0.1 | 14 (10) + 0.1 |

**Transfer accuracy/linearity**

| Range | 10 min, Tref ± 0.5 °C (ppm of reading + ppm of range) |
|---|---|
| 100 mV | 0.5 + 0.5 |
| 1 V | 0.3 + 0.1 |
| 10 V | 0.05 + 0.05 |
| 100 V | 0.5 + 0.1 |
| 1000 V | 1.5 + 0.05 |

Conditions
- Following 4-hour warm-up. Full scale to 10% of full scale.
- Measurements on the 1000 V range are within 5% of the initial measurement value and following measurement settling.
- Tref is the starting ambient temperature.
- Measurements are made on a fixed range (> 4 min.) using accepted metrology practices.

- Fluke 8588A (2019)


95 % Confidence

| Range | Zin | Full Scale | Relative Accuracy ± (µV/V of reading + µV/V of range): Transfer, 20 min [15] | Relative Accuracy: 24 Hour Tcal ± 1 °C | Relative Accuracy: 90 day Tcal ± 1 °C | Relative Accuracy: 365 day Tcal ± 1 °C | Relative Accuracy: 2 years Tcal ± 1 °C | Absolute Accuracy: 365 day Tcal ± 1 °C | Absolute Accuracy: 365 day Tcal ± 5 °C | Absolute Accuracy: 2 year Tcal ± 5 °C |
|---|---|---|---|---|---|---|---|---|---|---|
| 100 mV | Auto, 10 MΩ, 1 MΩ | 202.000 000 mv | 0.2 + 2.0 | 0.7 + 2.0 | 1.4 + 2.0 | 2.7 + 2.0 | 5.4 + 2.0 | 5.1 + 2.0 | 7.5 + 2.0 | 15 + 2.0 |
| 1 V | Auto, 10 MΩ, 1 MΩ | 2.02 000 00 mv | 0.06 + 0.3 | 0.5 + 0.3 | 1.4 + 0.3 | 2.7 + 0.3 | 5.4 + 0.3 | 2.8 + 0.3 | 2.9 + 0.3 | 5.8 + 0.3 |
| 10 V | Auto, 10 MΩ, 1 MΩ | 20.200 000 0 V | 0.05 + 0.05 | 0.5 + 0.05 | 1.4 + 0.05 | 2.7 + 0.05 | 5.4 + 0.05 | 2.8 + 0.05 | 2.9 + 0.05 | 5.8 + 0.05 |
| 100 V | Auto, 10 MΩ | 202.000 000 V | 0.4 + 0.3 | 1.0 + 0.3 | 2.6 + 0.3 | 4.0 + 0.3 | 8.0 + 0.3 | 4.1 + 0.3 | 4.3 + 0.3 | 8.5 + 0.3 |
| 100 V | 1 MΩ | 202.000 000 V | 2.0 + 5.0 | 2.0 + 5.0 | 4.5 + 5.0 | 9.0 + 5.0 | 18 + 5.0 | 9.0 + 5.0 | 9.5 + 5.0 | 19 + 5.0 |
| 1000 V | Auto, 10 MΩ | 1050.000 00 V | 0.4 + 0.5 | 1.0 + 0.5 | 2.6 + 0.5 | 4.0 + 0.5 | 8.0 + 0.5 | 4.3 + 0.5 | 4.4 + 0.5 | 8.9 + 0.5 |
| 1000 V | 1 MΩ | 1050.000 00 V | 4.0 + 25 | 4.0 + 25 | 4.5 + 25 | 9.0 + 25 | 18 + 25 | 9.1 + 25 | 9.6 + 25 | 19.2 + 25 |

Not surprisingly, 10 V range is the “golden mean”

# Calibrators, voltage standards

## Fluke 5700A Series II (1995)

**5720A/5700A Series II secondary performance specifications and operating characteristics**

| Range | Stability[1] ±1°C 24 Hours | Temperature coefficient[2] 10°C-40°C | 0°C-10°C 40°C-50°C | Linearity ± 1°C | Noise bandwidth 0.1-10 Hz pk-pk | 10-10 kHz rms |
|---|---|---|---|---|---|---|
| | ± (ppm output + µV) | ± (ppm output + µV)/°C | | ± (ppm output + µV) | | µV |
| 220 mV | 0.3 + 0.3 | 0.4 + 0.1 | 1.5 + 0.5 | 1 + 0.2 | 0.15 + .1 | 5 |
| 2.2V | 0.3 + 1 | 0.3 + 0.1 | 1.5 + 2 | 1 + 0.6 | 0.15 + .4 | 15 |
| 11V | 0.3 + 2.5 | 0.15 + 0.2 | 1 + 1.5 | 0.3 + 2 | 0.15 + 2 | 50 |
| 22V | 0.4 + 5 | 0.2 + 0.4 | 1.5 + 3 | 0.3 + 4 | 0.15 + 4 | 50 |
| 220V | 0.5 + 40 | 0.3 + 5 | 1.5 + 40 | 1 + 40 | 0.15 + 60 | 150 |
| 1100V | 0.5 + 200 | 0.5 + 10 | 3 + 200 | 1 + 200 | 0.15 + 300 | 500 |

[1] Stability specifications are included in the absolute uncertainty values in the primary specification tables.
[2] Temperature coefficient is an adder to uncertainty specifications that does not apply unless operating more than ±5°C from calibration temperature.

## Datron/Wavetek 4808 (early 90s)

**Option 10 - DC Voltage** (Requires Option 30 for 1000V Range)

| Voltage Range | Accuracy Relative to Calibration Standards ± (ppm OUTPUT + Floor) [1] 24 Hours Stability [2] | 90 Days Tcert [3] ± 1°C | 180 Days Tcert [3] ± 5°C | 1Year Tcert [3] ± 5°C | Calibration Uncertainty (±ppm Output) | Temperature Coefficient (±ppm/°C) |
|---|---|---|---|---|---|---|
| 100µV | 0.4 + 0.3µV | 3 + 0.4µV | 4.5 + 0.5µV | 7 + 0.5µV | 6 | 1 |
| 1mV | 0.4 + 0.3µV | 3 + 0.4µV | 4.5 + 0.5µV | 7 + 0.5µV | 6 | 1 |
| 10mV | 0.4 + 0.3µV | 3 + 0.4µV | 4.5 + 0.5µV | 7 + 0.5µV | 6 | 1 |
| 100mV | 0.4 + 0.3µV | 3 + 0.4µV | 4.5 + 0.5µV | 7 + 0.5µV | 6 | 1 |
| 1V | 0.3 + 0.5µV | 2 + 0.8µV | 3.5 + 1µV | 5 + 1µV | 3.2 | 0.5 |
| 10V | 0.3 + 1µV | 1 + 3µV | 2 + 3µV | 3 + 3µV | 2.4 | 0.15 |
| 100V | 0.5 + 20µV | 2 + 50µV | 3.5 + 50µV | 5 + 50µV | 3.3 | 0.5 |
| 1000V | 0.5 + 200µV | 3 + 500µV | 5 + 500µV | 7 + 500µV | 3.3 | 0.5 |

## Fluke 732A (early 1980s)

**Table 1-2. 732A Specifications**

OUTPUT VOLTAGE .................... 10 volts, 1.018 volts, or 1 volt

TRANSFER UNCERTAINTY ............ @18°C to 28°C

| Output Voltage | Time Interval 30 Days | 90 Days | 6 Months | 1 Year |
|---|---|---|---|---|
| 10V | 0.5 ppm | 1.5 ppm | 3.0 ppm | 6.0 ppm |
| 1.018V | 1.5 ppm | 4.0 ppm | 8.0 ppm | 12.0 ppm |
| 1V | 1.5 ppm | 4.0 ppm | 8.0 ppm | 12.0 ppm |

These specifications assume the unit has been continuously powered up with either ac or battery or both. The specifications include effects due to line regulation.

TEMPERATURE COEFFICIENT OF OUTPUT

| Range | Temperature Coefficient (ppm/°C) 0°C to 18°C | 28°C to 40°C |
|---|---|---|
| 10V | ±0.05 | ±0.05 |
| 1.018V | ±1.0 | ±1.0 |
| 1V | ±1.0 | ±1.0 |

## Fluke 732C (2018)

**Standard stability**

| Output voltage | Stability (± µV/V) 30 days | 90 days | 1 Year |
|---|---|---|---|
| 10 V | 0.3 | 0.8 | 2.0 |
| 1 V | 0.6 | 1.2 | 3.0 |
| 0.1 V | 1.2 | 2.9 | 9.8 |

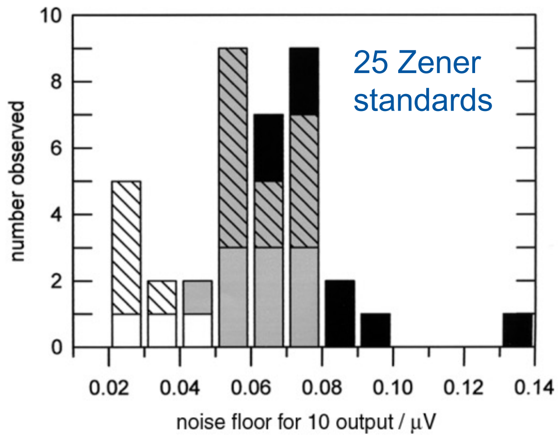
**Temperature Coefficient (TC) of Output**

From 15 °C to 35 °C, the temperature coefficient is bound by the information in the table below.

| Output voltage | Temperature Coefficient (± µV/V per °C) |
|---|---|
| 10 V | 0.04 |
| 1 V | 0.1 |
| 0.1 V | 0.2 |

# More on limitations

- For linearity tests, DVMs are perfectly good for our purposes (0.1 ppm on 10 V range). They are also better than calibrators
- All devices that use buried Zener voltage references *(i.e. all classical voltage metrology instruments)* are limited by the *1/f* noise of the reference
  - It varies between types, and also between units
  - Generally, in the range of 0.02-0.2 ppm rms
  - Taking longer measurements doesn't improve Type A uncertainty
  - Cannot be mitigated with reversals, because it's a gain error



From [13]

- Long-term stability of Zener standards is good enough for our purposes, especially for frequently calibrated, well managed reference devices

# Going beyond the specs – how?

- Improve the local environment
  - use a climatic chamber (reduce $\Delta T$)
  - use Faraday cage, special cables, etc.
  - don't stack many instruments, keep offenders away
- Use more measurement / reference devices (statistics!)
  - Works for random errors, e.g. noise
  - Becomes less effective when correlations are present (e.g. similar TC x $\Delta T$)
- Correct or compensate for known effects
  - Characterize your test equipment, count on the stability of some characteristics (e.g. TC)
  - Measure and track environmental variables, use for correction
  - "educated" Type B uncertainty vs manufacturer datasheet specs
- Arrange reversals or auto-zeroing
  - Not just DVM auto-zero; better somewhere early in the measurement chain
  - Works for offset errors (offset drift, EMFs, zero noise), but not for gain or linearity errors
- Exploit advanced measurement and signal processing methods
  - repeated measurements with ensemble averaging
  - cross-correlation, cross-spectrum, etc.

# Example: cross-PSD

- *When measuring noise, how do you call the "signal-to-noise ratio" (SNR)?*

*hay in a haystack*

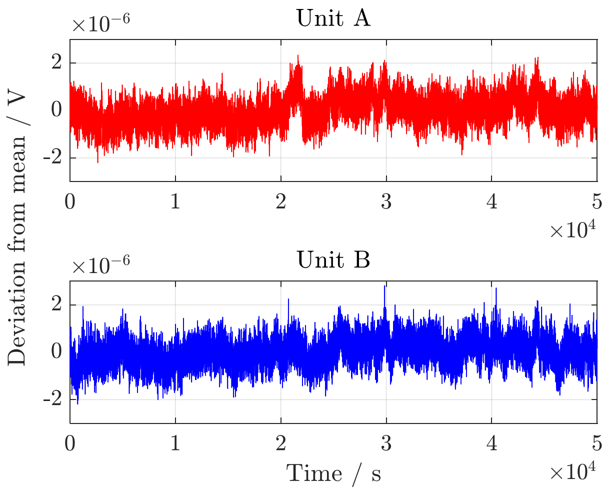
- indistinguishable, but has different sources
- *"noise signal"* could be below the *"measurement noise"*

- The idea: use two identical devices to measure the same *noise signal*
- Each of the two has its own noise, which contributes to the measurement
- Part of the measurement is coherent (common for the two), because it comes from the input signal
- This part can be estimated using cross power-spectrum density
  - PSD is the Fourier transform of the autocorrelation function
  - CPSD is the Fourier transform of the cross-correlation function

$$\underbrace{S_X(f)}_{\text{PSD}} = \int_{-\infty}^{+\infty} \underbrace{R_X(\tau)}_{\text{autocorrelation}} e^{-i\pi f\tau} d\tau \qquad \underbrace{S_{XY}(f)}_{\text{CPSD}} = \int_{-\infty}^{+\infty} \underbrace{R_{XY}(\tau)}_{\text{cross-correlation}} e^{-i\pi f\tau} d\tau$$

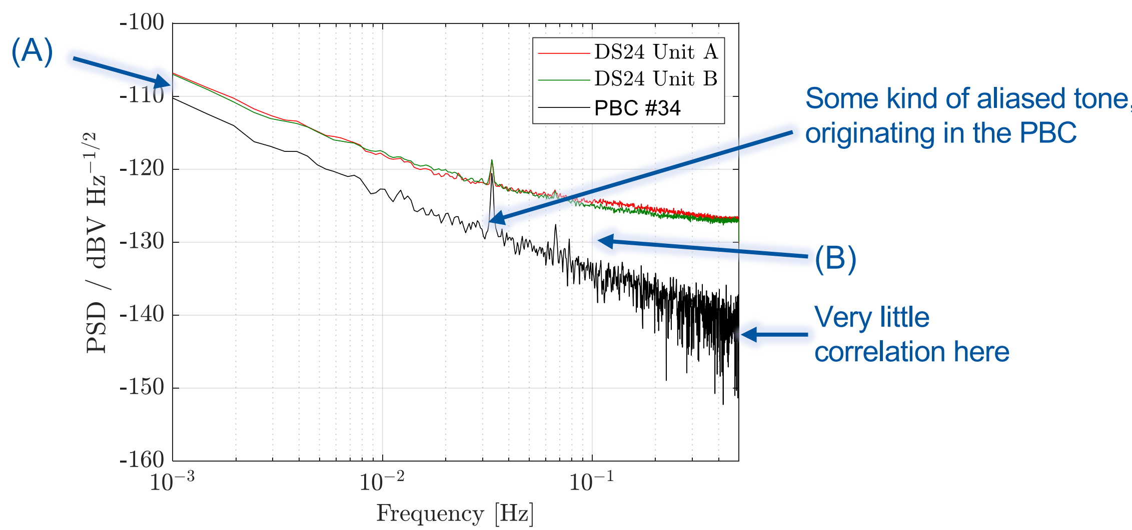
# Example: cross-PSD

- Example from DS24 testing
- The measurements contain noise both from the DUTs and from the 10 V source (PBC)
- The same PSD processing (Welch method, 2000-point Hanning window)
  - At 0.001 Hz – the estimated PBC noise is ≈3 dB below DUTs (A)
  - At >0.1 Hz it's >10 dB below → more uncertain CPSD estimate (B)
- Generally, works well for resolving up to 10 dB below the instrument noise floor, also for finding correlated artifacts. (But be careful when connected instrument inputs in parallel!)
- Long records (lots of averaging) needed for smooth plots and good frequency resolution




(part of the full record)

**Do you see any correlation?**



# Example: tests of upgraded CDC

- The challenge: verify 12-hour stability of 5 A within 0.2 ppm p-p
- The only feasible way: convert 5 A to 10 V (best effort), measure 10 V (best effort) – either against a 10 V standard, or using super stable digitizer(s)
- *In practice: use the whole bag of tricks*

DUT

50 mA current reference 5x PBCs

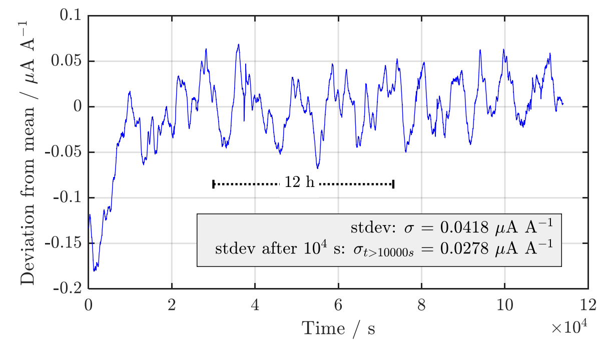
6x HPM7177

Current reversal H-bridge

Climatic chamber

0.2 Ω precision resistor

G=10 precision amplifier



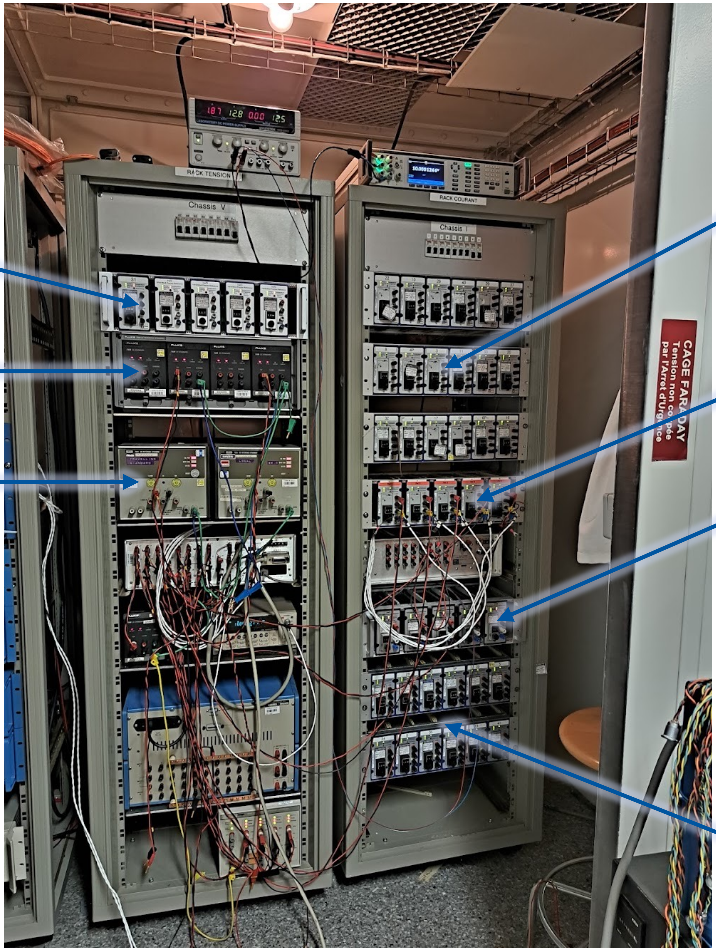

More information in Valerio Nappi's MSc thesis [14] *(also at CPEM-2024)*

# Voltage calibration infrastructure at CERN

New PBCs

Fluke 732B

Fluke 732A




regular PBCs

"reference PBCs"

New PBCs
(ADR1000-based)

*Less noisy than 732A/B/C*
*Hardware average of 5 units:*
*the quietest 10 V we have*

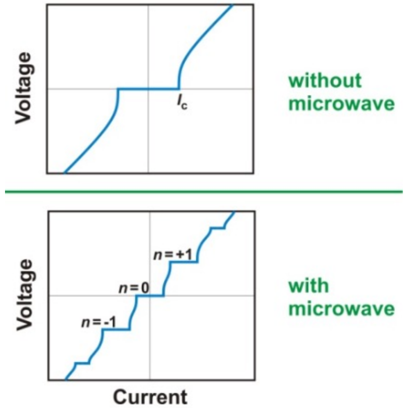
*(submitted to CPEM-2024)*

regular PBCs

**Typical uncertainty for absolute 10 V in the lab: ± 0.3 ppm Traceable to METAS**

# Voltage quantum metrology

- The Josephson effect – predicted theoretically by Brian Josephson in 1962, physics Nobel prize awarded in 1973
- Applications of Josephson junctions:
  - Superconducting Quantum Interference Devices (SQUID)
  - Single-electron transistors
  - Rapid Single Flux Quantum device (RSFQ)
  - Superconducing Tunnel Junction (STJ) detectors
  - Flux qubits (quantum computing)
  - **Josephson voltage standards**




- AC Josephson effect: irradiation with microwave (GHz) → quantized voltage steps (Shapiro steps)
- Basically, a *f* → U converter. Good frequency references are common
- One junction:

$$U = \frac{nf}{K_J}$$

$$K_J = \frac{2e}{h} = 483597.8484\ldots \times 10^9\ Hz\ V^{-1}$$ - Josephson constant (**exact since 2019**)

($f$ = 70 GHz, n = +1 → $U$ = 144.7483693… µV)

- Many junctions in series:

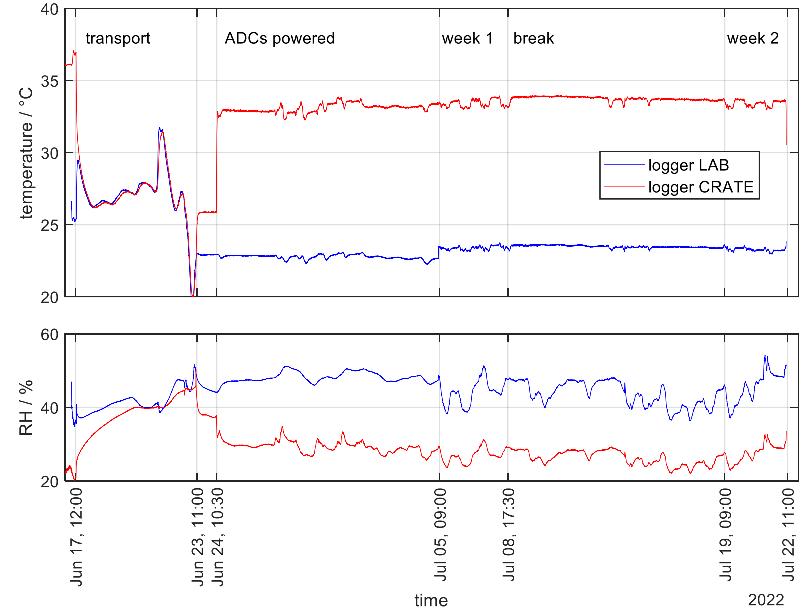
$$U(M) = \frac{nMf}{K_J}$$

($f$ = 70 GHz, n = +1, M = 6909 → $U$ = 1.0000664842… V)

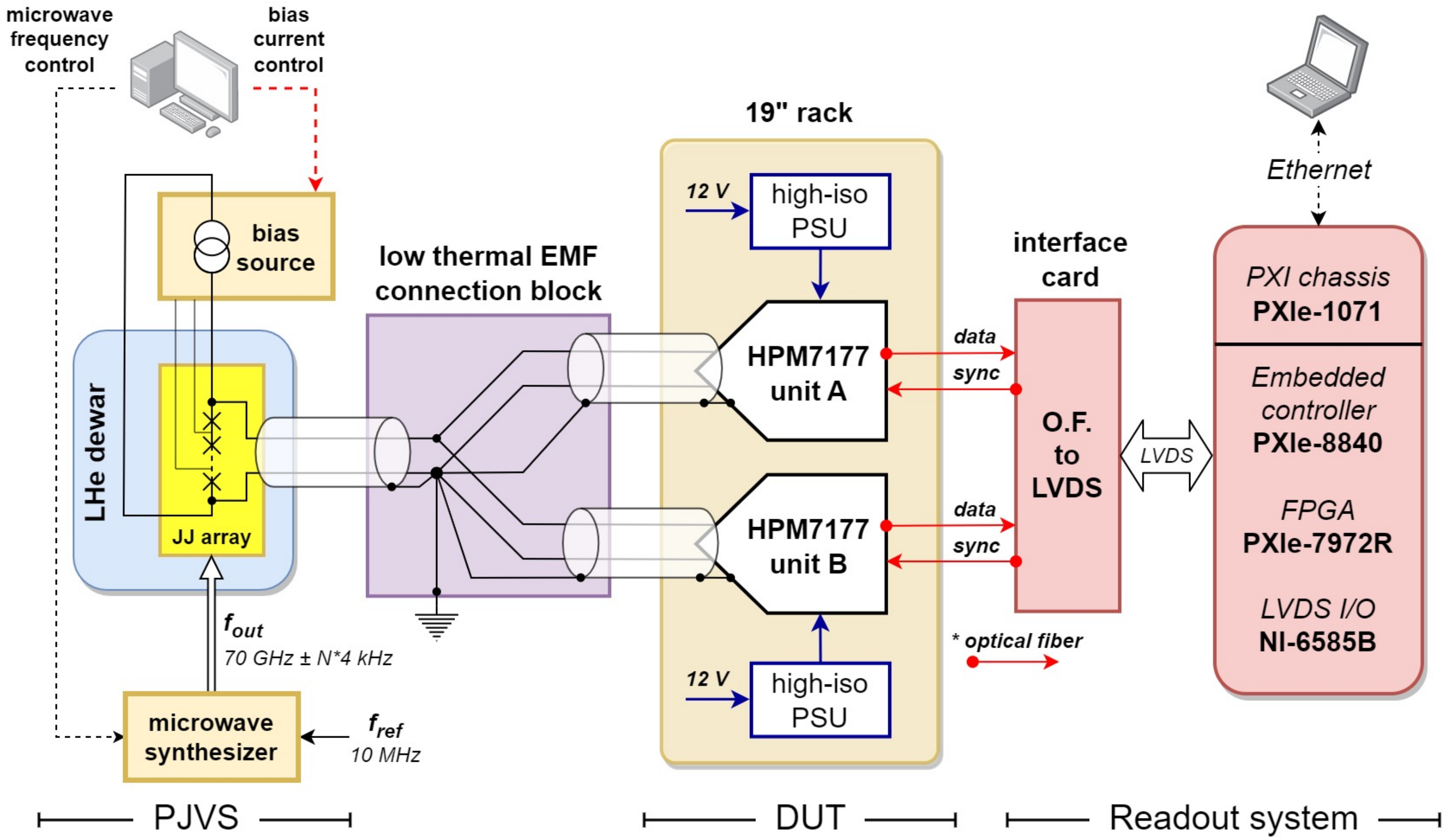
- The most stable and **fundamentally accurate** voltage source that exists
- Adopted as standard of voltage in 1972, becoming the first quantum electrical standard
- Since the 2019 redefinition of SI base units, $K_J$ has an exact value (no uncertainty)

# PJVS tests of HPM7177

- PJVS – Programmable Josephson Voltage Standard
  - Range: ±10 V
  - Flexible operation
  - Extremely low noise (practically negligible)
  - DC stability limited by thermal EMFs in cables
- Tests conducted at PTB – Braunschweig in 2022
- Very stable environmental conditions
  *(despite the unusually hot summer!)*
- Two HPM7177 units tested: the first V2 prototypes (ADR1000-based $U_{ref}$)
- In total ≈3 weeks (July 05 – July 22)
  - Most tests were carried out in week 1
  - Stability test: >10 days during break
  - Extra tests in the “safety margin” week 2
- DUTs were powered for ≈20 days prior to the tests
- Results published in IEEE Transactions on Instrumentation and Measurement [15] (open access)




# PJVS test setup – block diagram



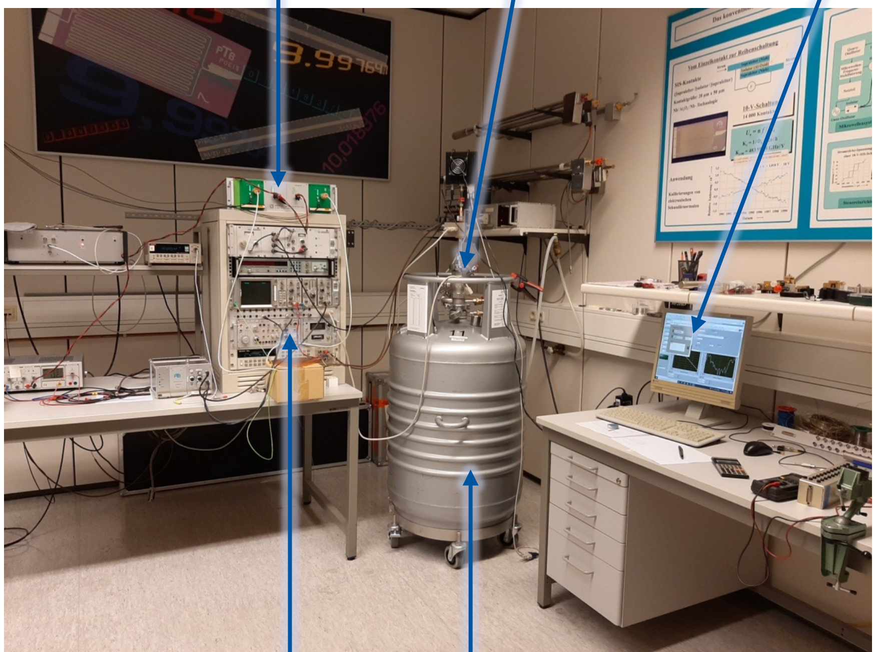
# PJVS setup - pictures

DUT

cryoprobe

PJVS control

T / RH loggers



PJVS bias source

LHe dewar

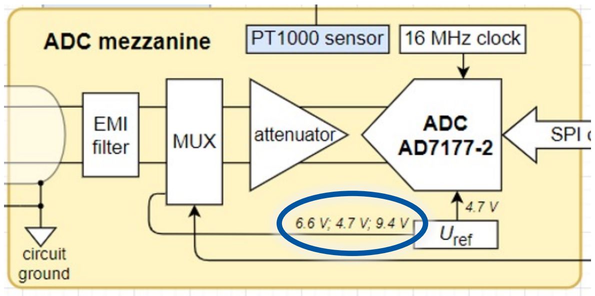
POF to LVDS

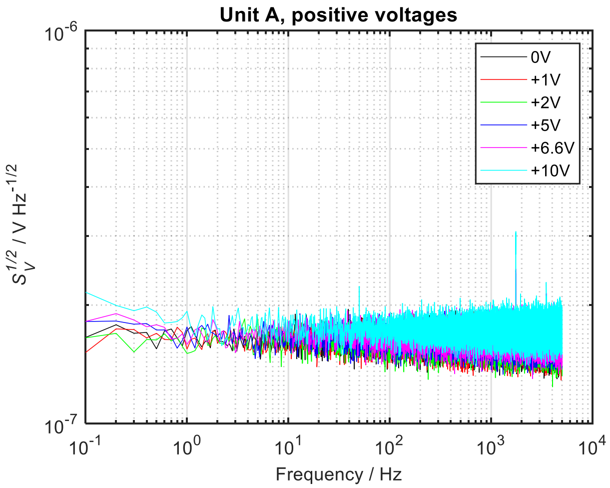
NI PXIe FPGA

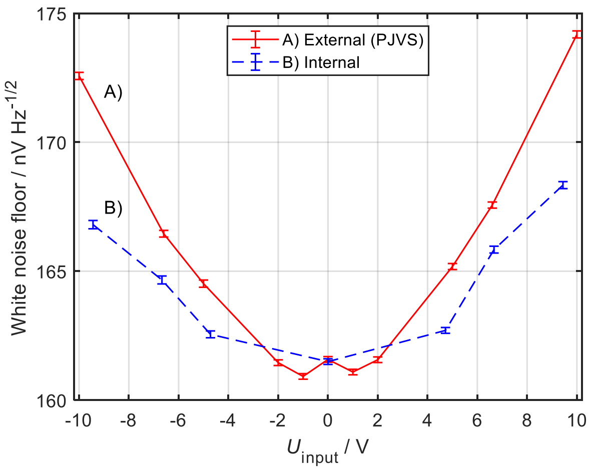
LabVIEW software

# Broadband noise

| Approximate voltage [V] | Actual voltage [V] | Number of JJs |
|---|---|---|
| 1 | 1.0000664842 | 6909 |
| 2 | 1.9999882200 | 13817 |
| 5 | 5.0000429241 | 34544 |
| 6.6 | 6.5999466510 | 45597 |
| 10 | 9.9999410998 | 69085 |



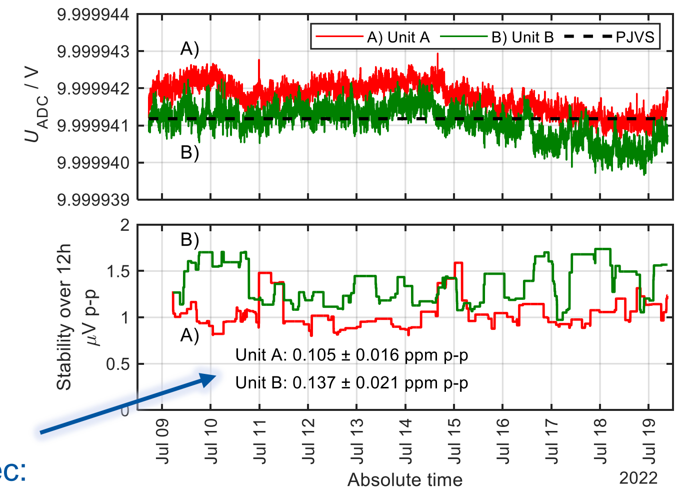



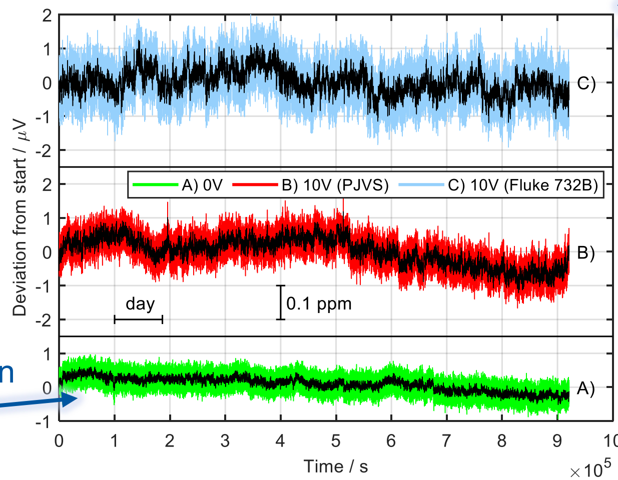

Slightly higher noise floor with higher input voltages

Test with internal voltages: suppression of correlated noise originating from *Uref*

# Low-frequency noise, stability

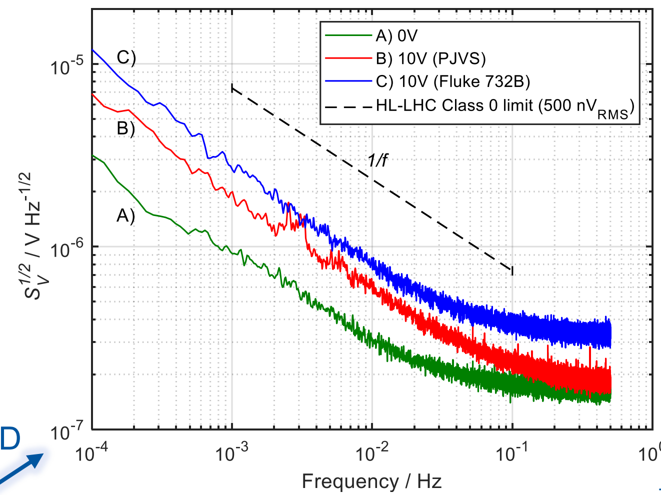



Toughest HL-LHC spec: 0.2 ppm in 12 h

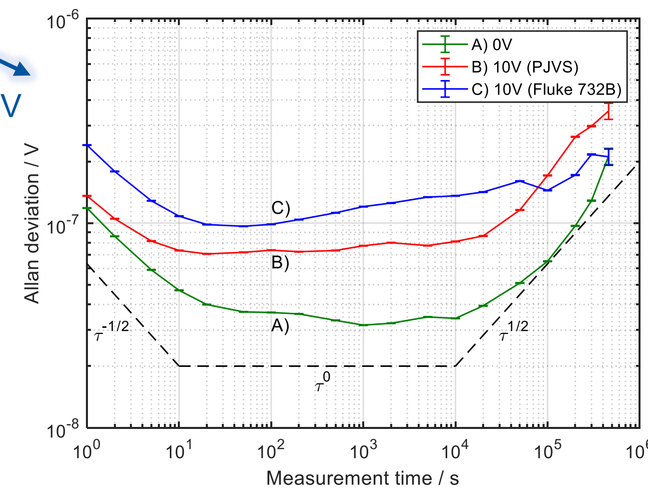



0 V: no contribution from Uref

PSD




ADEV

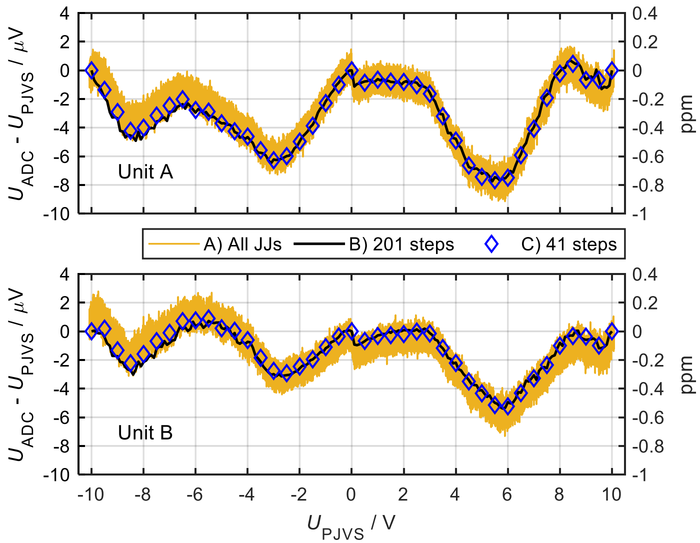



≈3 dB difference between 732B and PJVS @ 10V

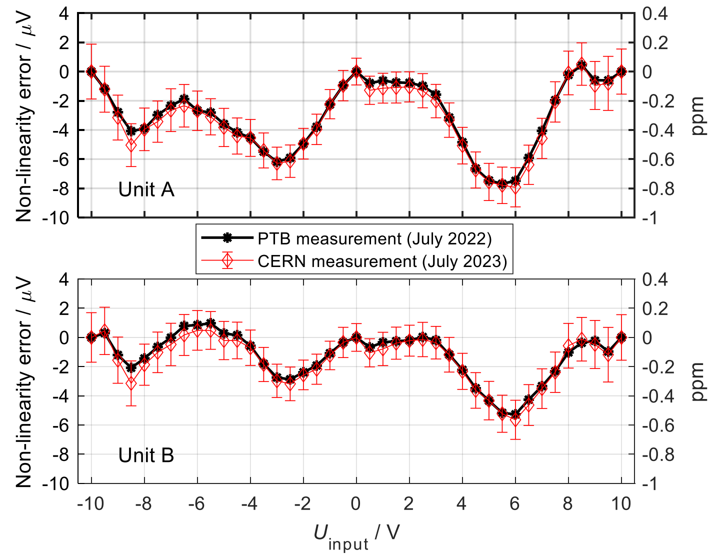
→ at 10 V HPM7177 has equal level of 1/f noise as the 732B

# Linearity

- Measured with different ramps from -10 V to +10 V
  *(plus ramps around 0 V to study the zero-transition kink)*
- Three-point calibration – at -10 V, 0 V, +10 V
- Longer dwell time → lower Type A uncertainty of the mean level at each step
- Measurement of the same units one year later at CERN using classical equipment (PWM-based voltage calibrator + 5 DVMs)



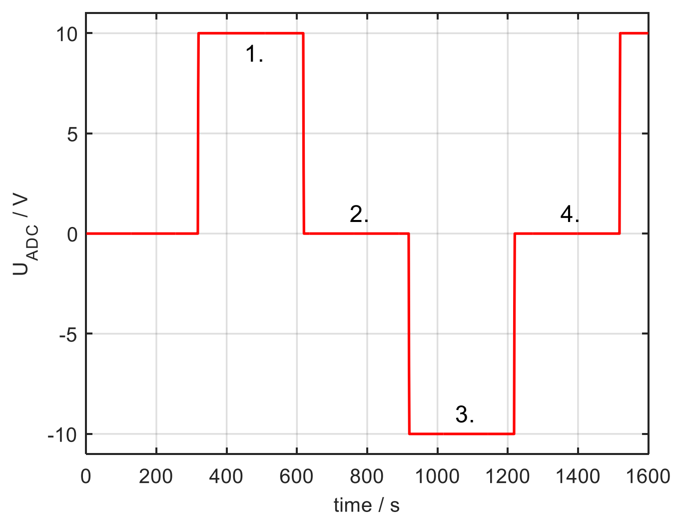

| Plot | Number of steps | Step magnitude (V) | Step dwell time (s) | Uncertainty ($\mu$V) |
|---|---|---|---|---|
| A) | 139265 | $\approx 145 \times 10^{-6}$ | 0.1 | 1.21 |
| B) | 201 | 0.1 | 10 | 0.12 |
| C) | 41 | 0.5 | 100 | 0.04 |

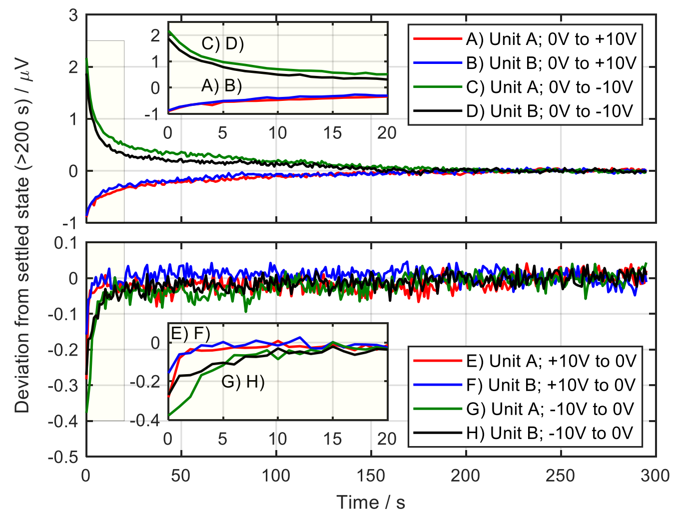



*Very small change,*
*within the limits of uncertainty*

# Settling to large steps

- Three levels: -10 V, 0 V, +10 V. Large positive and negative steps, return to 0
- Dwell time: 300 s on each step. Many cycles repeated overnight
- Ensemble averaging reduces noise by $\sqrt{N}$
- Earlier tests with the built-in MUX showed similar behaviour:
  Predominant gain settling, ≈ 0.1 - 0.2 ppm in 10-30 seconds, higher for ↓ steps
- Tests with PJVS are more conclusive, because they exclude the MUX, and because the voltage steps are not associated with changes in source impedance



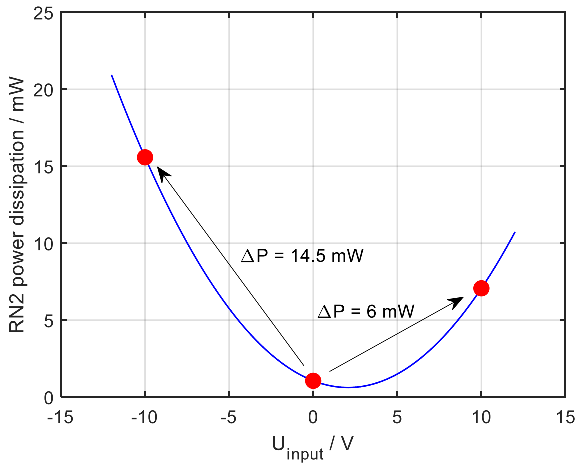
# Large steps – thermal response

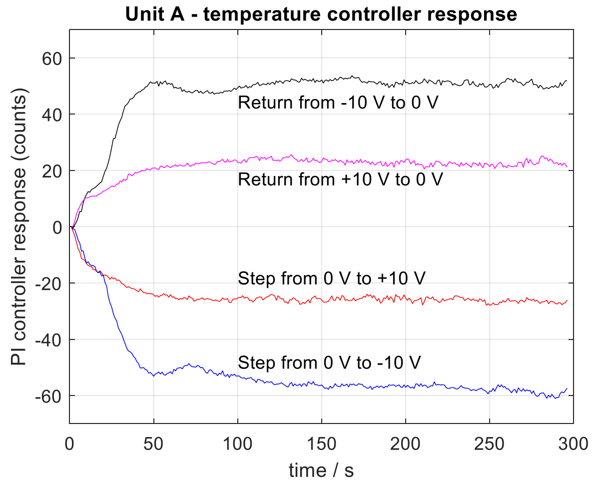
- The ADC mezzanine dissipates ≈ 1 W
- There is a small dependence on the input signal (worst-case ΔP ≈ 1.5 %)
- Mostly due to Joule heating in the resistor network RN2 (input signal path)
- When there is a large step in the input signal, the response of the temperature stabilization loop can be seen

  ***increase** in self-heating →*

  ***less heating** from the Peltier element*

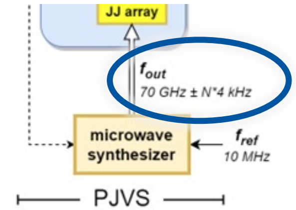
ΔT (ambient) = +1°C → -720 counts (measured)
ΔP (self-heating) = +14.5 mW → -60 counts
=> ΔT (self-heating) = 0.083 °C *(worst-case)*
*Rth* = 5.75 °C/W - consistent with other tests



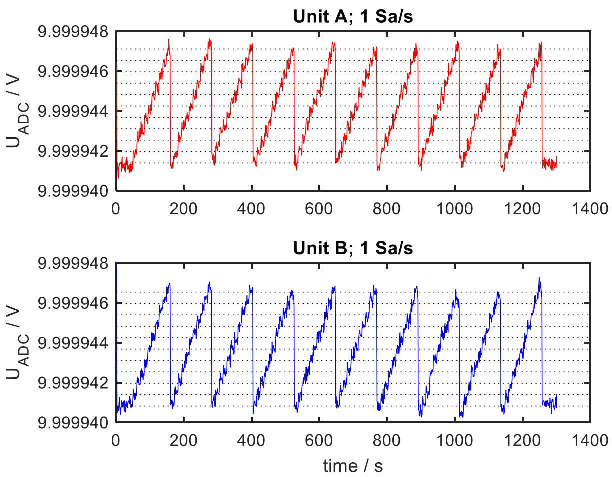



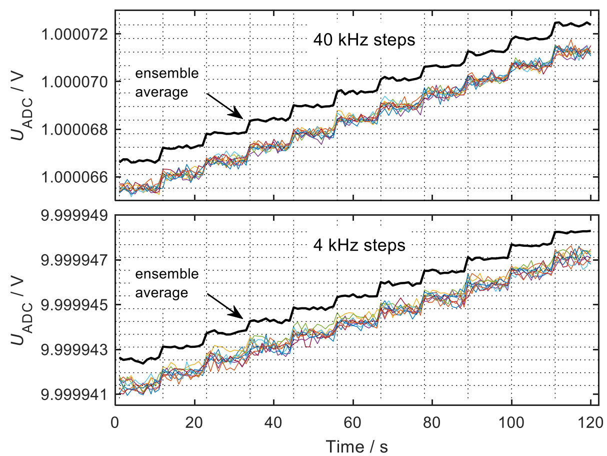
# Resolving of very small steps

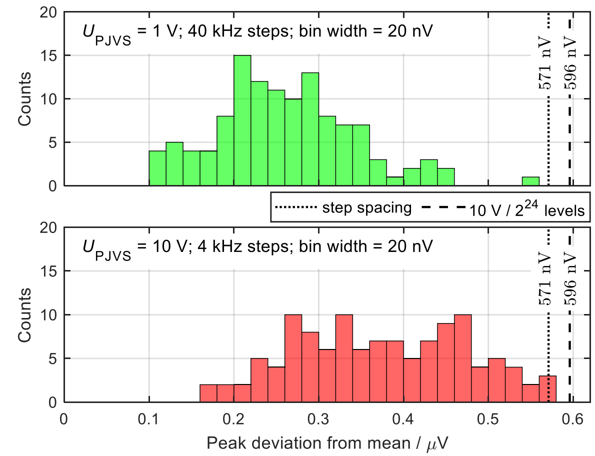
- The PJVS-generated voltage can be fine-stepped by modulating the 70 GHz microwave reference
- Resolution: 4 kHz -> 8.27 pV / Josephson junction
- At 10 V: 69085 JJs → 571 nV
- At 1 V: 6909 JJs → 57.1 nV – too small. 40 kHz steps used instead
- Repeated ramps (10x, 11 seconds per step)
- HPM7177 output data downsampled to 1 Sa/s (10000:1)
- peak-to-peak noise on steps ≈ step spacing
- Noise-Free Codes Resolution **≈ 24 bits** (of ±10 V range)




$$NFCR\,[bits] = log_2\left(\frac{V_{FS(p-p)}}{V_{excess\,noise(p-p)}}\right)$$

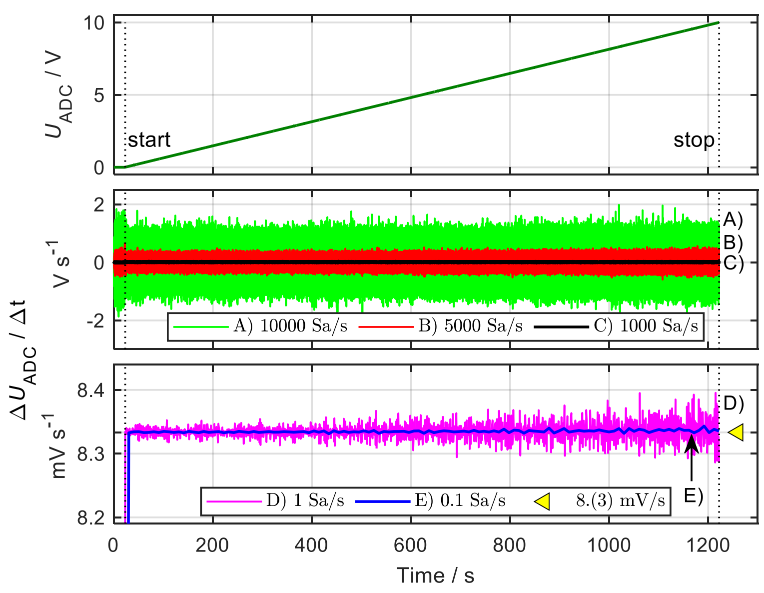


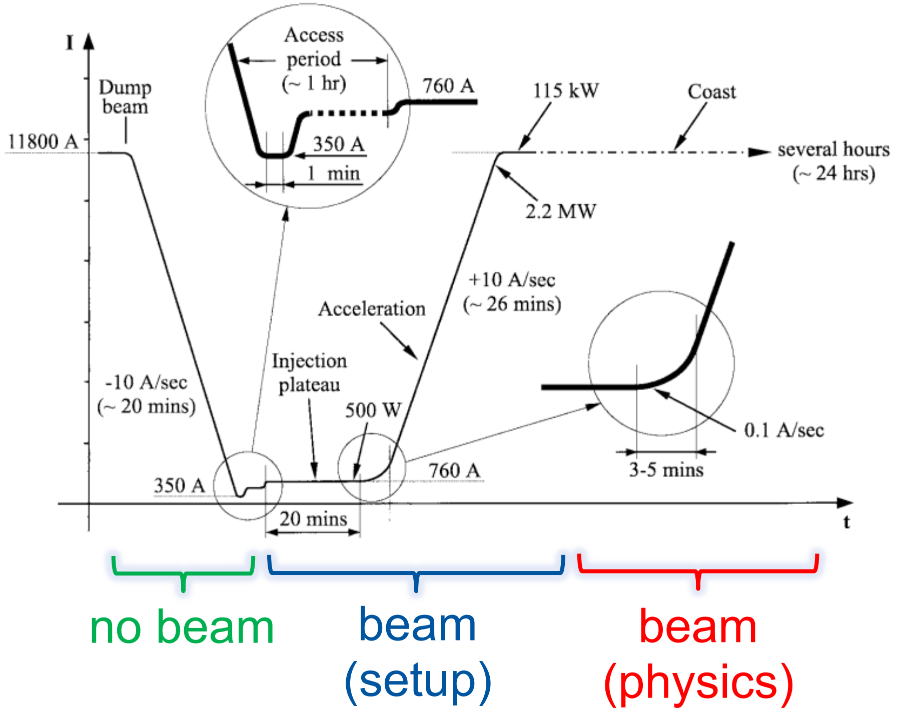



# Slow ramp test

- Test conducted with a slow ramp generated using **Audio Precision APx555**
- High-resolution DAC, fine steps (>20 bits)
- 20 minutes, from 0 V to + 10 V – similar to LHC ramp
- No artifacts seen on the ramp, only noise



# References


[1] Ch. 15 “Moore’s Law” in “The Art and Science of Analog Circuit Design”, ed. J. Williams, 1998

[2] R. H. Walden, "Analog-to-digital converter survey and analysis“ *IEEE Journal on Selected Areas in Communications*, vol. 17, no. 4, pp. 539-550, April 1999

[3] Hi Lumi project website https://hilumilhc.web.cern.ch/

[4] M. C. Bastos *et al*., "High accuracy current measurement in the main power converters of the Large Hadron Collider: tutorial 53," in *IEEE Instrumentation & Measurement Magazine*, vol. 17, no. 1, pp. 66-73, February 2014

[5] P. Horowitz, W. Hill. The Art of Electronics, 3rd edition. 2015

[6] Z. Ignjatovic, Y. Zhang. Analog-to-Digital Converters Employing Chaotic Internal Circuits to Maximize Resolution-Bandwidth Product - Turbo ADC. Proceedings of the 5th International Conference on Applications in Nonlinear Dynamics. Springer, 2019

[7] N. Beev, "Analog-to-digital conversion beyond 20 bits," *2018 IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*, Houston, TX, USA, 2018

[8] https://electrooptical.net/static/media/uploads/hobbsbeos3_chapter20.pdf

[9] B. Gordon, "Linear electronic analog/digital conversion architectures, their origins, parameters, limitations, and applications," in *IEEE Transactions on Circuits and Systems*, vol. 25, no. 7, pp. 391-418, July 1978

[10] C. D. Motchenbacher, F. C. Fitchen. Low-noise electronic design. John Wiley & Sons, 1973

[11] N. Beev, "Measurement of Excess Noise in Thin Film and Metal Foil Resistor Networks," *2022 IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*, Ottawa, ON, Canada, 2022

[12] R. Goldstein, G. Rosen, J. Musel. Study of Foil Resistors Under Exposure to High-Temperature, Moisture, and Humidity. Vishay Precision Group Application Note 110. https://foilresistors.com/docs/63516/VFR_TN110.pdf

[13] T. J. Witt and Y. Tang, "Investigations of noise in measurements of electronic voltage standards," in *IEEE Transactions on Instrumentation and Measurement*, vol. 54, no. 2, pp. 567-570, April 2005

[14] V. Nappi. Design and implementation of a new Controller for CERN's sub-ppm stable Current source. MSc Thesis, 2023. https://hdl.handle.net/10589/214506

[15] N. Beev, M. C. Bastos, M. Martino, D. Valuch, L. Palafox and R. Behr, "Design and Metrological Characterization of a Digitizer for the Highest Precision Magnet Powering in the High Luminosity Large Hadron Collider," in *IEEE Transactions on Instrumentation and Measurement*, vol. 73, pp. 1-10, 2024 https://ieeexplore.ieee.org/abstract/document/10363412

Thank you!