Multi slope A/D converters. Why the 50 years old technology is still (the only one?) relevant for the highest performance applications?

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# Is multislope relevant for today's metrology applications?

# Is multislope the only relevant technolgy for the same?

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FEI STU, Bratislava Is multislope relevant for today's metrology applications? Yes.

Is multislope the only relevant technolgy for the same? No.

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# From single slope to dual slope, multislope and charge balance ADC, part 1/6.



Not really an integrating ADC, though typically using integrator.

Requires stable passive components, though there are workarounds for that - AN-260 by Jim Williams [1]

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## From single slope to dual slope, multislope and charge balance ADC, part 2/6.



like Fluke 429100 Intersil ICL7106

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# From single slope to dual slope, multislope and charge balance ADC, part 3/6.





Suffering from usual problems: Slow acquisition for given resolution Limited due to comparator noise/offset and integrator capacitor dielectric absorption (DA) Integration time not easy to scale



Solution to that? Add more slopes, obviously.

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Jaromir Sukuba jaromir@jaromir.sk Variant of dual-slope ADC with different runup/rundown resistors for faster conversion. Not much of an improvement on other issues.

# From single slope to dual slope, multislope and charge balance ADC, part 4/6.



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# From single slope to dual slope, multislope and charge balance ADC, part 5/6.



Multislope ADC for faster and more precise rundown, making it somehow easier for the comparator. Still, simple runup.

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counter

+/-/

control

logic

This runup scheme actively "fights" the charge accumulated in the integrator by controlled periodic addition of opposite charge to keep integrator voltage within determined bounds

output

R2\*N

R3\*N

output

comparator

### Charge balance ADC, part 1

performance digitizer and R1 Critical points: DC metrology - reference stability meeting Ux - resistor ratios R2 - R1 tempco +VREF February 19, - C1 DA 2024 R2\*N <sup>comparator</sup> - precise timing R3 A bit less critical ones: - switches FEI STU, -VREF R3\*N Bratislava - comparator

For variants and more details of this

method, see [2] and [3]

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High

### Charge balance ADC, part 2

High performance digitizer and DC metrology meeting

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Jaromir Sukuba jaromir@jaromir.sk Increased effective integrator voltage (several kV or more)

Lower value integrator capacitor and average charge

Partial result obtained during runup, less weight on the rundown.

Runup can be scaled as needed to find a compromise between noise and acquisition speed



#### Charge balance ADC, part 3

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Jaromir Sukuba jaromir@jaromir.sk Simple runup algorithm would produce different number of switching actions for various runup patterns (input voltages) causing linearity errors

Multiple methods of keeping this number constant [2]



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### Charge balance ADC, part 4

Charge balance ADC fixed some of the dual-slope issues:

- sensitivity to integrator capacitor DA
- slow acquisition rate for given resolution
- sensitivity to comparator parameters
- runup is easy to scale now

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Jaromir Sukuba jaromir@jaromir.sk Charge balance (not much of multiple slopes here) ADC with integrator readout ADC, called Multislope III in patent [5]

# From multislope to less multislope and sigma-delta, part 1/3



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Input is on all the

No run-down phase

Higher modulation

Frequency (100s of

single MHz for MS V)

kHz for MS III and

time

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# From multislope to not that multislope and sigma-delta, part 2/3

AGND < +5VB 16 U411 V1 MUXDX FN4 AĞND L4Ø1 14 1/113 15 212 4 3/3 AGND ≀44Ø ⊦2.2K AĞND R4 3Ø Ø

A snippet from 34401A schematics

Ux

control

logic

-VREF

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#### Summing point DAC Integrator +VREF ADC ADC

DAC

Multislope III and Multislope IV by HP (see patent [6] and [7]) being similar to delta sigma ADCs, filling the spectrum of integrating ADC architectures

# From multislope to well... uhm... multislope and sigma-delta, part 3/3



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#### Other long scale integrating ADC principles

Mark-scale (PWM) ADC (patent [8] from 1971 and [9] from 1974), often used in long scale Solartron voltmeters



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#### Multiple ramp ADC (patent [10] from 1972) by Prema





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### Long scale non-integrating ADC principles

Recirculating remainder ADC (see patent [11] from 1971) by Fluke





Successive approximation register ADC, like AD4630 and derived models INL:  $\pm 0.9$  ppm maximum

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## Summary

Integrating ADCs, especially varaints of charge-balance flavour still dominate the precision ADC sector.

In recent years, new integrated ADCs, like AD4630 and derived models entered the market and offer viable alternative for some high precision applications, while shortening development time and decreasing PCB footprint.

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Still, integrating ADCs do offer better linearity, may be easier to integrate into an instrument.

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#### Resources

digitizer and DC metrology [1] AN-260 A 20-Bit (1 ppm) Linear Slope-Integrating A/D Converter by Jim Williams meeting [2] HP journal 4/1989 [3] HP3456A service manual [4] N.Beev, Measurement of Excess Noise in Thin Film and Metal Foil Resistor Networks February 19. 10.1109/I2MTC48687.2022.9806690 2024 [5] Patent US5117227 - Continuously integrating high-resolution analog-to-digital converter [6] Patent US6876241 - Circuit for generating from low voltage edges higher voltage pulses having precise amplitudes and durations [7] Patent US6876241 Precision low noise-delta-sigma ADC with AC feed forward and merged coarse and fine results [8] Patent US3475556 Analogue to digital converter FEI STU, [9] Patent US3942172A Bipolar mark-space analogue-to-digital converter Bratislava [10] Patent US3765012 Analog-digital converter utilizing multiple ramp ingegrating techniques [11] Patent US3703002 Analog to digital converter and indicator using recirculation of remainder

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High

performance