Assembly and Testing of ATLAS ITk pixel detector modules
+ Argonne Micro Assembly Facility (AMAF) virtual tour

2024, May 15

DPF-PHENO 2024 at University of Pittsburgh/Carnegie Mellon University

https://indico.cern.ch/event/1358339/contributions/5899237/

Argonne NATIONAL LABORATORY

ATLAS EXPERIMENT

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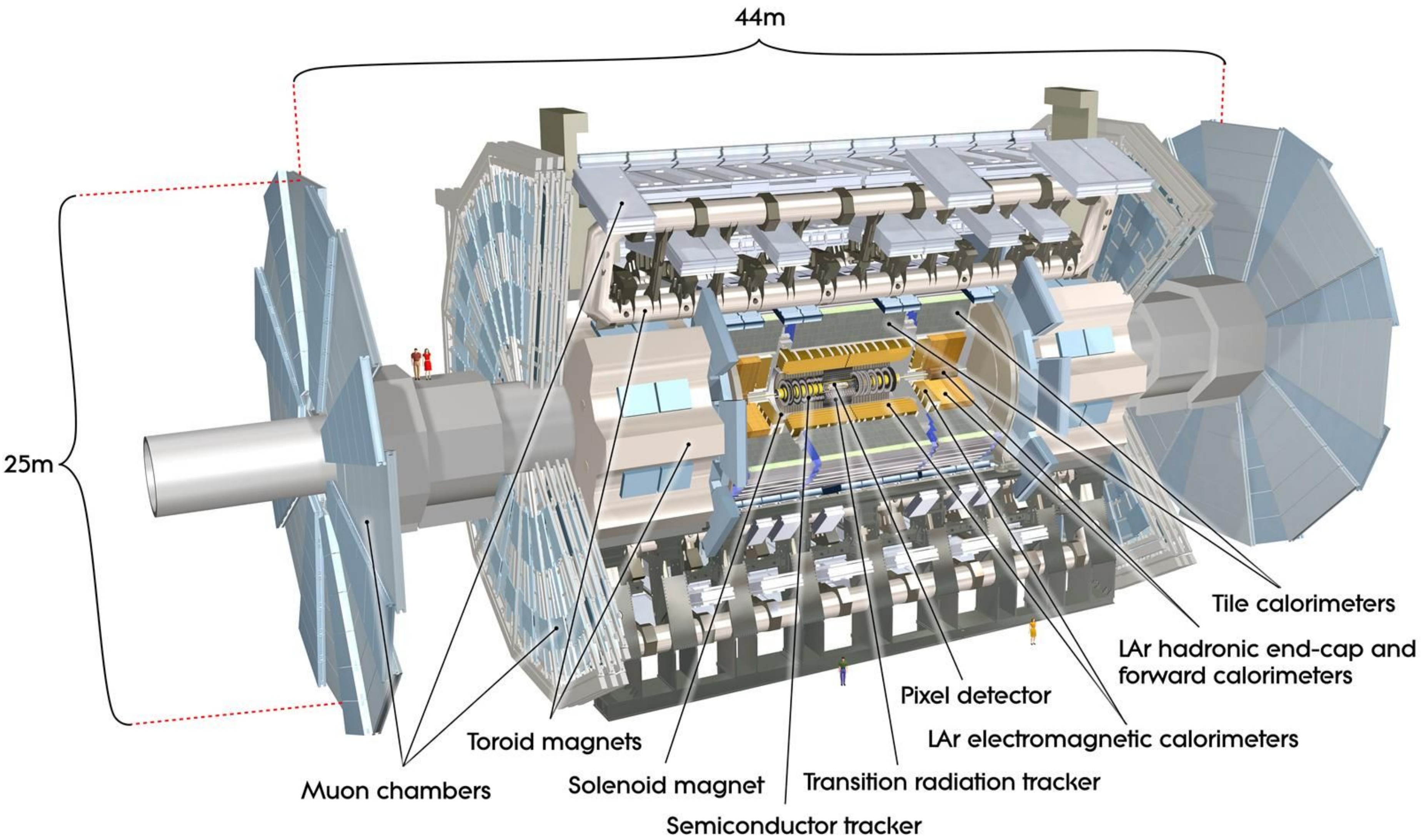
Argonne National Laboratory

Why we want the HL-LHC upgrade?

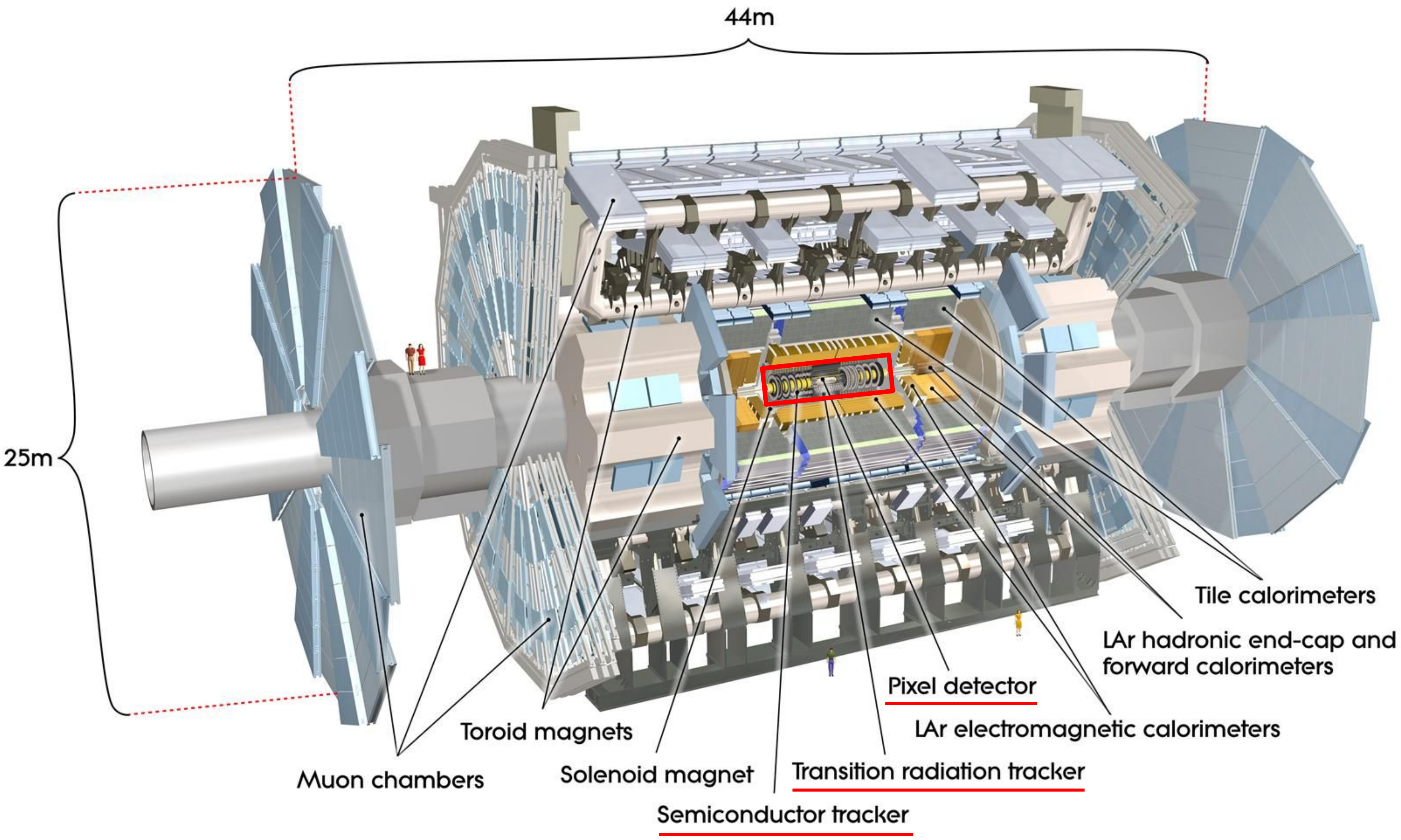
GOAL of the HL-LHC:
to increase the integrated luminosity by a factor of 10 beyond the LHC's design value

Photo by Maximilien Brice, CERN

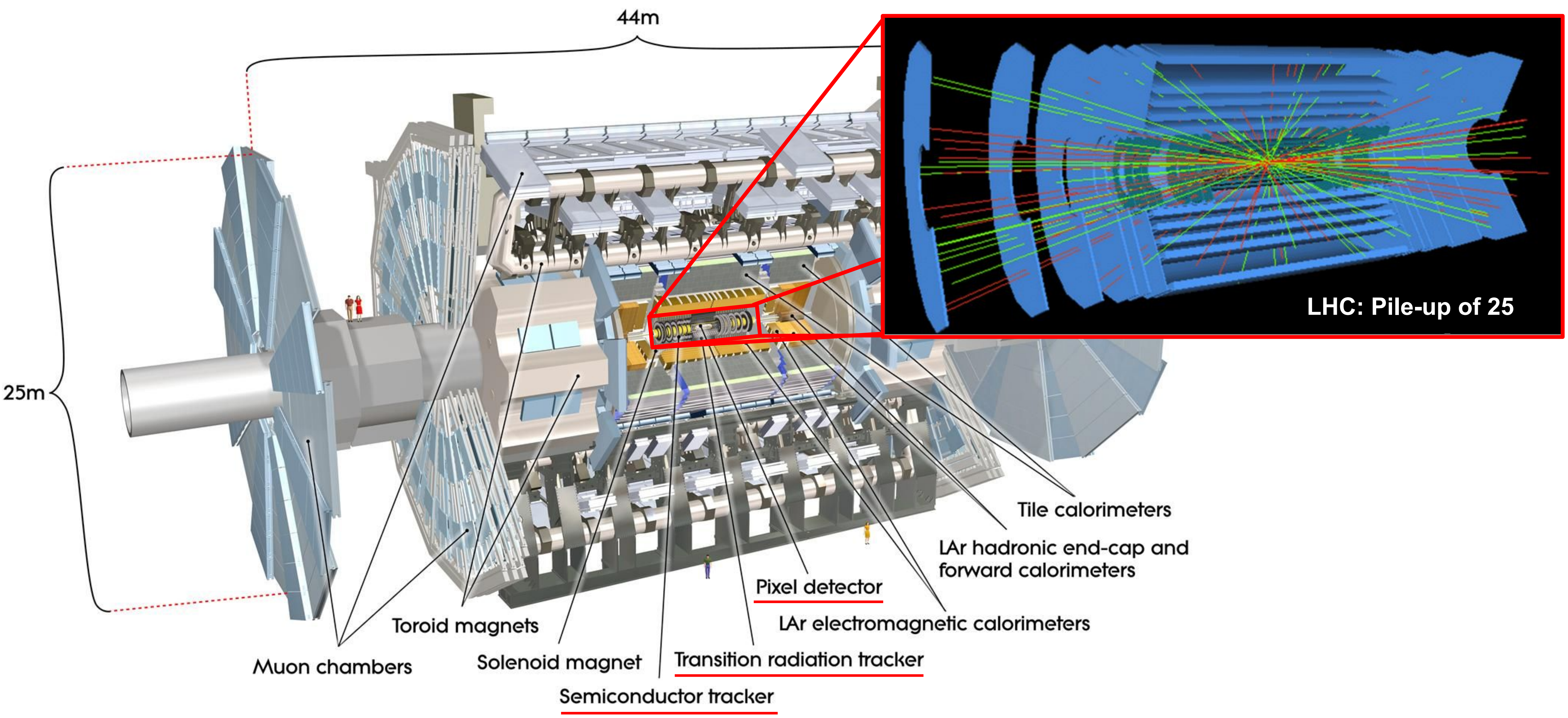
ATLAS: multi-purpose particle detector



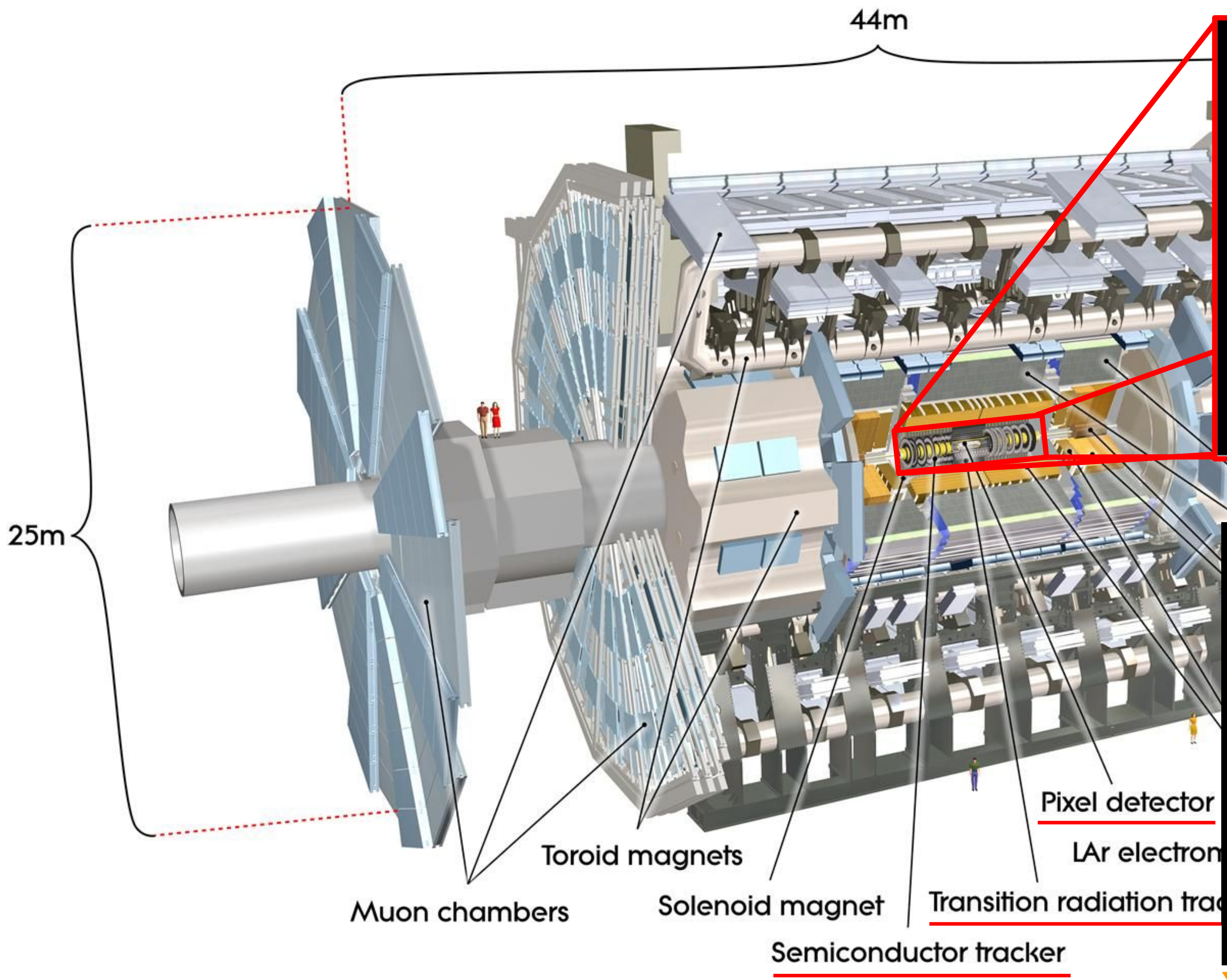
Inner Detector: current ATLAS tracker for LHC



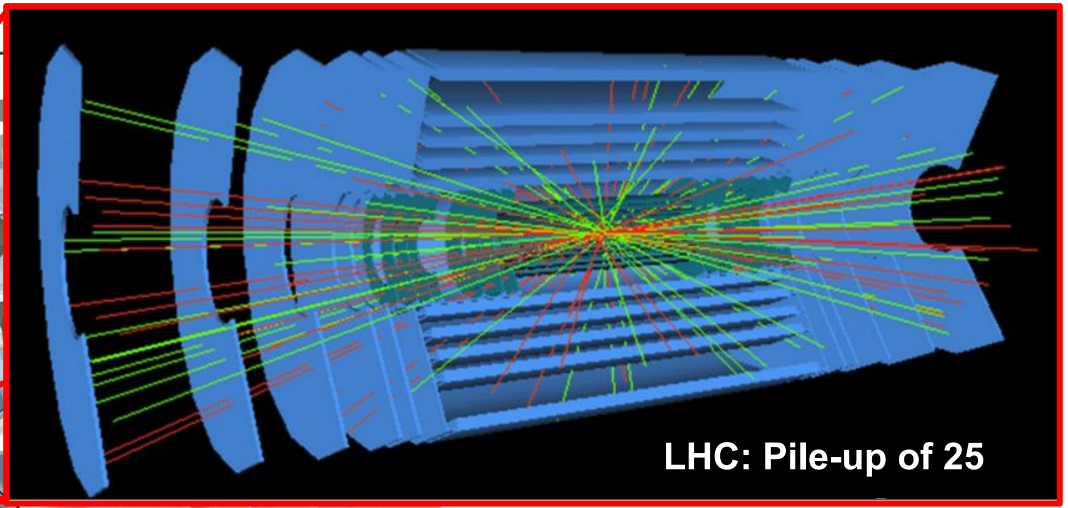
Inner Detector: current ATLAS tracker for LHC

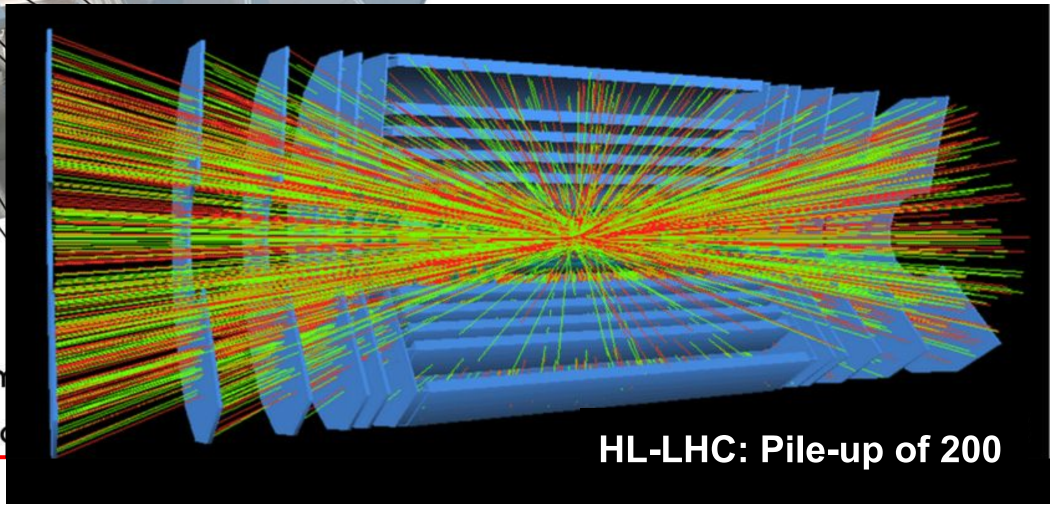


Challenges in HL-LHC data taking condition



future

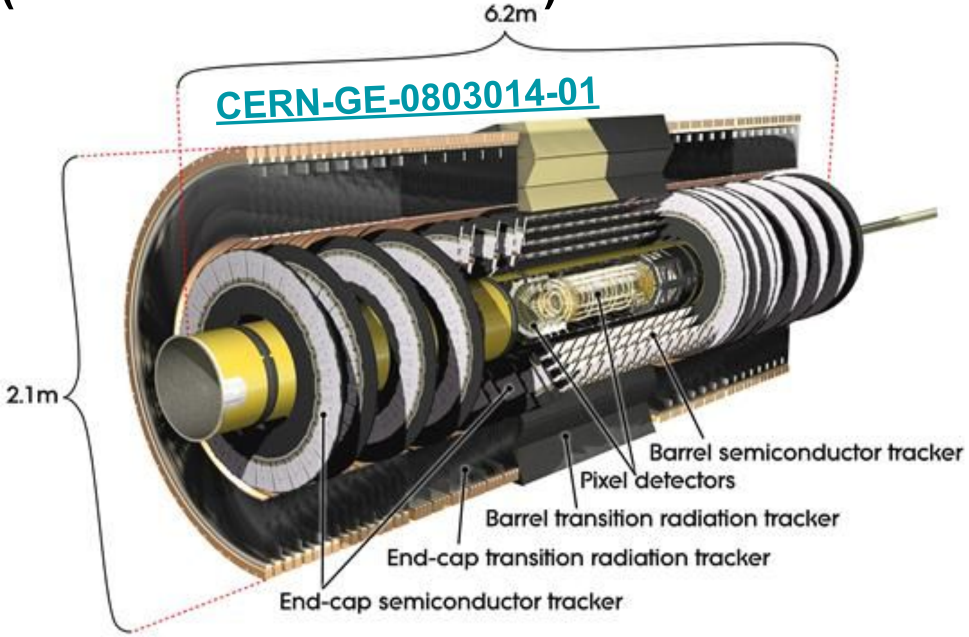




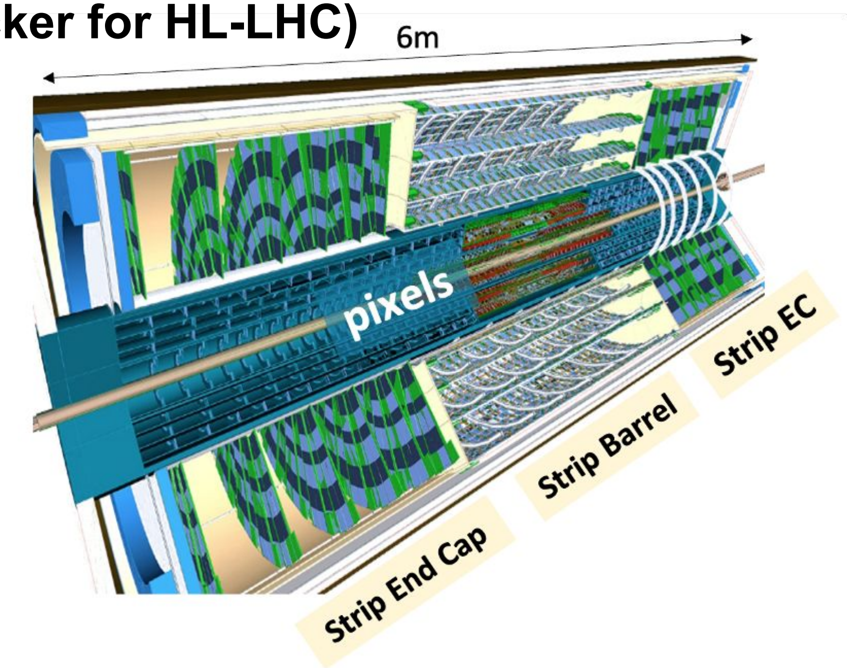
X5 more pile-up
unprecedented radiation environment

ATLAS Inner Tracker (ITk) Upgrade

Inner detector
(current tracker for LHC)



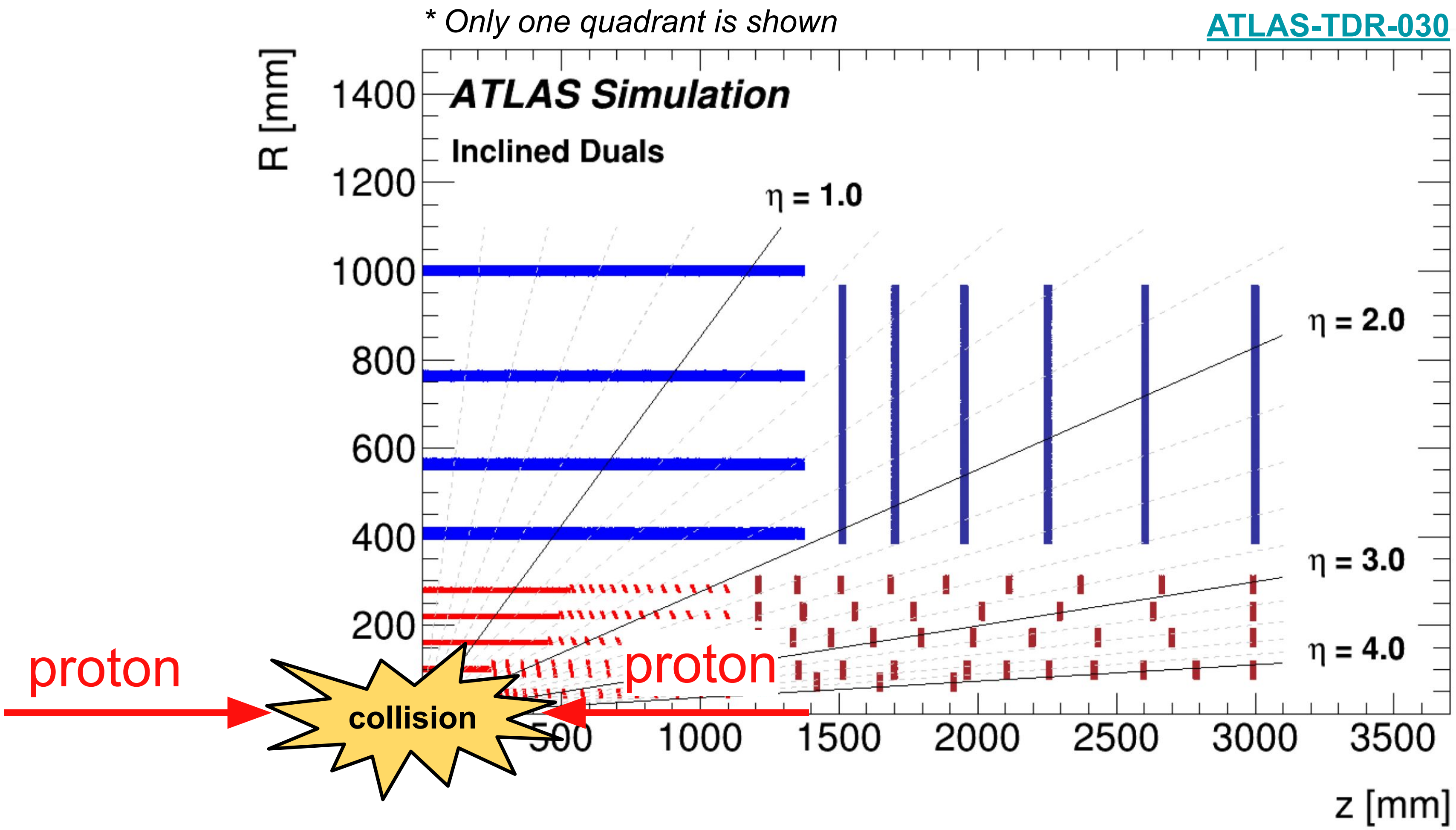
Inner Tracker
(future tracker for HL-LHC)



- HL-LHC upgrade will involve current ATLAS tracker being replaced by all-silicon Inner Tracker (ITk) ATLAS ITk
- **New technology:** silicon sensors, readout, data transmission, and improved radiation hardness

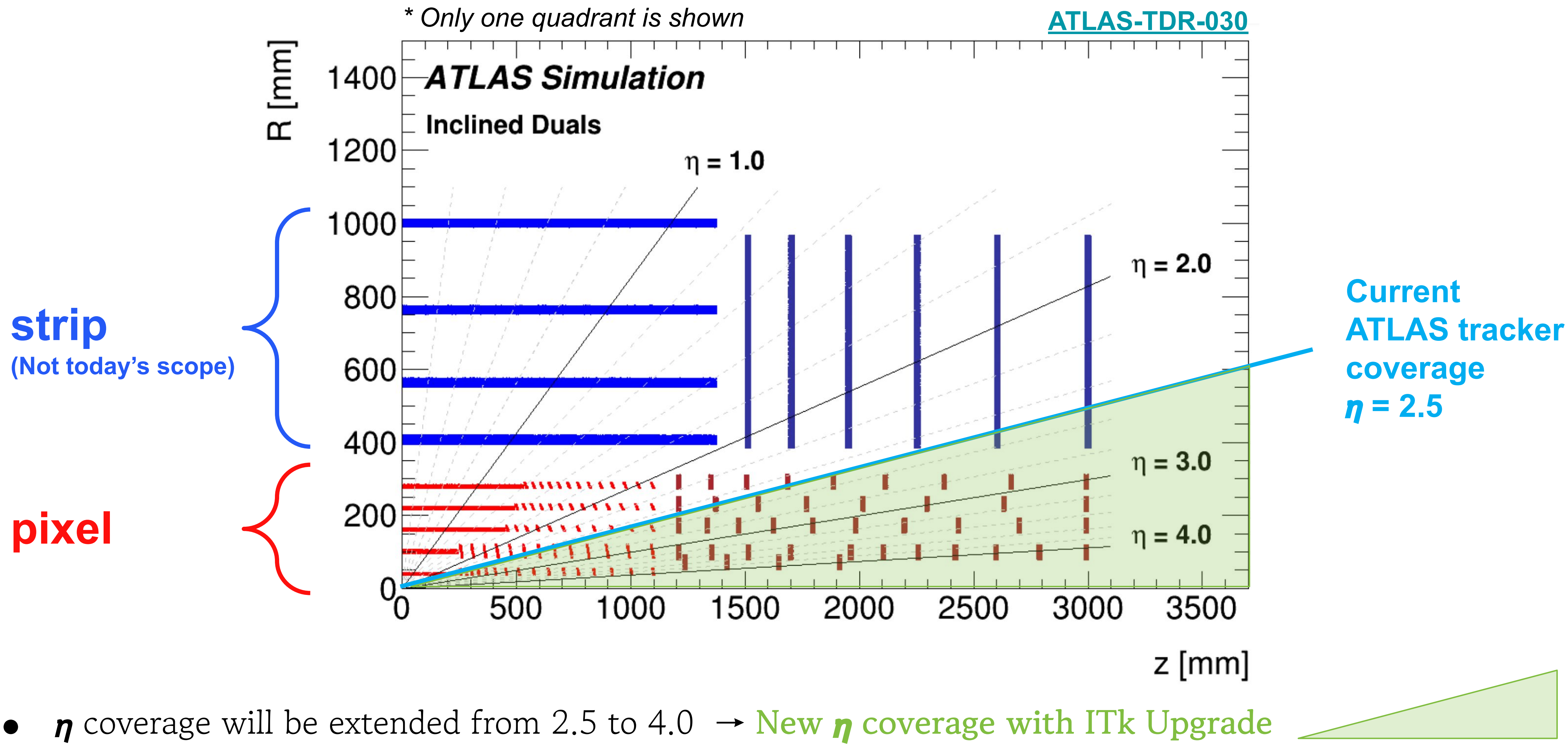
	Inner Detector	Inner Tracker	
# of pixels	92 milliion	5 billion	X 55
Pixel Silicon area	1.9 m^2	12.98 m^2	X 6.5
Trigger rate	100 kHz	1 MHz	X 10
η coverage	2.5	4	

New territory with the ITk Upgrade



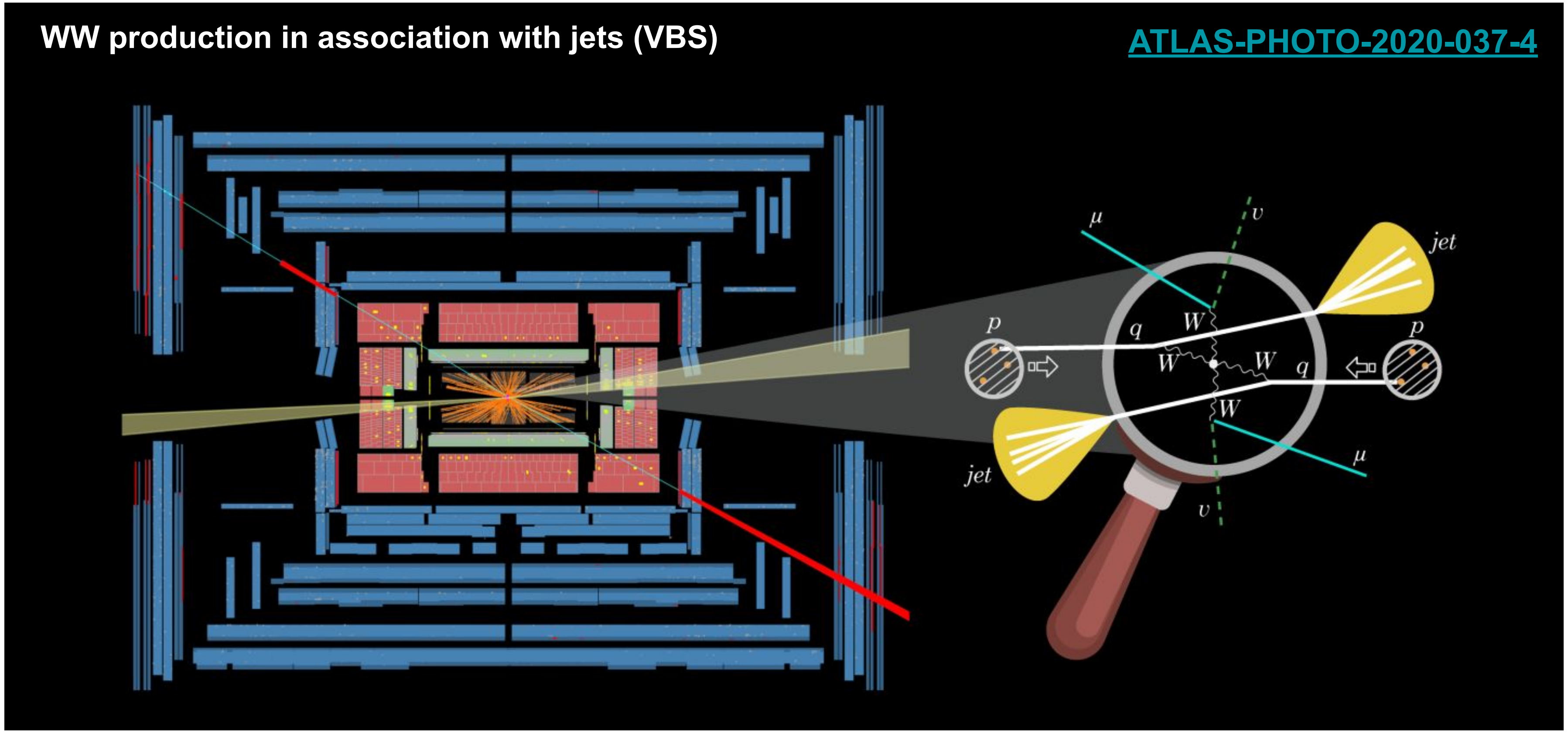
Schematic Layout of the ITk

New territory with the ITk Upgrade



- η coverage will be extended from 2.5 to 4.0 → New η coverage with ITk Upgrade

New territory with the ITk Upgrade

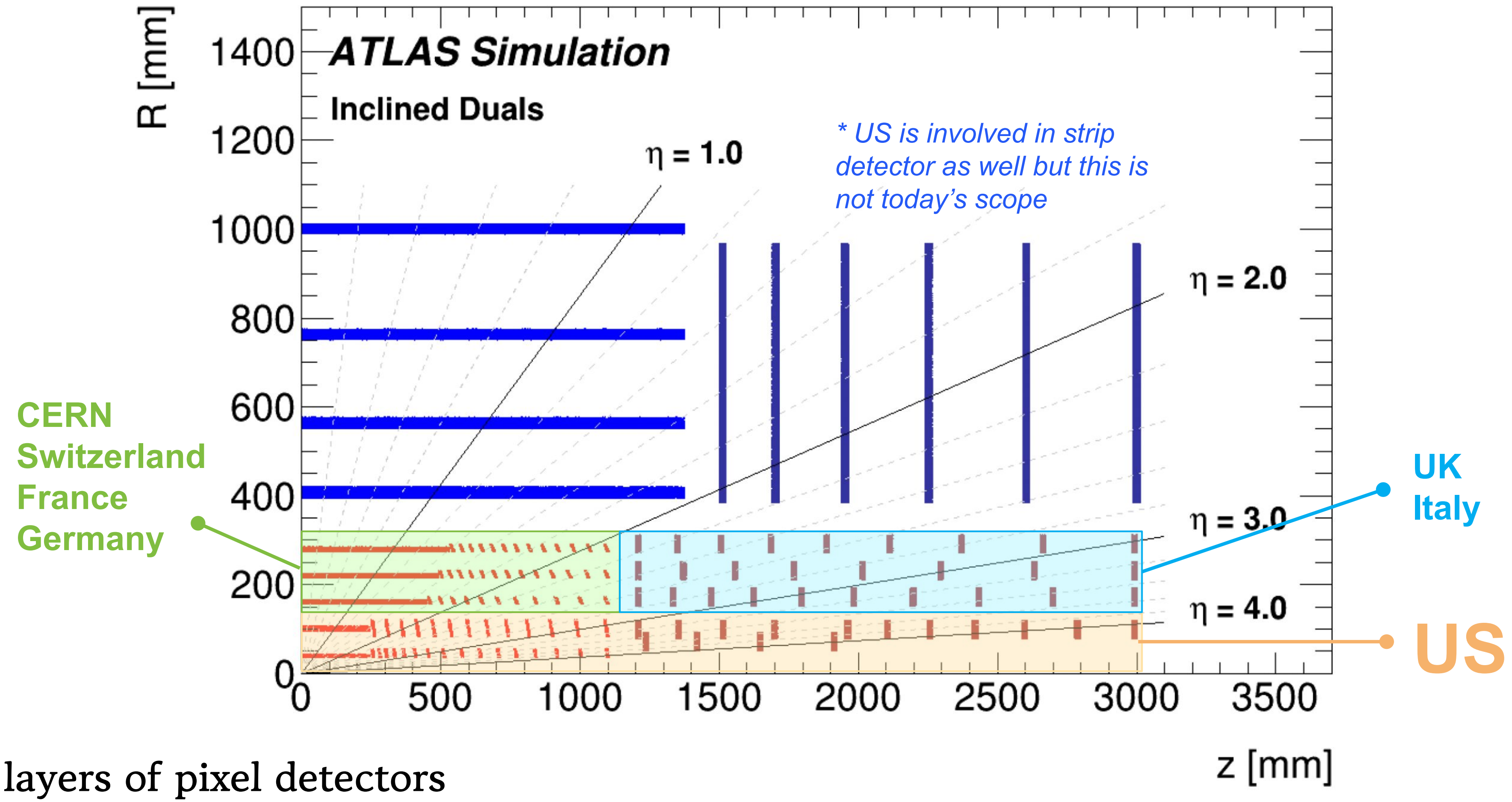


- The forward tracker extension significantly improves the measurement precision in the benchmark physics channels
- Simply increasing the integrated luminosity will not lead to significant improvement without the forward extension

ATLAS ITk pixel

** Only one quadrant is shown*

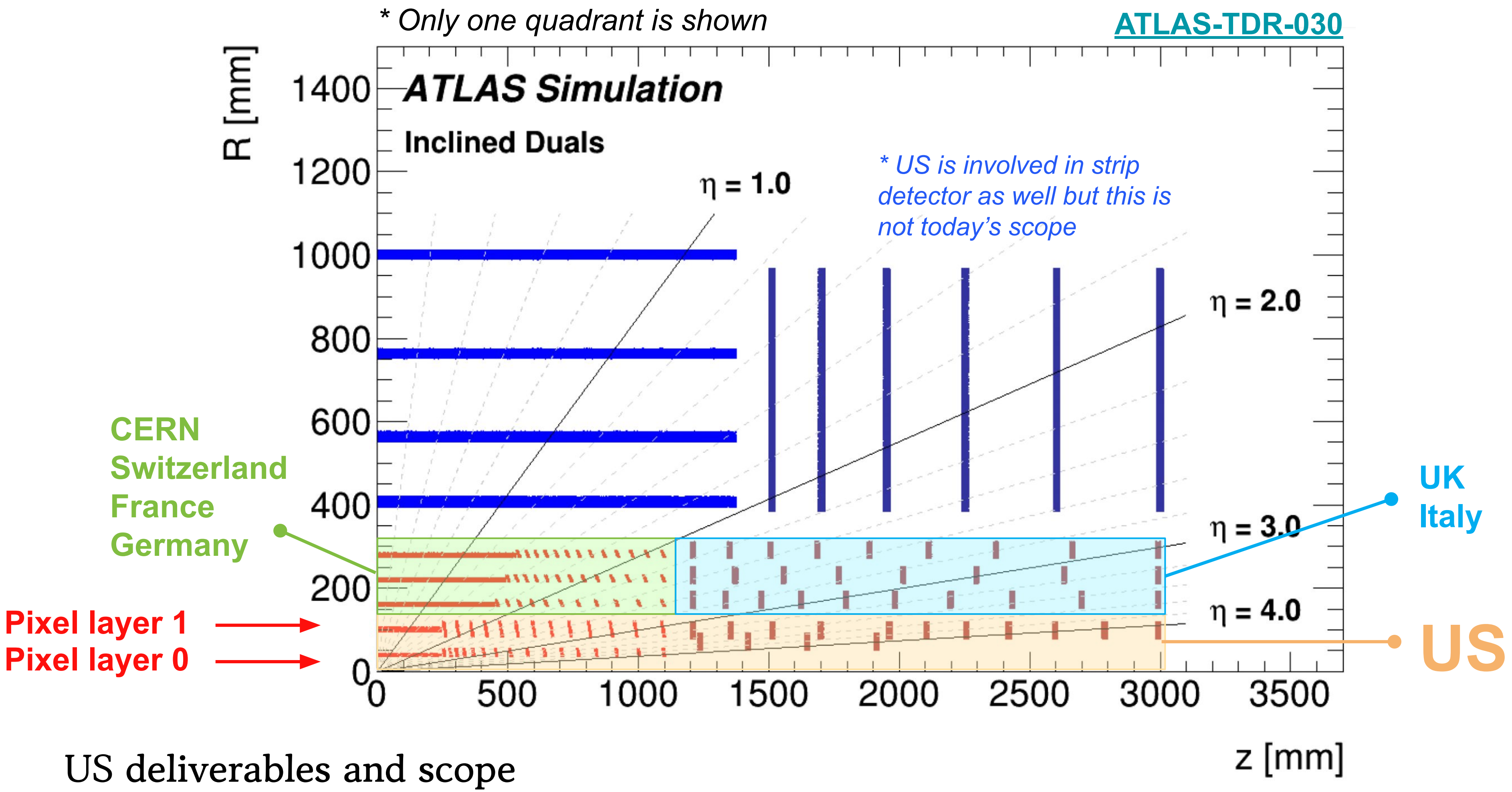
ATLAS-TDR-030



5 layers of pixel detectors

- Layers 0-1: Inner System (IS)
- Layers 2-4: Outer System (OS) 1) Outer Barrel (OB) 2) Endcaps (EC)

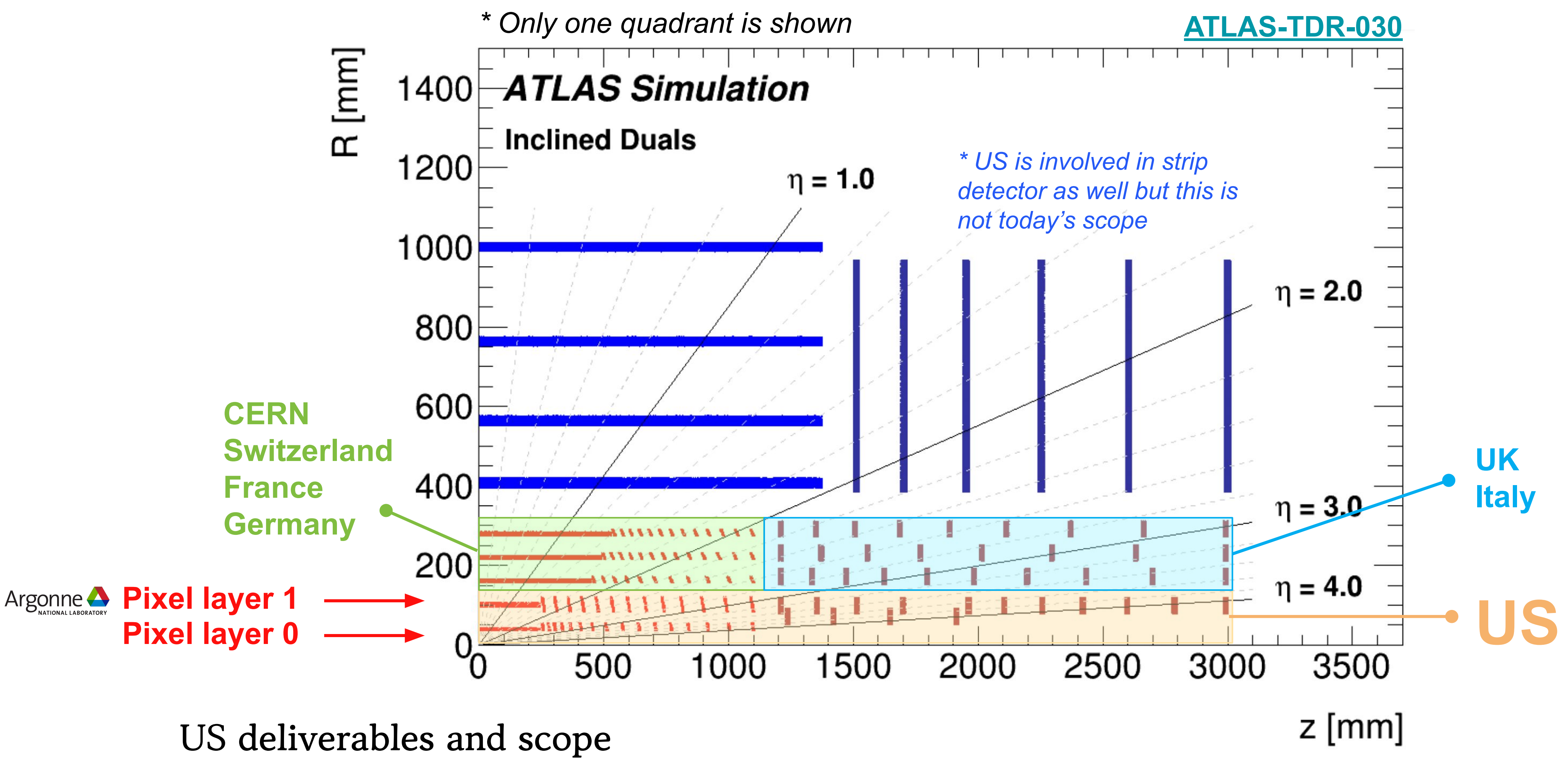
ATLAS ITk pixel



US deliverables and scope

- Layers 0-1: Inner System (IS) → A fully integrated standalone detector
  - Mechanical design, Module assembly and loading, integration

ATLAS ITk pixel

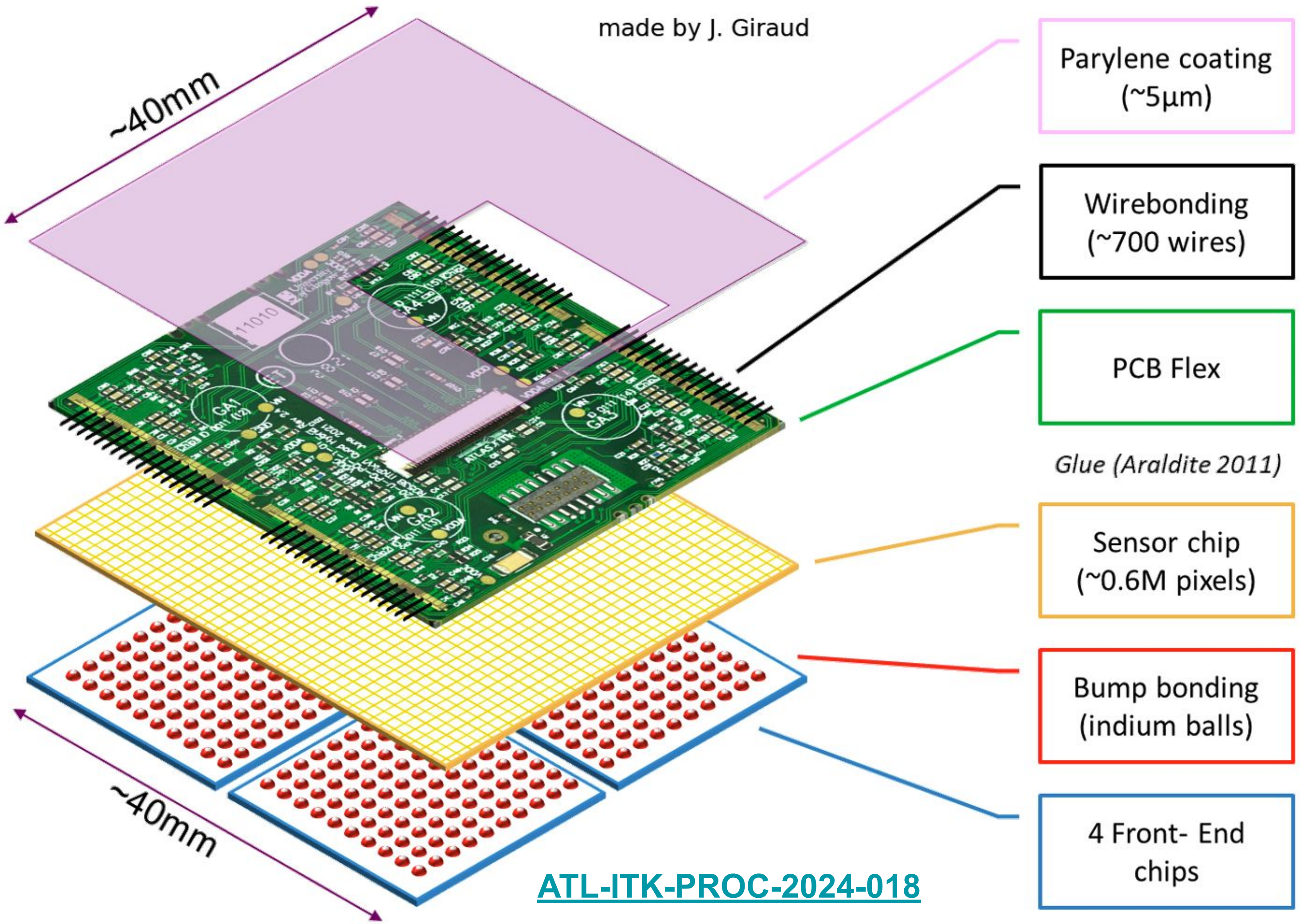


US deliverables and scope

- Layers 0-1: Inner System (IS) → A fully integrated standalone detector
  - Mechanical design, Module assembly and loading, integration

ITk pixel sub-detector: Layers 1 of Inner System (IS)

Quadruplet module for Layer 1



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will assemble ~1100 (70%) quadruplet modules!
+ test ⅓ of assembled modules

Major challenges:

- **High production rates**
  - fast assembly & testing → high level of automation and parallelization are required
- **Over a temperature range of ~80 ℃**
  - No glue delamination
  - No disconnected bumps

AMAF Avengers

Jessica Metcalfe

Tim Cundiff

Manoj Jadhav

Tanvi Wamorkar

Kim Doyeong

Daniel Aceves

Jon Dale Nichols

Matias Mantiñan

Welcome to AMAF :)

ITk Pix Module at A… …MAF?

Argonne Micro Ass…

…sting | Coating

…ntrance

Visual Inspection

Metrology

Wire Bonding

Gluing

Coating

Bare Module IV

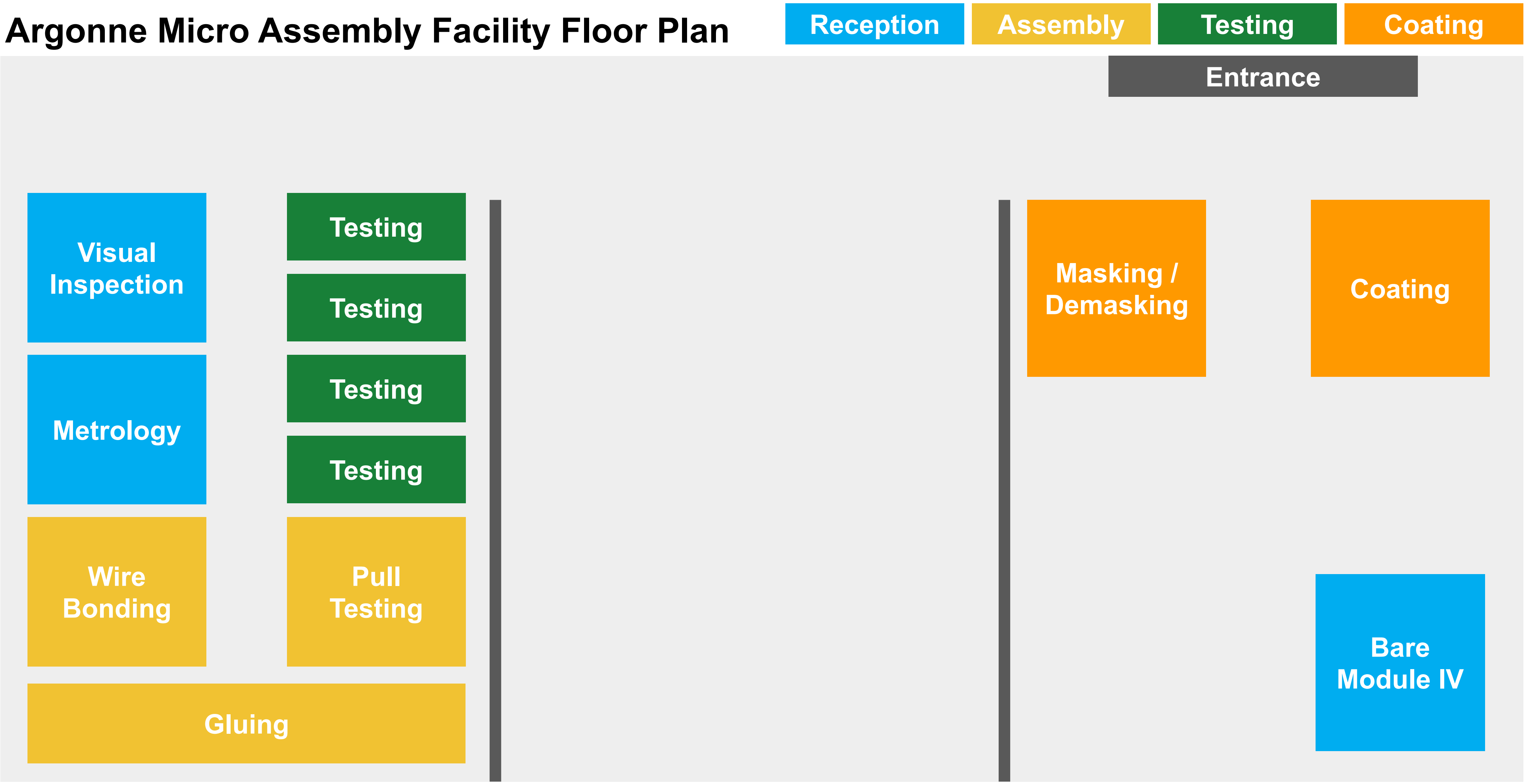
AMAF is ISO 7 clean room

AMAF user attire

- *Hair net*
- *Mask (while handing silicon)*
- *Gloves (while handing silicon)*
- *Lab coat*
- *ESD safe clean-room shorese OR booties*
- *Safety glasses*

What's going on at AMAF?

Argonne Micro Assembly Facility Floor Plan



Workflow at Argonne

Reception | Assembly | Testing | Coating

Module Assembly

- Bare Module Metrology + IV Scan
- Flex PCB Metrology

→ Bare Module to Flex PCB attach → Wire Bonding

Testing temperature

Room (+20℃)
Cold (-15℃)

1 Initial Module Characterisation
* Full set of QC
Warm & Cold tests
(13 tests x 2)

→ **2 Parylene Coating ****
* Full set of QC
Warm & Cold tests
(13 tests x 2)

→ **3 Thermal Cycling**
Minimum Health Test
Pixel Failure Analysis

→ **4 Long-term Stability Test**
* Full set of QC
Warm & Cold tests
(13 tests x 2)

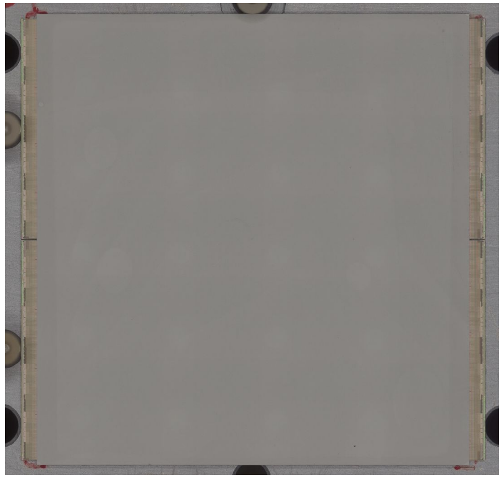
→ **Module Shipment to Loading Site SLAC**

Inventory

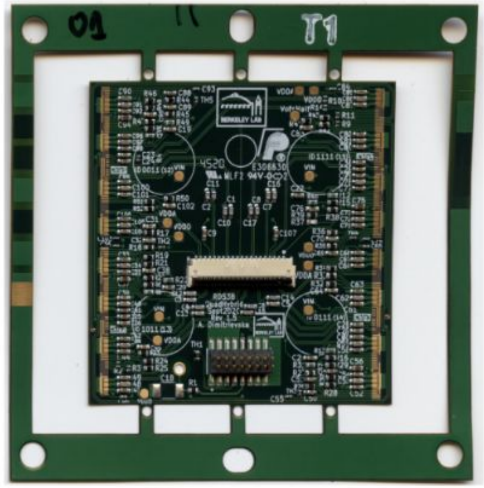
Reception

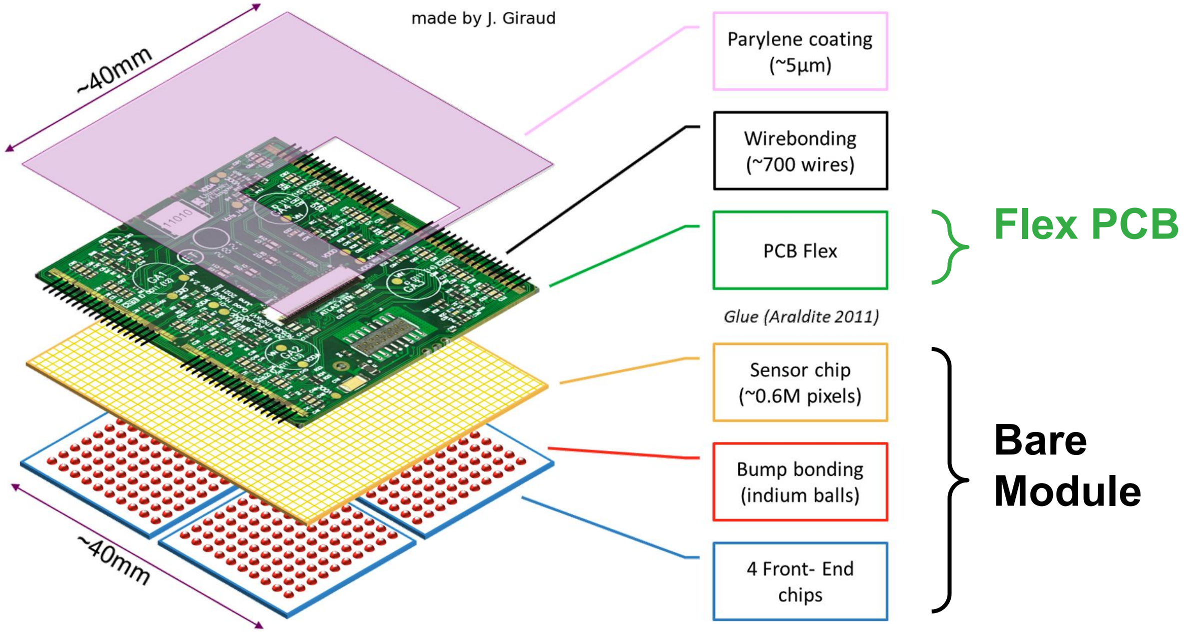
Bare Module

= sensor + 4 front-end chips
bump bonded



Flex PCB





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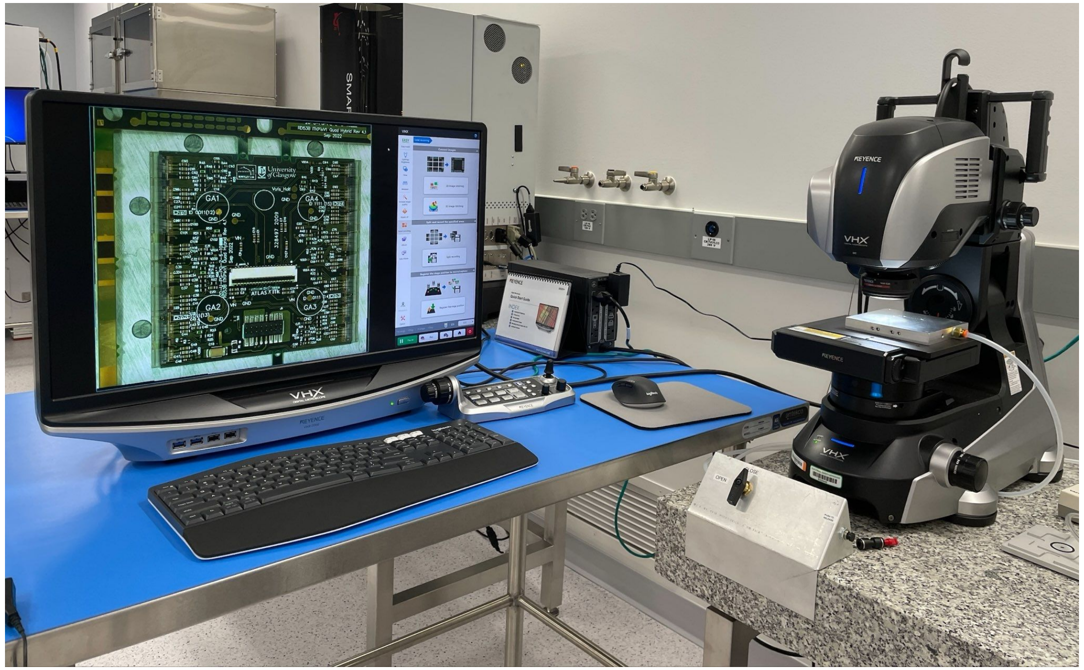
Bare module and **Flex PDB** are provided by industry

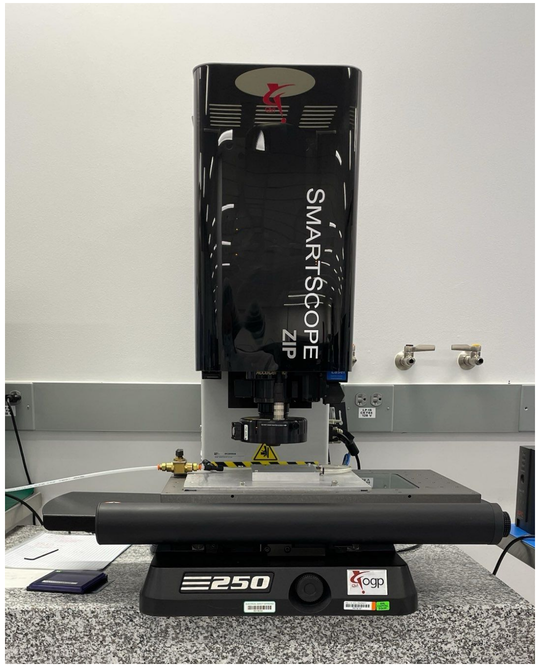
Inventory

Reception

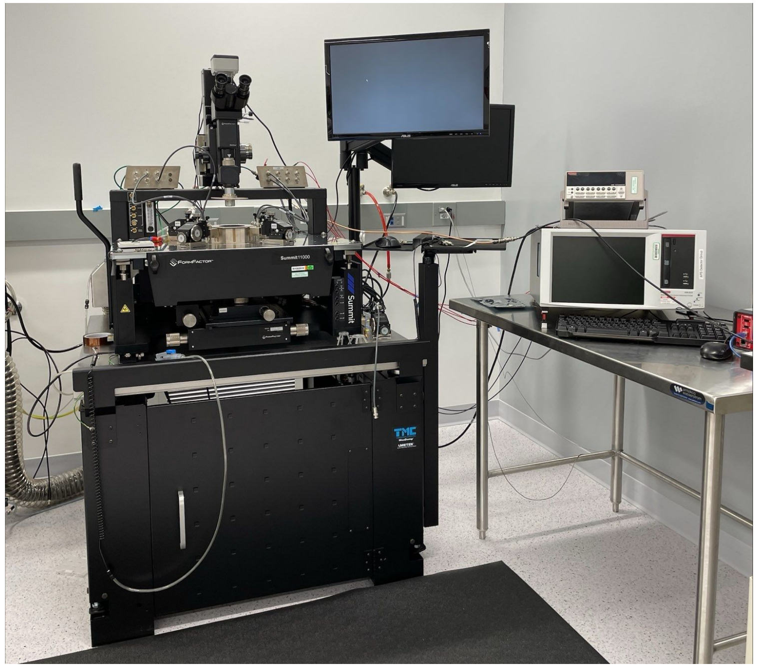
3D Scope



Smart Scope



IV Probe Station



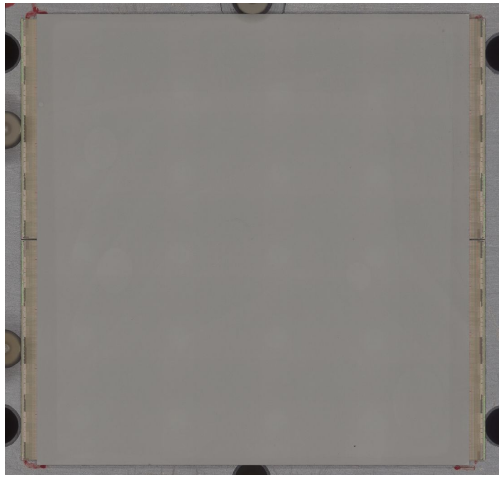
- Visual inspection and metrology are performed both before and after the module assembly
- The processes of measurement with Smart Scope, data visualization, and uploading to the PDB are fully automated, allowing for quick verification of whether the module metrology results are within the specified range

Inventory

Assembly

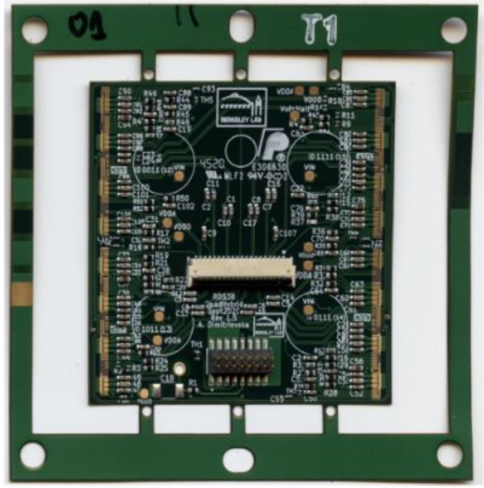
Bare Module

= sensor + 4 front-end chips
bump bonded



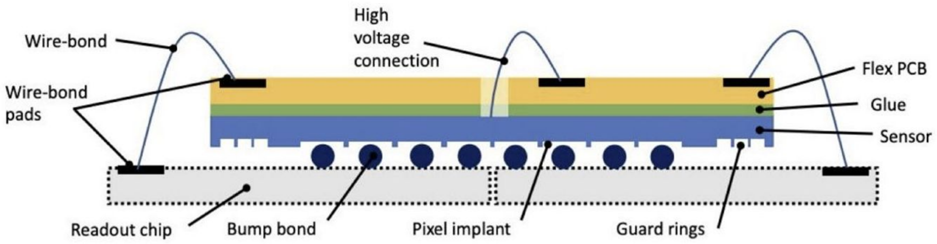
+

Flex PCB



→

Assembled Module



flex PCB is

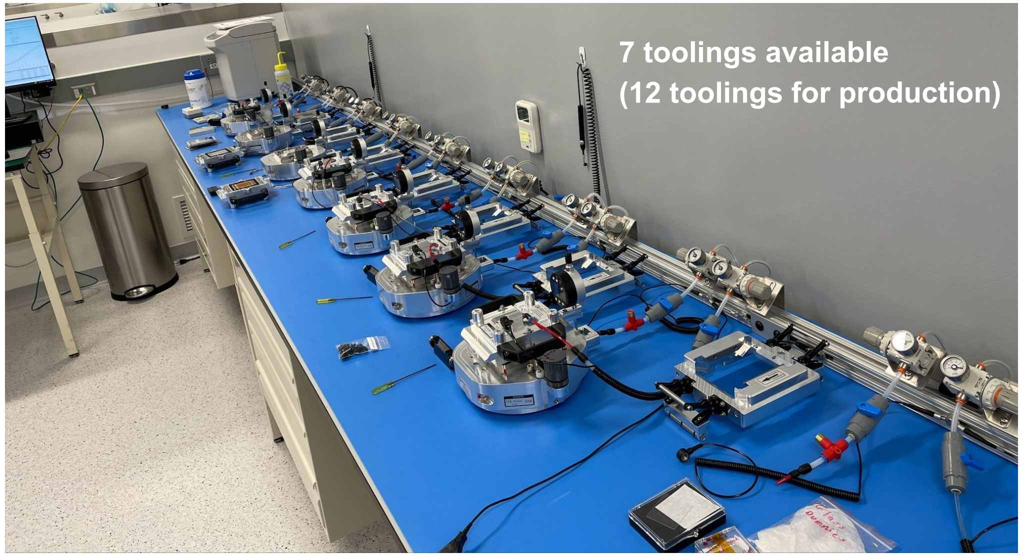
1) glued to the backside of the sensor tile
2) wirebonded to the front-end chips

Inventory

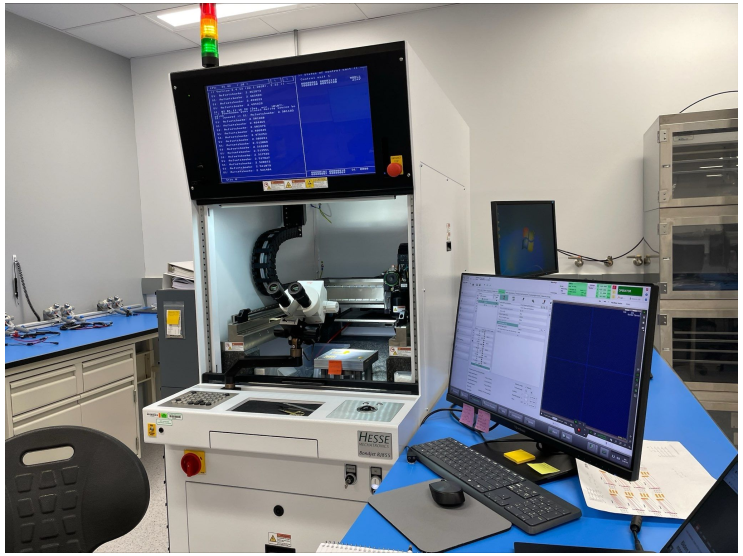
1 day / batch

Assembly

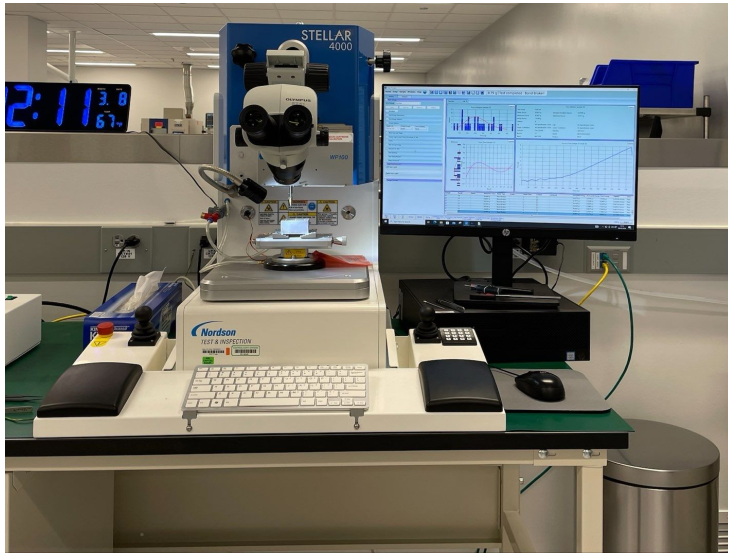
Gluing Toolings



Wire Bonder



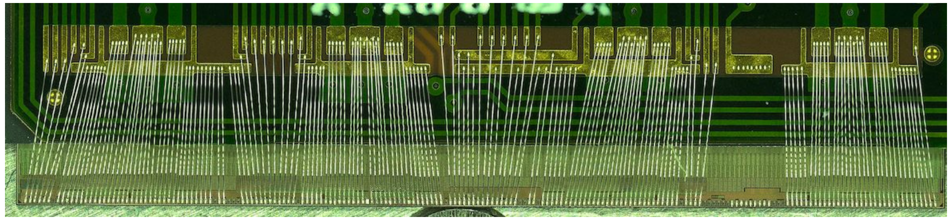
Pull Tester



- Gluing requires 1) large glue coverage (>80%) 2) uniform glue distribution (±15μm) 3) alignment (<±100μm)
  - 8h curing time (over night)

Essential to the success of wire bonding

- Wire bondings
  - ~170 wire bondings / chip (high density, various lengths and angles)
  - 0.5h wire bonding & pull testing (in the morning)
  - other preparation (handling, PDB uploading)



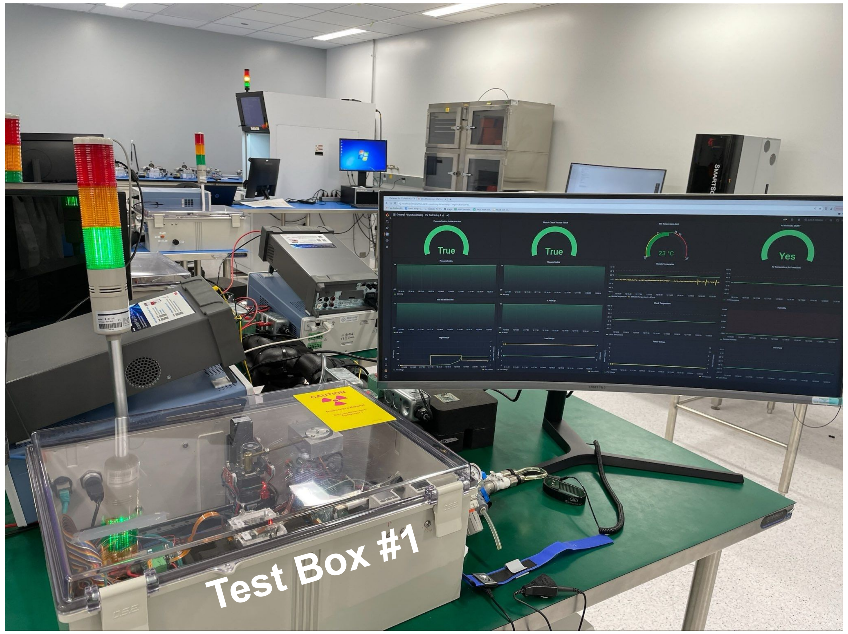
Wire bondings for one front-end chip

Inventory

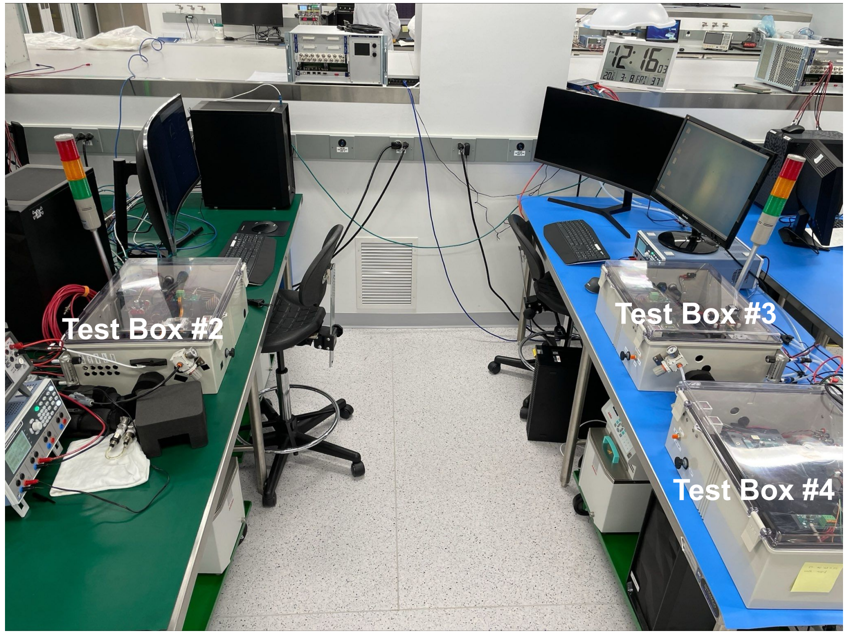
Same day testing

Testing

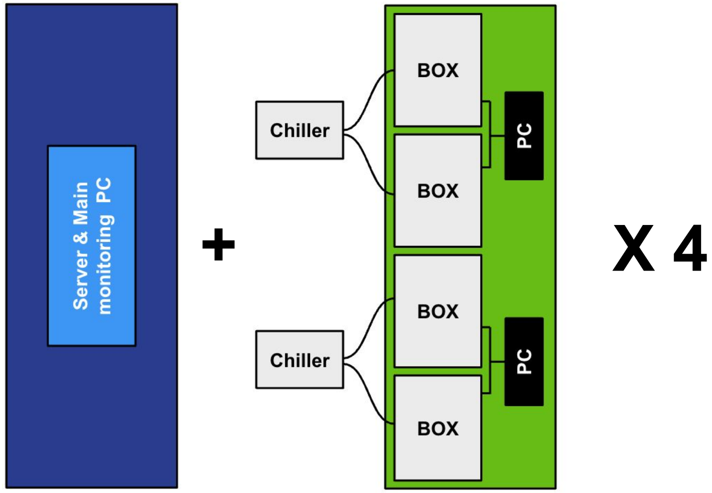
Test setup #1



Test setup #2, 3, 4

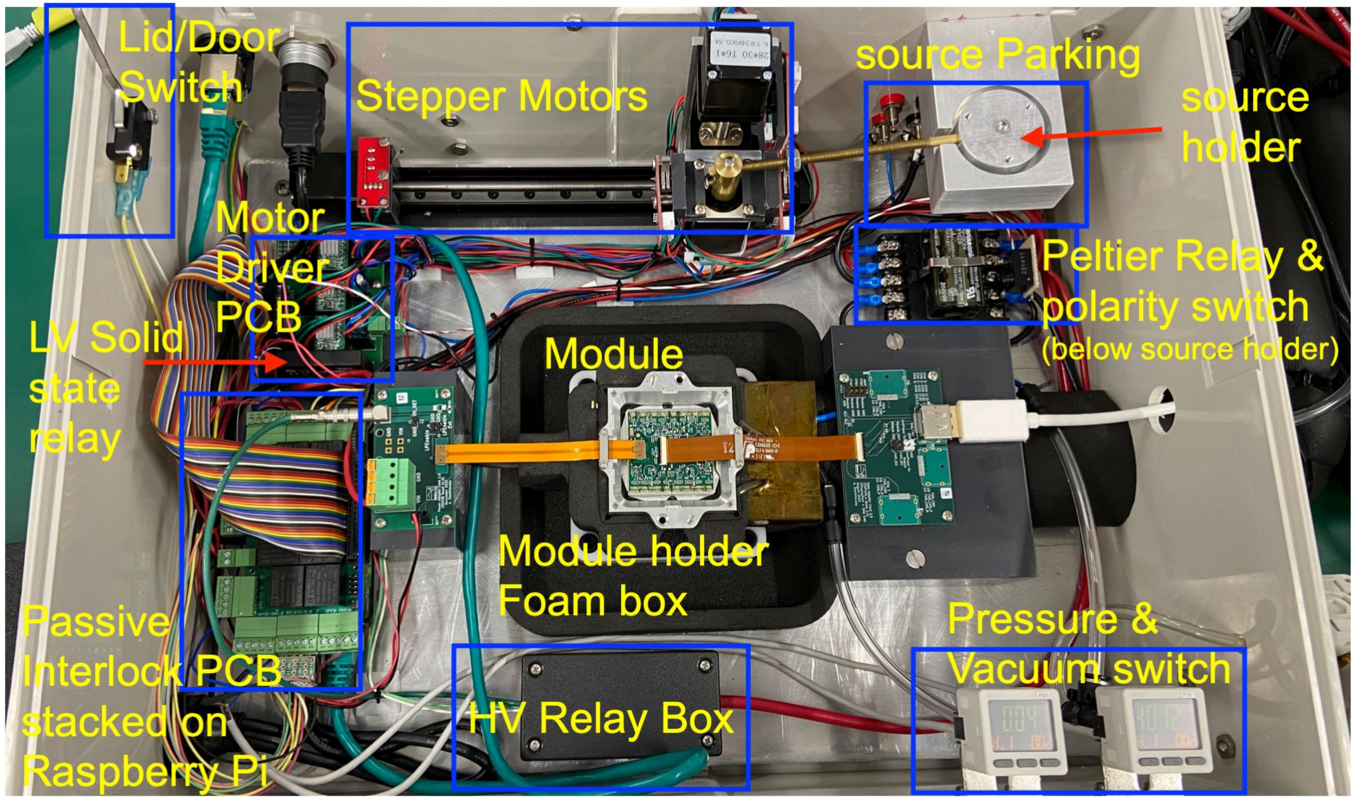


Final configuration for production



- Four test boxes are available (aim to have 16 test boxes for production)
- After all the assembly process, the module is tested on the same day (basic electrical tests & source scan)
  - **Aim to performed all tests with one button** (We are almost there!)
  - Six team members are trained for testing

ANL's test setup



List of testings

Testing

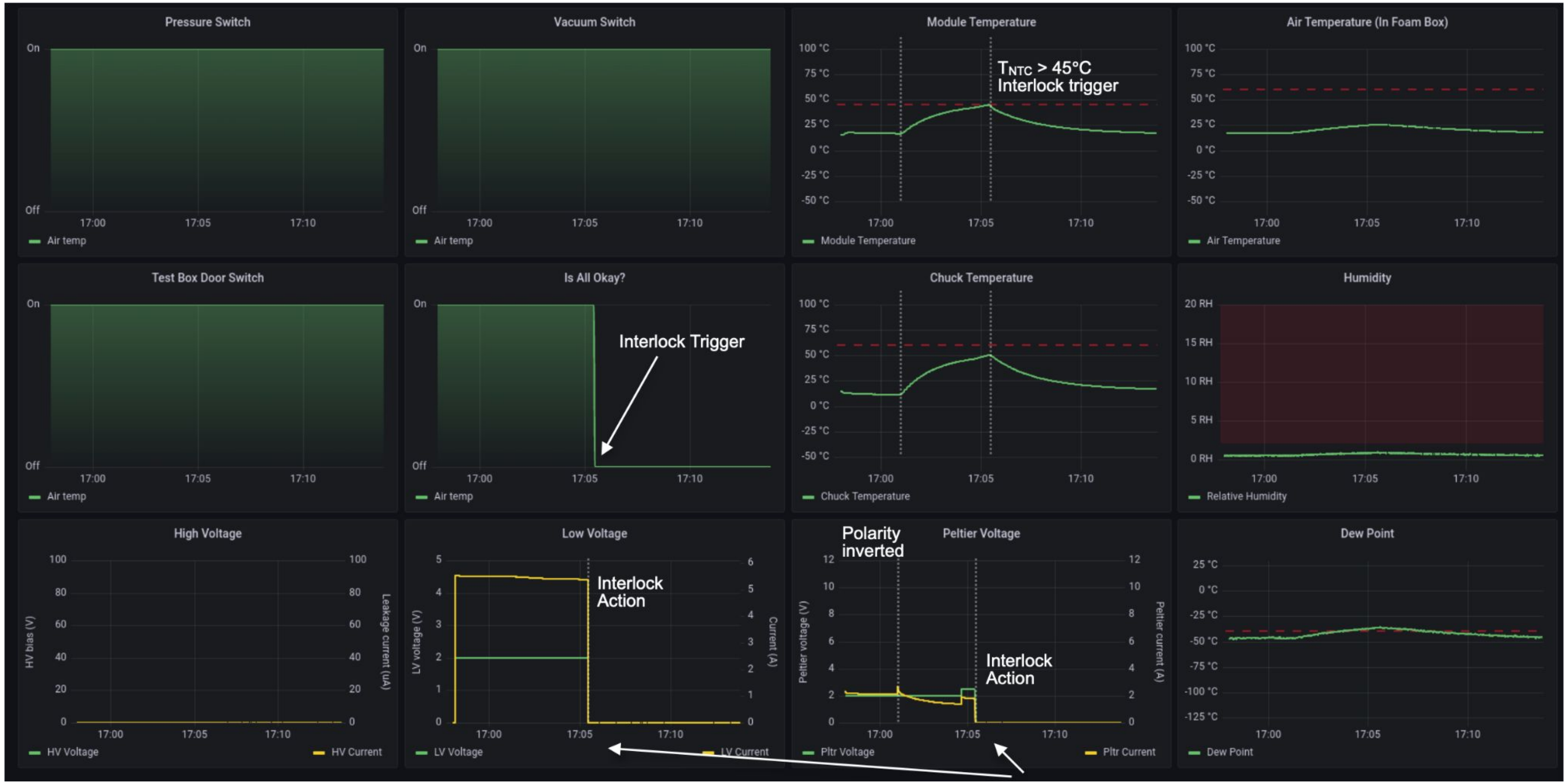
5h for warm tests
6h for cold tests
per module
for initial characterization

- ✓ Calibration scans
- ✓ Pixel thresholds tuning
- ✓ Pixel failure analysis
  - Disconnected bump scans
  - Threshold scan with zero bias
  - Source scan
  - Others
- ✓ Front-end chip testings
- ✓ Assembled module IV-scan

- All tests (at warm and cold temperatures and thermal cycle) can be done in this box without moving the modules around
- All instruments can be controlled remotely
- All tests are automatically logged, and results are automatically uploaded to the local database

Module Test Setup Box - Interlocks

- Raspberry Pi sends module&air temperature, humidity, dew point, vacuum, pressure, a box lid switch to DAQ
- The HV-LV voltages/currents and Peltier voltages/currents are recorded directly using SCPI commands
- The values are fed to InfluxDB with Grafana display (monitoring every 1s, visualization sync every 5s)



LV and Peltier power turned off

Module Test Setup Box - Interlocks

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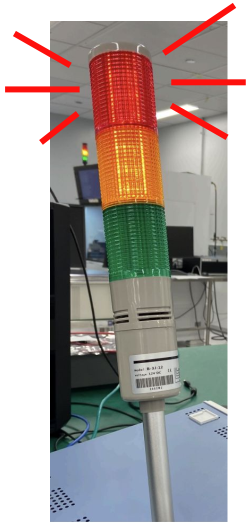
LV and Peltier power turned off

Interlock triggered

- ❏ Shut down all instruments (LV, HV, Peltier, chiller)
- ❏ Beeping
- ❏ LED Red light
- ❏ Auto email alert

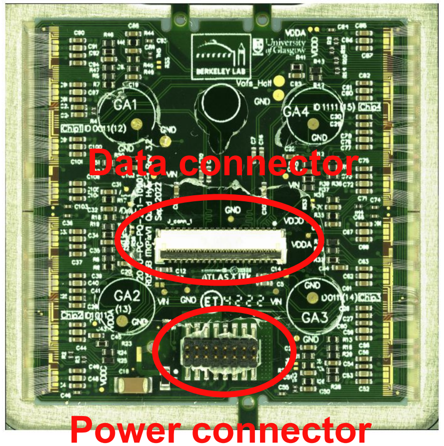


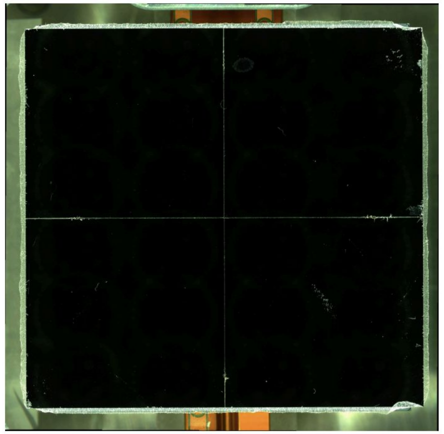
Inventory

Coating

Parylene coater

Masking/demasking station





Real module after demasking

- Specialized plastic coating material to protect sensitive electrical components
  - Spark protection
  - Scratch protection
  - Wirebond protection
  - Bump bond strengthening
- Specific areas (power connector, data cable connector) should remain w/o parylene

Full QC Workflow

Reception | Assembly | Testing | Coating

Module Assembly

- Bare Module Metrology + IV Scan
- Flex PCB Metrology
- → Bare Module to Flex PCB attach → Wire Bonding

Testing temperature

Room (+20℃)
Cold (-15℃)

WE'RE HERE!

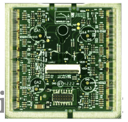
1 – Initial Module Characterisation
* Full set of QC
Warm & Cold tests
(13 tests x 2)

→ **2 – Parylene Coating ****
* Full set of QC
Warm & Cold tests
(13 tests x 2)

→ **3 – Thermal Cycling**
Minimum Health Test
Pixel Failure Analysis

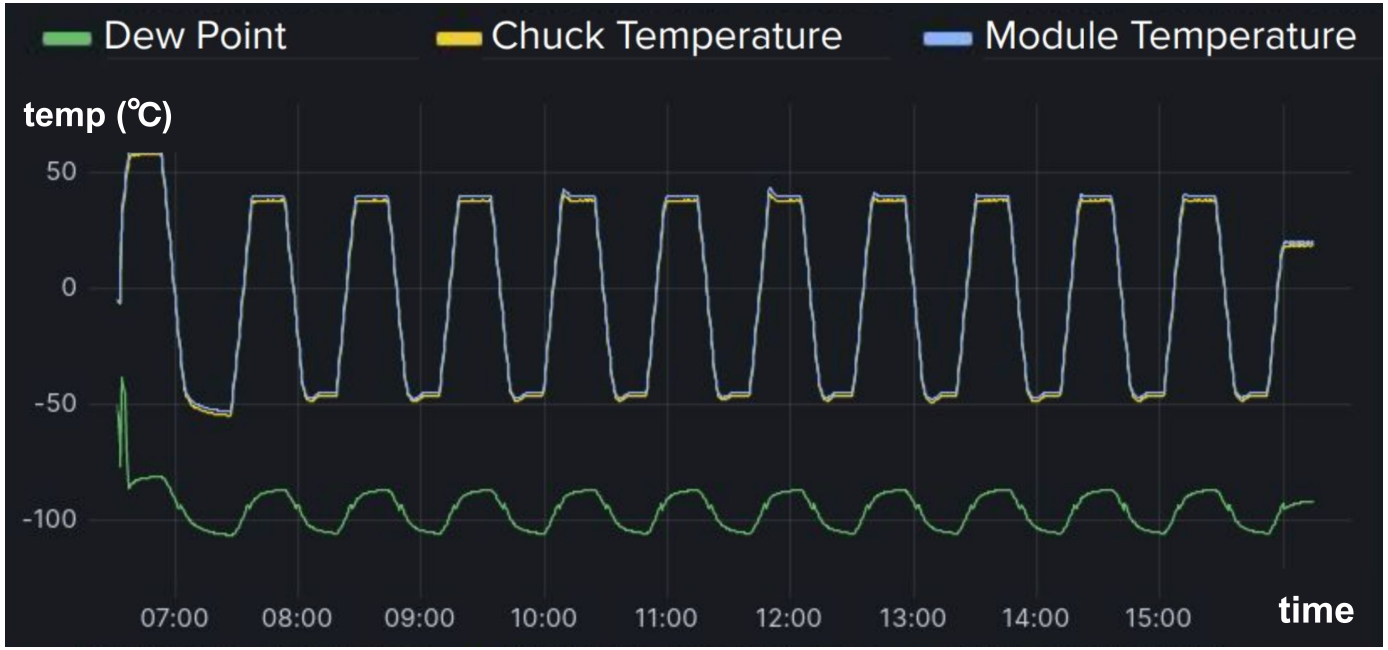
→ **4 – Long-term Stability Test**
* Full set of QC
Warm & Cold tests
(13 tests x 2)

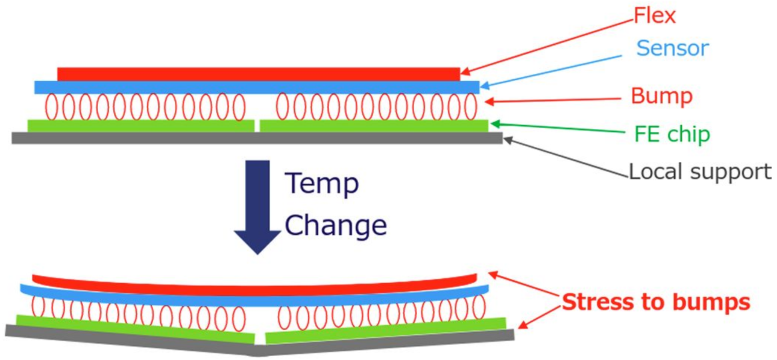
→ **Module Shipment to Loading Site** SLAC



Coated modules are evenly distributed to the three testing sites

Thermal cycle





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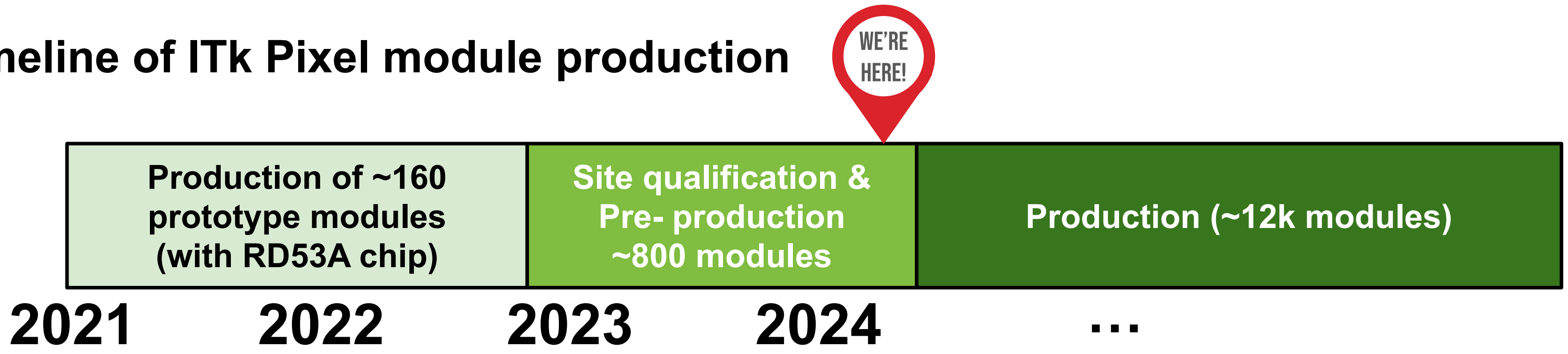
- The quality control of the modules also involves characterising the module again after applying some thermal stress (1 extreme cycle [-55, 60]℃ + 10 cycles [-45, 40]℃)
- During the thermal cycles, the bump bondings connecting the sensor tile to the front-end chips are stressed and may disconnect → **Pixel failure analysis**

Summary and outlook

Timeline of ITk Pixel module production



- ANL is fully ready to deliver massive ATLAS ITk pixel module production for HL-HLC upgrade
  - Most of the steps from assembly to testing are automated
  - Most of the team members are trained for testing and assembly process
- The excellent track parameter resolution and the forward tracking extension are essential for reaching our milestones in the HL-LHC physics program

  ex) VBF, VBS, Higgs Self-Coupling, Long-lived particle, and many more!

Backup