Multi-vertex Jet Trigger at ATLAS' upgrade for HL-LHC Level 0

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Outline

Introduction

- High Luminosity LHC

Physics motivation

- Hard-QCD jets at HL-LHC Run 4
- Single- vs multi-vertex events

Trigger strategy

- Boosted Decision Trees to classify single vs. multi-vertex

FPGA implementation

- Preliminary High Level Synthesis results

High Luminosity LHC

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	LHC Run 3	**HL-LHC Run 4**
Luminosity	$2 \cdot 10^{34}\ cm^{-2}\ s^{-1}$	$7.5 \cdot 10^{34}\ cm^{-2}\ s^{-1}$
Pile Up	~60 collisions/bunch crossing	~200 collisions/bc

⇩

TDAQ system upgrade

- Hardware-based Level 0 Trigger

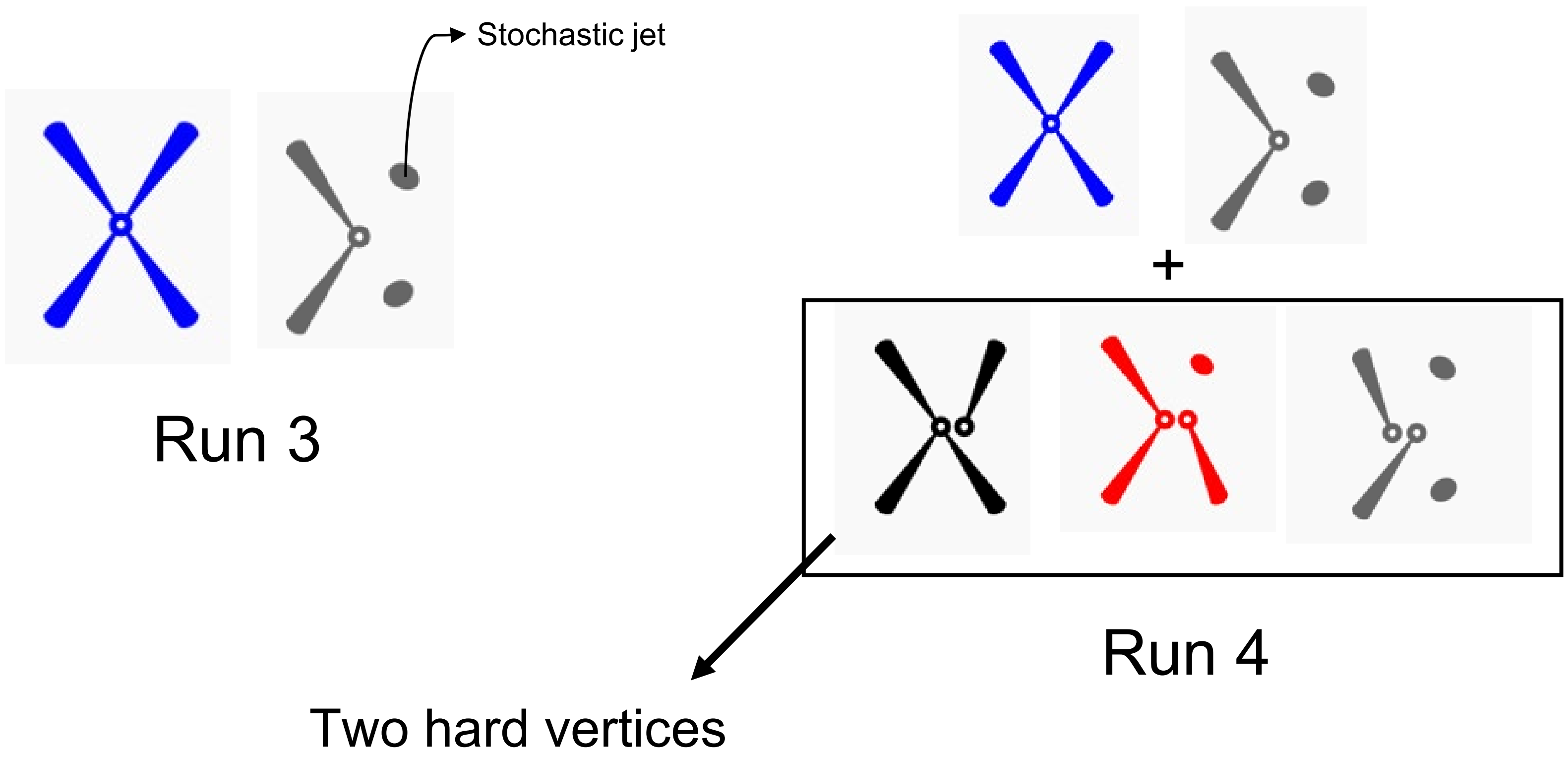
  Filters data from 40MHz to 1 MHz with a latency of 10 μs

- Software-based Event Filter

Source: ATLAS TDAQ Phase II Upgrade TDR (2018)

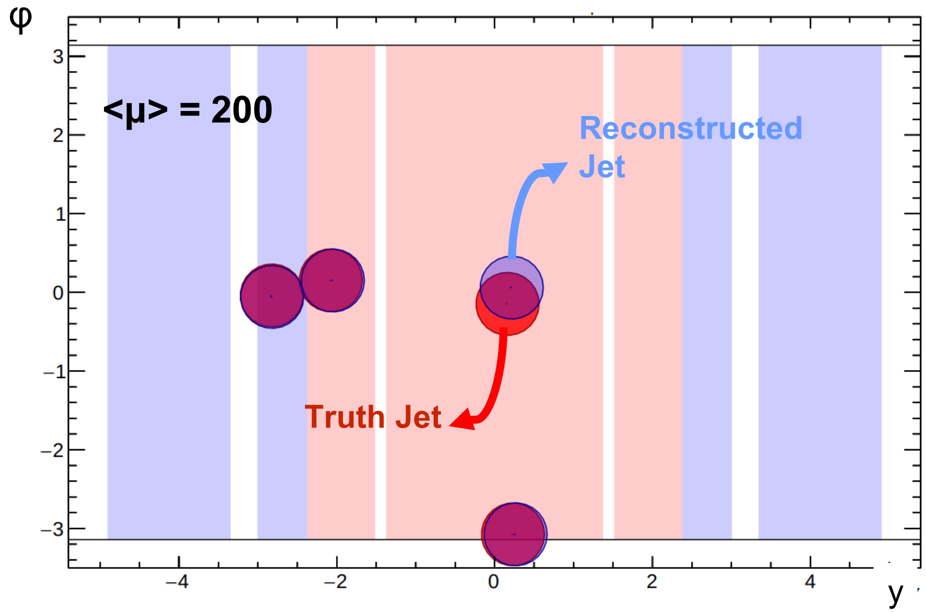
Physics motivation

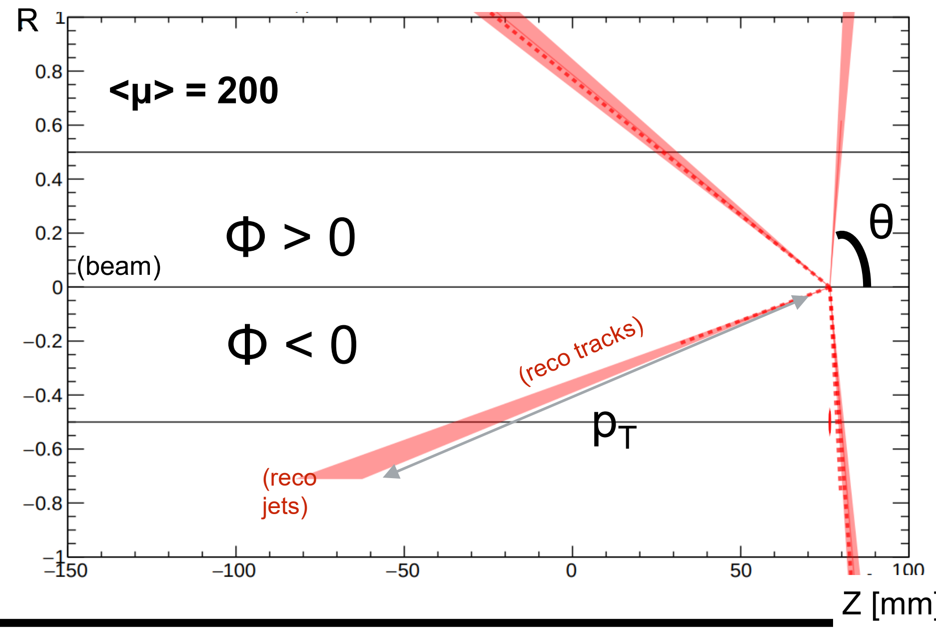
- Current pile up suppression algorithms target stochastic and soft-QCD jets.
- Run 4: new relevant PU source → **hard-QCD PU**
- **Hard-QCD PU ⟹multiple hard scatters**
- Goal: develop a new trigger for L0 that targets hard-QCD PU
- Motivation: HH→4b and any process with a 4-jet final state.



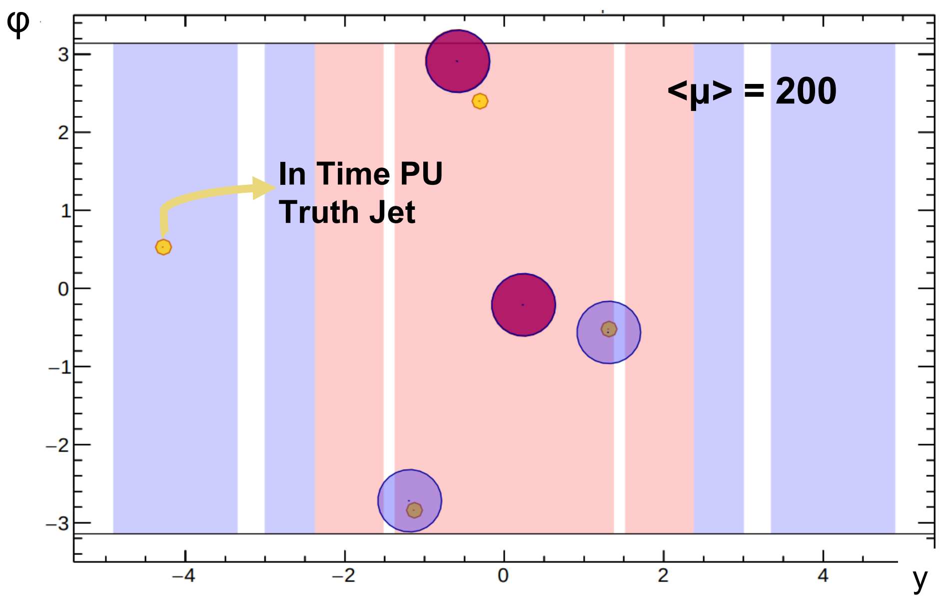
Single vs. multi-vertex

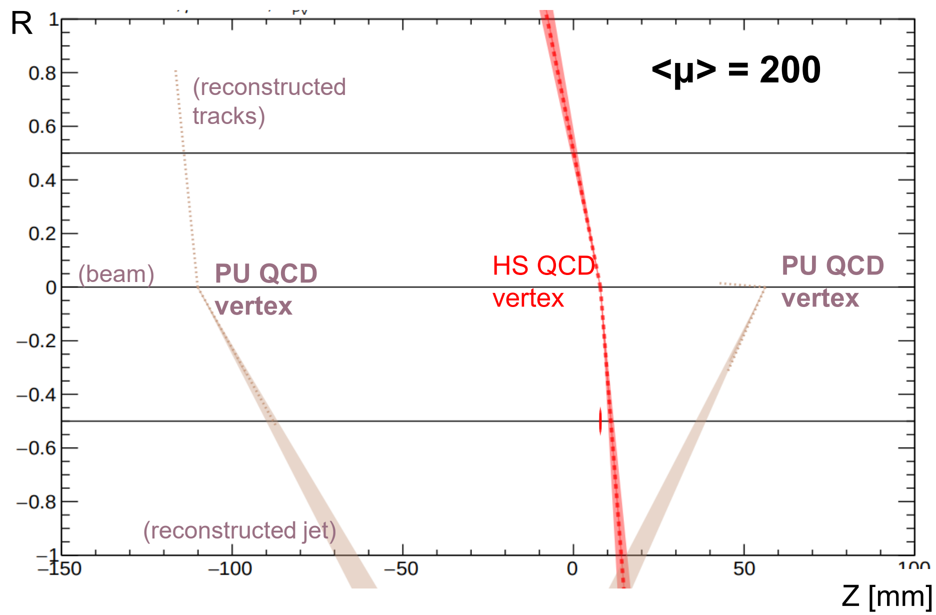
Signal: 4 jets from a single vertex





Background: 4 jets from multiple vertices





Single vs. multi-vertex

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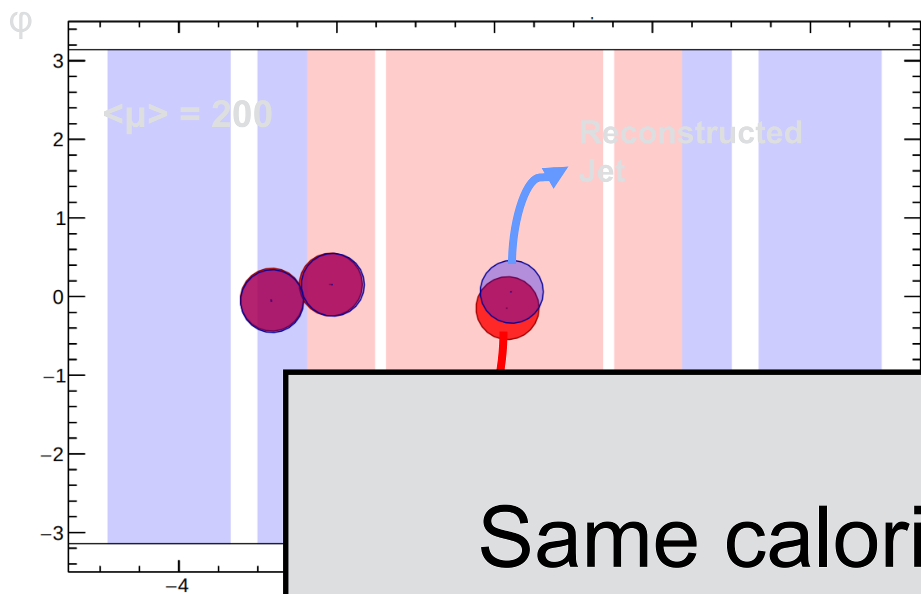
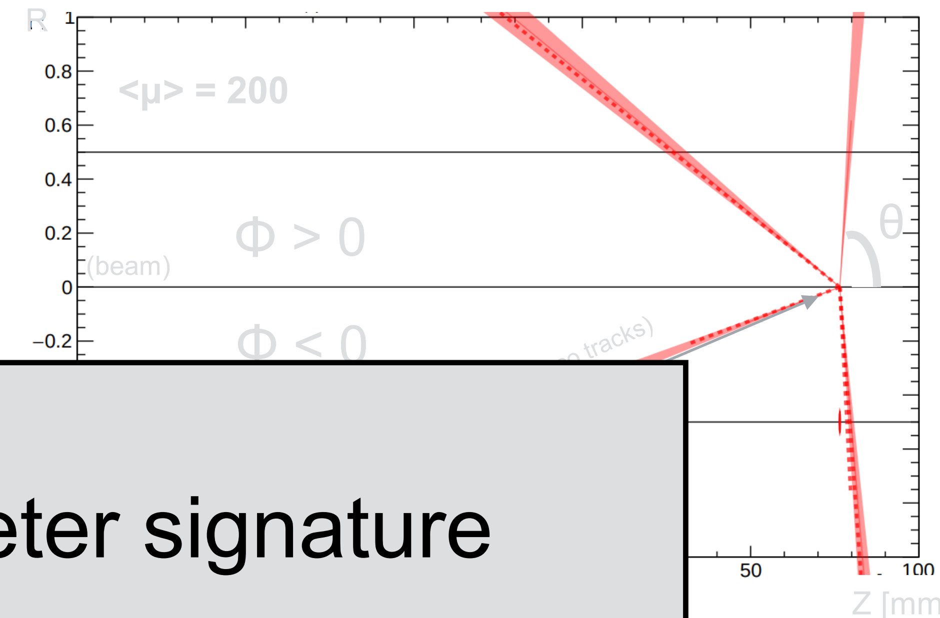
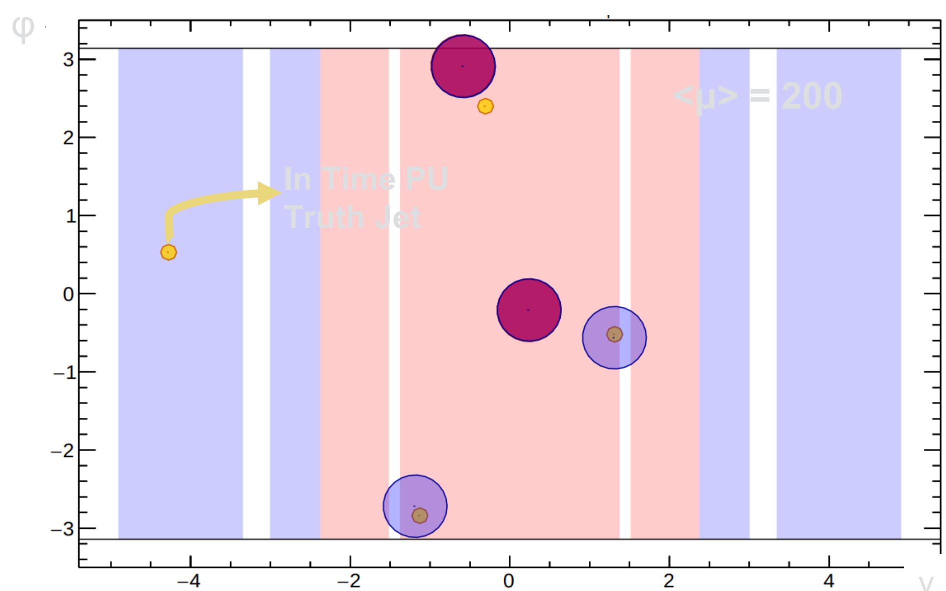
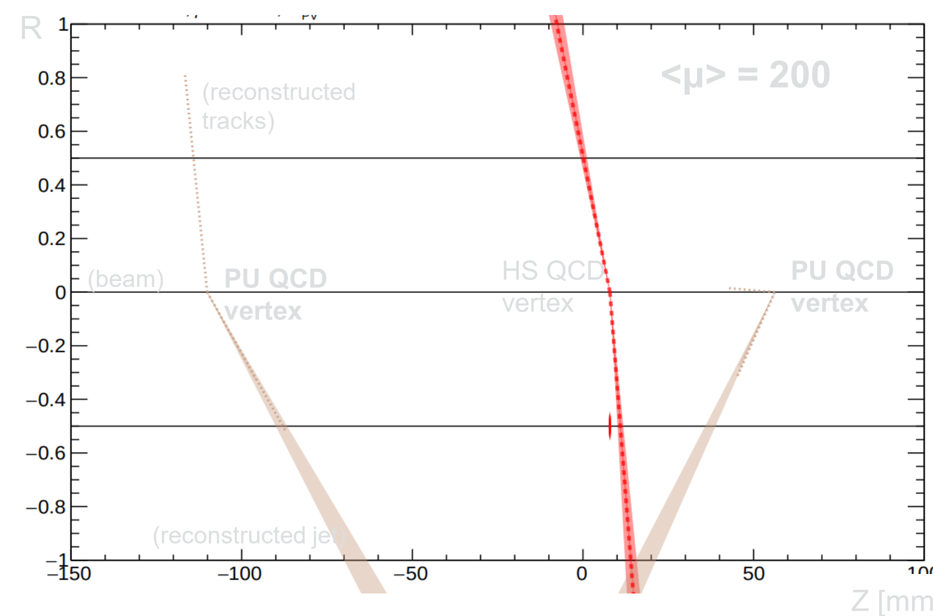
Signal: 4 jets from a single vertex





Same calorimeter signature





Event composition (4+ jets)

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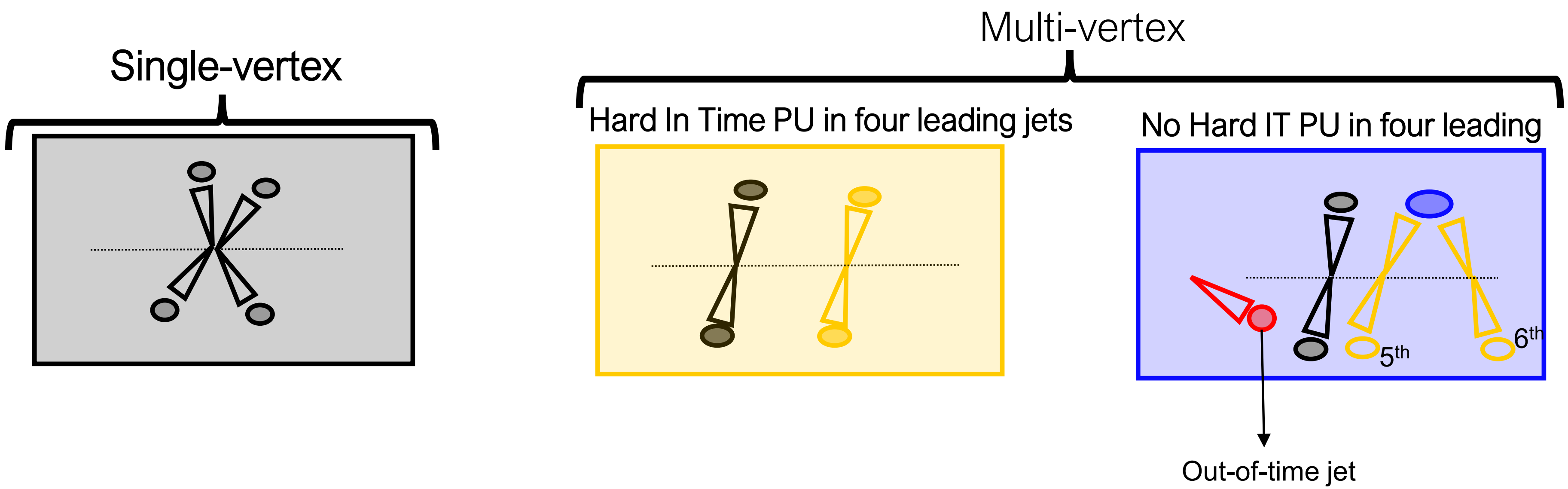
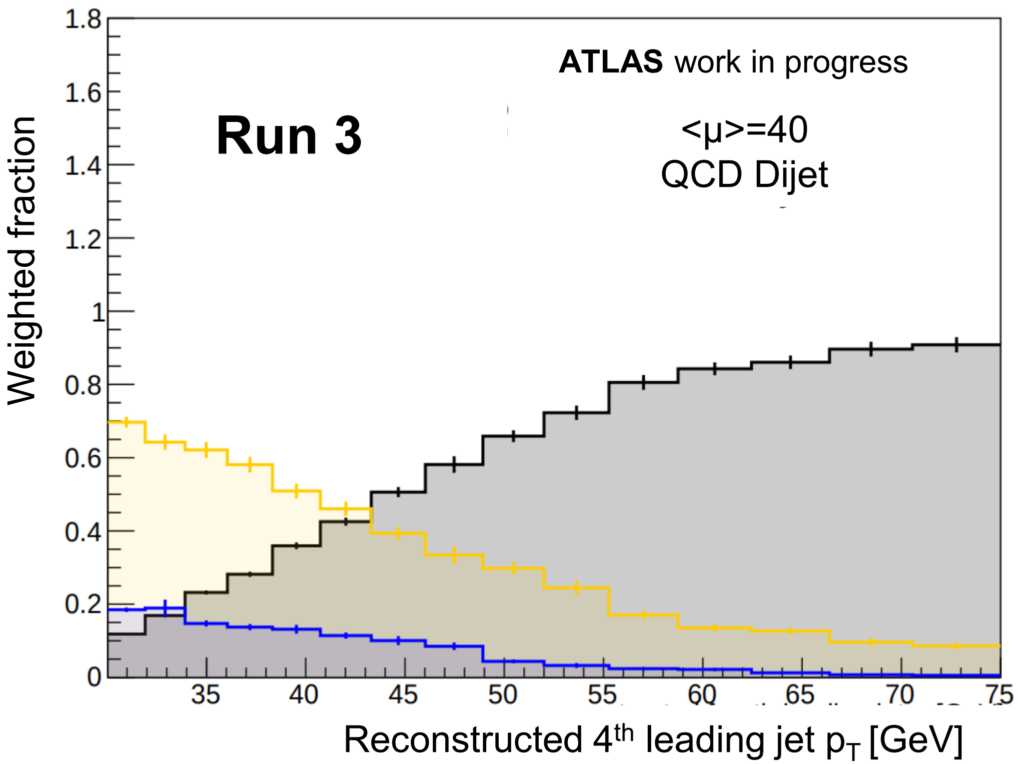
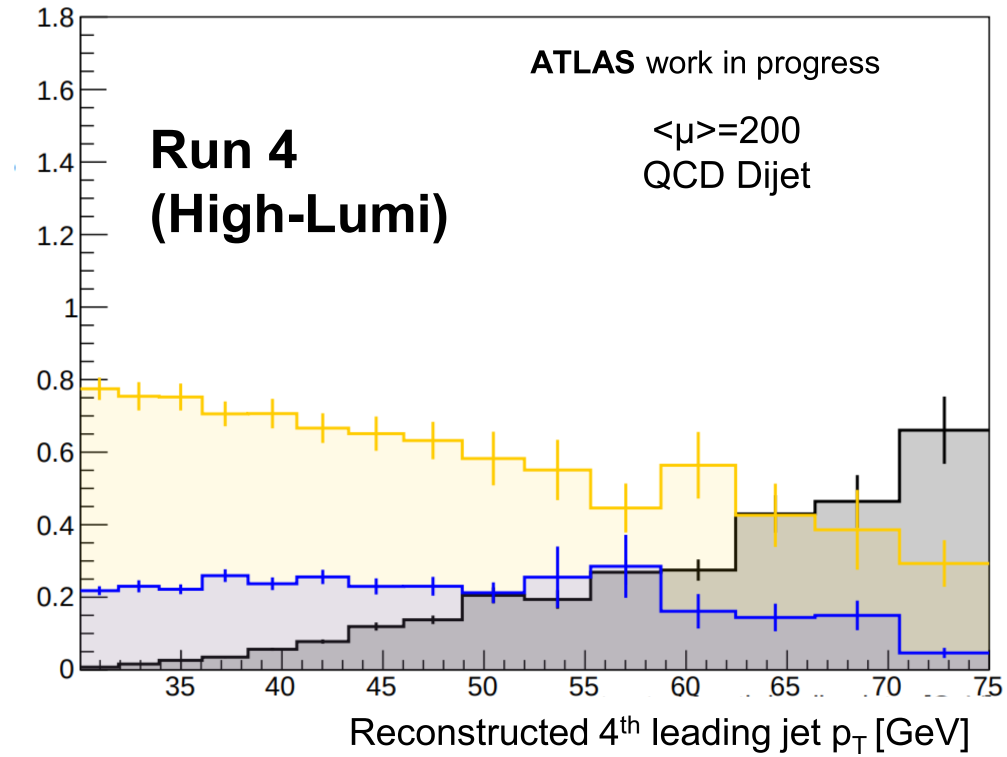






Trigger strategy: BDTs to classify

Why ML?

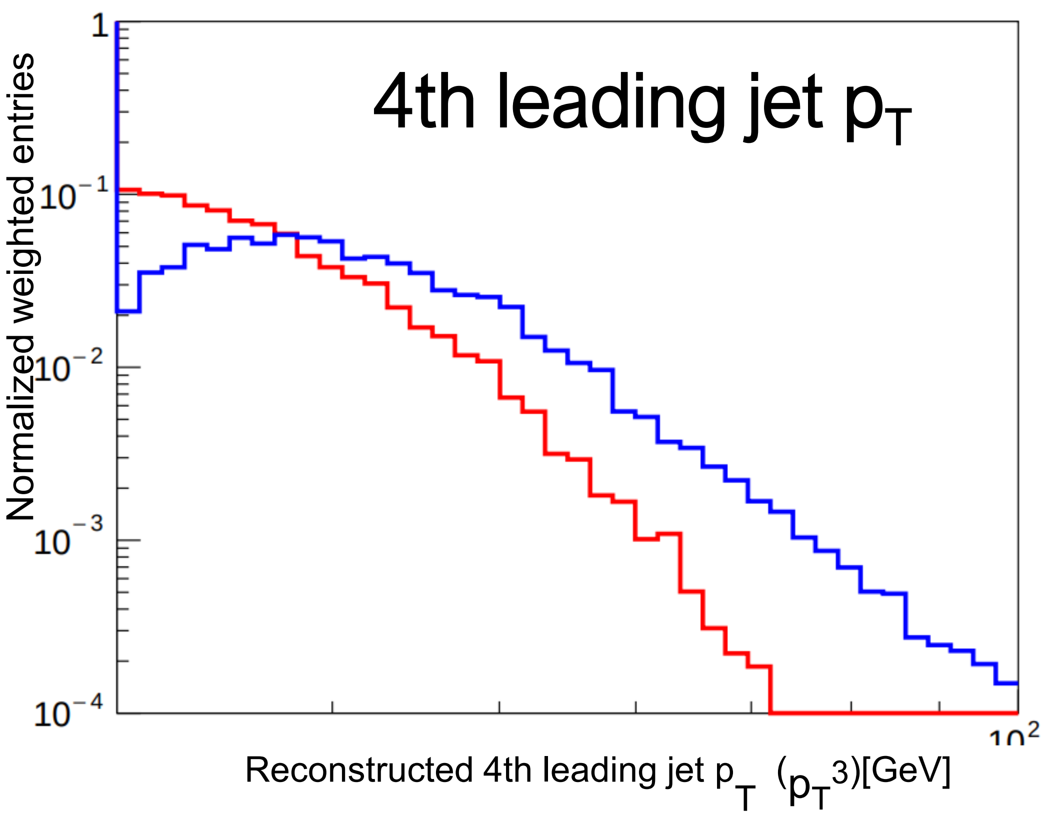
- Current methods allow abundant hard QCD PU contamination
- Level 0: no track or vertex information
- Topological variables suggest ML can do the classification

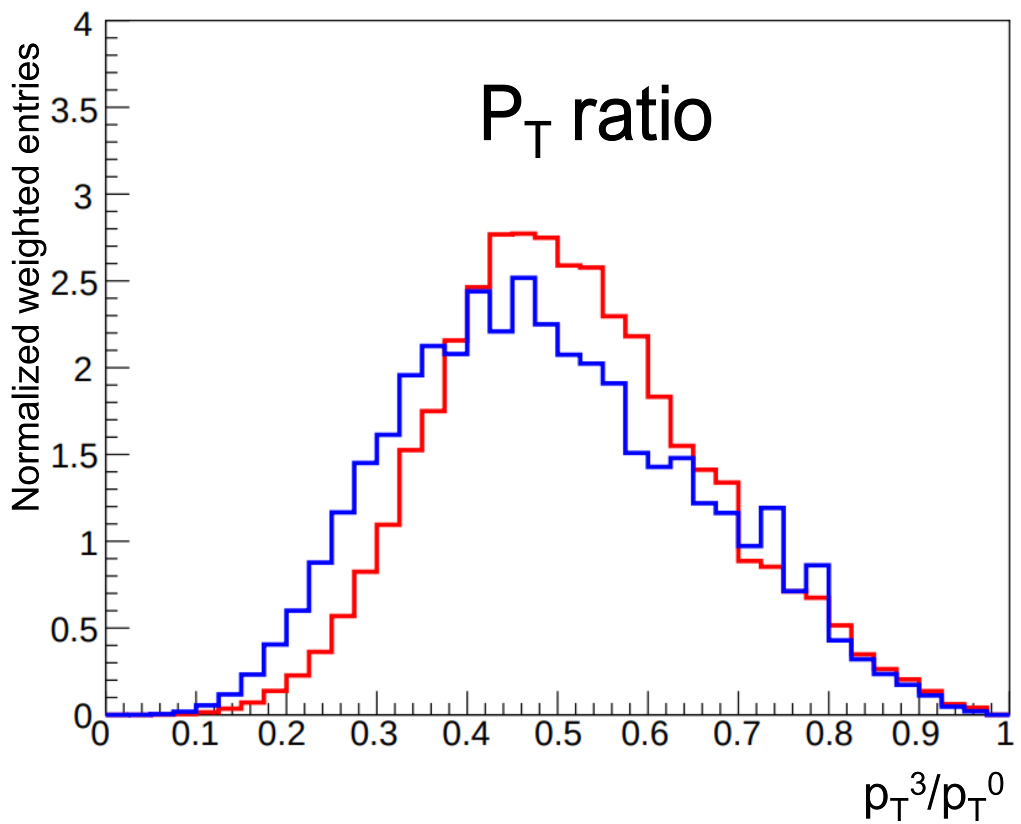
Why BDTs?

- Low latency and good performance
- Efficient infrastructure for FPGA implementation using TMVA, fwXmachina (fwx.pitt.edu) and Vivado

BDT inputs

- Kinematics: (P_T, η, φ) , P_T ratios , Δφ
- Training:
  - Signal: QCD Single vertex
  - Background: QCD Multi-vertex





BDT performance

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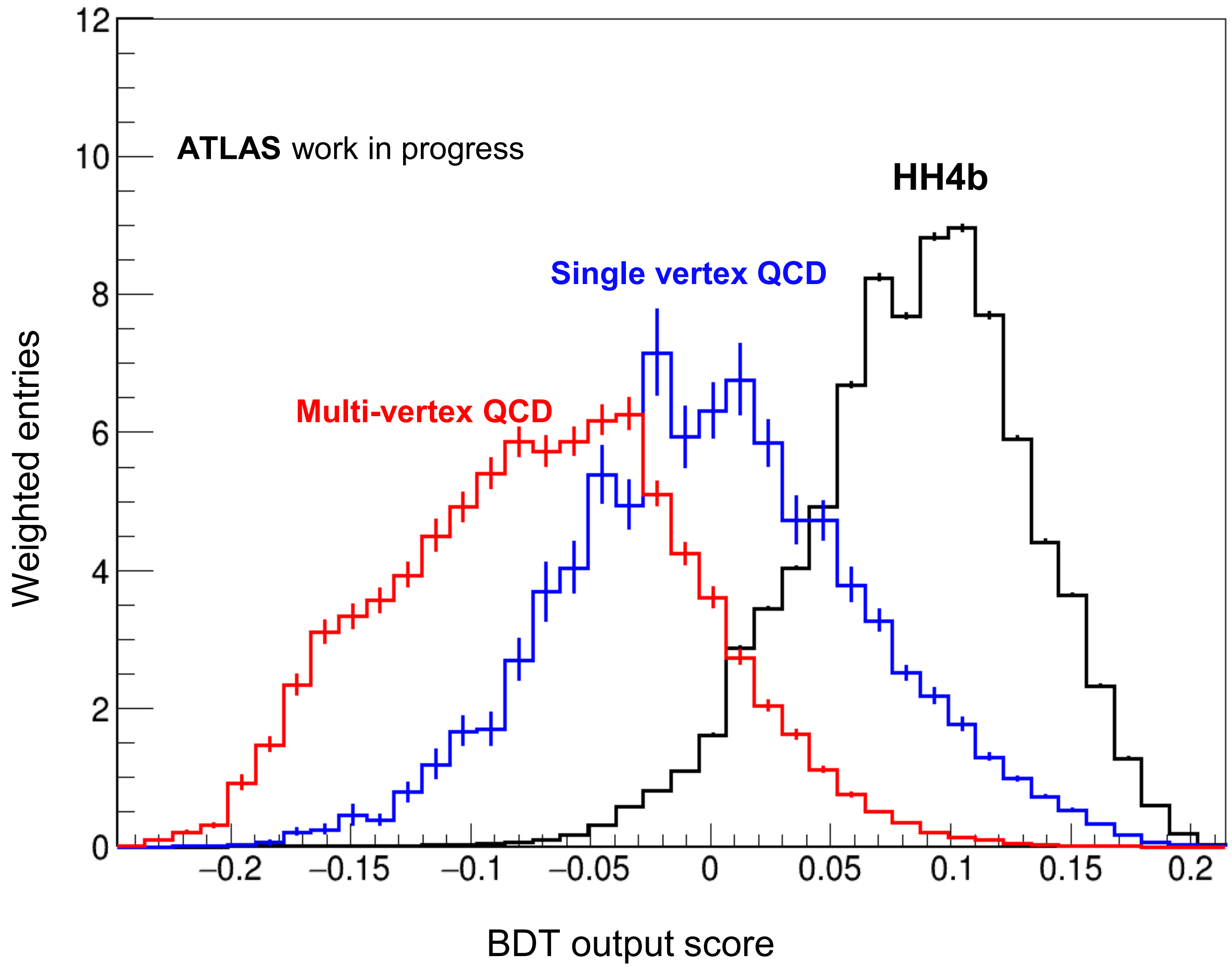
Training
- Signal: QCD Single vertex
- Background: QCD Multi-vertex

Testing
- Signal: HH4b sample
- Background: QCD dijet sample



BDT performance (2)

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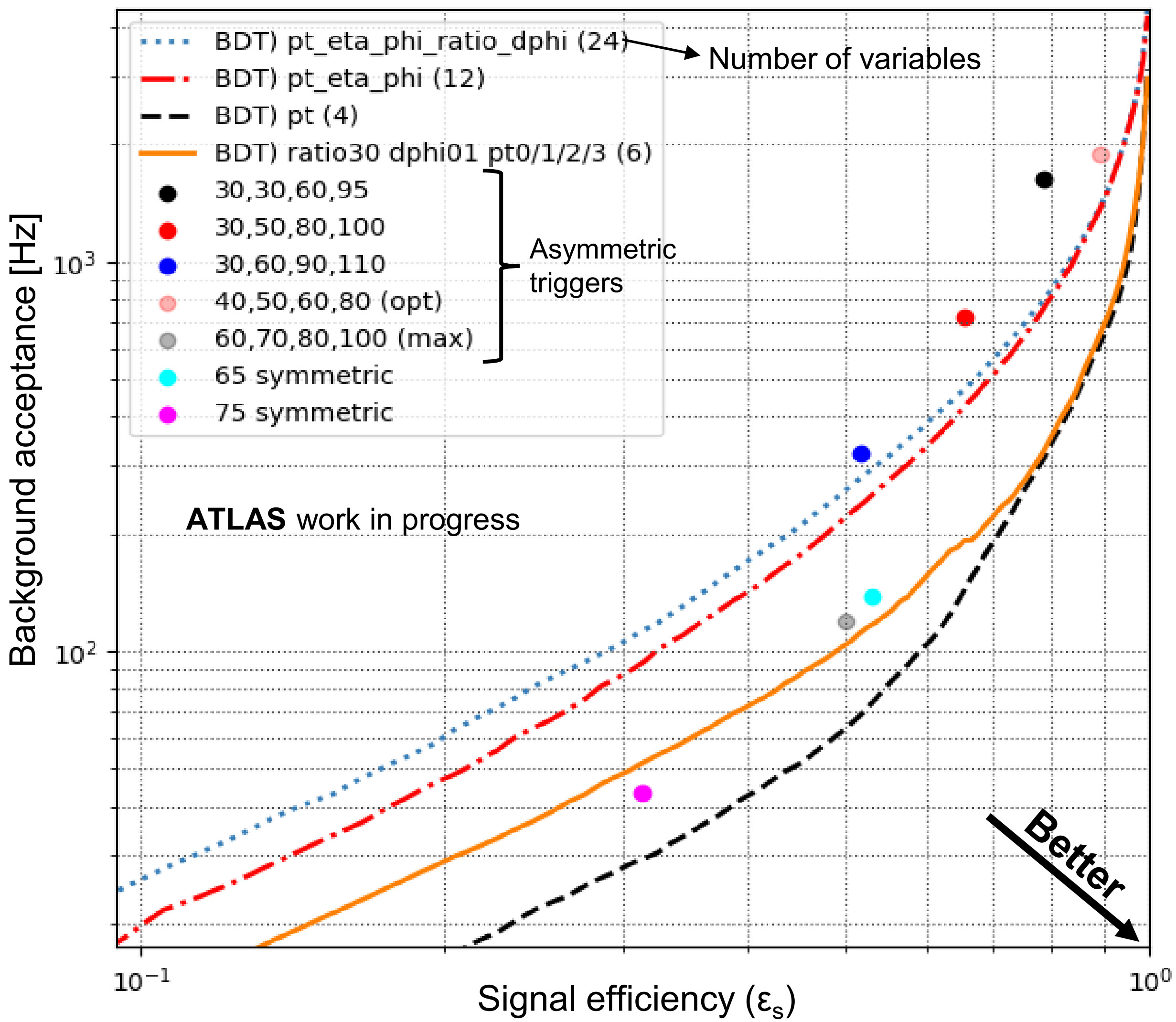
Training
- Signal: QCD Single vertex
- Background: QCD Multi-vertex

Testing
- Signal: HH4b sample
- Background: QCD dijet sample



FPGA implementation

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- With fwX and VitisHLS, different BDT configurations were synthesized
- Targeted FPGA: Virtex Ultrascale+ VCU118

1 clock tick = 3.125ns

Nvariables	Ntrees	Flip Flops	Look Up Tables	Latency (cycles)	II (cycles)
8	120	4136	56339	6	1
8	200	8540	96489	6	1
12	120	8543	65702	7	1
12	200	17207	112152	7	1
24	10	219	2757	4	1
24	60	2371	30097	7	1
24	200	11692	103113	7	1

<1% of board (Flip Flops)

<10% of board (Look Up Tables)

< 22ns (Latency)

Conclusion

- Special treatment at L0 of this new “Hard-QCD PU” is needed
- Preliminary results: BDT has better performance than asymmetric triggers
- FPGA implementation is feasible → <u>very low latency and resource usage</u>
- <u>Next steps</u>: Study the effect of multiple high energy vertices on Run 3 data (of high $\langle\mu\rangle$=50/60).

Thank you!

Backup

Single vertex event

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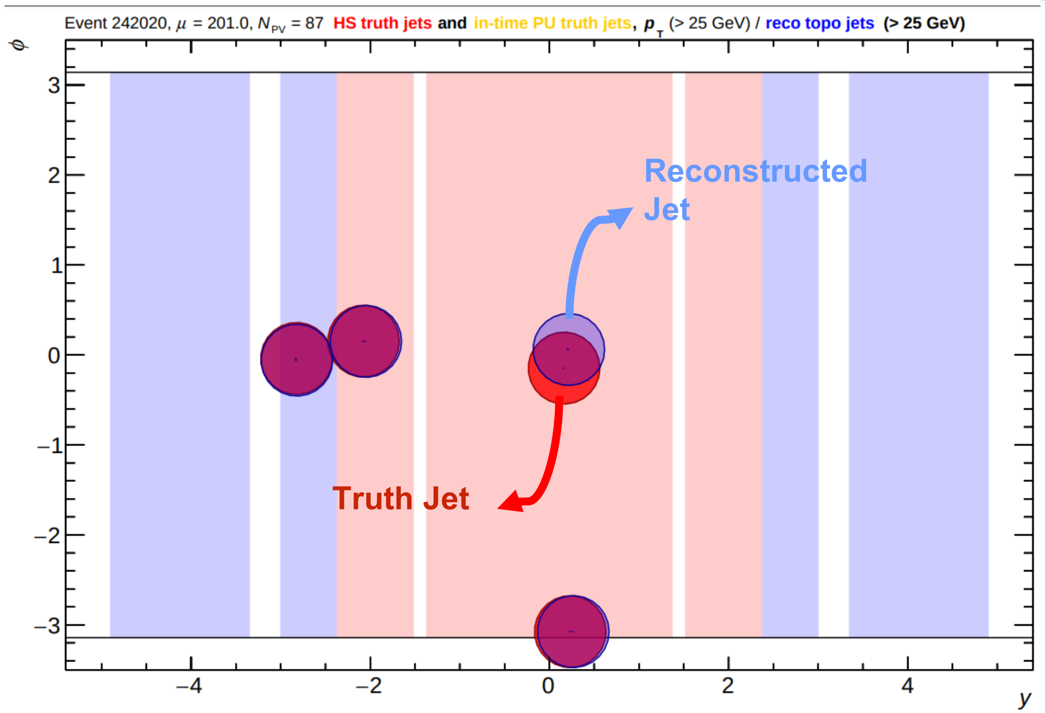
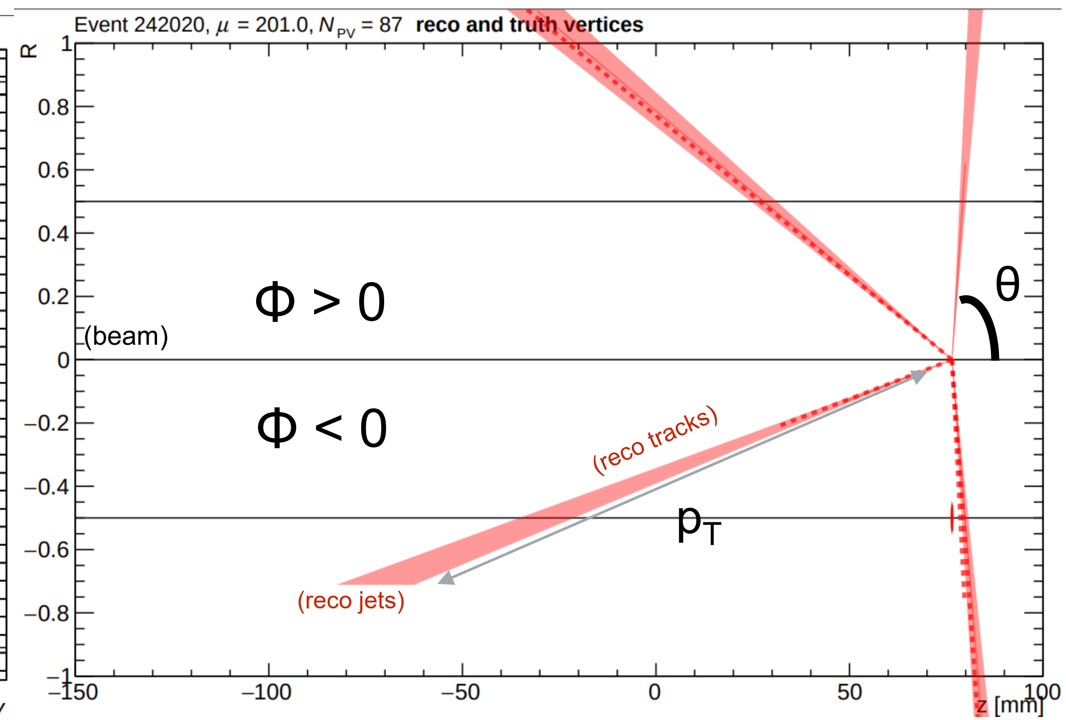
- Single vertex events are our signal.

- Interesting for HH→4b analysis or other physics with 4 jets in the final state





- This event will pass a Level 0 trigger of 4 jets with P_T>25GeV

Multi-vertex event

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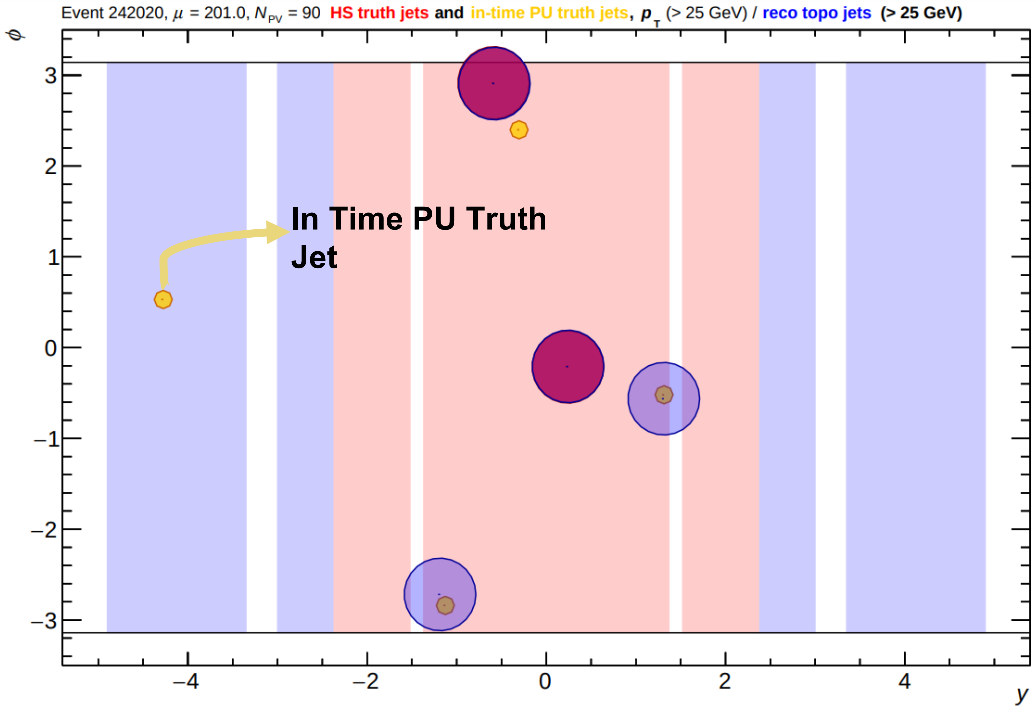
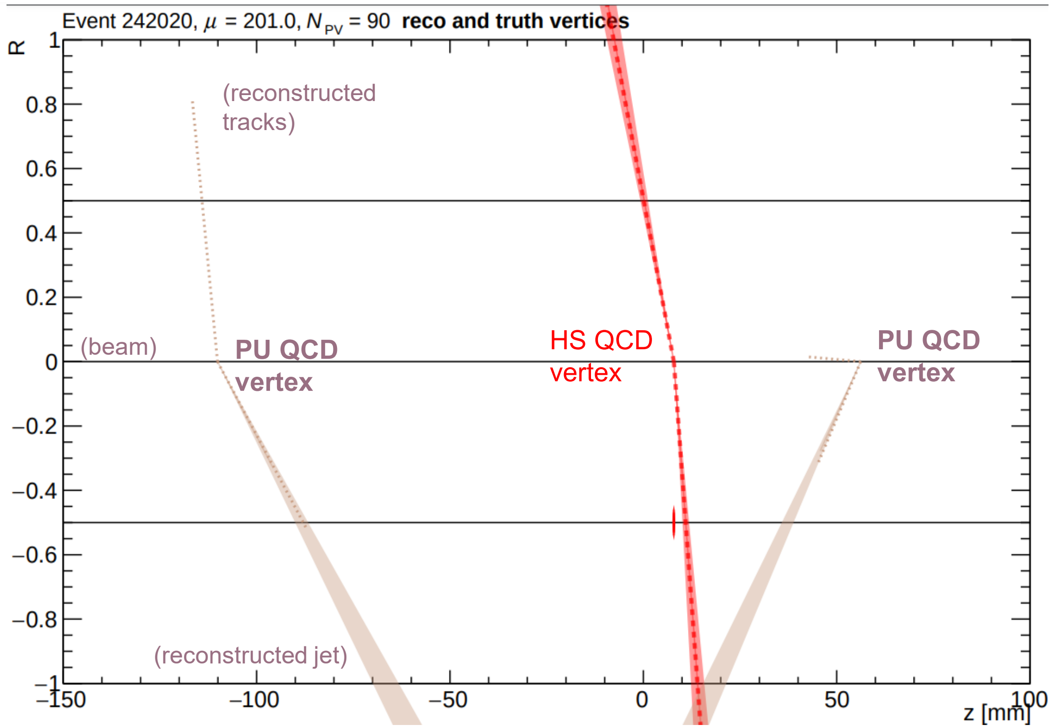




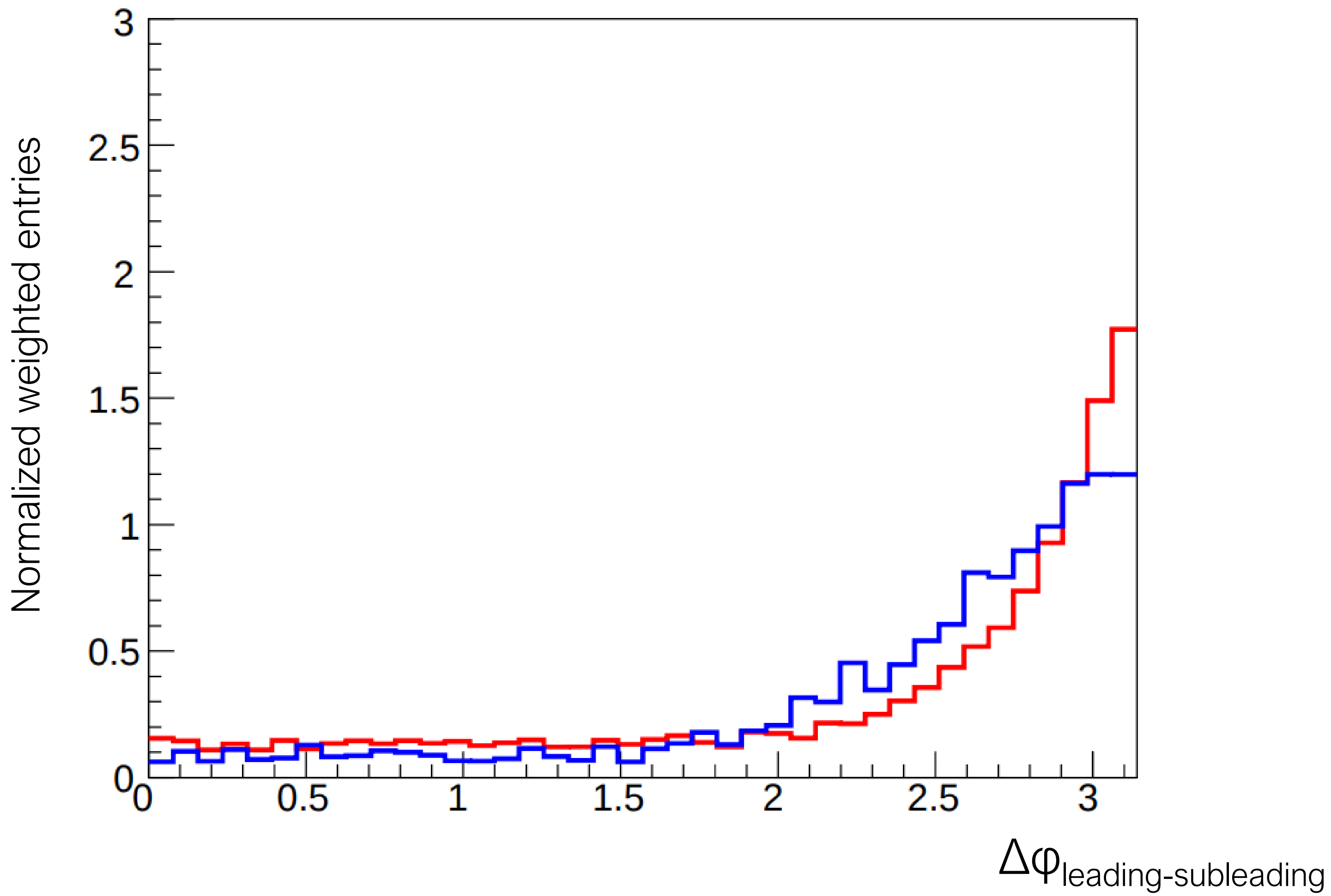
- It is a dijet QCD event ⟹ we want to eliminate it.

- Same calorimeter signature as single-vertex. It will <u>also</u> pass a Level 0 trigger of 4 jets with P_T>25GeV.

⟹ new trigger is needed.

BDT inputs (2): Δφ

- Training:
  - Signal: QCD Single vertex
  - Background: QCD Multi-vertex



BDT performance (3)

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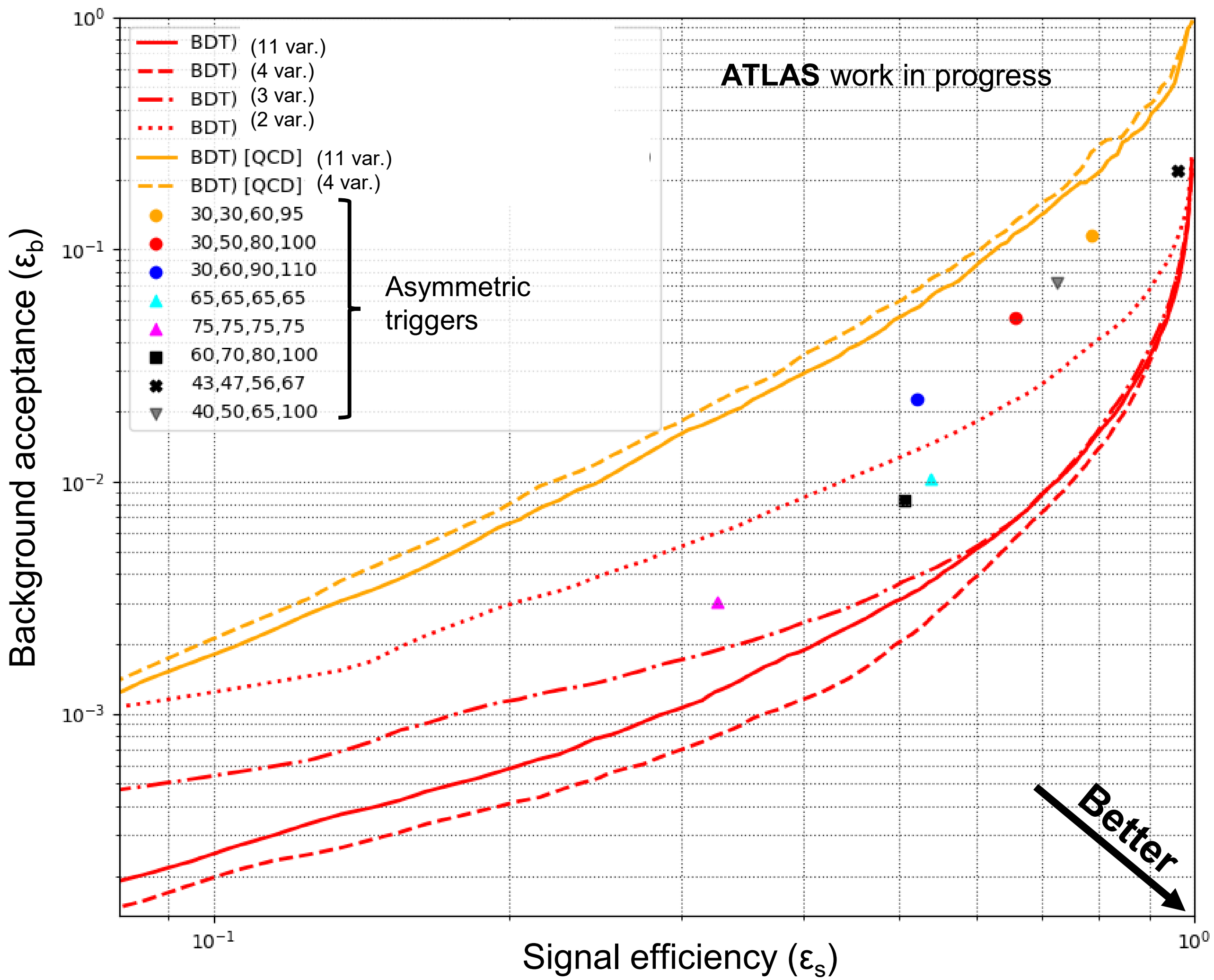
- Red curves: Training with QCD, testing with HH4b
- Orange curves: Training and testing with QCD Dijet samples.



FPGA implementation (2)

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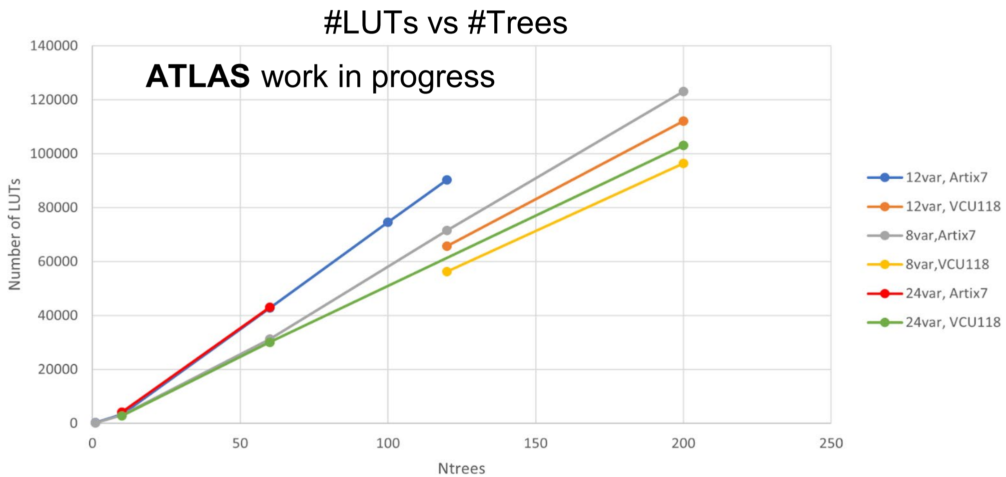
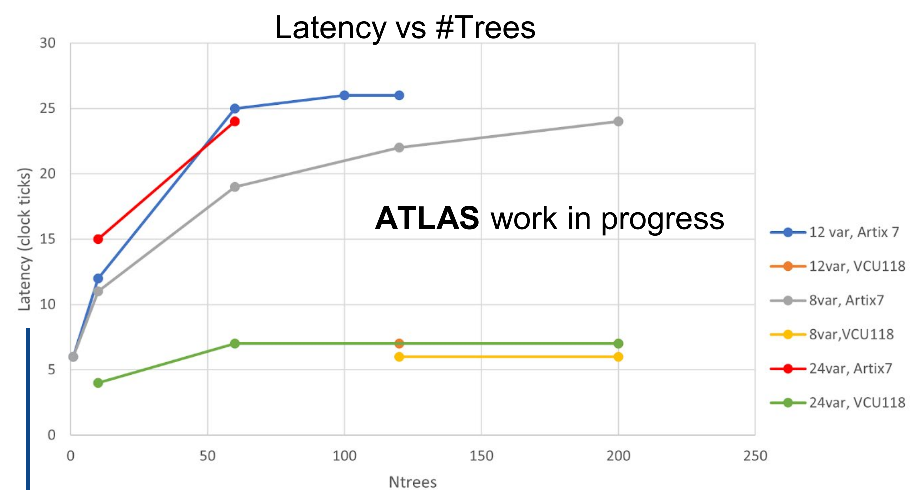
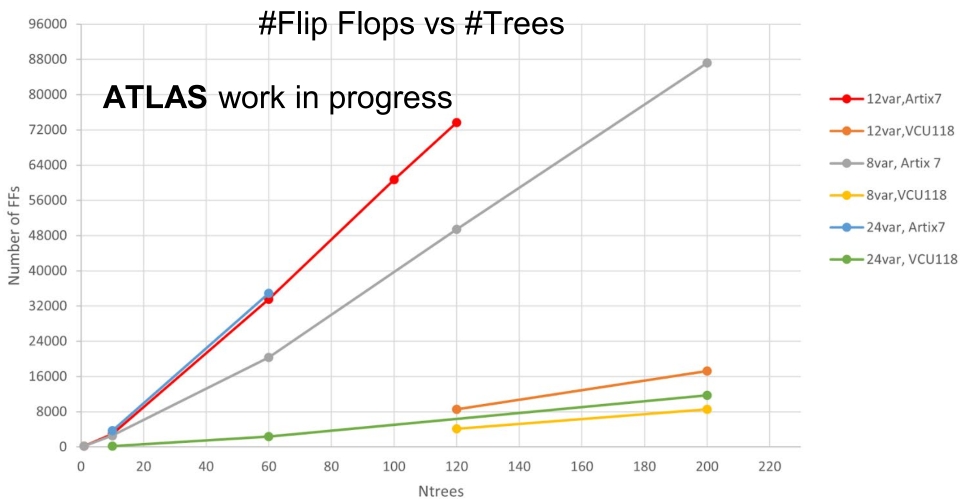
- With fwX and VitisHLS, different BDT configurations were synthesized.
- Targeted FPGA: Virtex Ultrascale+ family (VCU118)





1 clock tick = 3.125ns (320 MHz)



FPGA	Nvariables	Ntrees	Flip Flops	Look Up Tables	Latency(cycles)	II (cycles)
VCU118	8	200	8540	96489	6	1
	12	120	8543	65702	7	1
	24	60	2371	30097	7	1
	24	200	11692	103113	7	1
Artix7	8	200	87235	123142	24	1
	12	120	73676	90327	26	1
	24	60	34911	43097	24	1