Pattern recognition demo FPGA - LabVIEW

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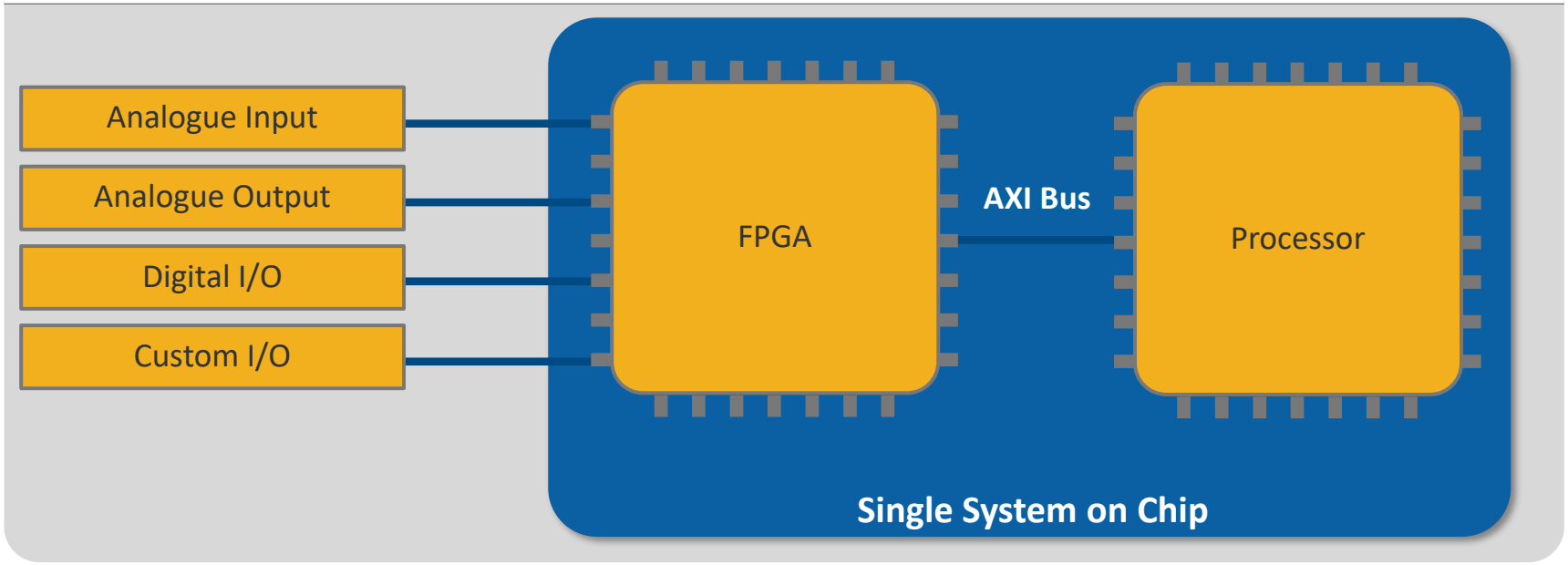
NI myRIO Product Overview: Front View

XILINX Zynq SoC

- Small Size, Low Power
- 667 MHz Dual-Core ARM Cortex-A9 Processor
- Artix-7 FPGA, 28k logic cells
- 16 DMA Channels
- 92 Billion calculations per second

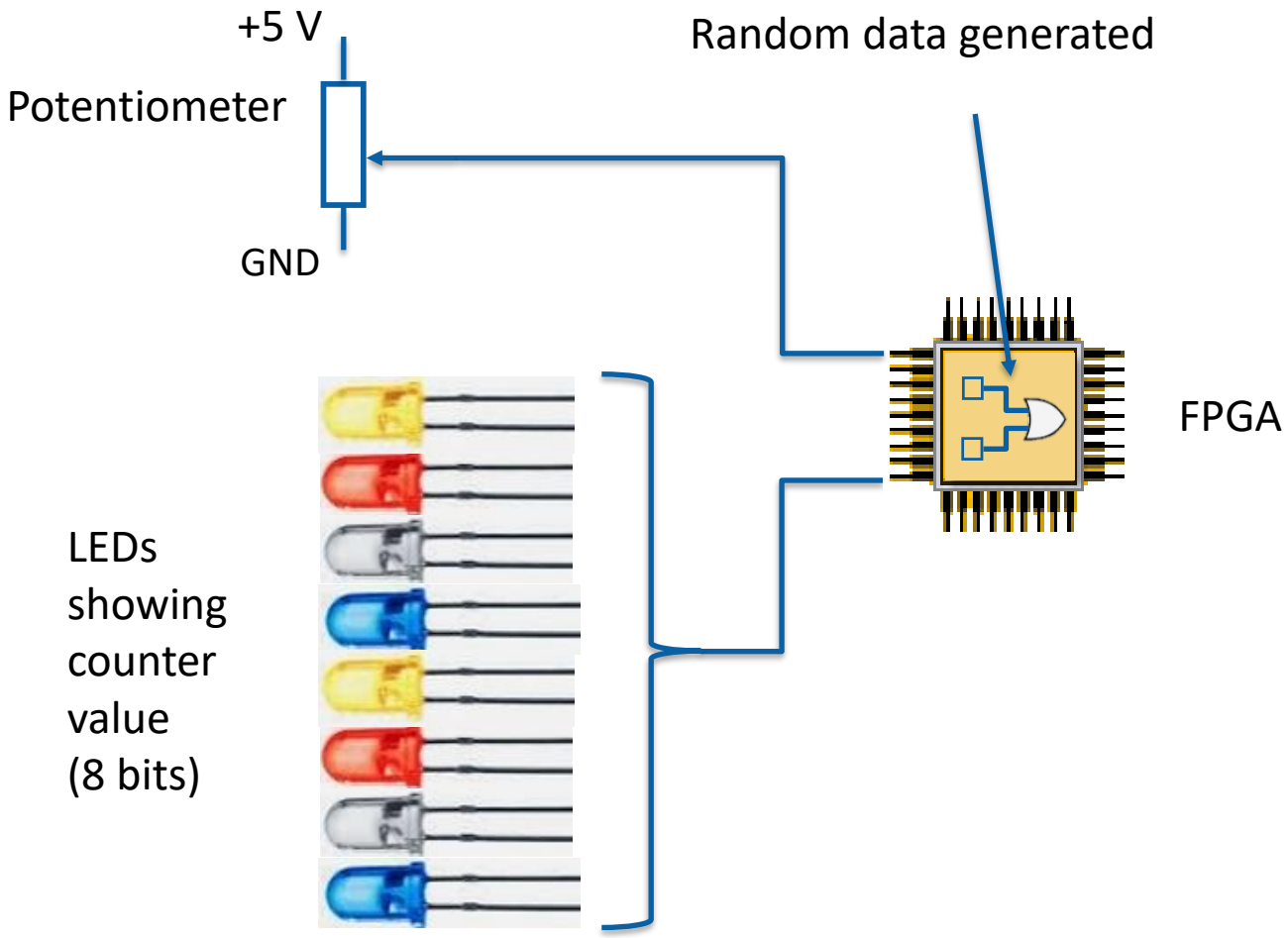
What is Zynq?

Traditional Implementation



Pattern recognition demo

"Finding a needle in a haystack"



Pattern recognition demo

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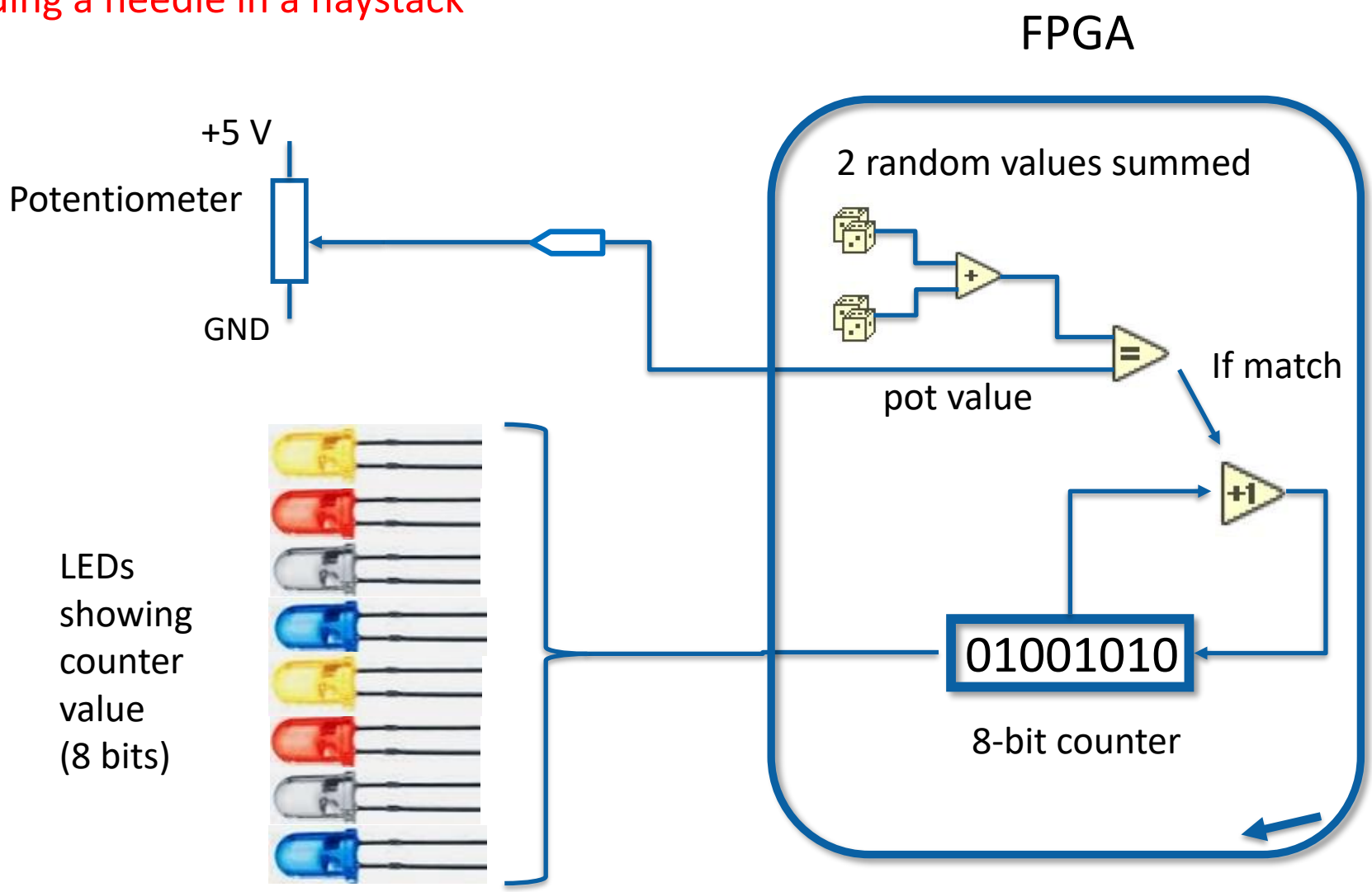
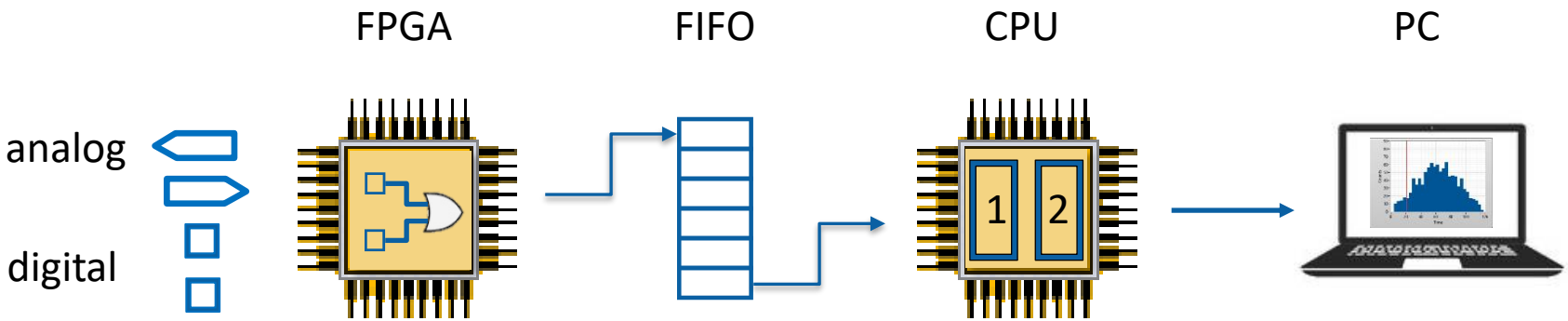
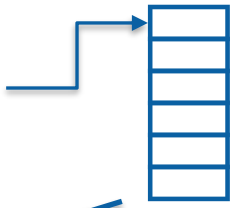


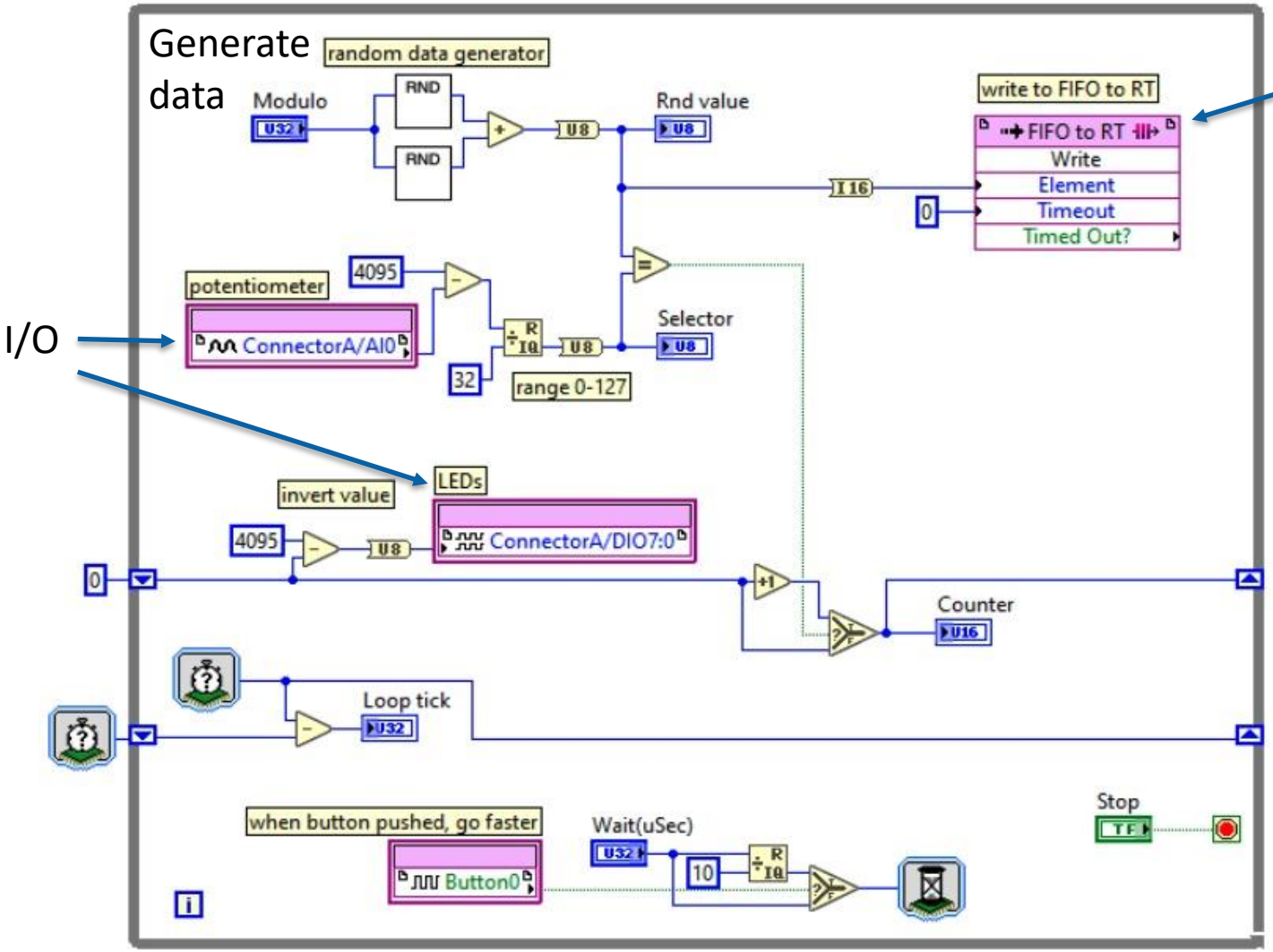
Pattern recognition demo

Data flow FPGA -> ARM -> PC

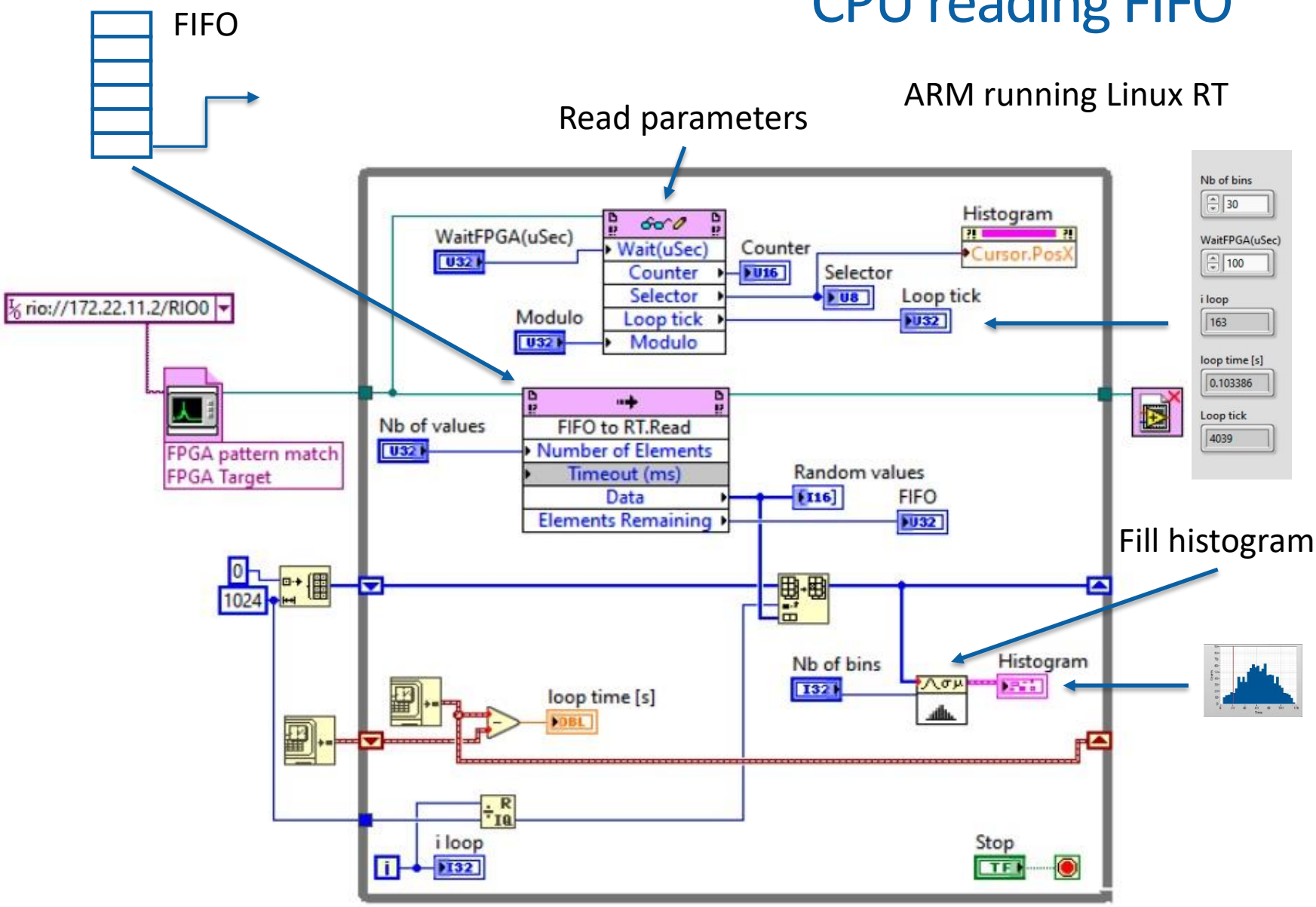


FPGA filling the FIFO

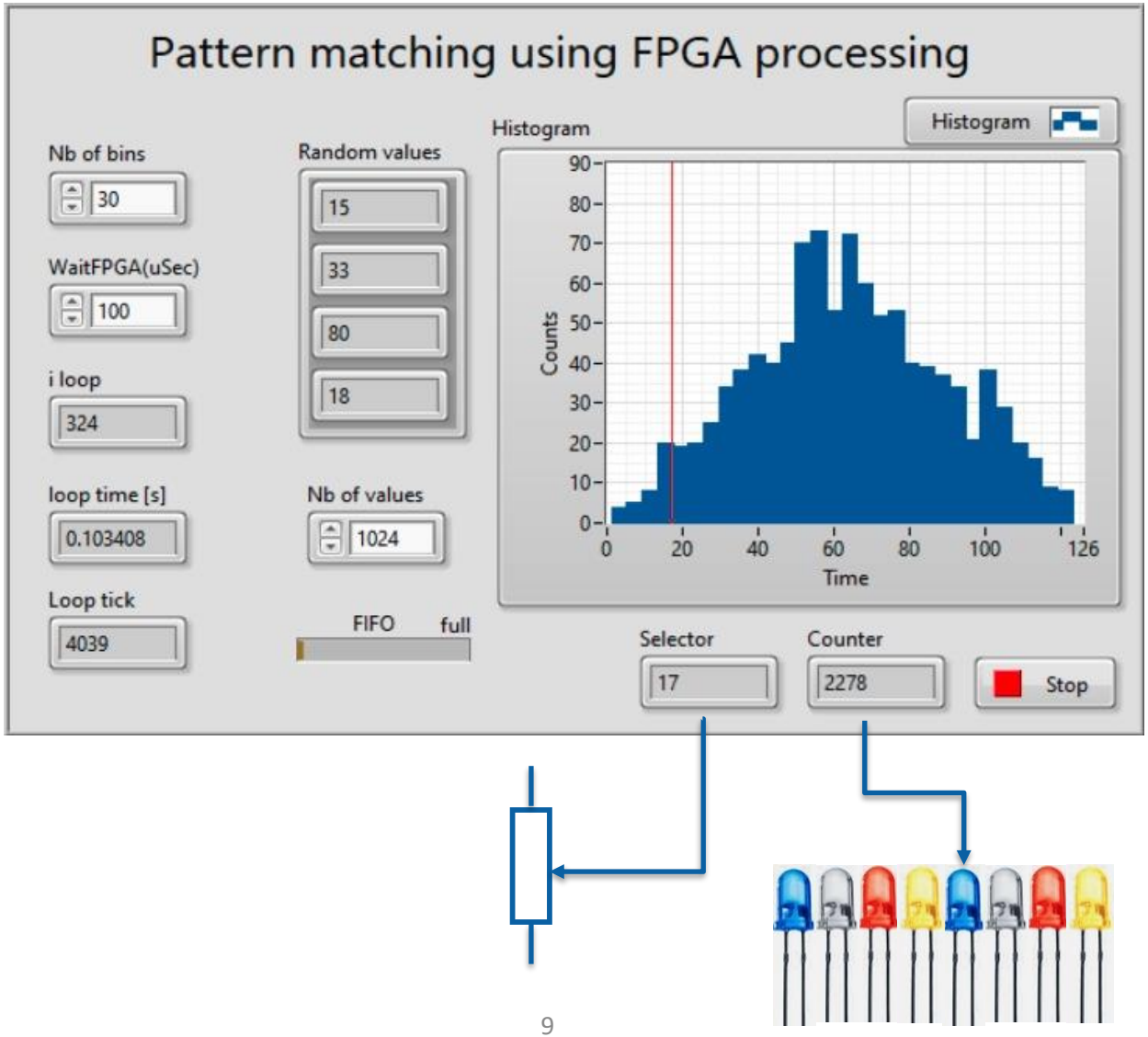




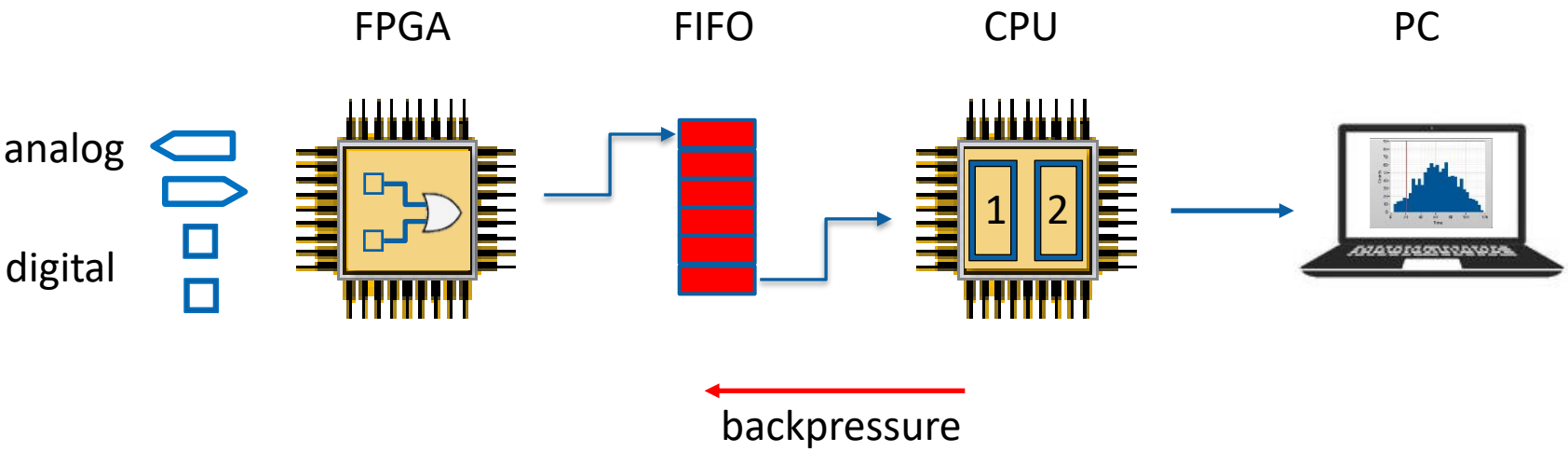
CPU reading FIFO



Display on PC



Backpressure from ARM processor



1. If CPU too slow to empty FIFO
2. FIFO will fill up
3. When FIFO full, data will be lost