

Electrical Performance of a Silicon Microstrip Super-Module Prototype for the High-Luminosity LHC Collider

Tuesday 6 December 2011 12:10 (20 minutes)

The Large Hadron Collider (LHC) at CERN is currently providing proton-proton collisions with continuous increase in the luminosity delivered to the experiments. ATLAS is a general purpose detector designed to fully exploit the physics potential of the LHC at a nominal luminosity of $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. It is planned to extend the LHC physics programme by increasing the instantaneous peak luminosity by one order of magnitude in the so-called High-Luminosity LHC (HL-LHC). For ATLAS, an upgrade scenario will require the complete replacement of its internal tracker, since the current detector will start to be inefficient due to cumulated radiation damage and the huge increase in the channel occupancy. A new all-silicon based tracker is currently being designed. Several international R&D programmes are investigating all aspects required for a successful new tracker, like radiation hardness of the silicon sensors and front-end electronics and novel power distribution schemes for the reduction of services.

The super-module concept is presented as the integration solution for the barrel strip region of the future ATLAS tracker. The minimal detecting unit is a double-sided silicon micro-strip module. It consists of two n-on-p silicon micro-strip sensors glued back to back to a central Thermo-Pyrolitical-Graphite (TPG) baseboard. The TPG provides mechanical stability and ensures excellent thermal contact for optimum heat dissipation. Two aluminum-nitride facing plates located at each far-end of the baseboard and four hybrids, two per module side, are bridged on top of the facings so that the hybrids are not only thermally decoupled from the silicon detectors but also any electro-mechanical damages to the sensors are being minimized. Each hybrid contains 20 readout ABCN25 ASICs. The heat generated from the front-end electronics and the detector is transferred to the cooling pipes located in the lateral sides of a light-weight carbon-carbon support structure in which the modules are mounted.

Several double-sided silicon micro-strip module prototypes have been integrated into a common support-structure, so called Super-Module. The digital voltage for the readout ASICs is provided by prototype SM01C DC-DC converters. For each hybrid, a Buffer-Control-Chip (BCC) multiplexes the data-signals from the two columns of ABCN25 chips into a single data-stream running up to 160 Mbps. Three different services buses have been produced at CERN and are used in the Super-Module. The Data-bus is used to drive the common LVDS signals to control both the BCCs and the ABCN25 ASICs, and to receive each multiplexed data-stream coming from up to 16 BCCs. A high-voltage bus is used to bias each sensor individually and a Low-voltage bus for powering the DC-DC converters. A Super-Module Board (SMB) interfaces all signals to the external DAQ.

In this talk, the latest electrical results obtained with the super-module prototype are presented.

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Session Classification: Strips

Track Classification: Strips