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Design and verification of an FPGA based bit error rate tester

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In characterizing a serial data transmission link, Bit Error Rate (BER) test provides the most stringent measurement. We will present a BER tester implementation using the Altera Stratix GX/GT signal integrity development kits. The Stratix II GX tester operates up to 6.5 Gbps and the Stratix IV GT tester operates up to 10Gbps, both in 4 duplex channels, with information of each single bit flip stored for off-line analysis. The BER testers are used in irradiation and in-lab characterization of ASICs and other components. Results from those tests will be presented as demonstration to the functionality of these BER testers.

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