清華大學工程物理系
Department of Engineering Physics, Tsinghua University

1st DRD1 Collaboration Meeting

Development of Front-end ASIC for MPGD Emphasized with TPC

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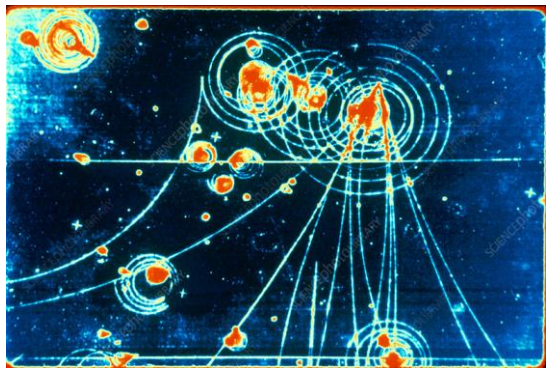
01/31/2024

CONTENTS

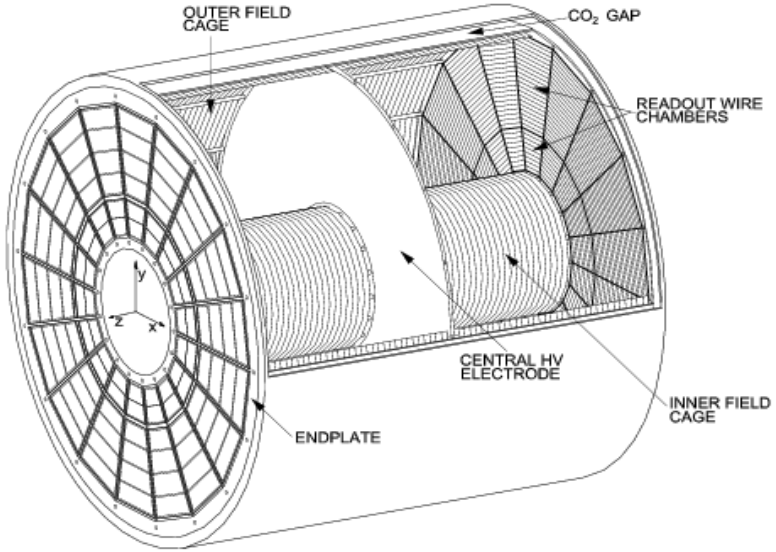
01 | Introduction

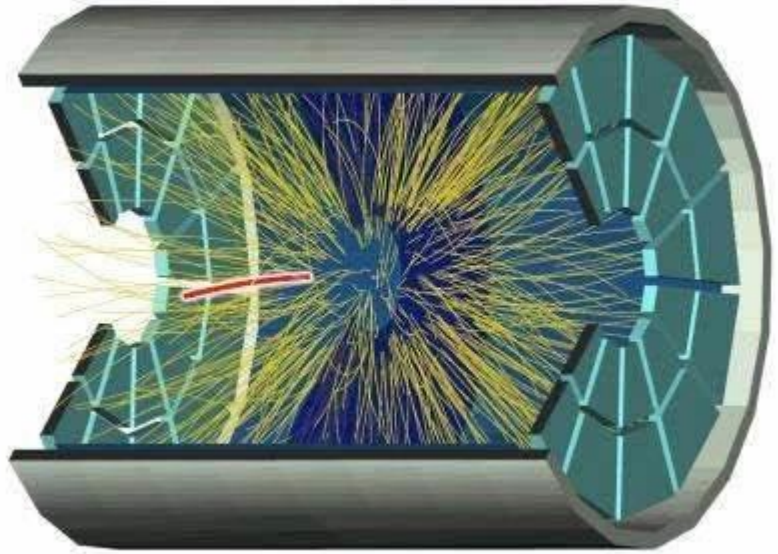
TPC: Time Projection Chamber

- Invented by David Nygren in 1970s
- TPC can provide large-volume high-precision 3D track measurement with the capability of measuring dE/dx
- TPC has been widely used in high energy particle and nuclear physics, rare event searching and astrophysics experiments



Bubble Chamber





Time Projection Chamber

MPGD: Micro-Pattern Gas Detector

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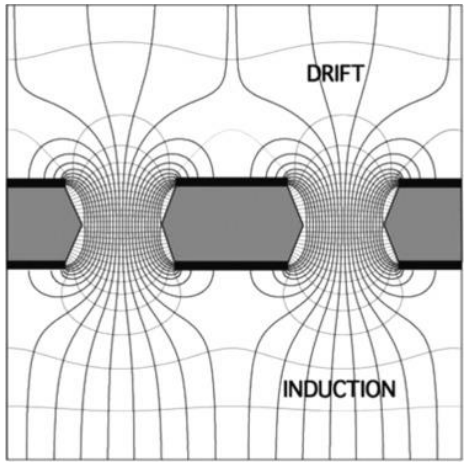
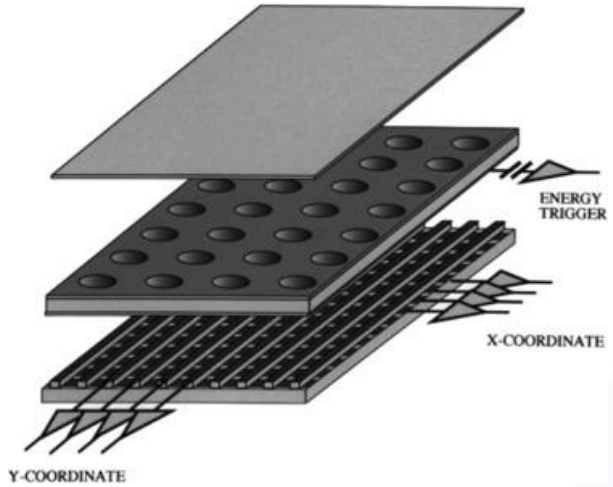
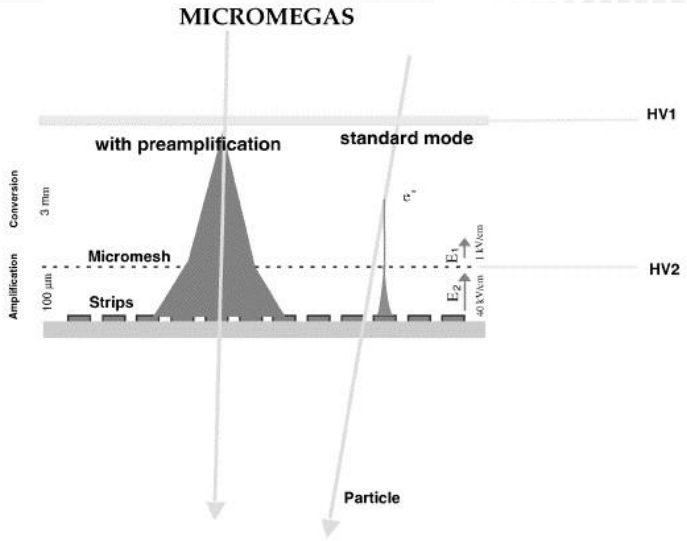
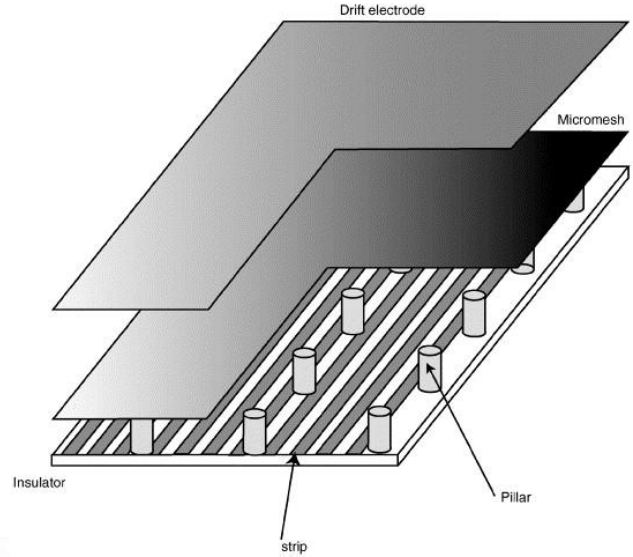
- Most recent TPC are readout by micro-pattern gas detector at the end-plate, such as GEM or MicroMEGAS
- Primary signals are amplified by MPGD with high spatial resolution and high counting rate
- Highly demanding on low power readout ASIC, especially the front-end





F. Sauli, GEM: A new concept for electron amplification in gas detectors, NIMA, Vol. 386, 1997



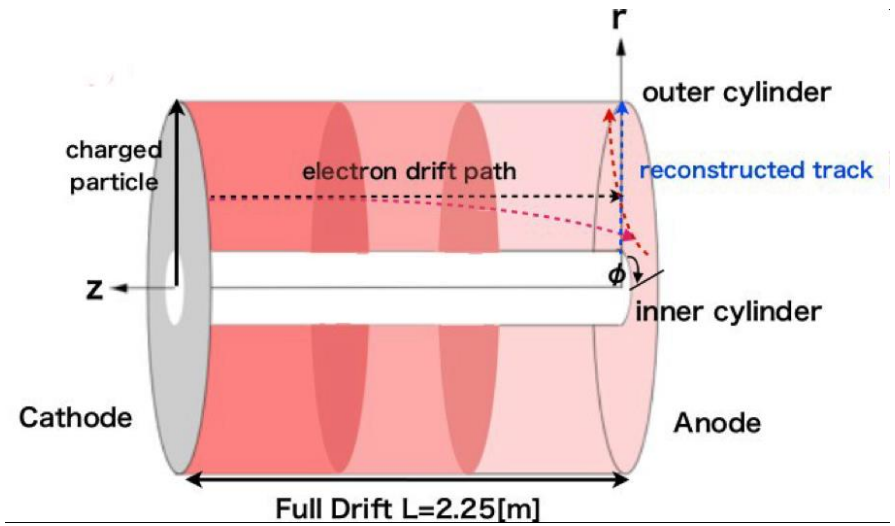


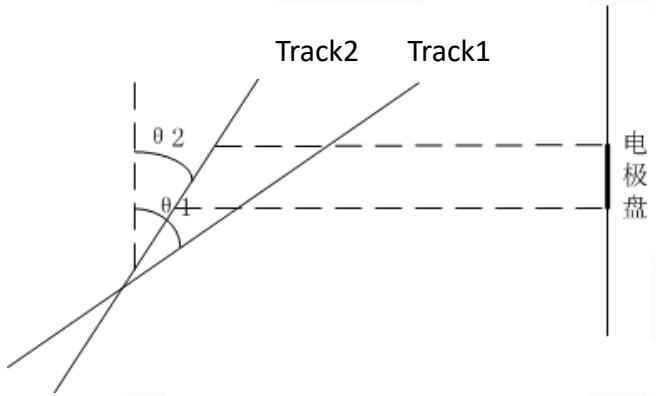
G Charpak, J Derré, Y Giomataris, Ph Rebourgeard, Micromegas, a multipurpose gaseous detector, NIMA, Vol. 478, 2002

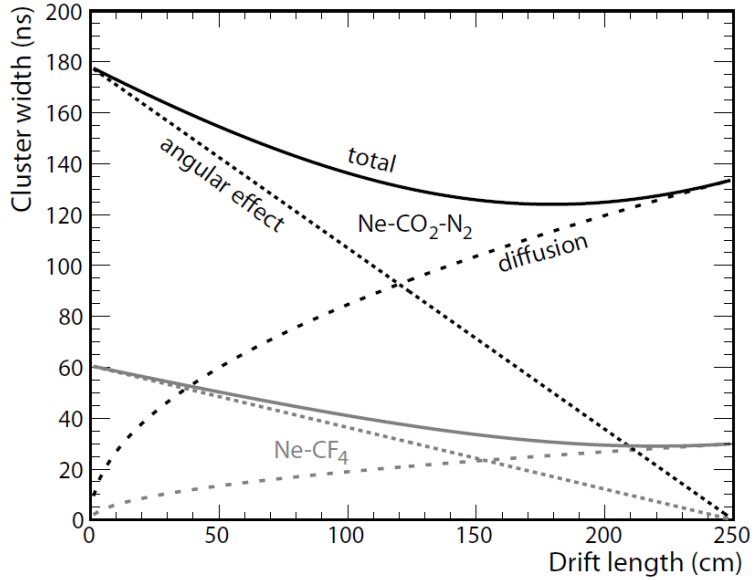
TPC Readout Requirements

- Measure energy and time simultaneously
- Variation of signal durations:
  - Parallel to charge collection panel → short
  - Vertical to charge collection panel → long
- BD (Ballistic Deficit) vs. pileup

waveform sampling







Overview of ASICs for gas detectors @ Tsinghua

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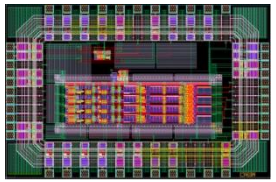
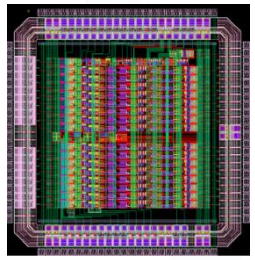
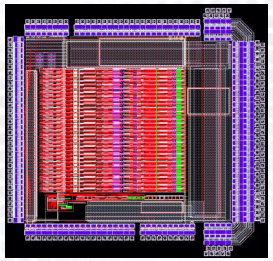
- Development starts since 2006
- From analog front-end (CASA) to SCA and ADC waveform sampling chips



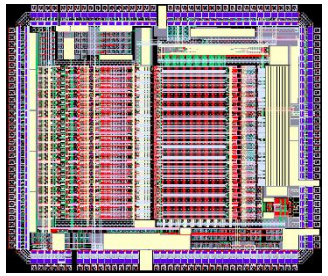
CASA: 4ch CSA+Shaper



CASAGEM: 16ch CSA+Shaper

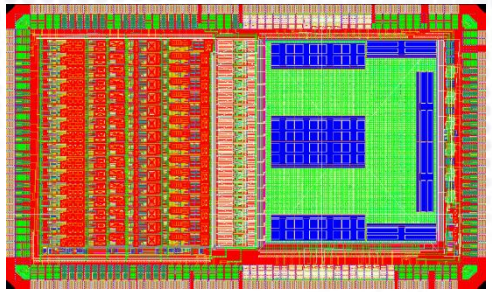


CASA32: 32ch CSA+Shaper



CASCA: 32ch CSA+Shaper+SCA

GERO: 16ch SCA



WASA: 16ch AFE+ADC+DSP

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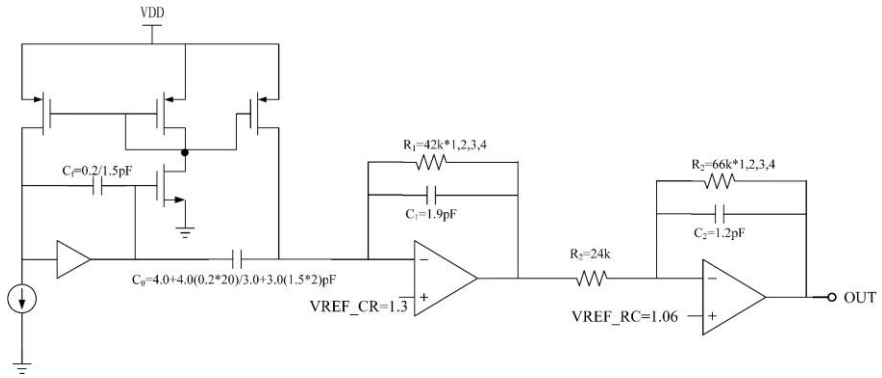
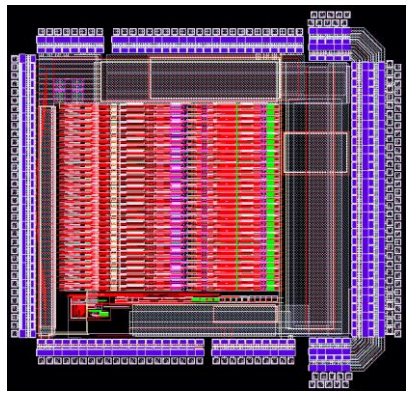
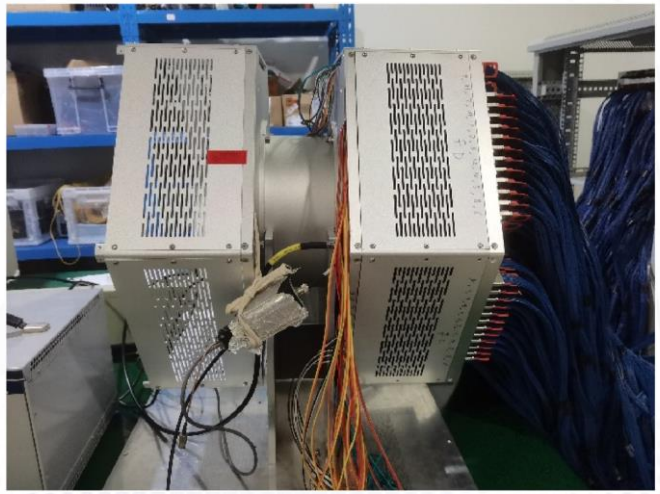
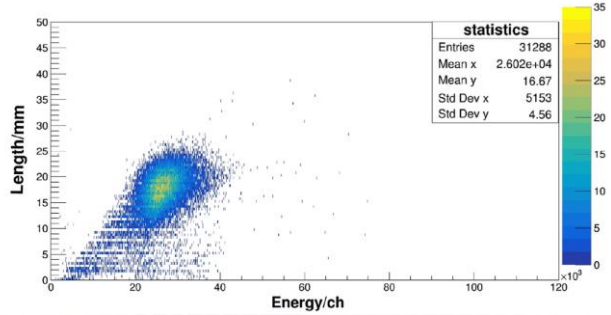
➢ Applications of CASA32 chips

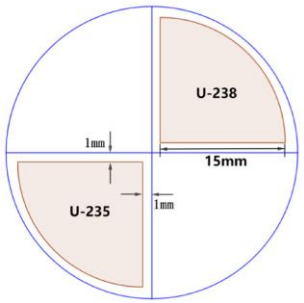


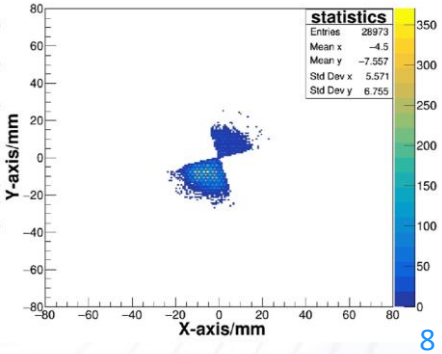


Parameters	Specs
Gain	2-40mV/fC
Shaper	CR-RC
Tp	100-400ns
ENC	<2000e @ 10pF
INL	<1%
Crosstalk	<1%
Channel no.	32









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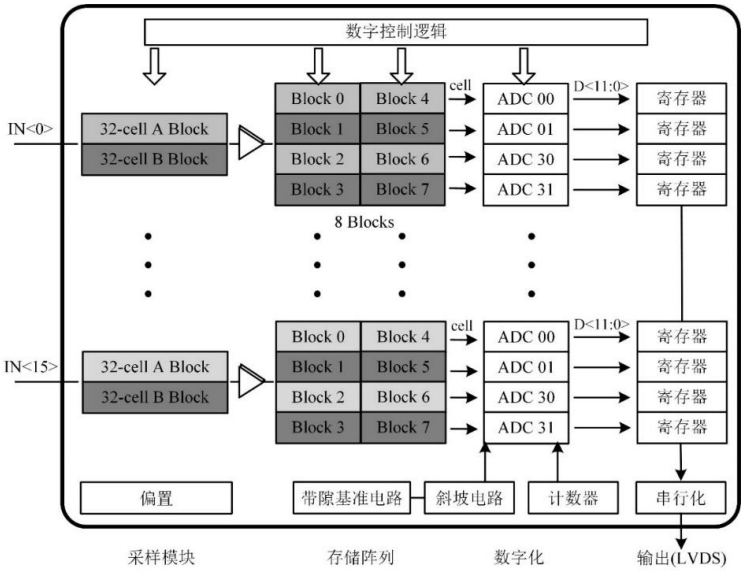
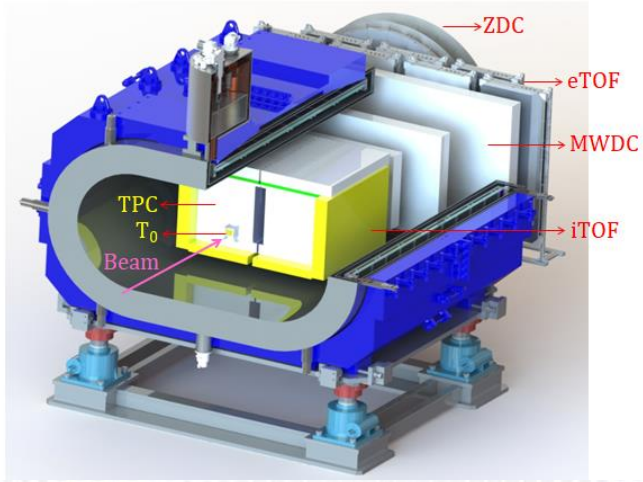
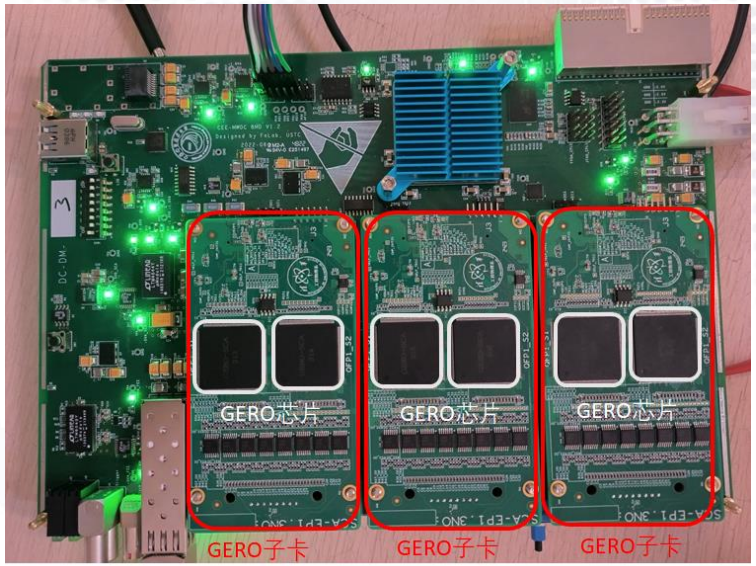
➢ Applications of the SCA chip (GERO)



parameters	specs
Power supply	1.8 V，2.5 V
Input range	0.3V - 1.3 V
Sampling rate	100 MS/s
Sampling resolution	> 10 bits
Buffer depth	256
ADC clock	100 MHz
ADC counter	12 bits
ADC conversion time	42 μs
Dead time (max.)	336 μs
Power consumption	2.3 mW/ch
Process	0.18 μm

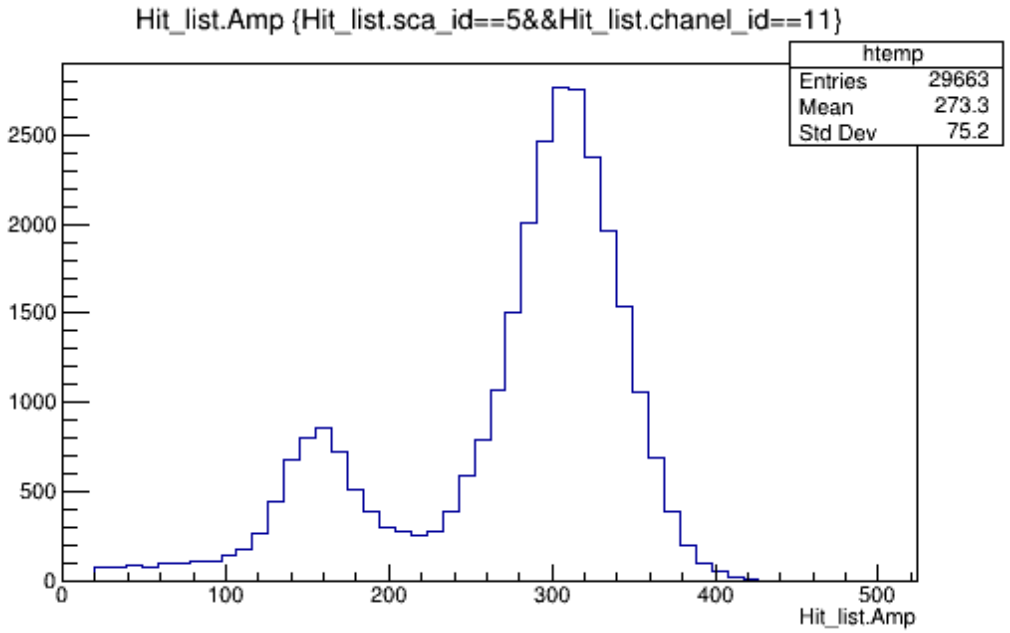




ASICs for gas detectors @ Tsinghua

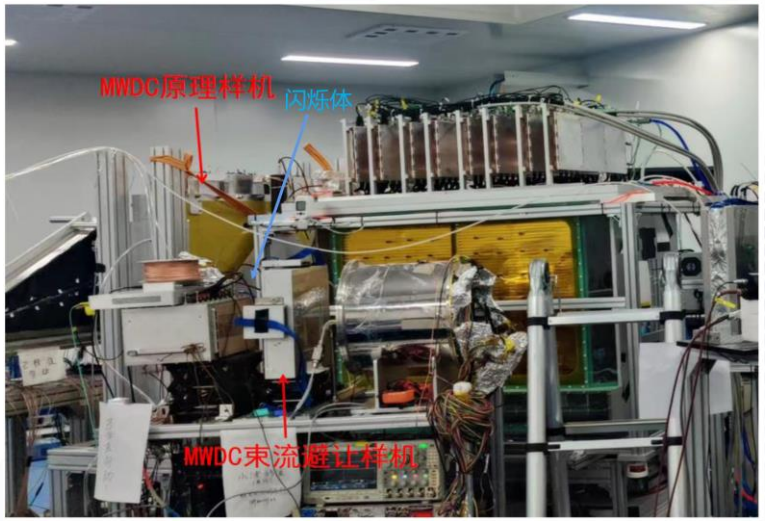
➢ Application of GERO in MWDC

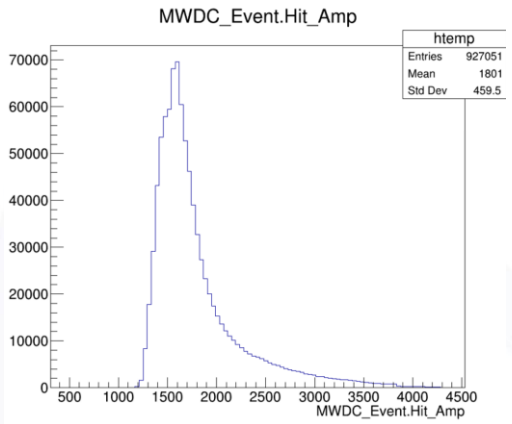
Fe-55 Spectrum

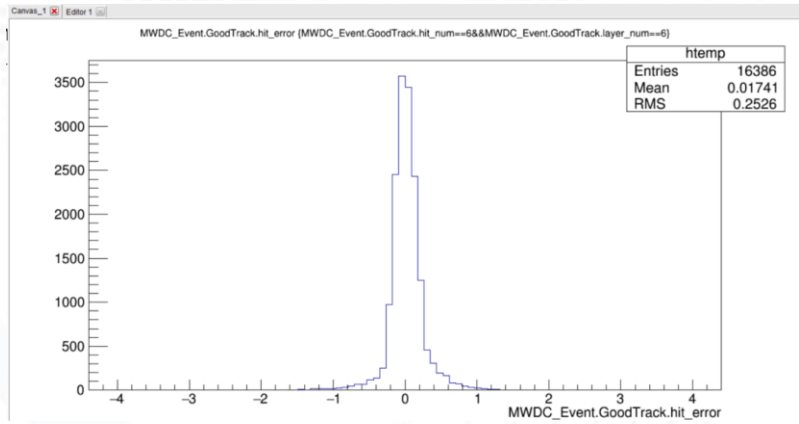


- Gas: Ar+CO2(80:20)
- Energy resolution: ~25%(FWHM)

Beam Tests







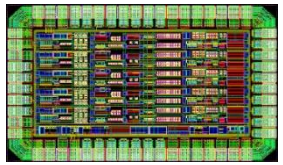
02 | Progress on WASA chip

WASA: Waveform Sampling ASIC

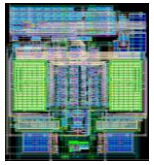
- A low power and high integration front-end ASIC developed for CEPC-TPC

2017

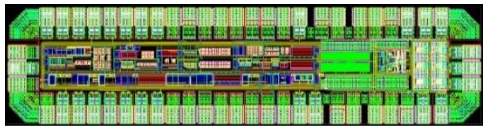
5ch Analog FEE



SAR ADC

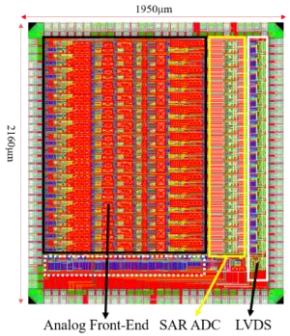


AFE+SAR ADC



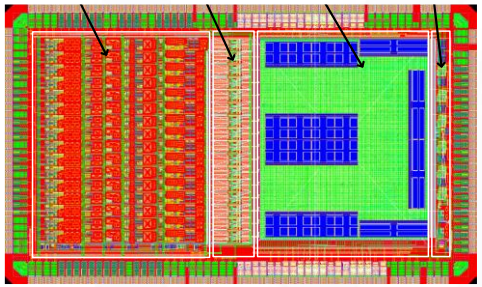
2019

WASA_v0



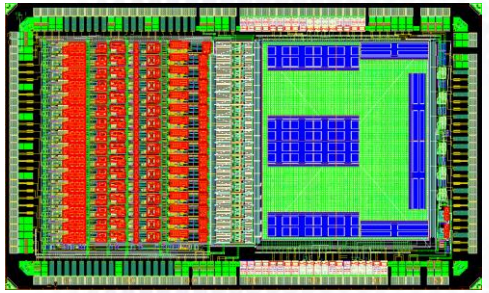
2021

WASA_v1p0

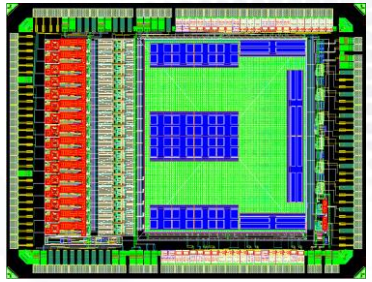


2022-2023

WASA_v1p1

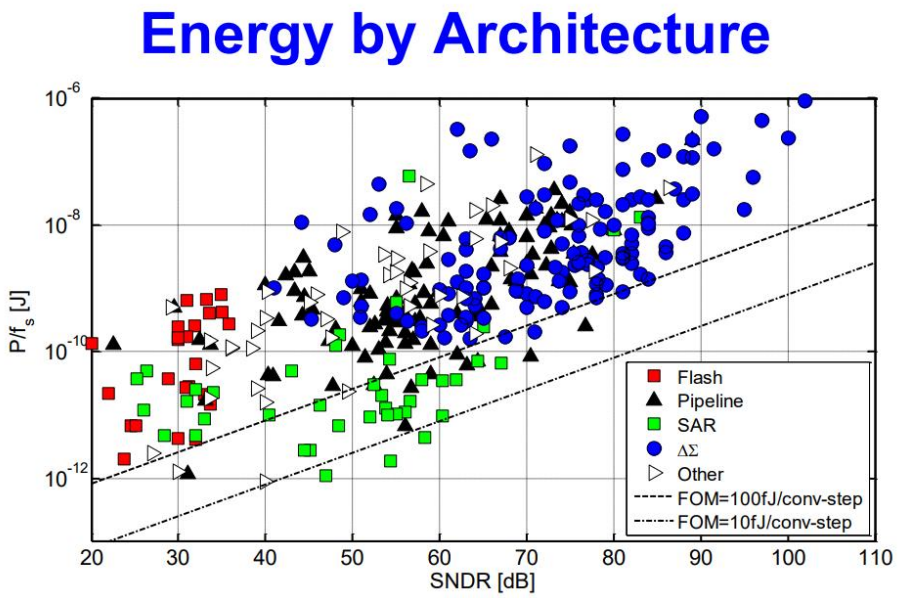


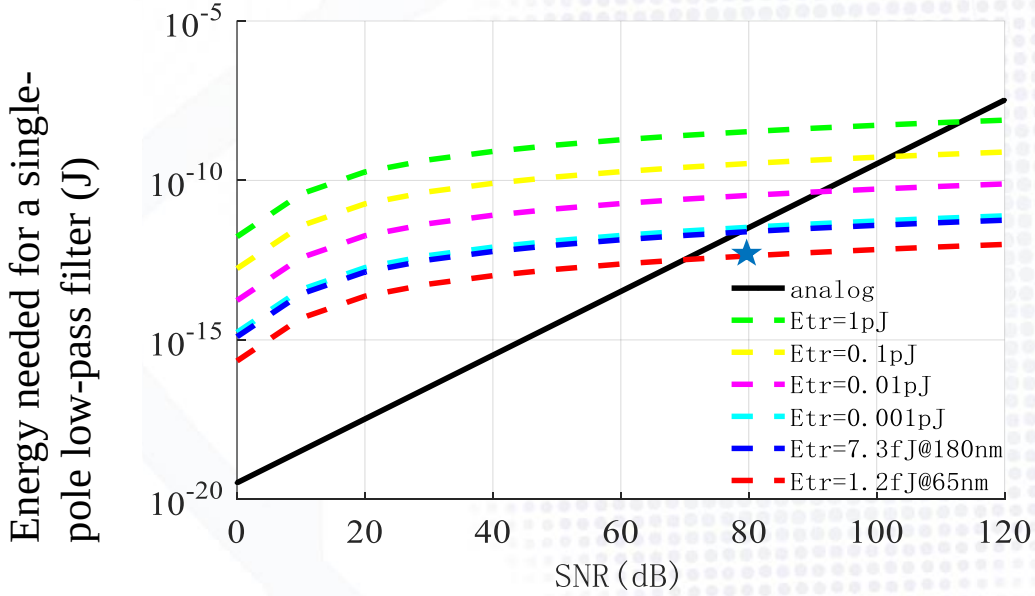
WASA_DSP_v1p0



WASA Chip Design

- Power consumption!!!
  - Pipeline ADC vs. SAR ADC
  - Analog filter vs. Digital filter

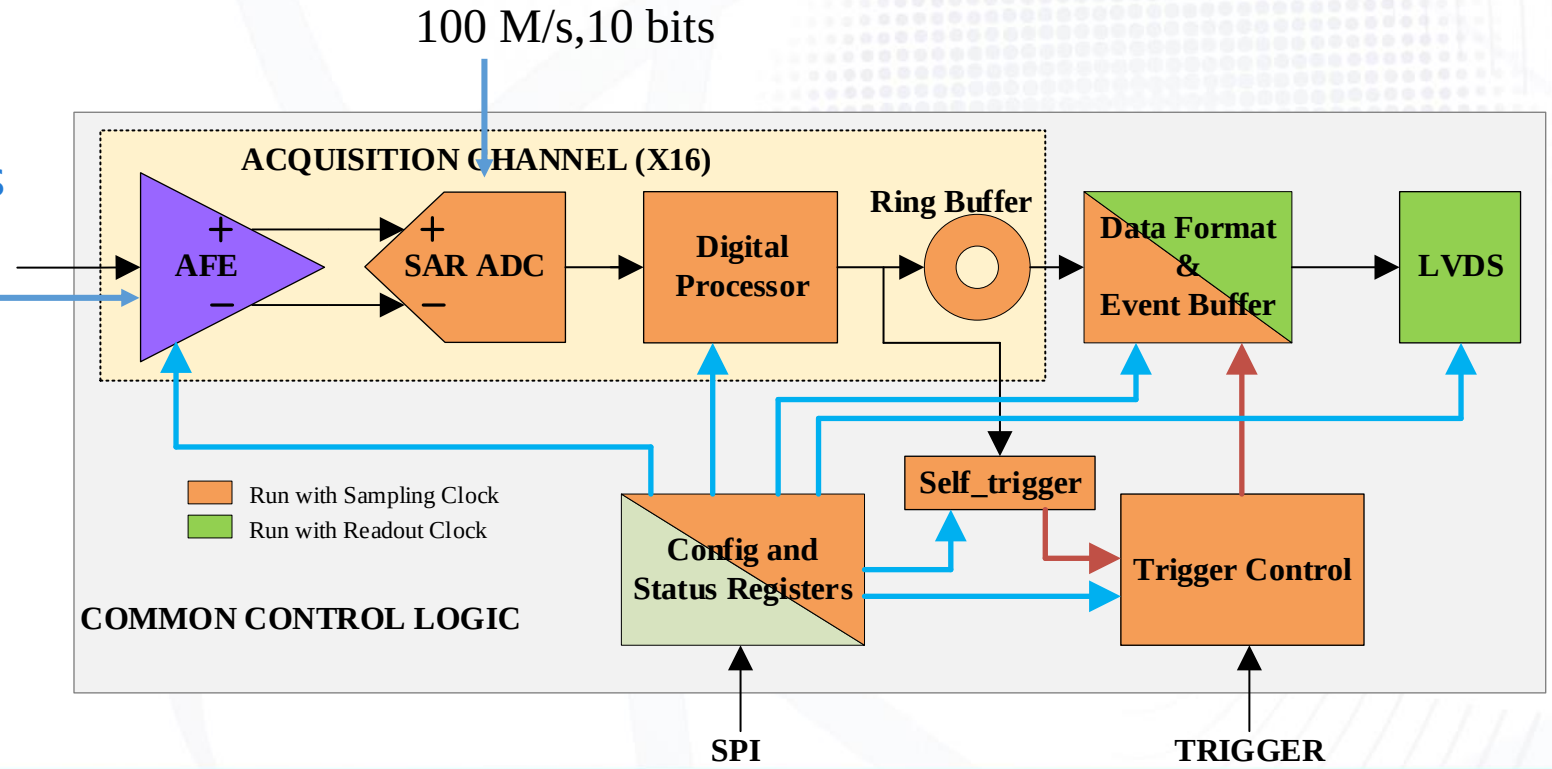




WASA Chip Design

- Chip architecture
  - Analog CR-RC shaper+ Digital filters: baseline correction + digital trapezoid
  - Trigger mode: Self-trigger, External trigger, External trigger window + self trigger
  - Data buffers: Ring buffer + de-randomize buffer
  - Trigger latency: 25.6 μs @ 40 MHz (1024 samples)
  - Event size: 1-256 samples
  - Buffer Depth: 4
  - Readout bandwidth: 3.2 Gbps

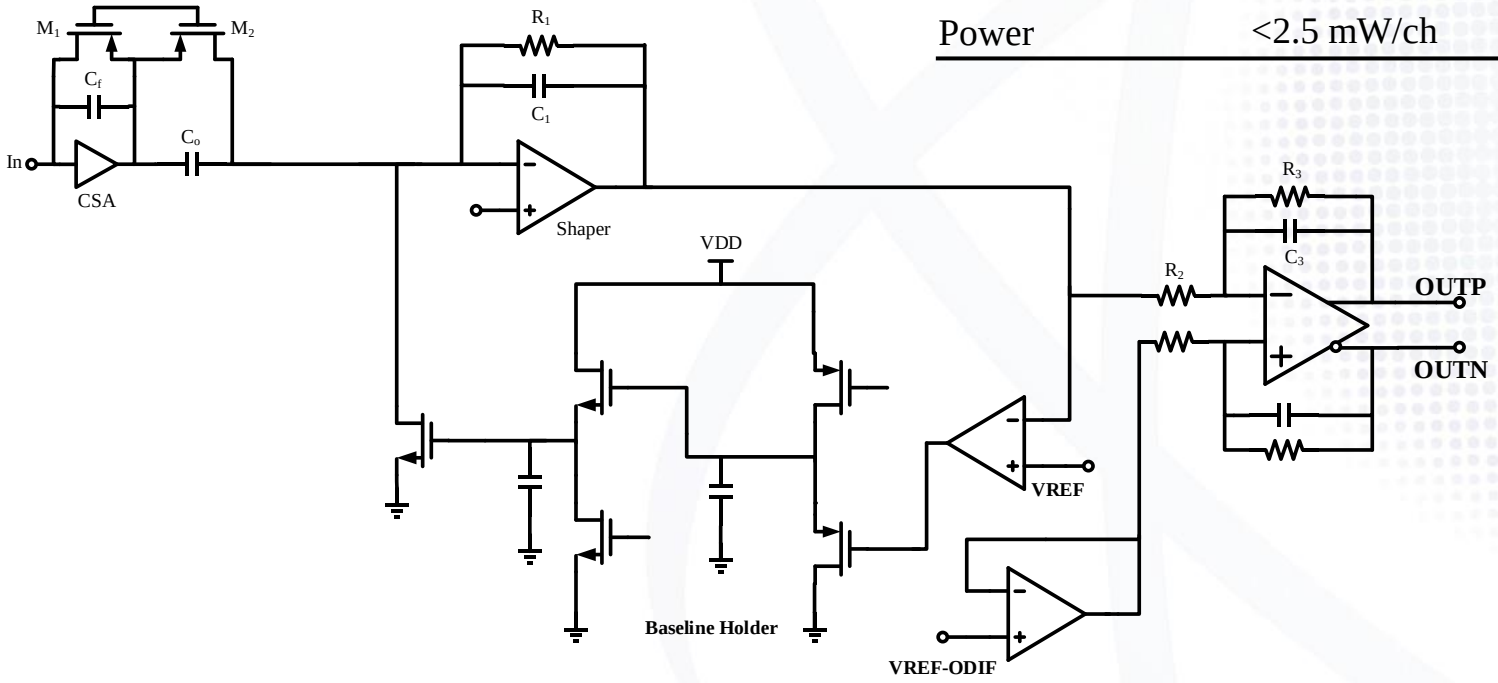
CSA+CR-RC
10-40 mV/fC,160-400 ns



WASA Chip Design

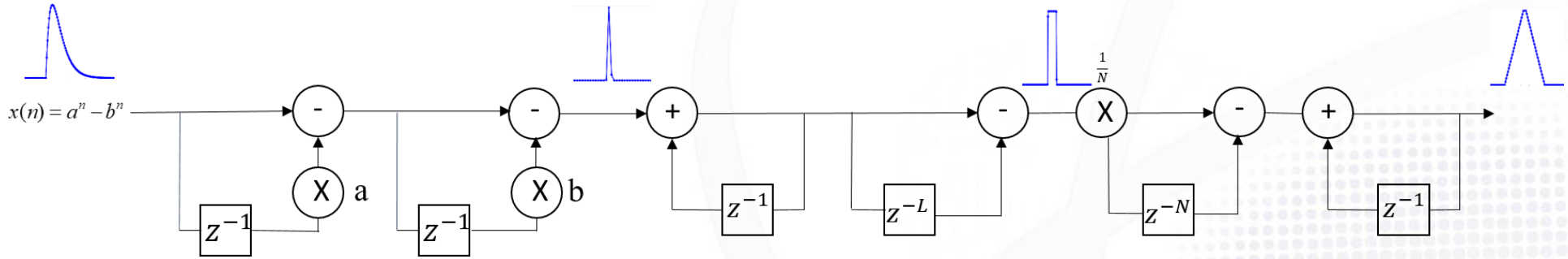
- Analog Front-end
  - Low power supply design: 1.2 V
  - Fully differential output
  - Power optimization orientated

Parameters	SPECs	Simulation
Shaper	CR-RC	CR-RC
Shaping time	160 ns	160 ns
Gain	10 mV/fC	10 mV/fC
Dynamic Range	120 fC	120 fC
INL	<1 %	<1 %
ENC	500 e @ 10 pF	306 e @10 pF
Crosstalk	<1 %	0.12 %
Power	<2.5 mW/ch	1.4 mW/ch

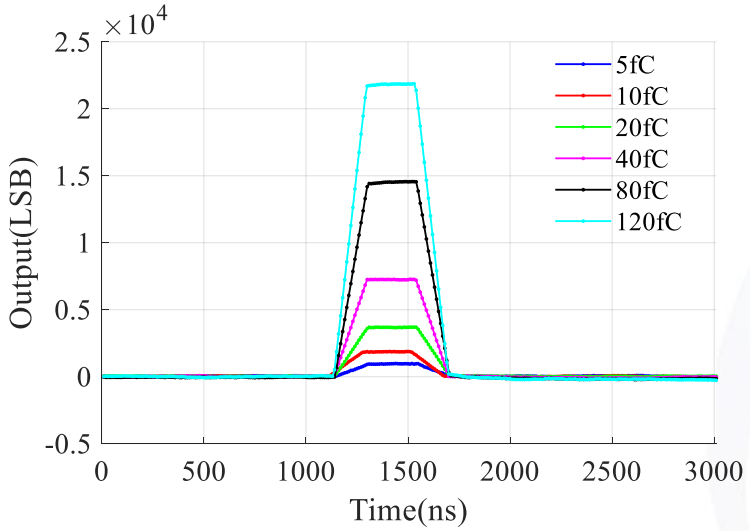


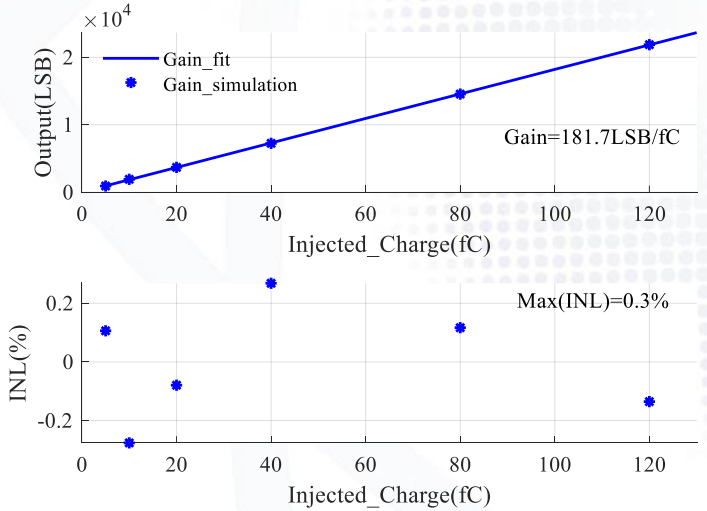
WASA Chip Design

➢ Digital Trapezoid Filter



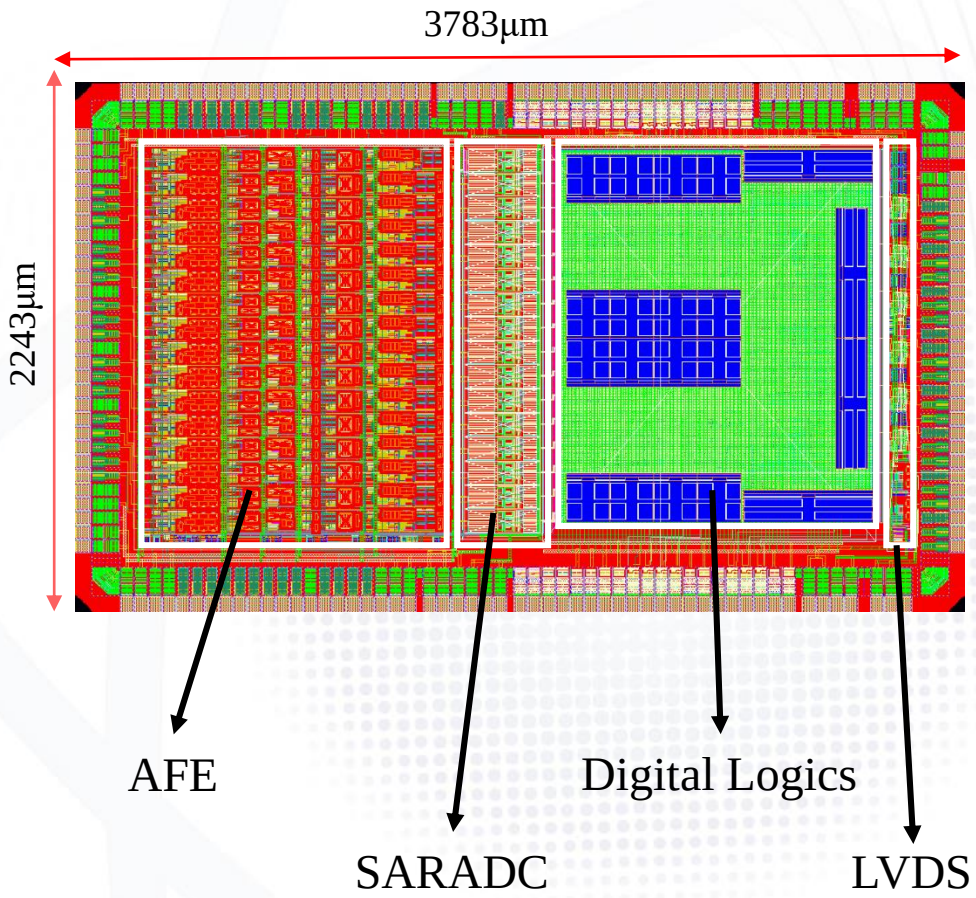
Valentin T. Jordanov, Unfolding-synthesis technique for digital pulse processing. Part 1: Unfolding, NIMA Vol 805, 2016，63-71





WASA Chip Design

- Layout floor plan:
  - The die size: 3783 μm x 2243 μm
  - Separated power supply:
    - Analog Front-End
    - SAR ADC
    - Digital Logics
    - LVDS driver
    - Guarding ring insert between
- ASIC submitted in Jan, 2022 and received in March, 2022



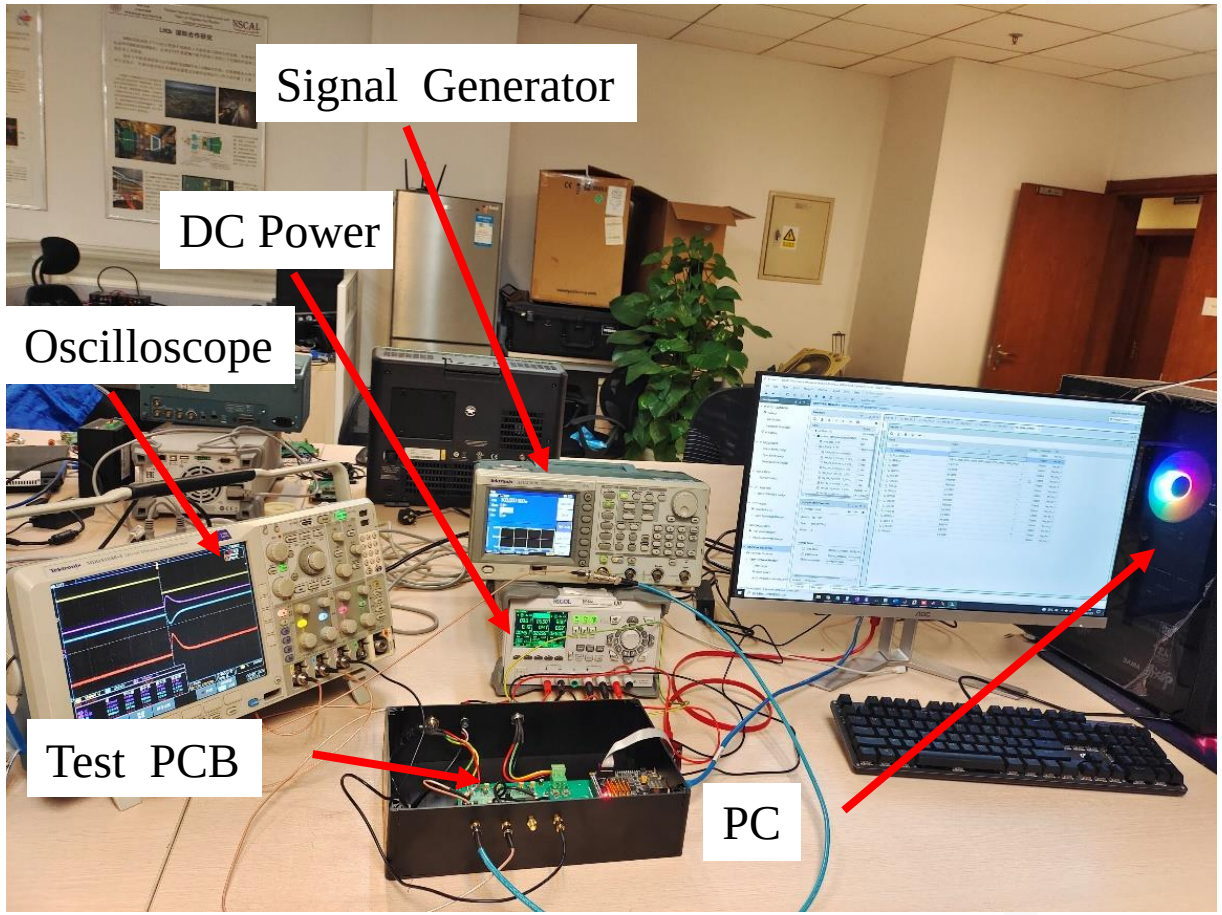
WASA Chip Design

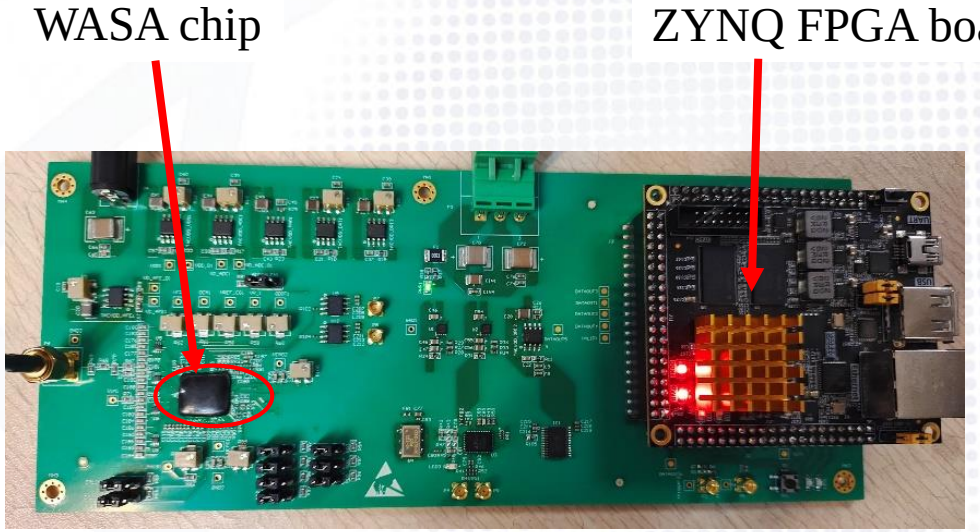
➢ Specs

	PASA+ALTRO	Super-ALTRO	SAMPA	WASA
TPC	ALICE	ILC	ALICE upgrade	CEPC
Pad size	4x7.5 mm^2	1x6 mm^2	4x7.5 mm^2	1x6 mm^2
Number of channels	5.7× 10^5	1-2 × 10^6	5.7 × 10^5	2 x×10^6
Readout detector	MWPC	GEM/MicroMegas	GEM	GEM/MicroMegas
Gain	12 mV/fC	12-27 mV/fC	20/30 mV/fC	10-40 mV/fC
Shaper	CR-$(RC)^4$	CR-$(RC)^4$	CR-$(RC)^4$	CR-RC
Peaking time	200 ns	30-120 ns	80/160 ns	160-400 ns
ENC	370+14.6 e/pF	520 e	246+36 e/pF	569+14.8 e/pF
Sampler	Pipeline ADC	Pipeline ADC	SAR ADC	SAR ADC
Sampling rate	10 MHz	40 MHz	10 MHz	10-100 MHz
Resolution	10 bit	10 bit	10 bit	10 bit
Power (ana.)	11.7 mW/ch	10.3 mW/ch	9 mW/ch	1.4 mW/ch
Power (ADC)	12.5 mW/ch	33 mW/ch	1.5 mW/ch	0.8 mW/ch@40 MHz
Power (digital)	7.5 mW/ch	4.0 mW/ch	6.5 mW/ch	2.7 mW/ch@40 MHz
Total Power	31.7 mW/ch@10MHz	47.3 mW/ch@40 MHz	17 mW/ch@10 MHz	4.9 mW/ch@40 MHz
CMOS Process	250 nm	130 nm	130 nm	65 nm

WASA Chip Test

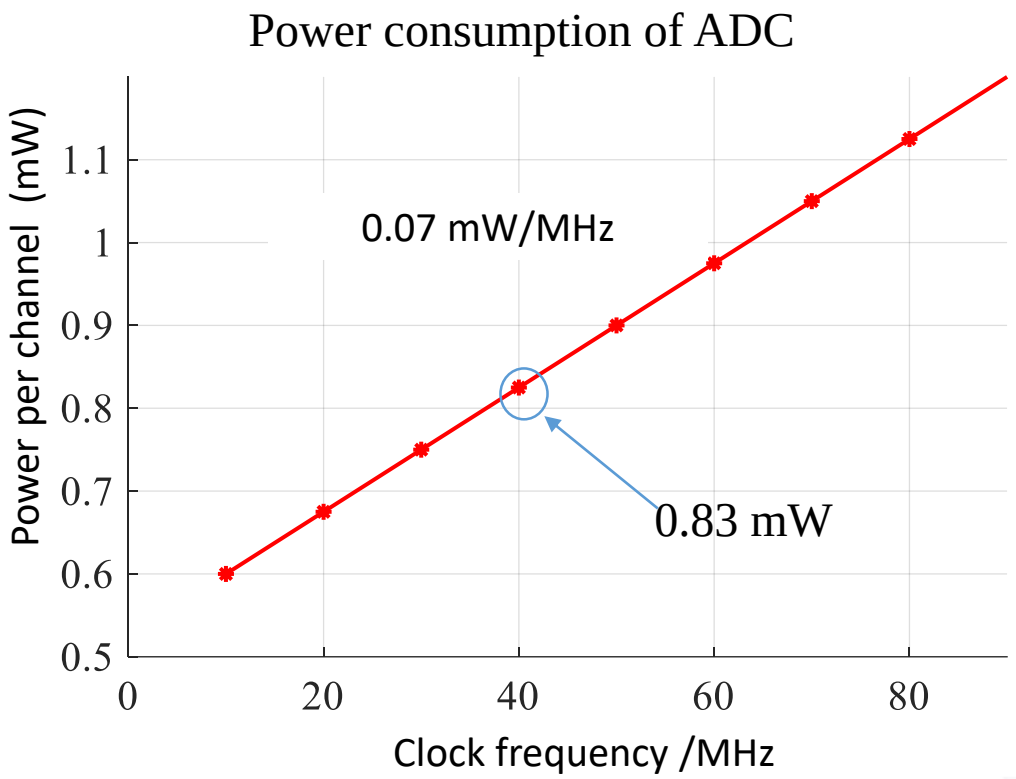
➢ Test setup

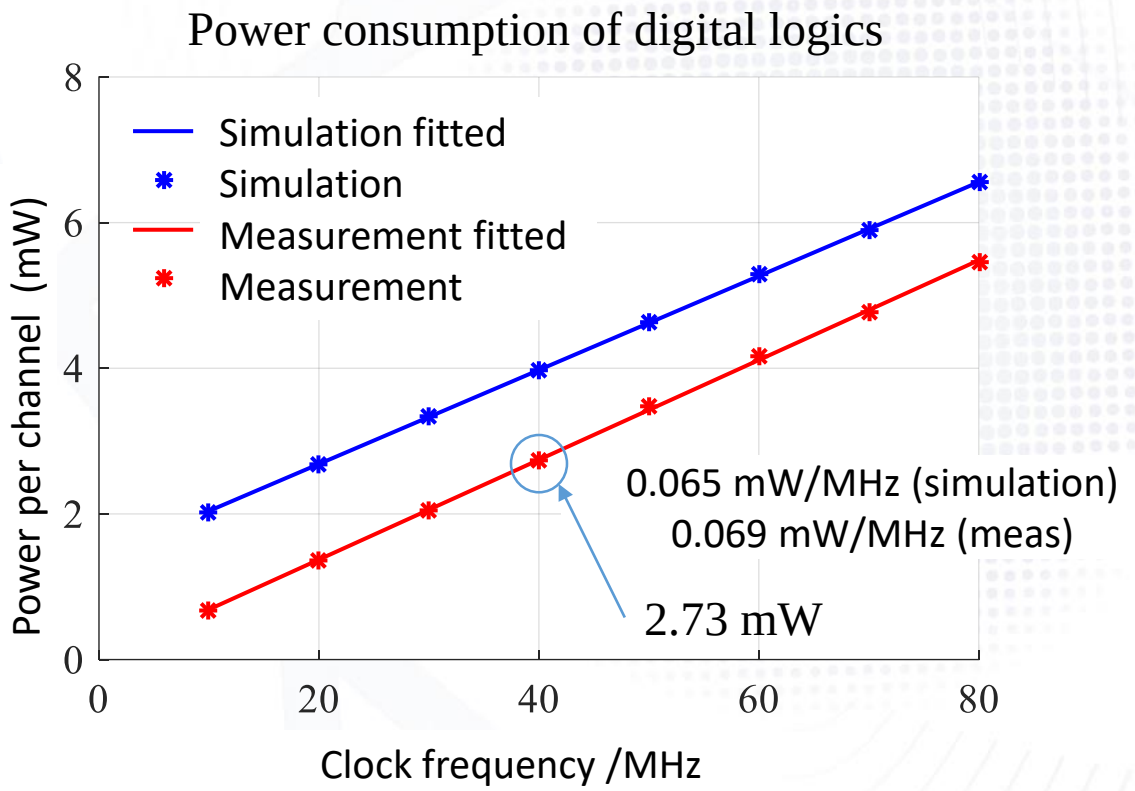




WASA Chip Test

- Power: 4.94 mW/ch@40 MHz
  - AFE: 1.38 mW/ch
  - ADC: 0.83 mW/ch
  - Digital logics: 2.73 mW/ch





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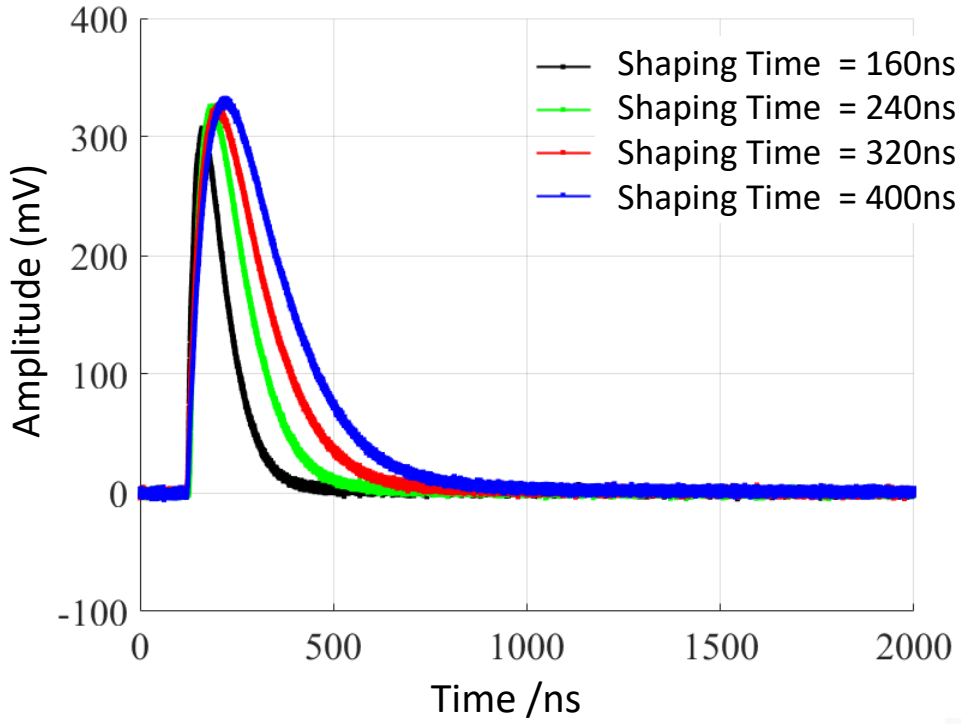
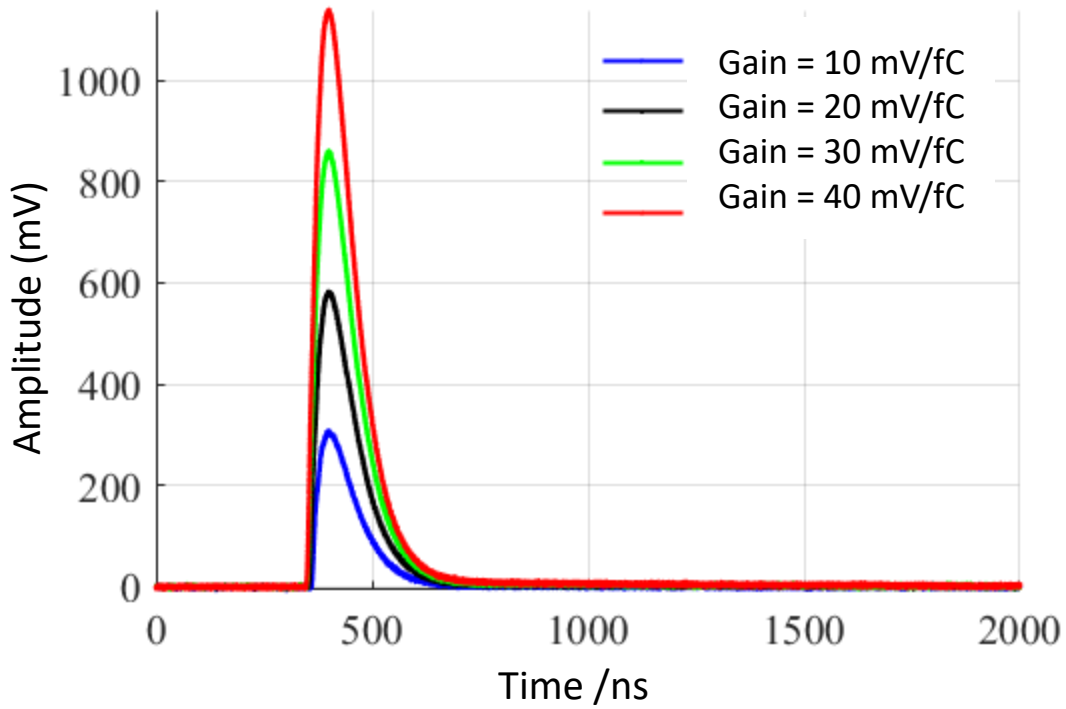
➢ Transient response: Analog part

Transient analog outputs (different shaping time)

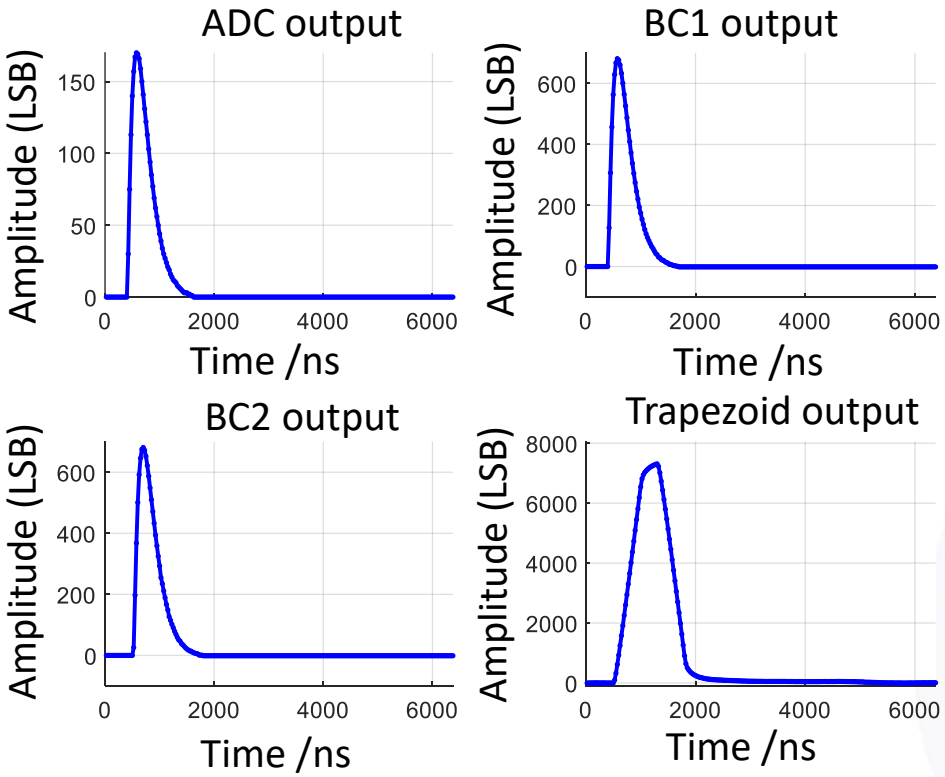


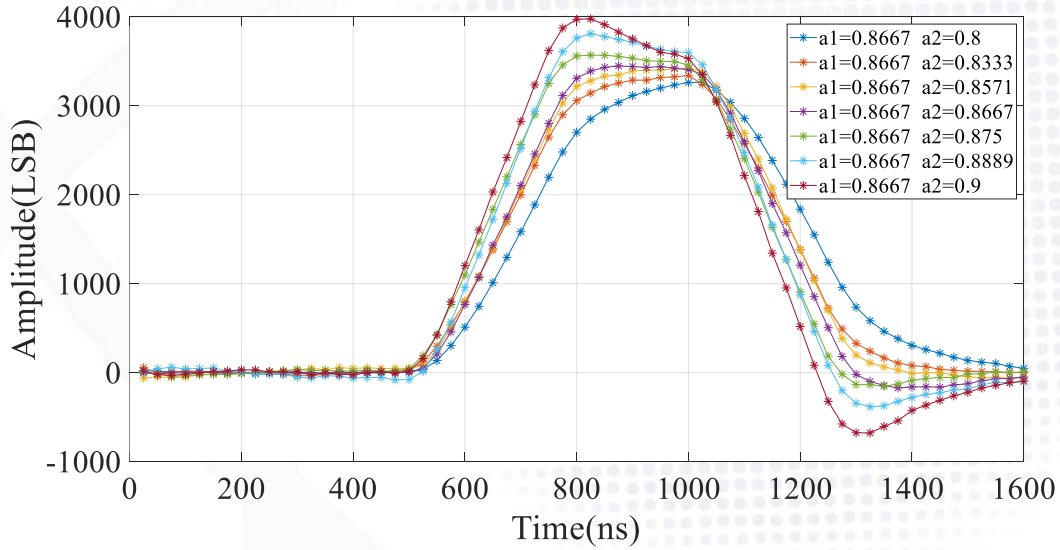
Transient analog outputs (different gain)



WASA Chip Test

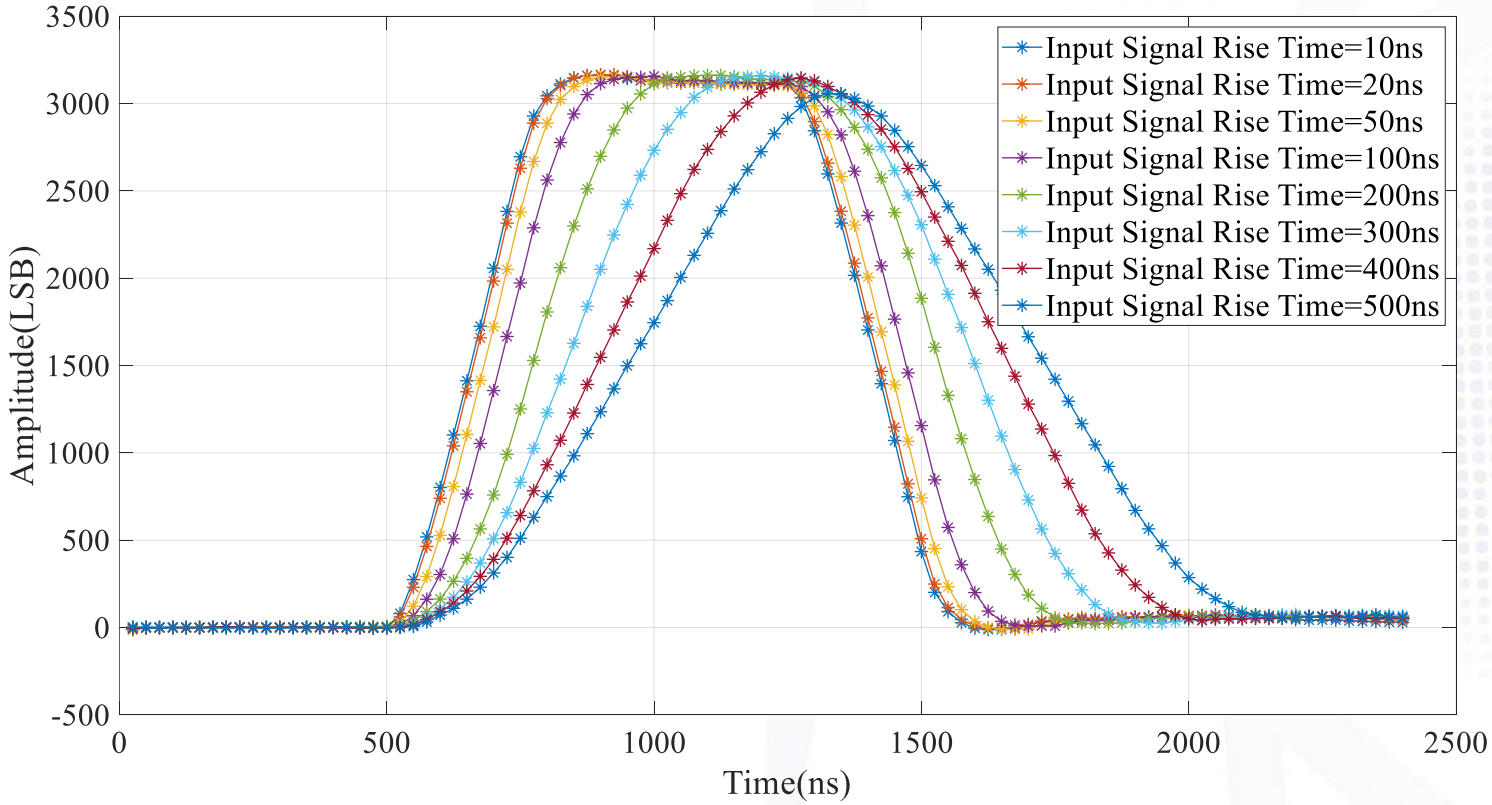
- Transient response of digital filter
  - AFE: gain=10 mV/fC, shaping time = 160 ns, Qin=120 fC
  - ADC sampling rate: 40 MHz
  - Trapezoid: tr = 600 ns, t_flat = 200 ns





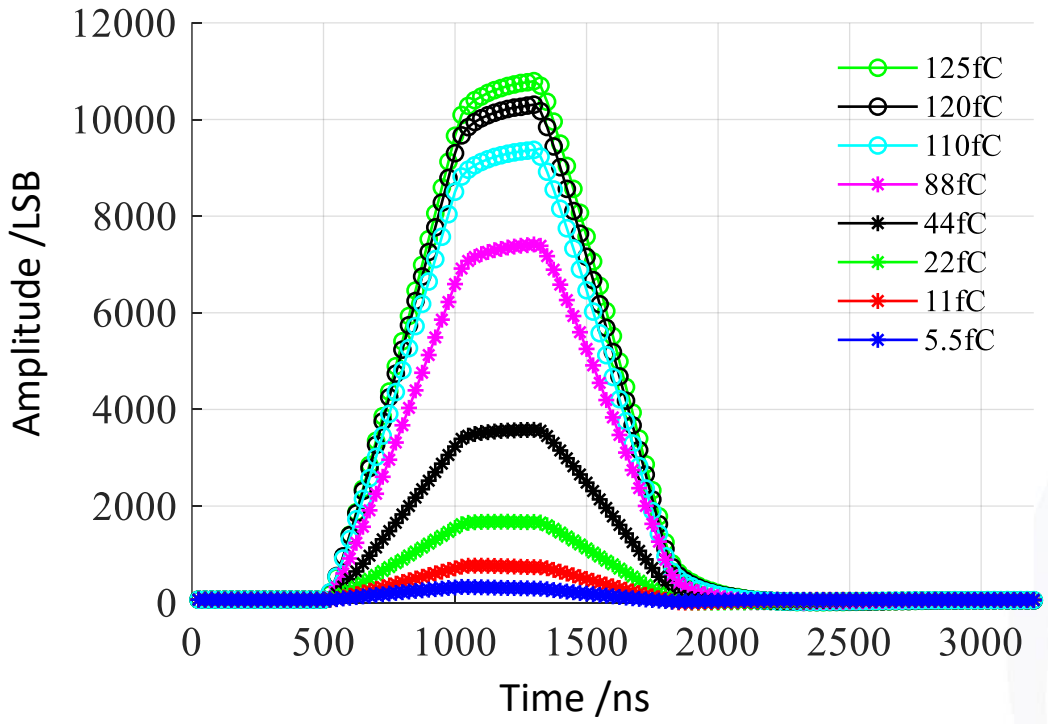
WASA Chip Test

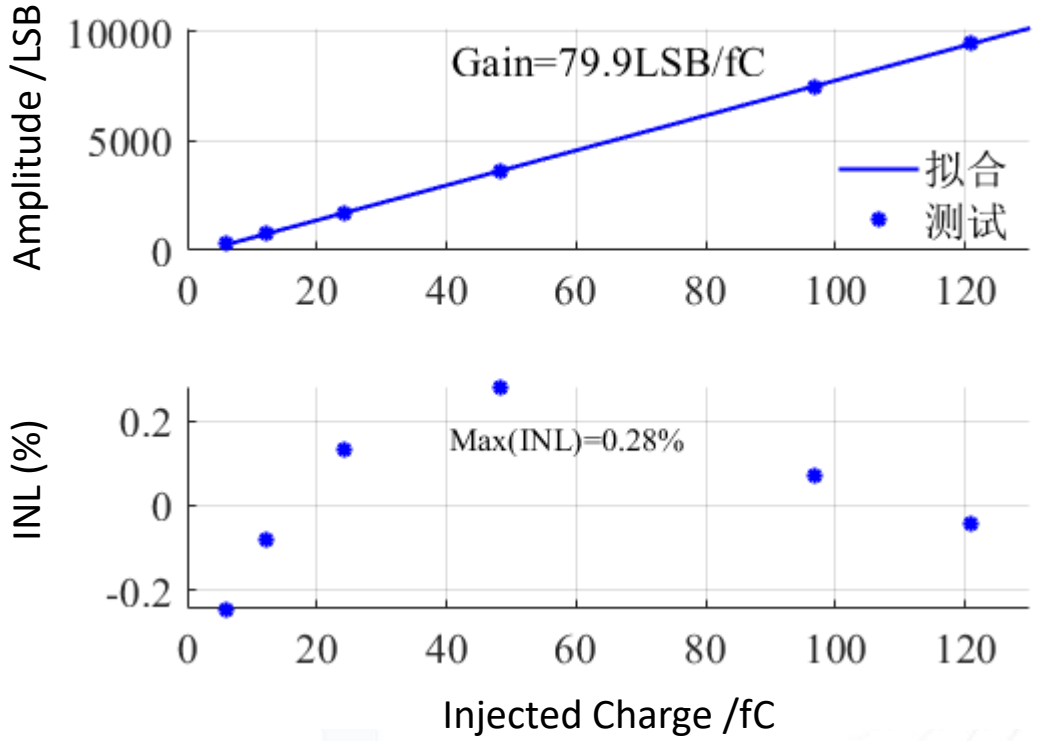
- Transient response of digital filter : BD



WASA Chip Test

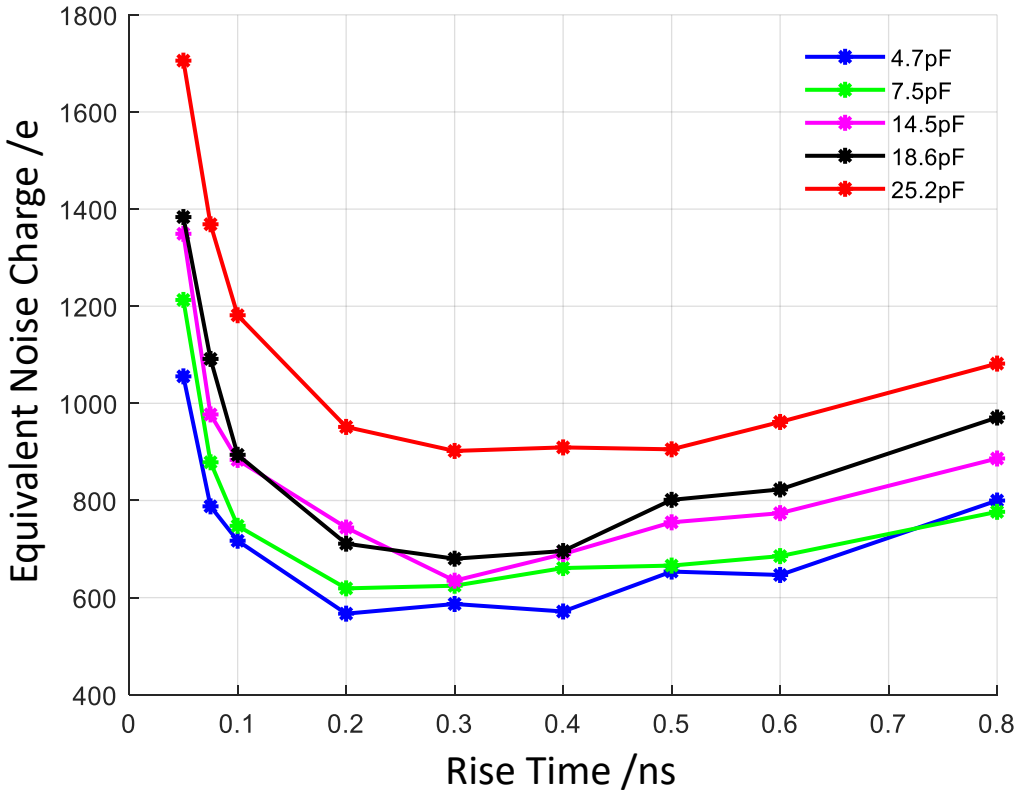
- Linearity
  - AFE: gain = 10 mV/fC, shaping time = 160 ns
  - ADC sampling rate: 40 MHz
  - Trapezoid: tr = 600 ns, t_flat = 200 ns

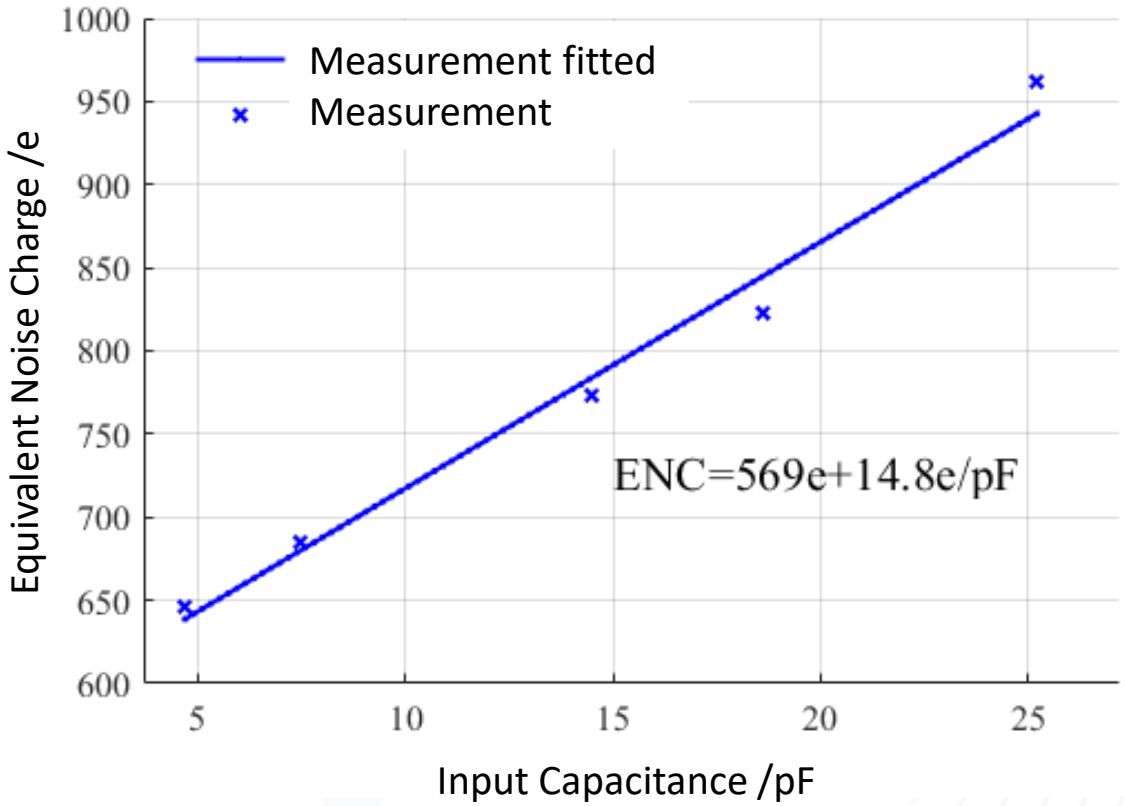




WASA Chip Test

- Noise
  - AFE: gain = 10 mV/fC, shaping time = 160 ns
  - ADC sampling rate: 40 MHz
  - Trapezoid: t_flat = 200 ns

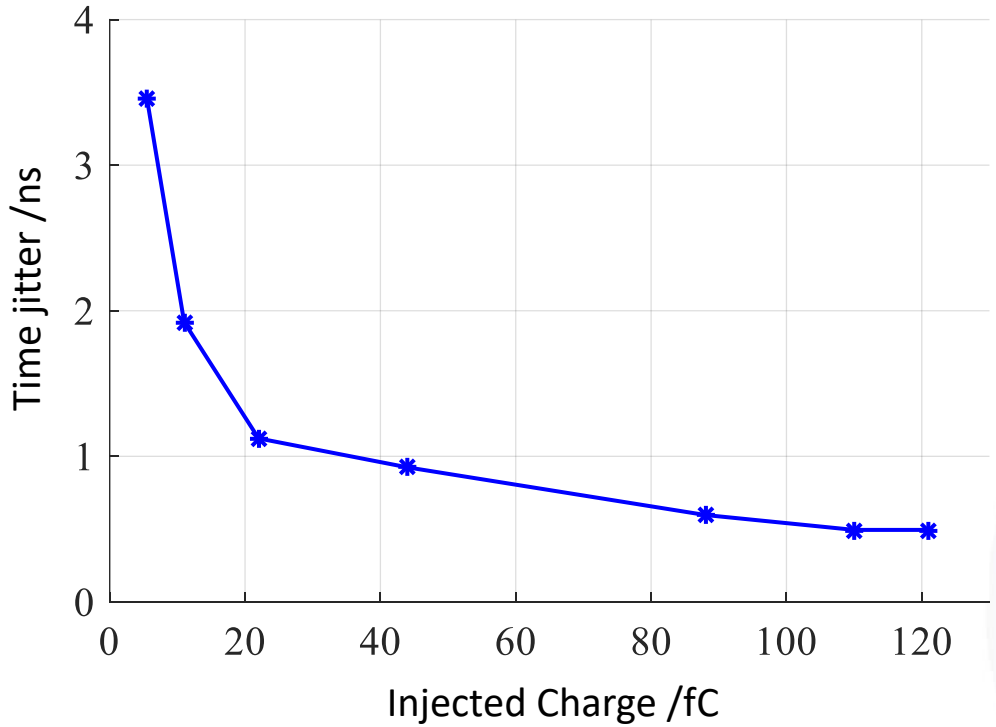


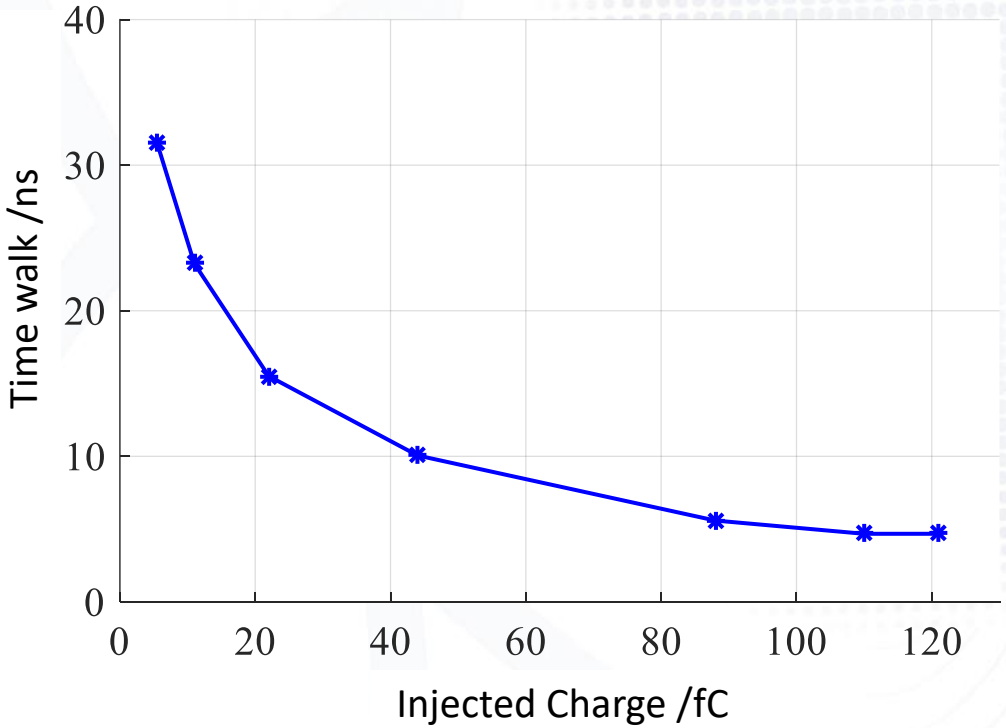


WASA Chip Test

- Timing
  - AFE: gain = 10 mV/fC, shaping time = 160 ns
  - ADC sampling rate: 40 MHz
  - Trapezoid: tr = 600 ns, t_flat = 200 ns
  - Timing method: time centroid

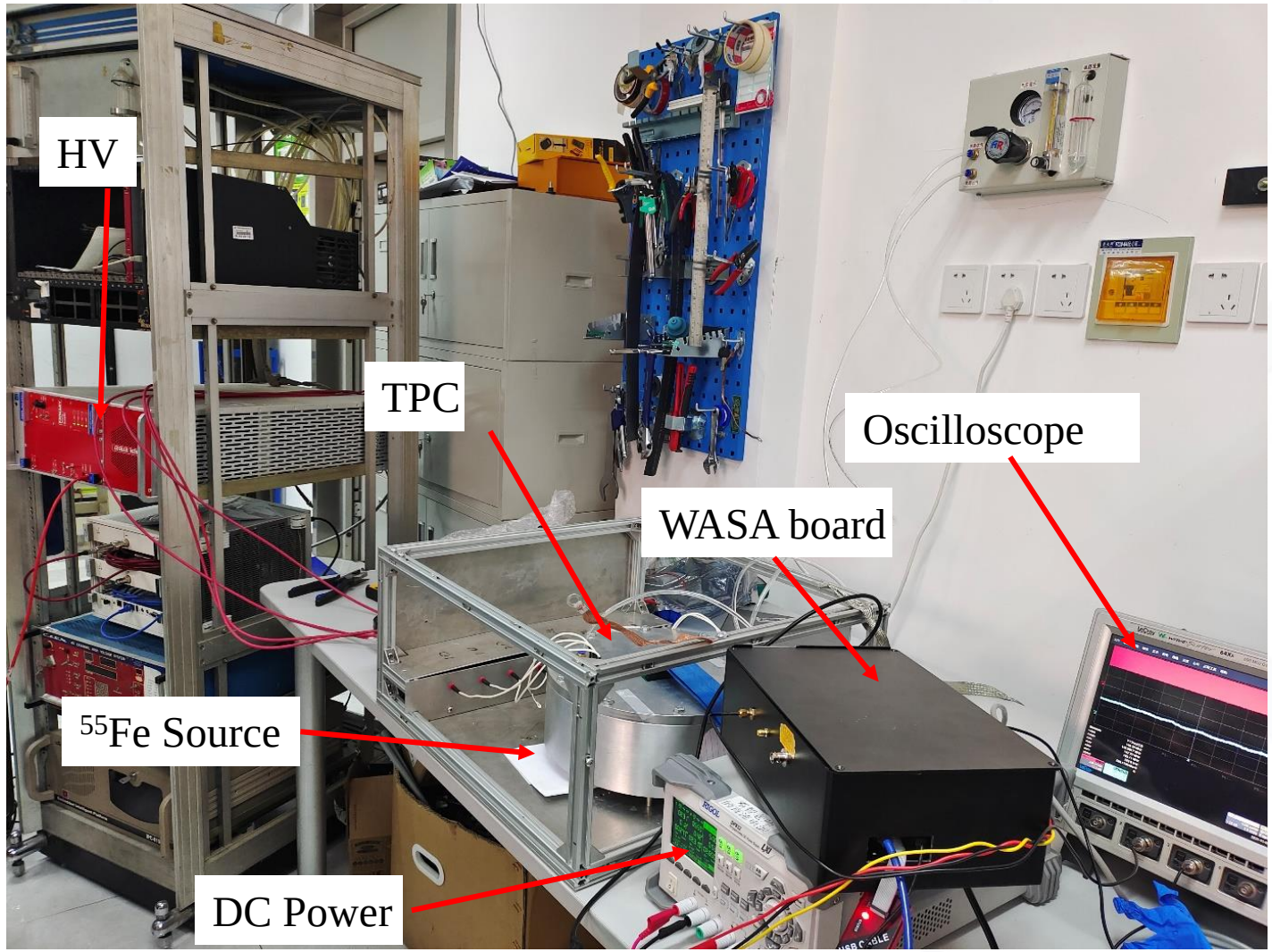
$$t = \frac{\sum t_i \times f(t_i)}{\sum f(t_i)}$$





WASA Chip Test

➢ Detector test: Fe-55



TPC setup

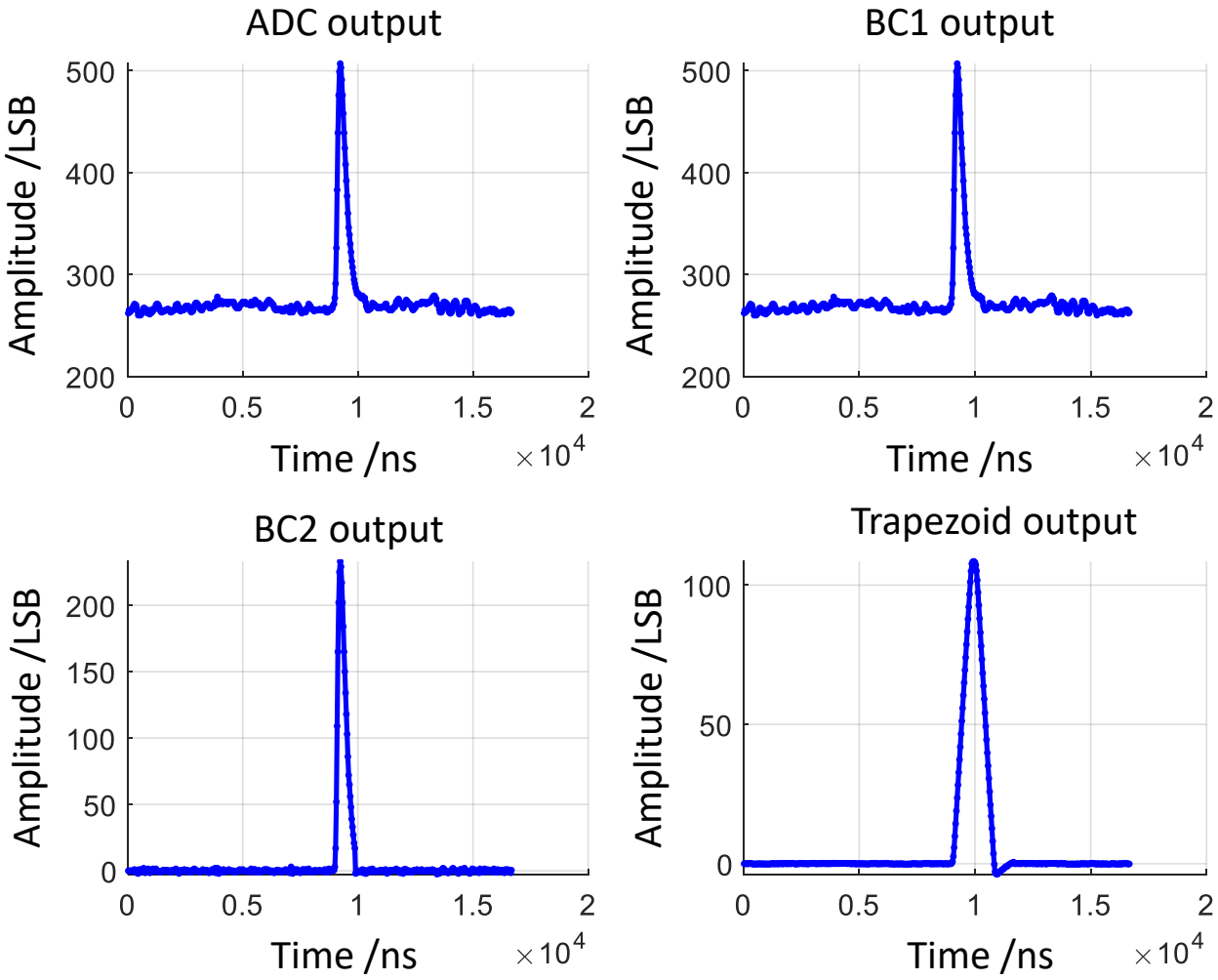
- GEM HV: 310 V
- Drift E: 3.23×10^{4} V/m
- Gas: T2K ($Ar/CF_4/iC_4H_{10}$ 95/3/2)

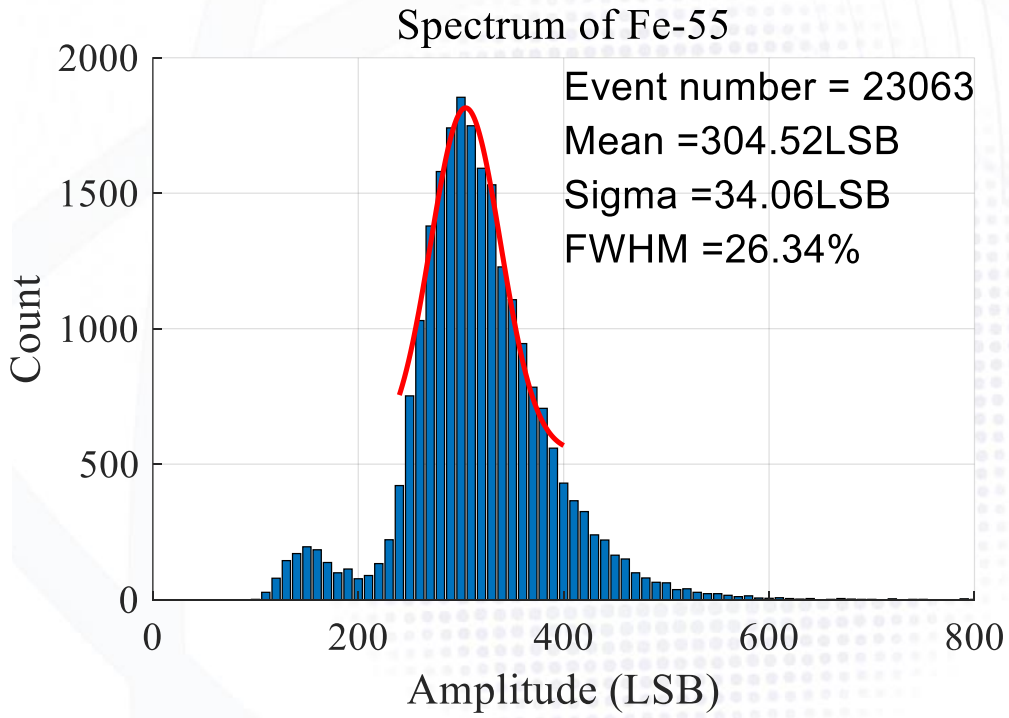
Electronics setup

- Gain = 20 mV/fC
- Sampling rate = 30 MHz
- Self trigger

WASA Chip Test

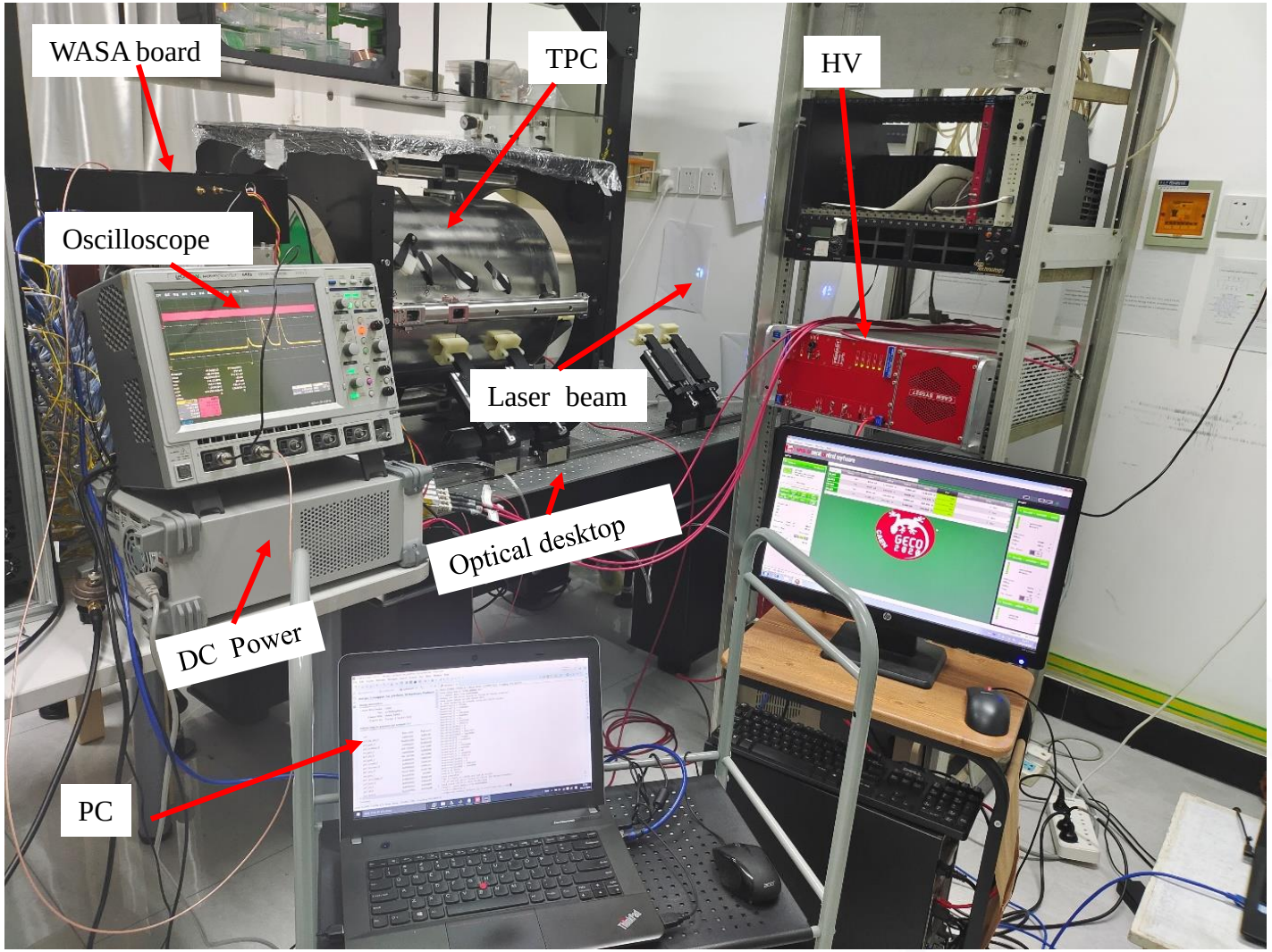
➢ Transient waveforms and Fe-55 spectrum





WASA Chip Test

➢ Detector test: laser tracks



TPC setup

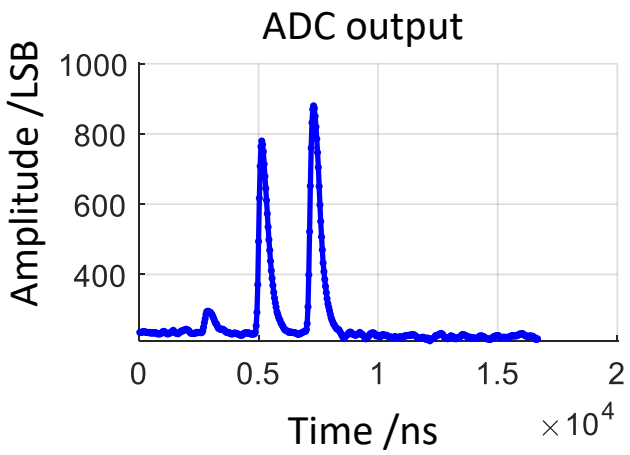
- GEM HV: 280 V
- Drift E: 9000 V/50 cm = 180V/cm
- Gas: T2K ($Ar/CF_4/iC_4H_{10}$ 95/3/2)
- Laser:7.2 mJ @20 Hz

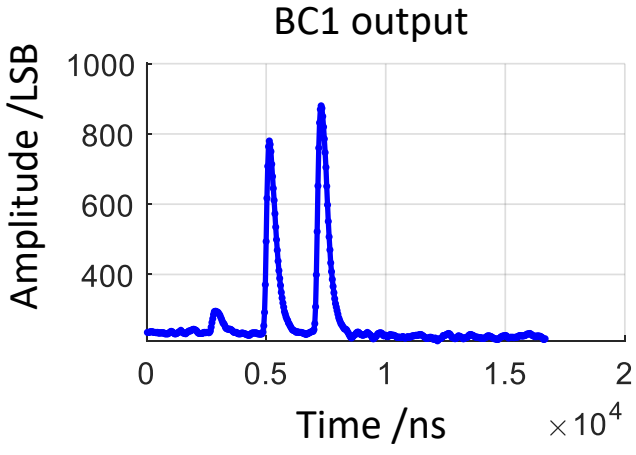
Electronics setup

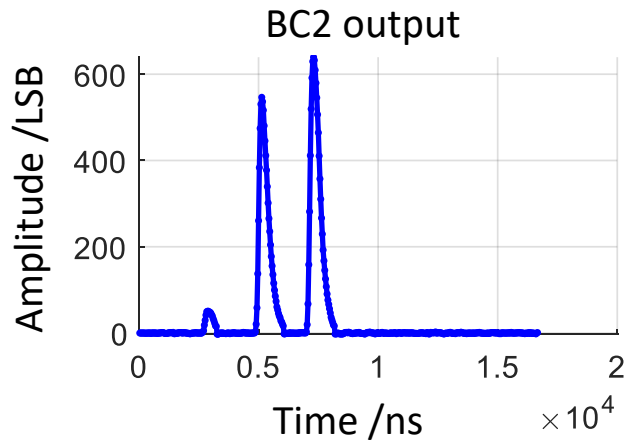
- Gain = 20 mV/fC
- Sampling rate = 30 MHz
- External trigger mode
- Trigger latency: 2500*8 ns=20 μs

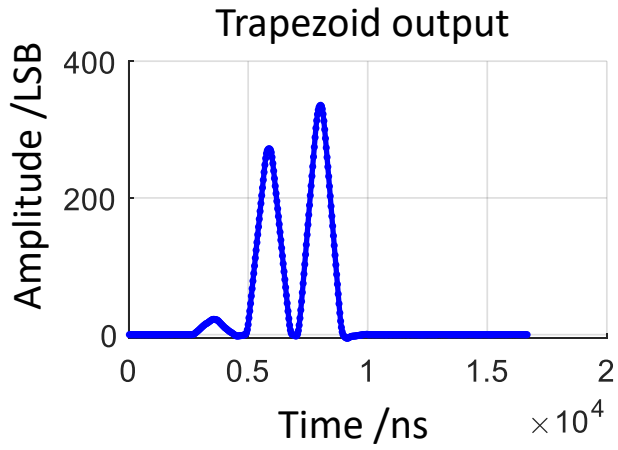
WASA Chip Test

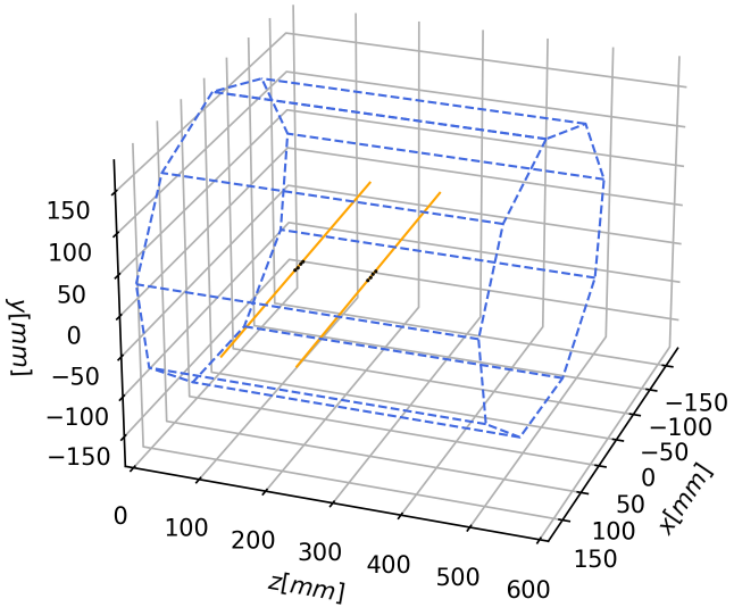
➢ Laser tracks

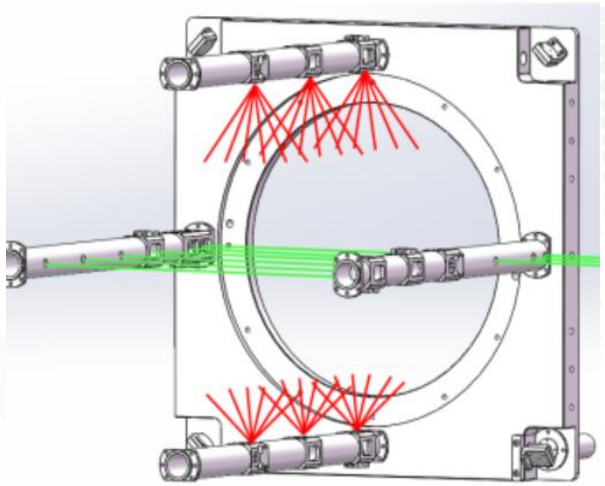












WASA Chip Test

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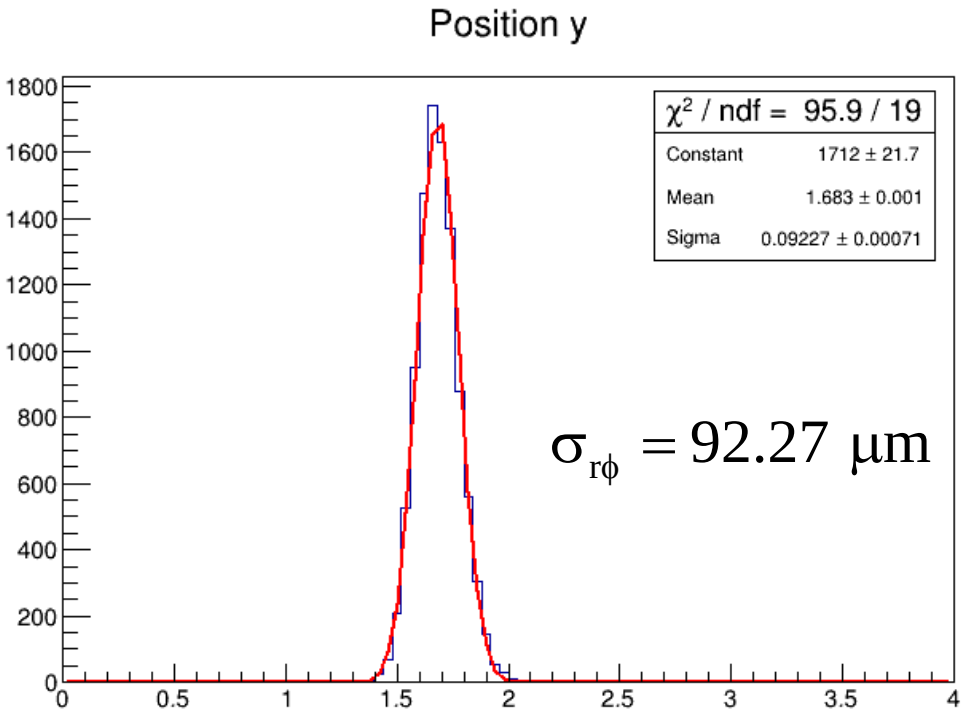
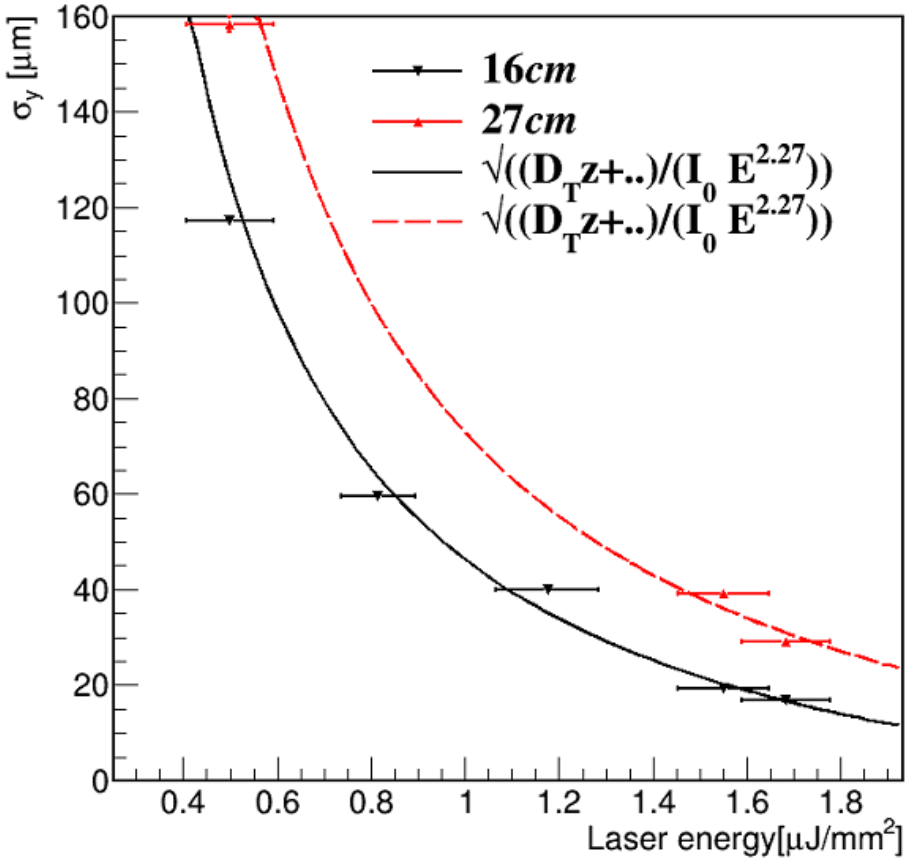
➢ Track resolution

Resolution in rφ



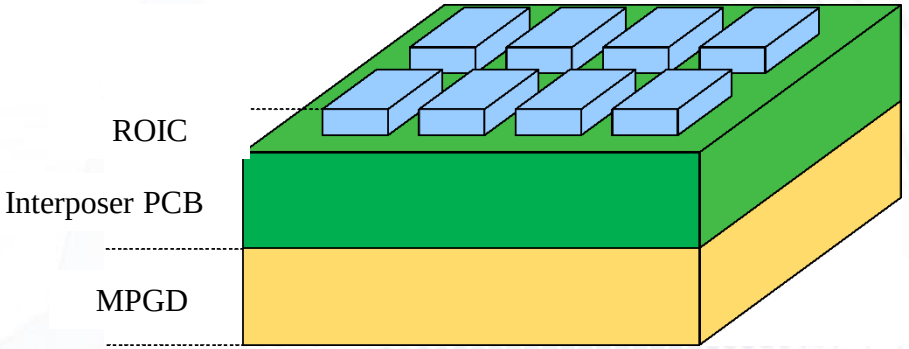
Resolution vs. layer energy

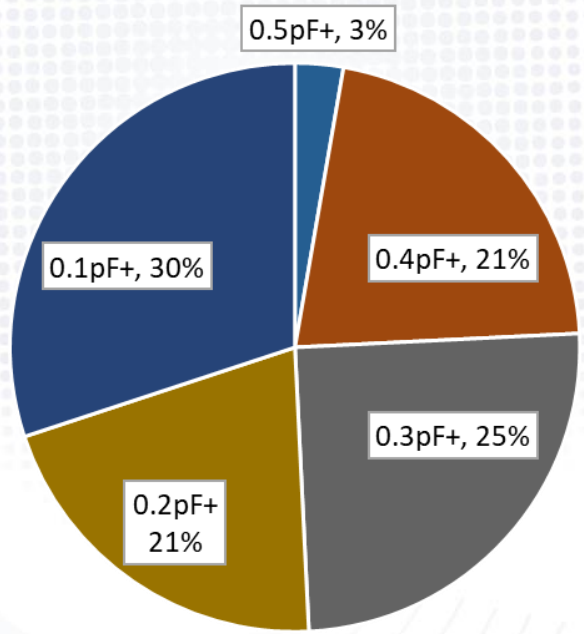


03 | Progress on TEPIX chip

Mini-pad Readout

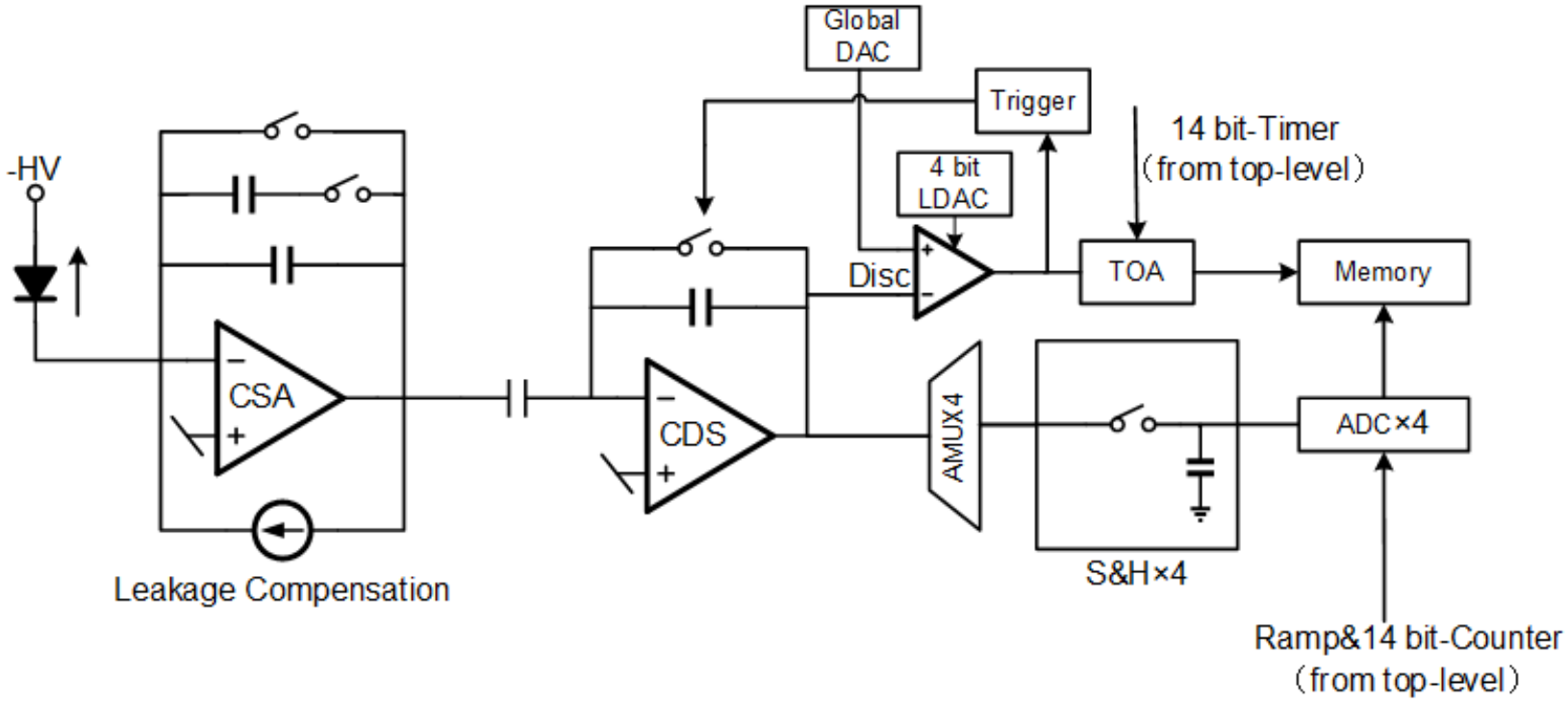
- Mini pad Readout
  - 1 mm x 6 mm → 0.5 mm x 0.5 mm pixel
  - Higher precision, higher rate
  - Potential for dN/dx
- Concept Design
  - ROIC +Interposer PCB as RDL
  - High metal coverage, 4-side buttable
  - Low power Energy/Timing measurement ASIC
  - ~160 e noise @ ~1pF input capacitance
  - 5 ns drift time resolution
  - <100 mW/cm2

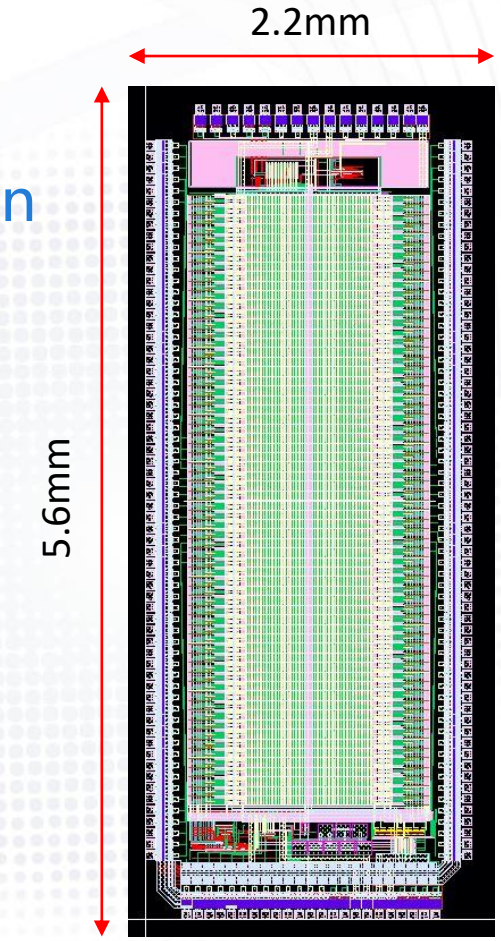




TEPIX Chip Design

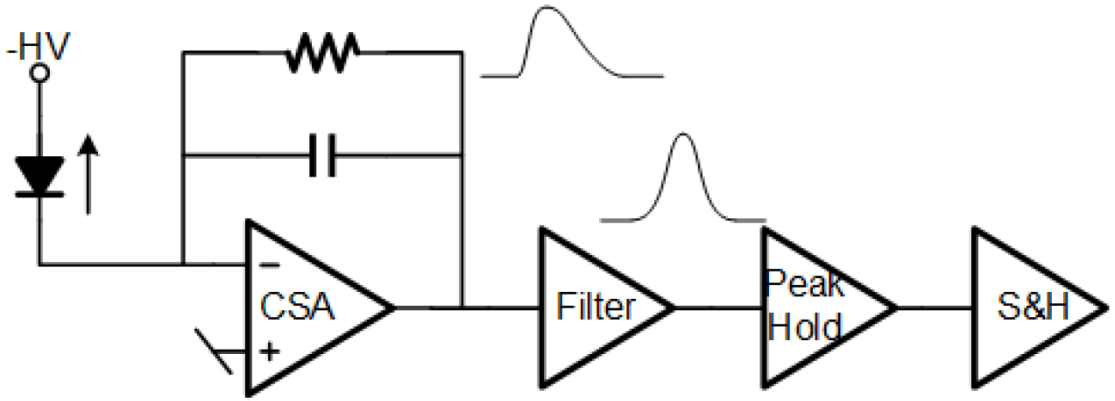
- Charge Sensitive Preamplifier(CSA)
- CDS amplifier provides additional gain and noise shaping
- 14-bit Wilkinson type ADC each pixel
- Timing discriminator with14-bit TOA (Time of Arrival) information



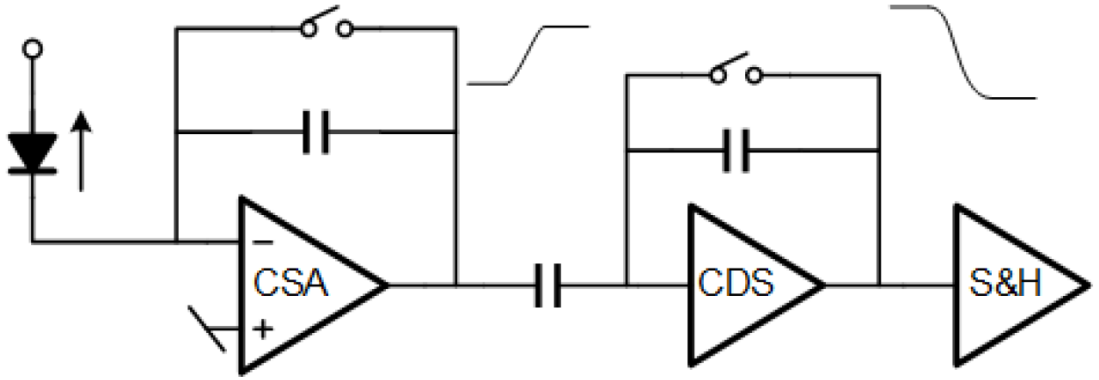


TEPIX Chip Design

- Conventional architecture
  - Continuous feedback
  - CR-RC shaper
  - Trigger based readout
  - Need peak/hold

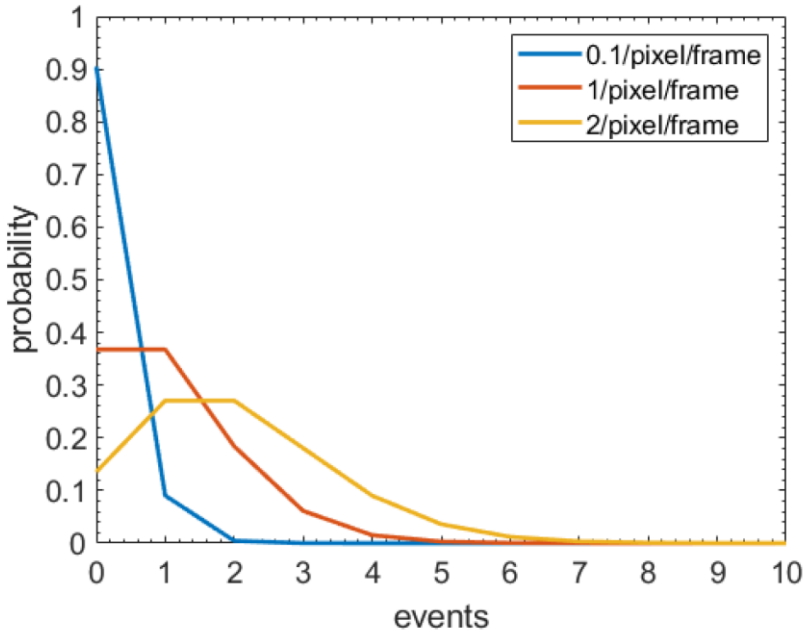


- TEPIX architecture
  - Pulse reset
  - CDS
  - Frame based readout
  - No need for peak/hold



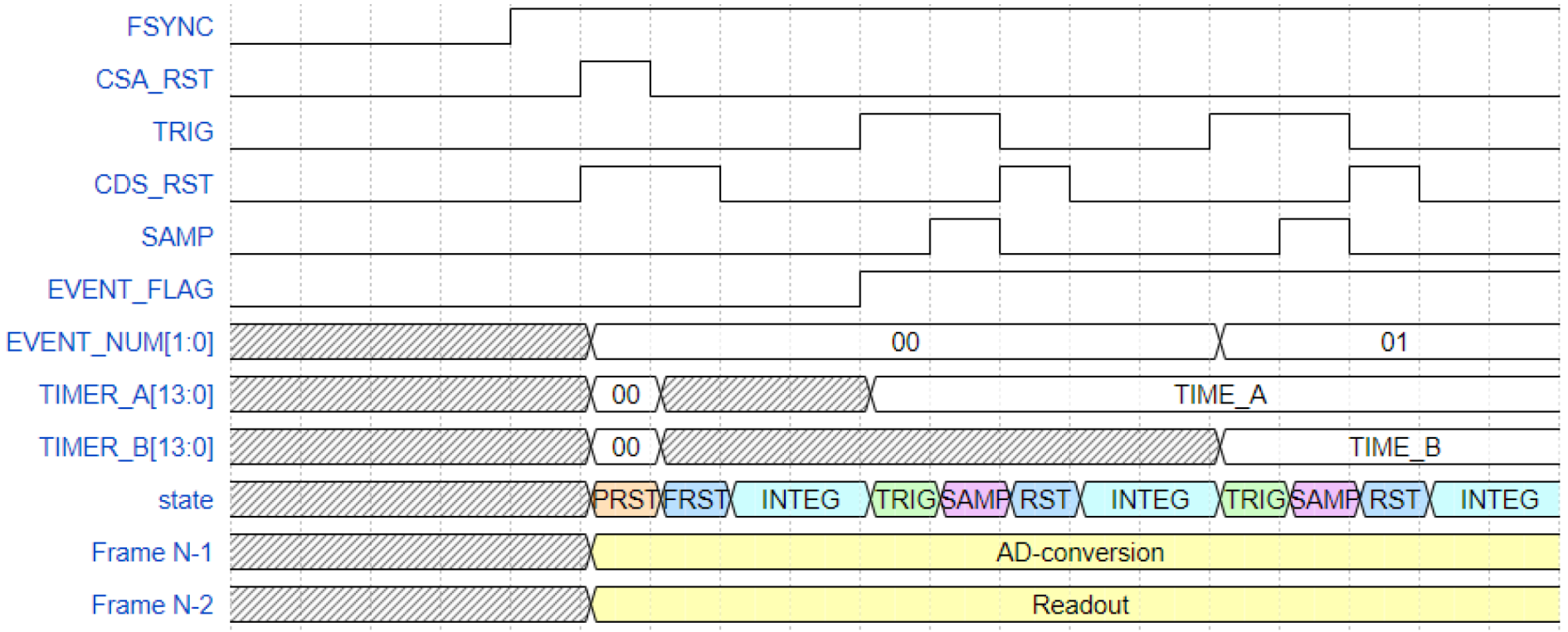
TEPIX Chip Design

- In pixel buffer depth
  - 0.1/pixel/frame: 10% for 1 event, 0.5% for 2 events
  - 1/pixel/frame: 1.5% for 4 events, 0.3% for 5 events
- Count rate per pixel = frame rate * occupancy
- Max. frame rate = 10 kfps



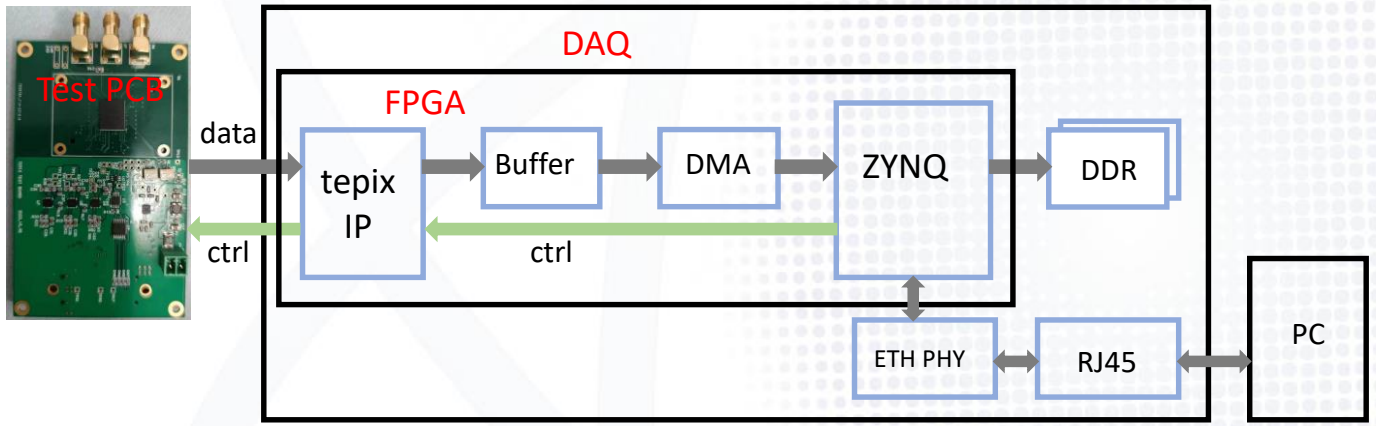
TEPIX Chip Design

- Frame-based mode, token ring readout
- Zero-dead time:
  - Dual S/H and registers at ping-ping mode
  - Pipelined processing: integration, A/D conversion and readout



TEPIX Chip Test

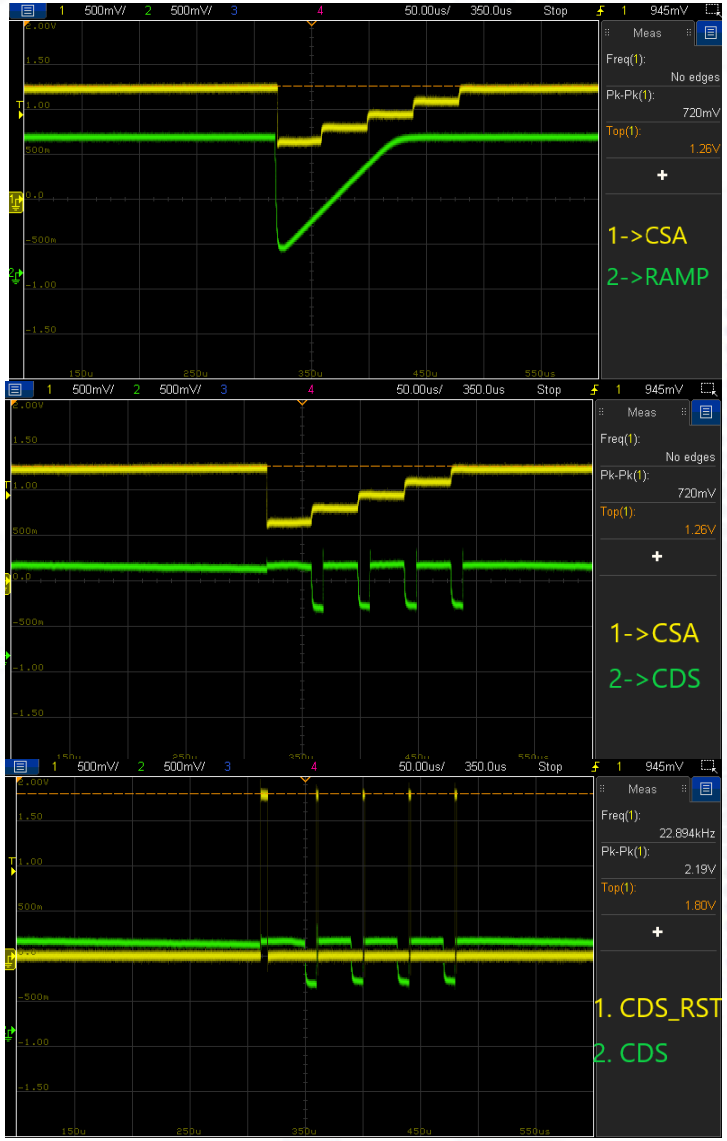
➢ Test setup



TEPIX Chip Test

- Power consumption = 0.36 mW/ch
  - 0.22mW for analog
  - 0.14 mW for digital
- Transient waveforms are correct

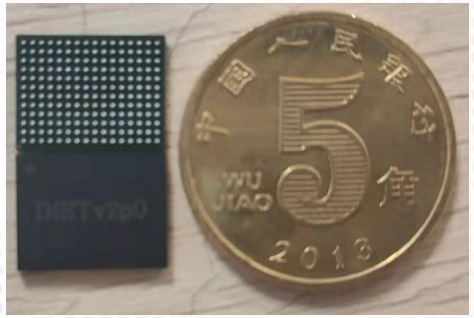
Power	Voltage (V)	Power (mW)
AVD	1.774	28
SVD	1.79	0
VDD	1.785	18



04 | Summary

Summary

- Various front-end ASICs for gas detectors have been developed at our group, from analog front-end only to SCA/ADC waveform sampling integrated
- Most recent readout ASIC (WASA) has been successfully developed for TPC
  - Power consumption is only 4.94 mW/ch @ 40 MHz
    - P_{AFE}=1. 38 mW/ch
    - P_{ADC} = 0.83 mW/ch
    - $P_{Digital}$ = 2.73 mW/ch
  - ENC = 569 e+14.8 e/pF @ gain=10 mV/fC
  - Next step: BGA package 16 x 11 (11.05 mm x 7.8 mm)
- R&D on mini-pad TPC has been started with TEPIX chip
  - The second version chip has been received and under test
  - Next step: ROIC and module test



Thank You