Interplay with DRD7

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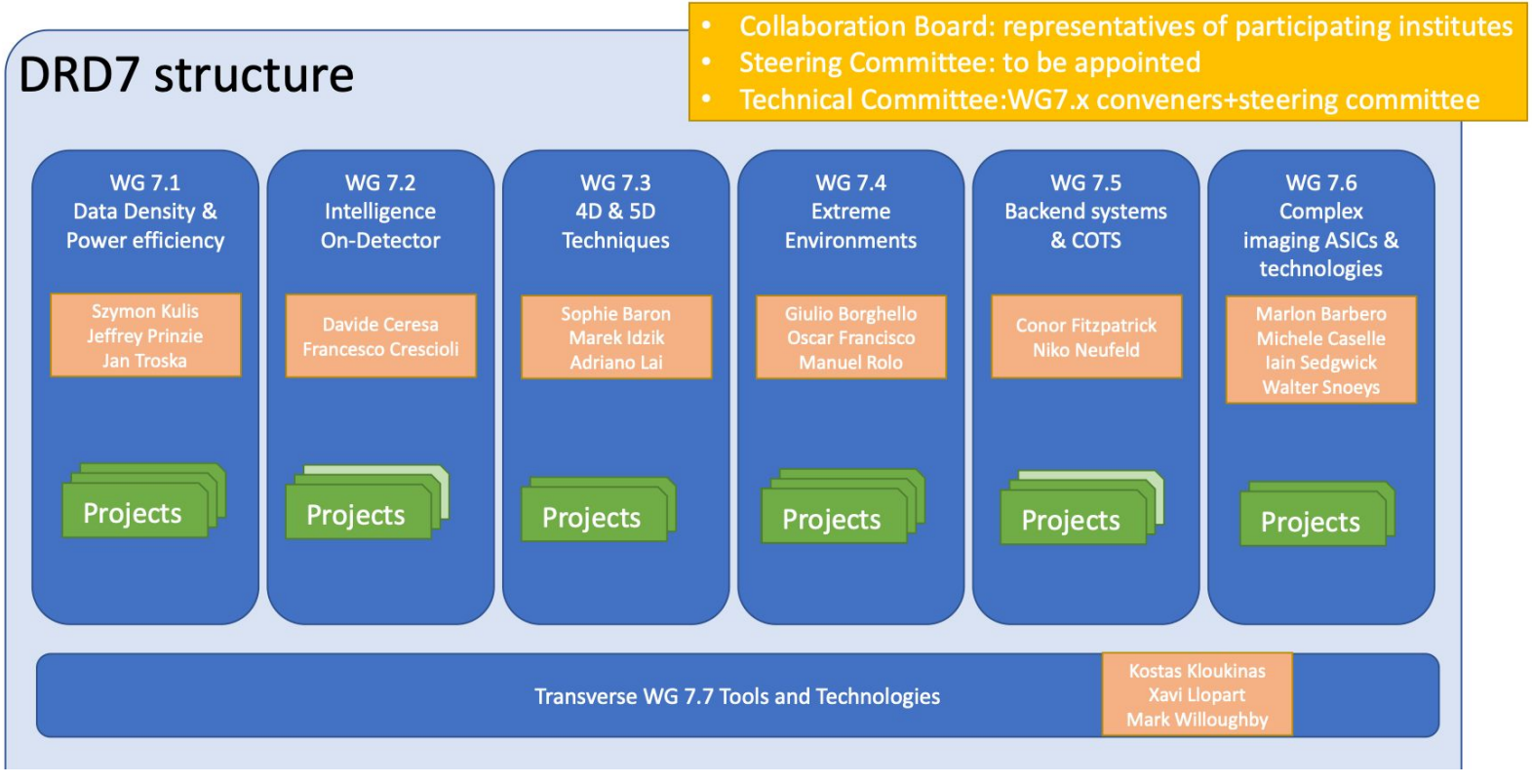
1st DRD1 Collaboration Meeting

Working Group 5: Electronics for gaseous detectors

31/01/2024

About DRD7: “Electronics”



DRD7 current proposed projects: a rich portfolio!

7.1.a Silicon Photonics Transceiver Development

• Medium-speed variant (4l x 25Gbps), and low-speed variant for cryogenic applications
– Design of PIC, driver, TIA
– Environmental characterization
– Packaging
– Fiber coupling, integration and testing

7.1.b Powering Next Generation Detector Systems

• High efficiency, low material budget
– High Voltage CMOS and GaN
– 28nm CMOS DCDC resonant converter IP
– High efficiency shunt LDO regulator
• Parallel and Serial Powering
– System-level characterization
– Radiation hardness and reliability

7.1.c Wireless Data and Power Transmission

• Multi-hop free space optical data transmission
– System-level analysis, demonstrators, custom design and full chain evaluation
• Exploration of wireless power transmission

7.4.a Modeling and development of cryogenic CMOS PDKs

• TSMC 65nm or 28nm
– Parameter extraction down to 4K
– Development of mixed-signal cold-IPs
– Characterization and documentation of developed IP blocks
– Demonstrator cryo-chip

7.4.b Radiation resistance of advanced CMOS nodes

• Rolling survey of technologies
– Focusing on specific nodes (i.e.7nm finfets or 3nm LGAA), or specific effects (low dose rate, NIEL scaling, noise, …)
– New material systems (GaN, SiGe, ...)
– Facilities and qualification protocols for ultra-high doses

7.4.c Cooling and cooling plates

• Ceramics cooling plates
– Fabrication and validation of high-pressure resistance, leak tightness, and performance
• Microchannel cooling
– Fabrication of silicon interposers with i

7.2.a eFPGA, Programmable Logic Array IP (TBC)

– Study and comparison of open frameworks
– Radiation hardening and characterization
– Development of software and infrastructure for synthesis and mapping of user-code

7.2.b Radiation-tolerant RISC-V processor and SoC platform

• Enabling reconfigurable, retargetable ASICs
– Abstract design methodology
– Reusable, standardized IP blocks
– Control processor (RISCV) and framework
– Programmable, flexible logic blocks

7.2.c Virtual electronic system prototyping

• High-level description of system, front-end to back-end
– Specification and performance modeling
– Reference for verification
– Virtual prototyping

7.5.a COTS architectures, tools and IPs

• Benchmark common TDAQ algorithms/workflows
– Define figures of merit
– Develop optimized reference implementations
– Maintain knowledge and community-led repository

7.5.b No backend, direct 100GbE rad-tol solutions from FE to DAQ

• Feeding directly COTS switches
– NICs or DAQ processors
• Feeding intermediate COTS-based aggregators
– Low latency bridge to COTS switch

7.5.c Generic backend board (TBC)

• Critically review specificities of DAQ systems in HEP
– Slow custom links from frontend, interfaces to custom timing system, additional monitoring and configuration data streams, inline processing, etc.
• Compare, discuss and benchmark performance of parallel developments
– Explore possibility of establishing a common X-experiments base in hardware, firmware and

7.3.a High performance TDC and ADC blocks at ultra-low power

• Medium/high resolution, multi-channel ADC @40MS/s,
• High precision, multi-channel TDC (10ps)
– Experts' platform for sharing, comparing and benchmarking ideas, designs and ASICs

7.3.b Time measurement and distribution

• Characterization, simulation and calibration of timing sources
– Develop and compare procedures
– Study and implement standard/generic solutions
• Timing distribution techniques and systems
– Explore limits of COTS components
– Investigate and compare alternatives
– Develop protocols for precise & deterministic clock distribution

7.6.a Common access to selected CMOS imaging technologies and IP blocks

• Tower-180nm, LFoundry-110nm, TPSCo-65nm
– Provide efficient and affordable access to technologies
– Develop and distribute PDKs and IPs
– Manage legal and commercial frameworks
– Share test results

7.6.b Common access to 3D and advanced integration

• Access to research or commercial facilities mastering chiplets, 2.5/3D and Si-photonics integration
– TSV, RDL, interposers, C2C, C2W and W2W bonding
• Development and prototyping of demo

7.7 Tools and Technologies

DRD7 “philosophy”: (from “Organisation of the DRD7 collaboration” V6, 09/5/23:)

- DRD7 is an R&D collaboration, and ***will not provide a design or fabrication service for ASICs or other components***; this is the role of engineering teams at institutes and laboratories participating in the various DRD projects.
- Where **common developments across DRDs** are agreed, either of IP, or of complete devices or subsystems, ***DRD7 is available to set up a review and coordination body***.
- ***Funding for specific electronic developments and prototypes in DRDs should be allocated to the relevant collaborations***, with prioritisation decisions made by the collaborations ***as part of their funding request and review***. In case of complex electronics developments (and in particular of ASICs), ***a review coordinated by DRD7*** will be instrumental in lowering the development risk and limiting duplication of effort.
- Funding for DRD7 R&D and coordination activities will be separately requested, including the costs of common tools, the costs of specialised personnel (for instance, verification experts), specific R&D developments at both device and system level, and the technical facilities necessary for R&D.
- **Proposals for R&D projects involving electronics and data-processing** can be included in either detector-related DRDs or in DRD7, taking into account the following guidelines:
  - ● Projects in DRD7 will target common generic developments, or exploration of cutting-edge technologies requiring negotiated access to frameworks and complex design flows. They may involve high costs, expert coordination or unique expertise, and can possibly only be effectively delivered as a common community effort. They will follow design practices enabling later volume production in industry and/or using COTS components.
  - ● Projects in individual DRDs will target developments driven by DRD-specific requirements. They will typically be smaller-scale prototypes exploring or benchmarking novel concepts or technologies and delivering demonstrators. They will focus on diversity and originality, but will not necessarily be suitable for large-scale production.

 DRD≠7 should try to identify if *common generic development* concerning ASIC and/or DAQ can be setup across collaborations

DRD1 needs for electronics. (work Packages extract)

Task	Performance goal	Comments	Possible deliverables next 3-5 y
(Muon systems) New front end electronics	- 1 fC threshold - Geometrical avalanche quenching - High sensitivity electronics and new detector structures to achieve stable and efficient operation (rate, occupancy) up to O(MHz/cm2)	- Study of the integration of the FE electronics in the detector Faraday cage - Study of the integration of electronics and readout PCB	- Conceptual electronics design based on gas detector simulation and experimental measurements - Development and test of a front-end prototype
(Large-volume drift chambers) Front-end ASIC for cluster counting	- High bandwidth - High gain - Low power - Low mass	achieve efficient cluster counting and cluster timing performances	full design, construction and test of a first prototype of the front-end ASIC for cluster counting
(Straw chamber) Electronic readout, ASIC	- Time readout with sub-ns precision - Leading edge and trailing edge time readout	- Dedicated R&D on ASIC	- ASIC - Readout system
(Time Projection Chambers) Low-power FEE	•< 5 mW/ch for >1e6 pad TPC - ASIC development in 65 nm CMOS	•continuous vs. pulsed	- Present stable operation of a multi-channel TPC prototype with a low-power ASIC
(Gaseous photon detectors) FEE	- High input C - Low noise - large dynamic range	•	- present an ASIC concept/prototype
(Gaseous timing detectors) Low-noise FEE	- High input C - large dynamic range - Fast rise time - sensitivity to small charge - Low noise	•	Define an ASIC
(Muon systems) Scalable multichannel readout system	•Front-end link concentrator to a powerful FPGA with possibilities of triggering an O(20GBit/s) to DAQ	- FPGA based architecture - FPGA with embedded processing for triggering and ML - Basic firmware and software can be bootstrapped from existing readout system	First prototype by end of 2024 for commissioning at test beams
(Large-volume drift chambers) Scalable multichannel DAQ board	- High sampling rate - Dead-time-less - DSP and filtering - Event time stamping - Track triggering	- FPGA based architecture - ML algorithms-based firmware	working prototype of a scalable multichannel DAQ board
(Straw chamber) Electronic readout, ASIC	- Time readout with sub-ns precision - Leading edge and trailing edge time readout	- Dedicated R&D on ASIC	- ASIC - Readout system

DRD7 rich portfolio, overlaps with DRD1 desiderata?

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several middle/long term “basic” R&Ds
that should be followed to keep us updated

7.3.a High performance TDC and ADC blocks at ultra-low power

“long term” answers to some of our requests are worked out here…

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here the forums and the exchange of knowledge occurs

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How DRD1 does see interplay with DRD7

Understood the more long term and generic R&D in DRD7:

- Gas targeted ASIC in DRD1, **we expect DRD7 support us in accessing foundries and design kits** (-> WG 7.7 OK!). Repository for IP exchange is also very welcome.
  - We acknowledge and share the concern about NDAs and technology access limitations/boundaries. May be, DRD7 can help/coordinate having pre-approved(*) framework/models of NDAs that simplifies the cooperation of groups from different institution and countries working on the same task/project, as well as basic assistance and guidelines for "export licences" when they are needed
- There may be technological aspects specific to DRD1 in the course of various developments that may need a "heavier" endorsement than what the teams in DRD1 alone can provide.
- DRD1 (RD51) has an history of developing (quite) general purpose scalable acquisition system (SRS), and plans to continue doing. How does that fit/interact with DRD7? Not now… may be in the future?
- Electronics development is ultimately carried out by individual researchers or institutes as sub-task of individual DRDs (and in most cases funding follows the same pattern). With increasing development cost comes the need for the community to stay together and help each other also across DRDs
  - An example is the joint collaboration between developers in DRD6 and DRD1 on electronics for calorimetry
- Would DRD7 being the place where electronics developers of different DRDs will "meet", "exchange experiences", and "know each other", and, eventually, collaborations are triggered? i.e. should DRD7 organize meetings for this purpose, without absorbing any deliverables from the other DRDs? WG 7.7 ?

(*) the idea here is to have a NDA document, already discussed and approved by (CERN?) lawyers and involved companies (e.g. foundries) that, as long as the clauses inside are respected, can be used (signed) to support effective cooperation (full project sharing) between people of different institutions and countries, avoiding case by case long negotiations.

Comments?
Suggestions?
Requests?

Electronics “wish-list” in DRD1

- High performance charge-sensitive front-end circuit specific for medium and large volume gaseous detectors (MPGD, TPC, drift chambers, straw tubes, RPC, …)
  - High input capacitance (2-2000 pF)
  - Low noise/high sensitivity (eg. ~100e@2pF; 50mV/fC)
  - Low power (~ few mW/ch)
  - High dynamic range (12-14bits, 1:50000, several strategies)
  - Precise timing (10-100ps - linked to Ion tail processing and extraction of electron charge peaks)
  - High event-rate (1MHz/cm2 -> several MHz/channel)
- Pixelated readouts (charge- or photon-sensitive detectors with high timing resolution)
  - Optimization of pixel size (>200 μm)
  - Provide a large-area pixel-based readout
- Architectural innovations R&D
  - Versatile front-end circuitry (variable parametric front-end and shaping circuit, variable resource distribution,…)
  - Cluster-counting (continuous readout, 1GHz analog bandwidth front-end, 2GSps high-sampling rate, on-line processing with direct mathematical algorithms or Machine Learning)
  - Deadtime-less readout, self-trigger vs continuous sampling with digital data compression
  - High-rate data-acquisition (> 1MHz/ch, up to Tb/s total DAQ bandwidth – scalable systems mapped on switched networks, generic DAQ for different Front-Ends)
- Technological developments
  - High-voltage tolerance/spark protection
  - Detector biasing via ASIC (eg TSV for HV)
  - Combined detector & electronics assembly technology, cooling & services integration (integration of the FE electronics in the detector Faraday cage)
- Platform for sharing and collaborative development of Processing IPs and building blocks
  - Sharing and co-design of front-end building blocks.
  - Signal/Event Processing on- or off-chip (eg. peak finding, baseline restoration, feature extraction, etc.… - reusable IP library for online use in FPGA/ASIC or offline in software)
  - Proper mechanism for open access, end user agreement, protection of Intellectual Property and authorship recognition.