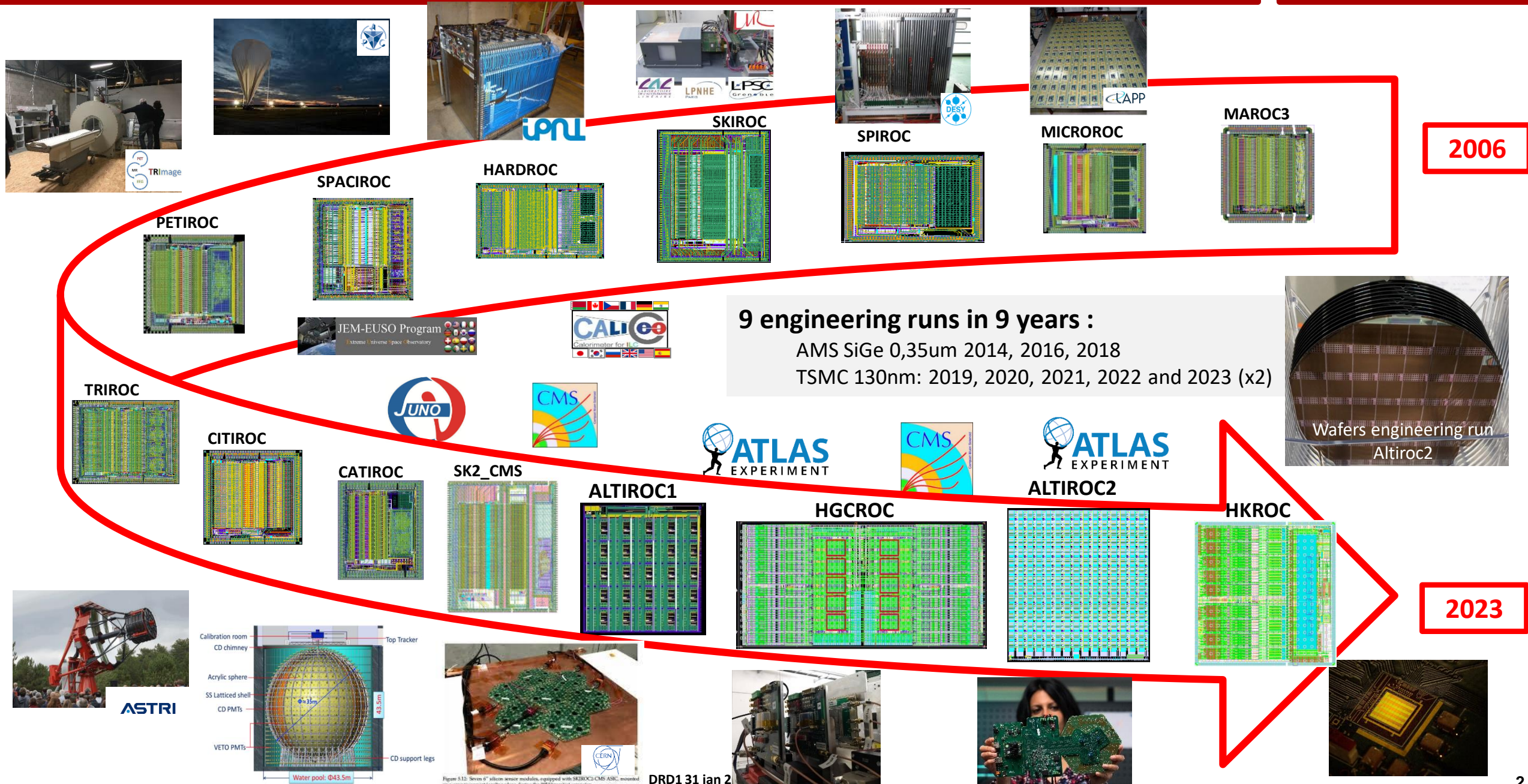


HGCROC and HKROC

DRD1 meeting CERN 31 jan 2024

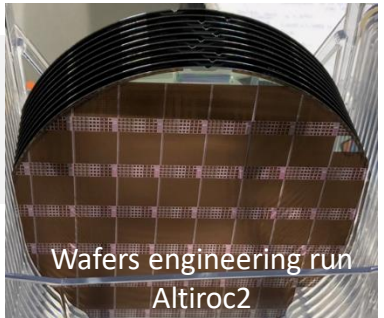
Ch. De LA TAILLE – taille@in2p3.fr
Ecole Polytechnique – CNRS

OMEGA ASICs : overview

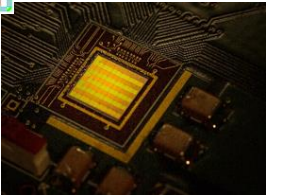


2006

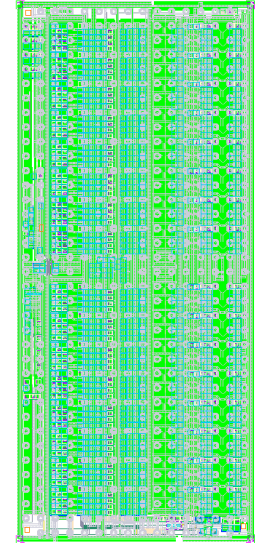
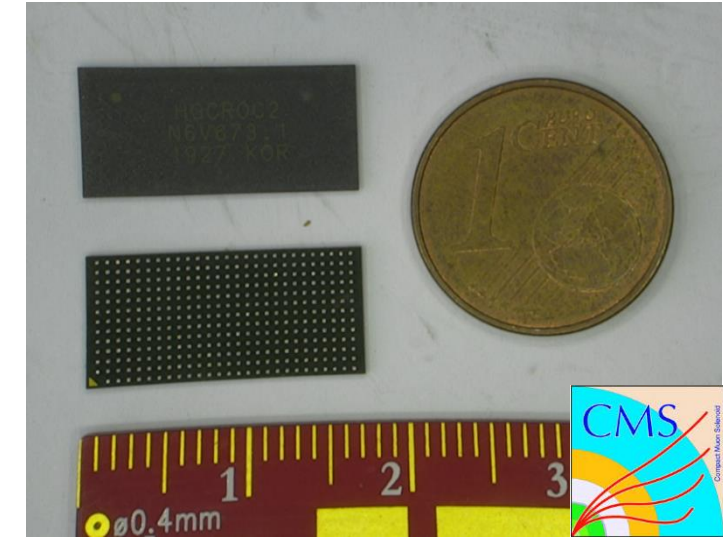
2023



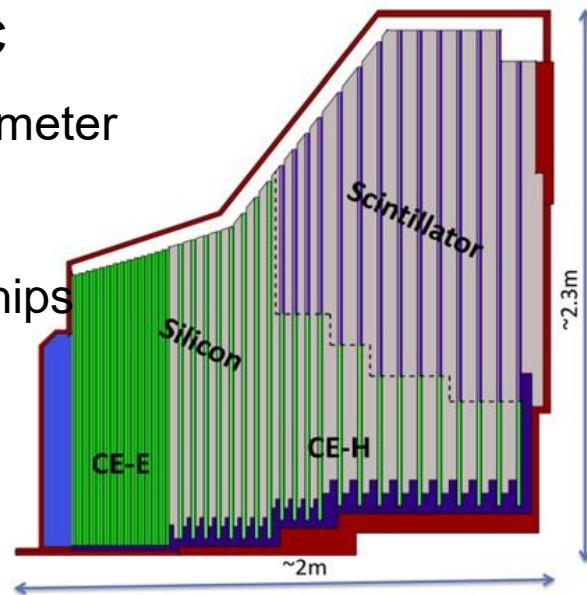
Wafers engineering run Altiroc2



- Omega strongly involved in LHC ATLAS & CMS upgrades
- HGCROC/H2GCROC : High Granularity Calorimeter Read Out Chip
 - 78 channels of Si/SiPM readout for calorimetry
 - ADC + TOT + TOA
 - Collaboration : AGH, CEA, CERN, Imperial, OMEGA
- HKROC : PMT readout for PM tubes
 - 3*12 to 36 channels (tri-gain or mono gain)
 - ADC + TOA
 - Collaboration : AGH, CEA, CERN, Imperial, OMEGA
- LIROC : ATTRACT project for space based LIDAR
 - 64 high speed (GHz) amplifiers/discriminators « à la petiroc »
 - 3 ns double pulse resolution on single photons
 - Collaboration OMEGA-WEEROC
- CMOS 130 nm process rad hard up to 300 MRad



- Upgrade of CMS at HL-LHC
 - New “5D” imaging calorimeter
 - Si and SiPM sensors
 - HGCROC/H2GCROC chips



	CE-E Silicon	CE-H Silicon	CE-H Scintillator	Total
HGCROC	60 324	31 596	8 496	100 416
Motherboards	5 004	2 556	384	7 944
Bidirectional data/control links	5 004	2 556	384	7 944
Trigger links	4 020	2 556	768	7 344

Requirement: Use very similar FE electronics for the readout of both detectors

- Si (~ 4 fC / MIP)
- SiPM-on-tile (~ 1.7 pC / MIP)

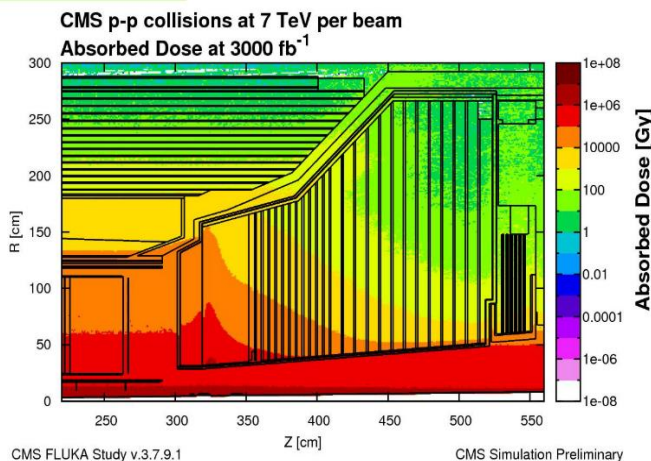
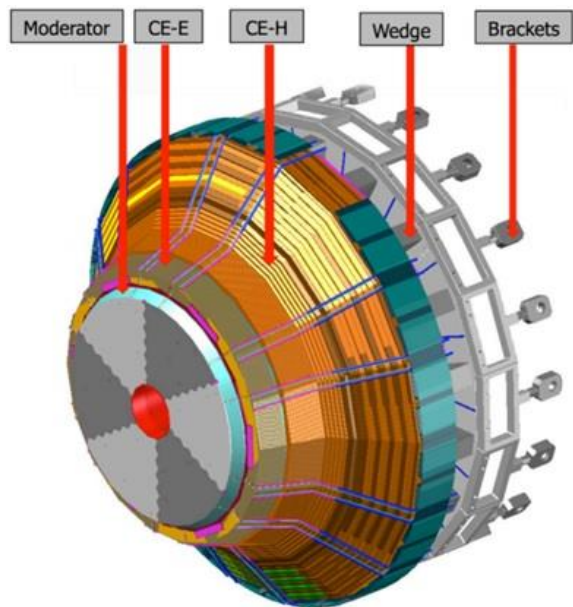
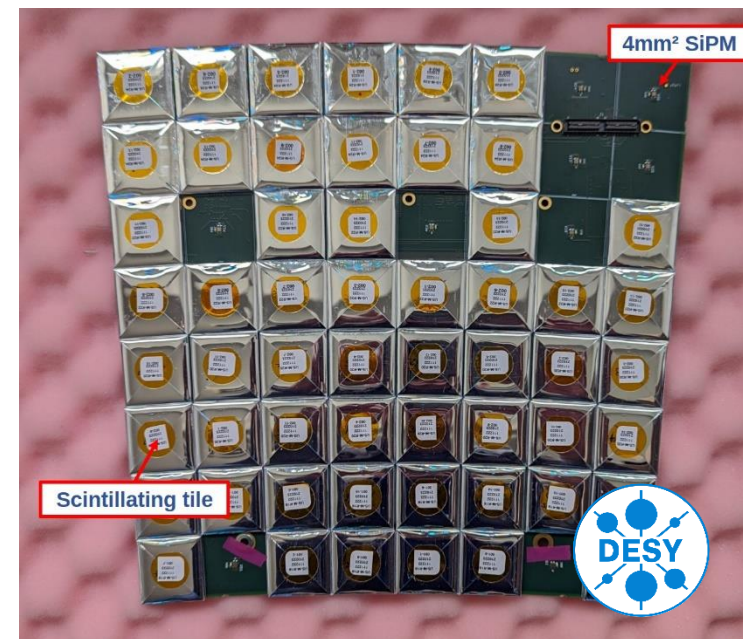


Figure 1.1: Dose of ionizing radiation accumulated in HGCal after an integrated luminosity of 3000 fb^{-1} , simulated using the FLUKA program, and shown as a two-dimensional map in the radial and longitudinal coordinates, r and z .



Overall chip divided in two symmetrical parts

- **1 half is made of:**
 - 39 channels: 18 ch, CM0, Calib, CM1, 18 ch
 - Bandgap, voltage reference close to the edge
 - Bias, ADC reference, Master TDC in the middle
 - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

Two data flows

- **DAQ path**
 - 512 depth DRAM (CERN), circular buffer
 - Store the ADC, TOT and TOA data
 - 2 DAQ 1.28 Gbps links
- **Trigger path**
 - Sum of 4 (9) channels, linearization, compression over 7 bits
 - 4 Trigger 1.28 Gbps links

Control

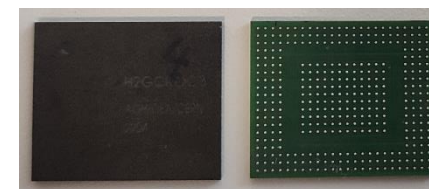
- **Fast commands**
 - 320 MHz clock and 320 MHz commands
 - A 40 MHz extracted, 5 implemented fast commands
- **I2C protocol for slow control**

Ancillary blocks

- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain

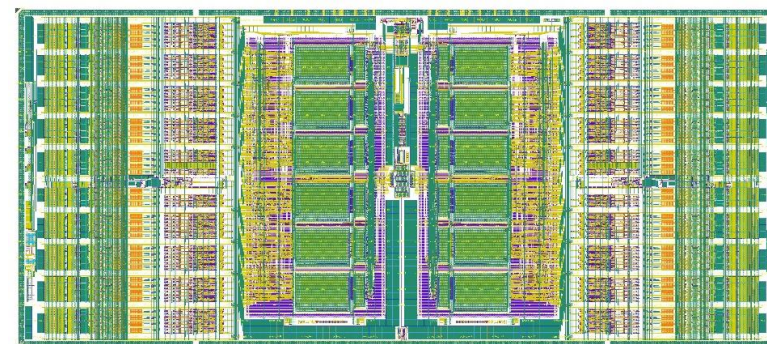


HGCROC3
High density

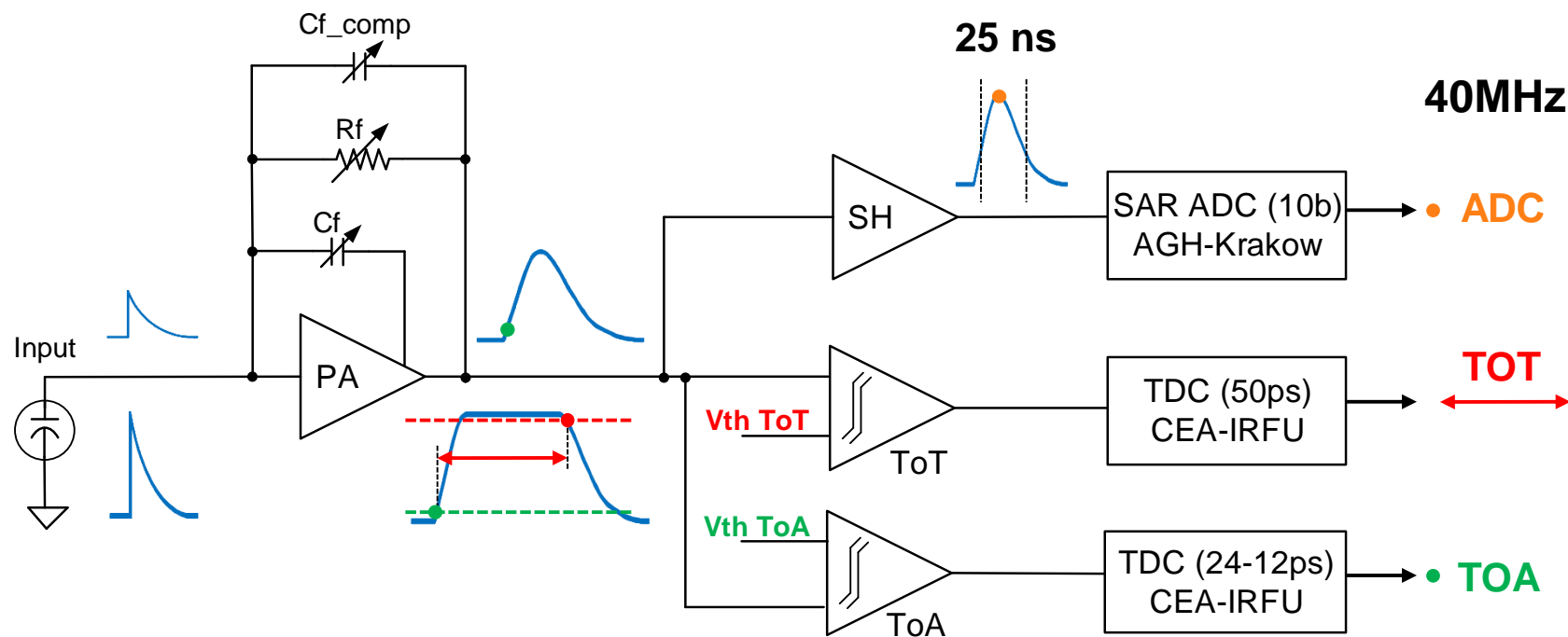
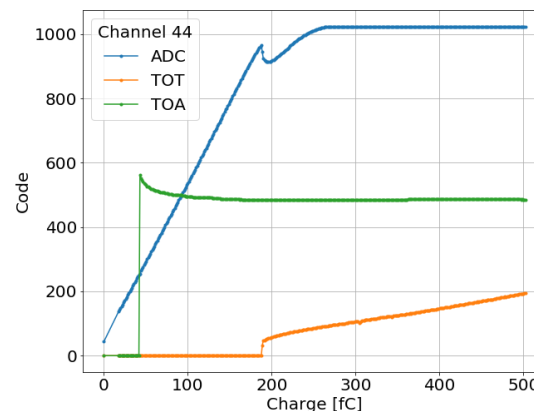


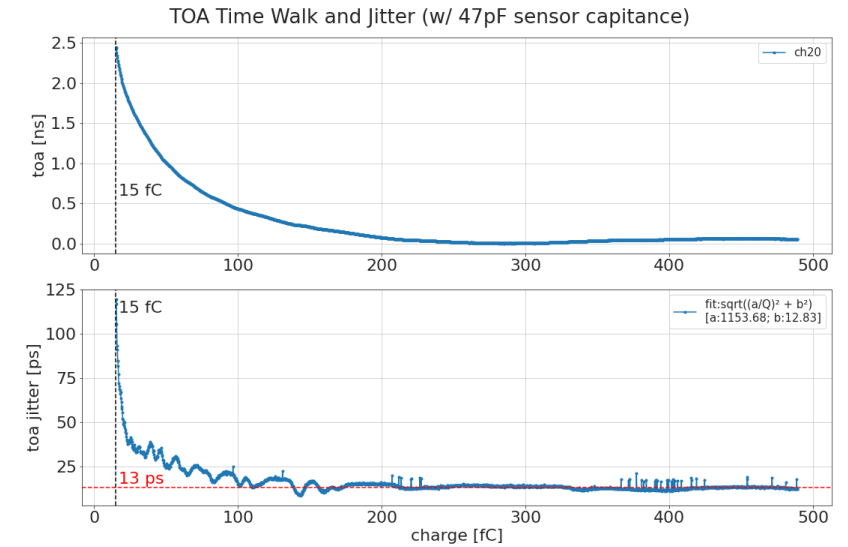
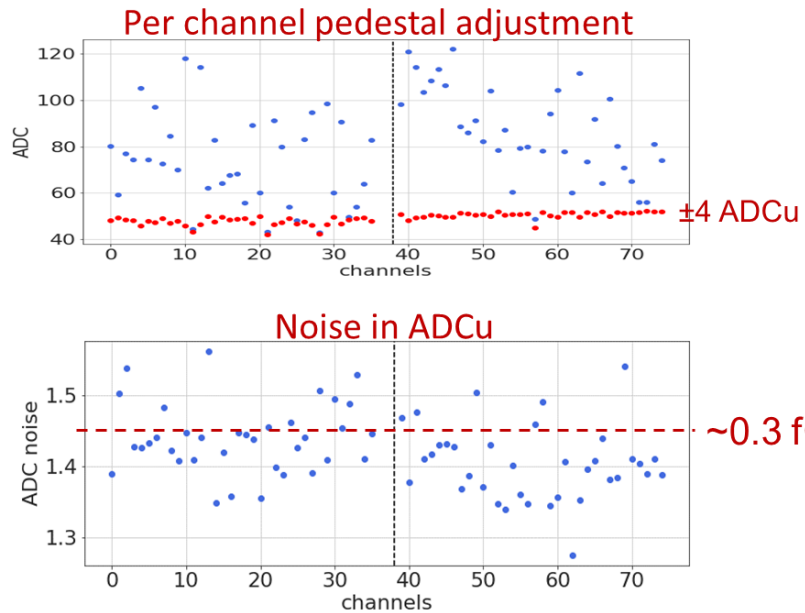
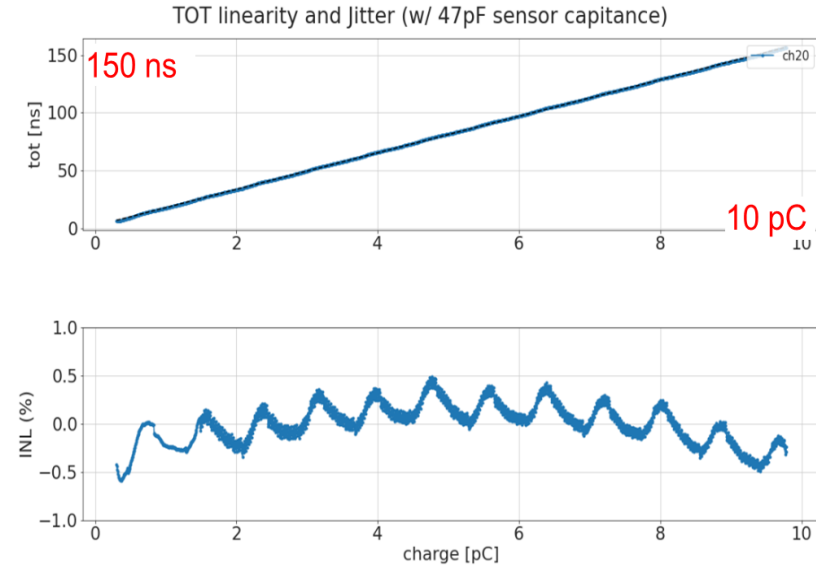
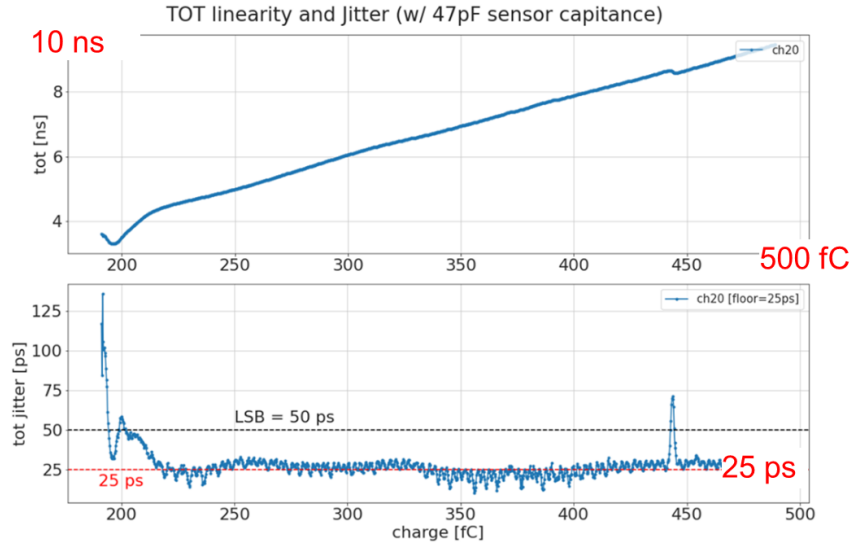
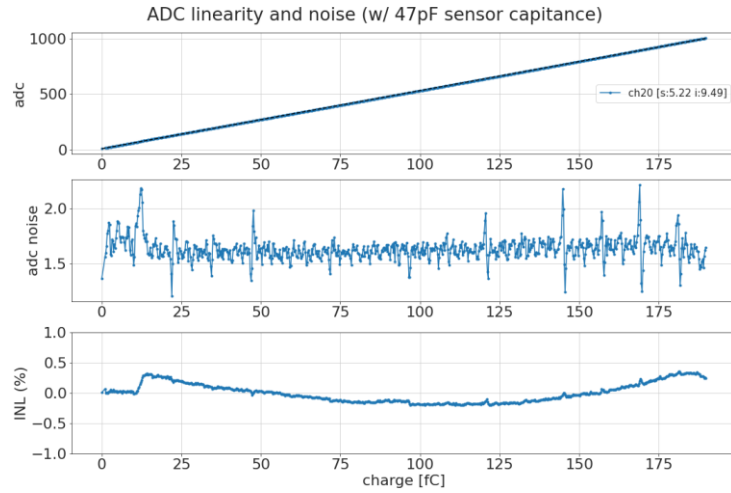
H2GCROC3
Low density

HGCROC3 Layout:



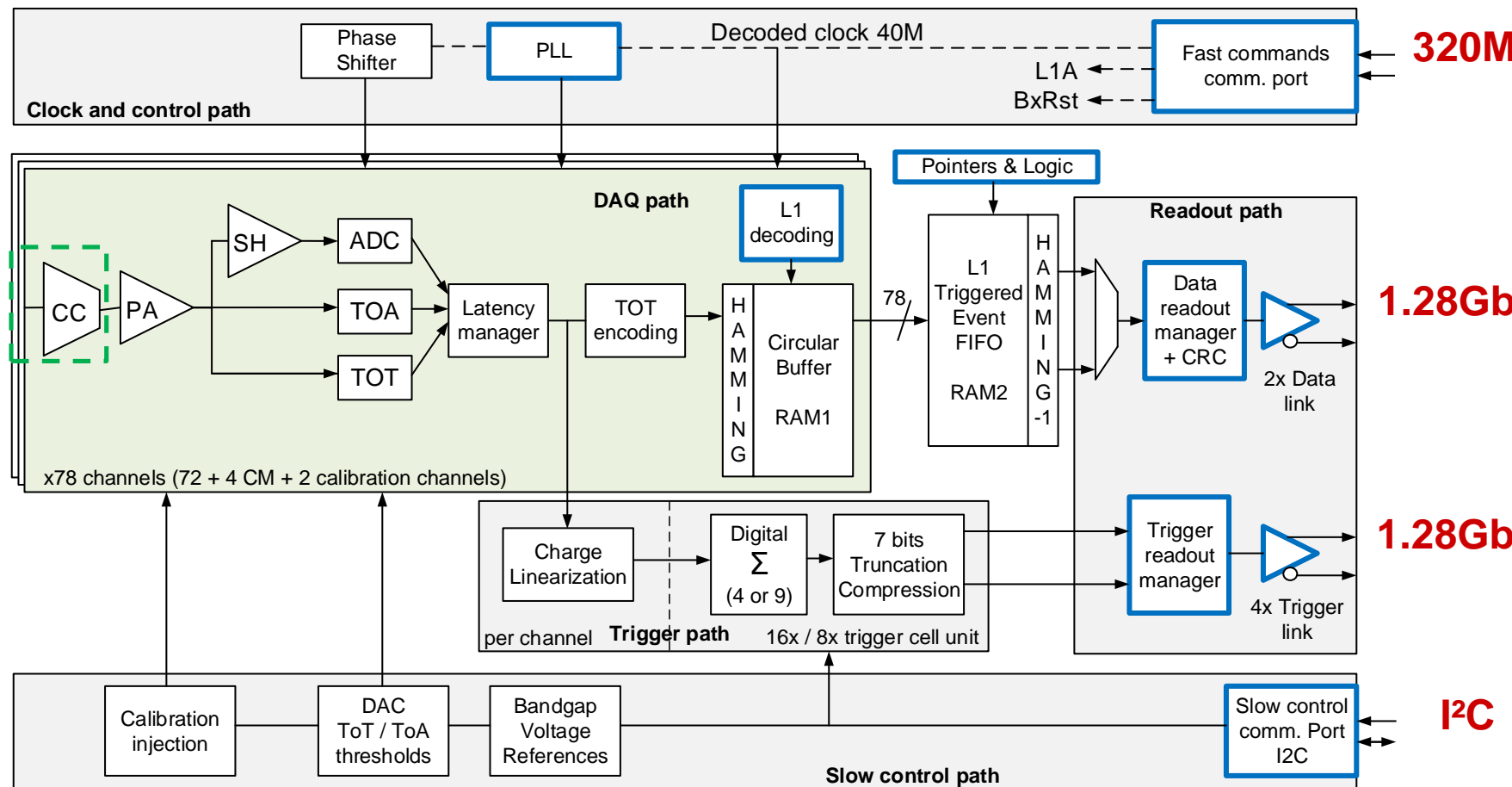
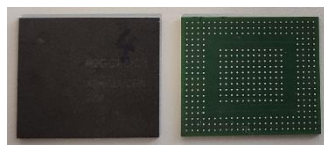
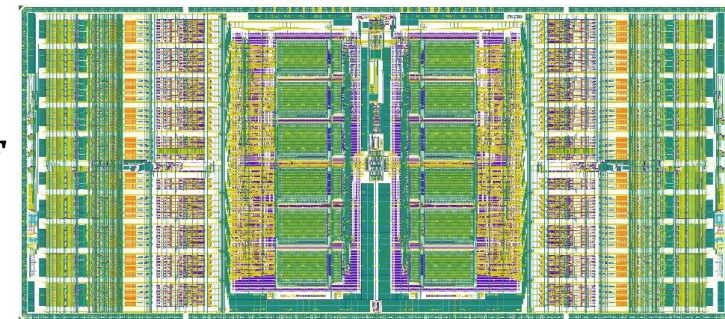
- **Calibration pulser**, 0.5pF and 10 pF calibration cap.
- **Preamp** : adjustable gains for 80, 160 and 320 fC ranges
- **Tunable TOT** over 5 bits
- **Sallen Key shaper RC4**, $t_p < 25$ ns, tunable ($\sim 20\%$) with 2 bits, $BX+1/BX < 0.2$
- Temperature stabilization to < 0.5 mV/K
- **10 bit ADC** from Krakow AGH
- **TOT and TOA TDCs** from CEA-IRFU





Requirements for H2GCROC (The SiPM version of the ASIC):

- Charge dynamic range : **160 fC to 320 pC**
- Timing accuracy **< 100ps** for pulses above **3 MIPs (4.5pC)** for a $C_{det} = 100pF$
- Compensation of the leakage current up to **1mA**
- Radiation resistance up to **300 kRad**
- **Input DAC** to tune the overvoltage



Current Conveyor based on KLAUS chip from Heidelberg UNI.



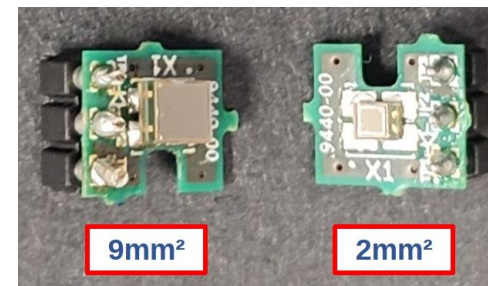
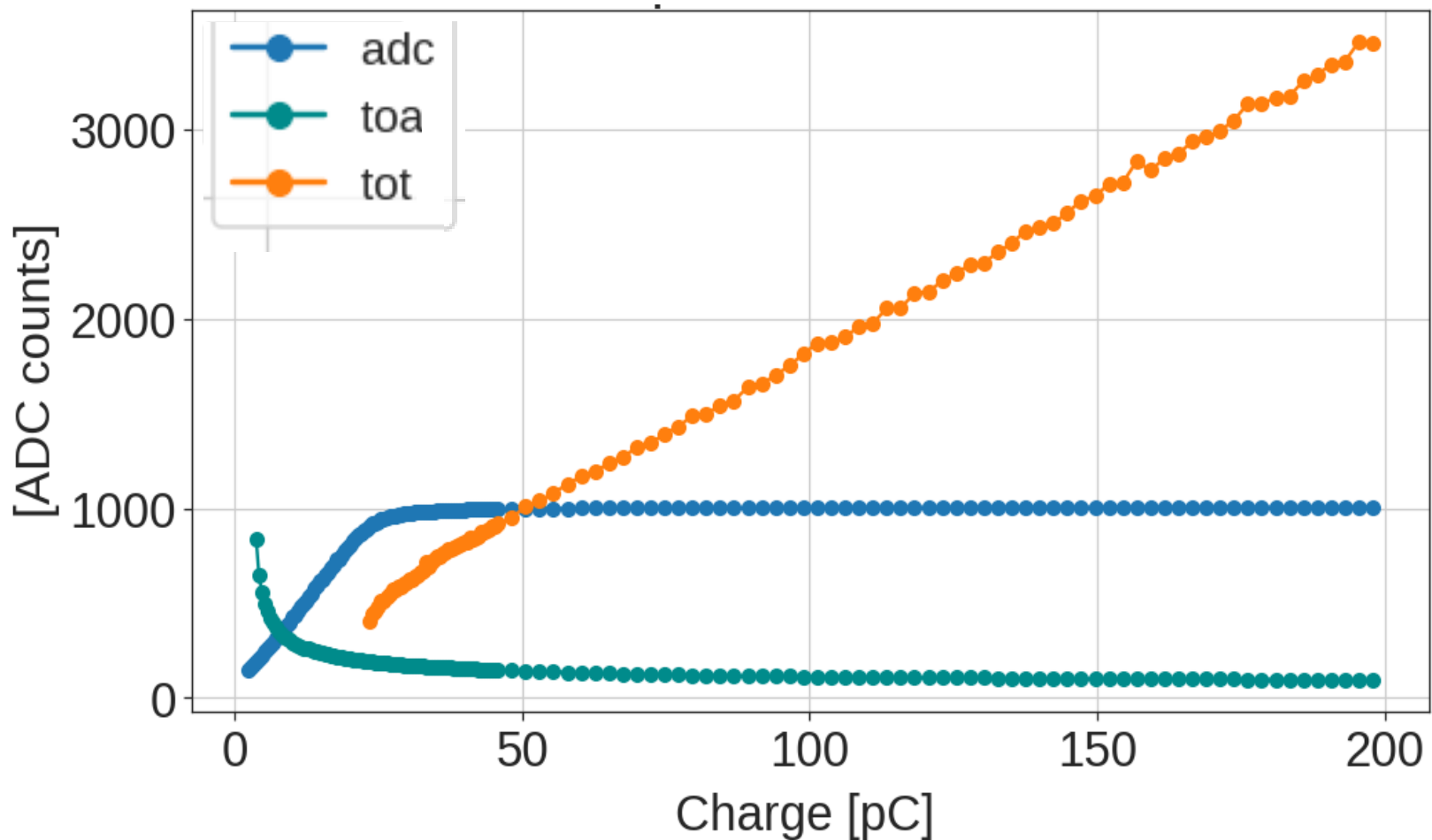
Attenuates the current at the input with 4 bits.



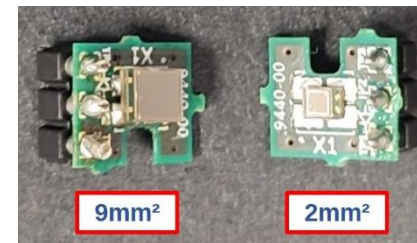
CC gain:
0.025 to 0.375
(step 0.025)



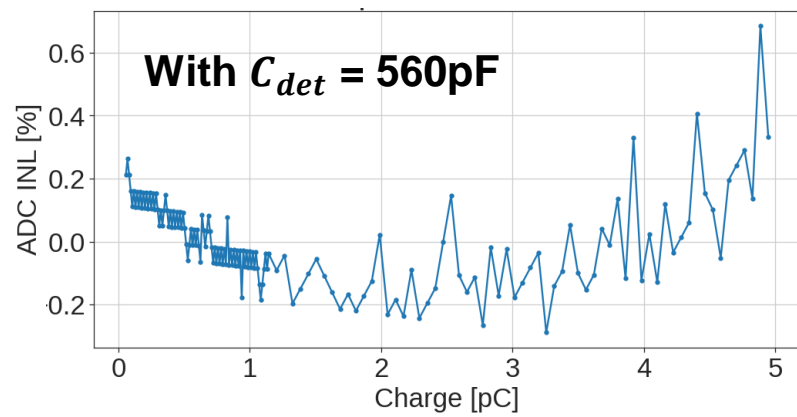
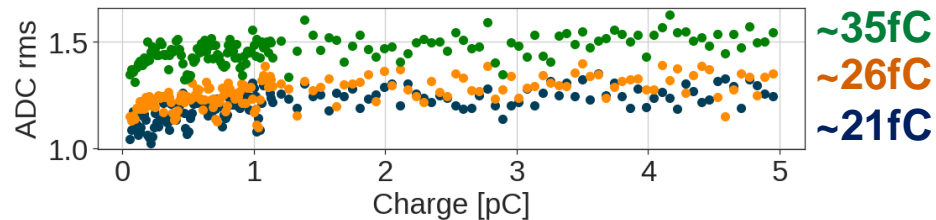
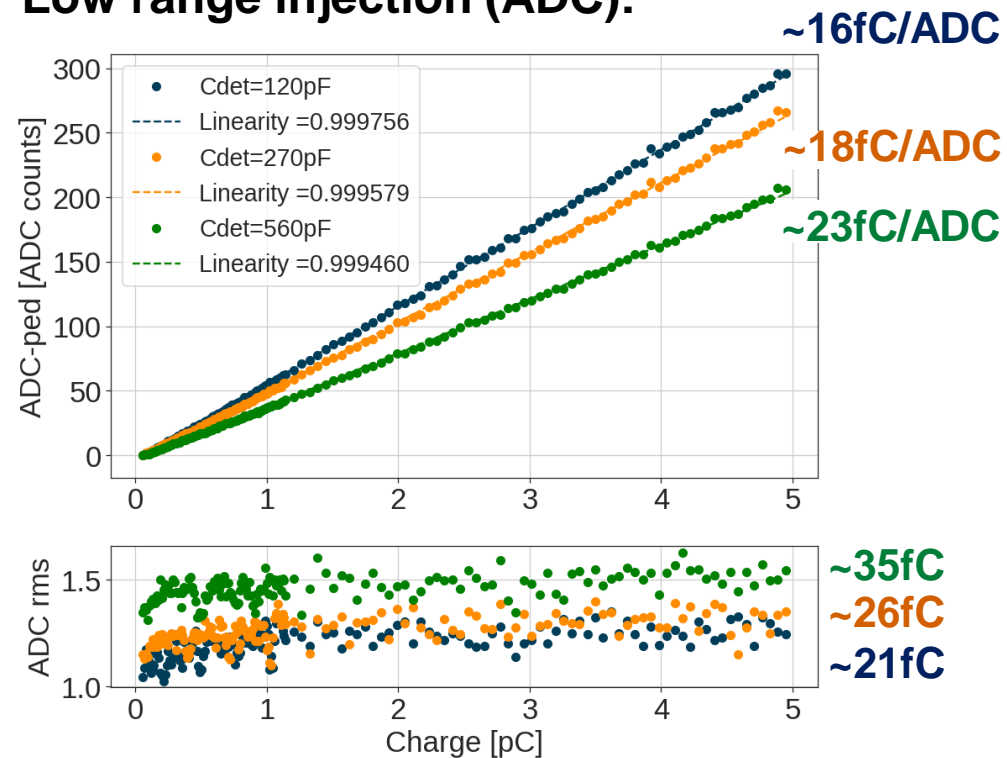
- 16bit dynamic range split in 10 bit ADC and 12 bit ToT
- Tests with 2 sizes of SiPM : 2mm² (120 pF) and 9 mm² (560 pF)



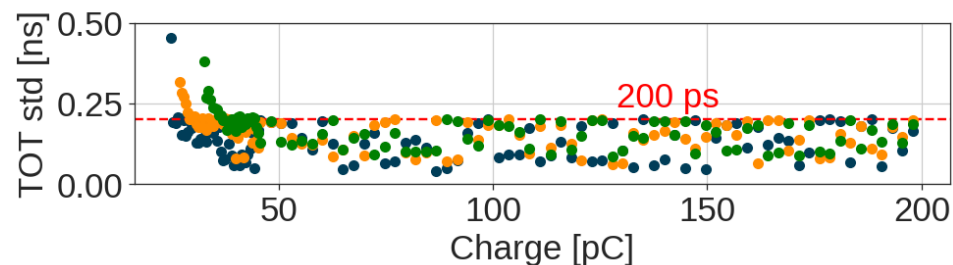
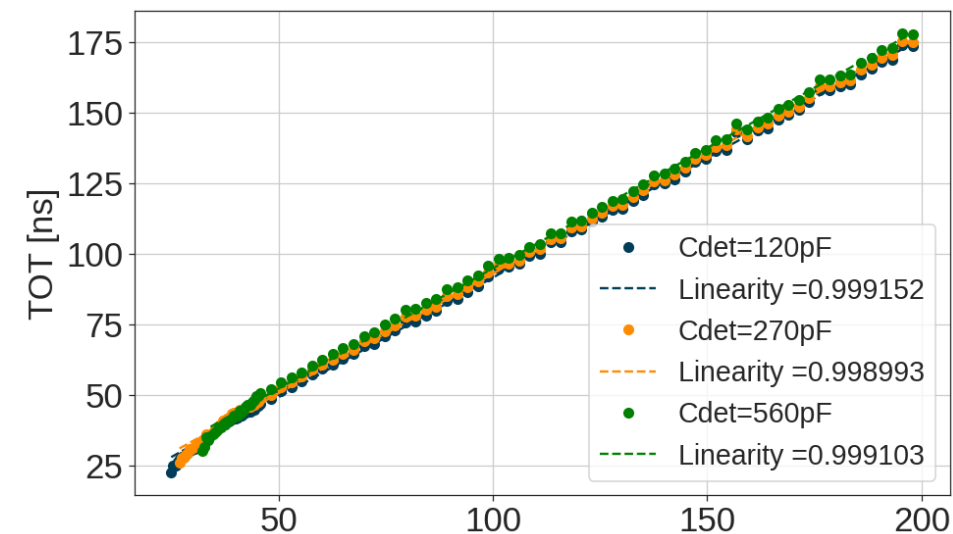
- ~ 60 fC minimum detectable charge efficiently, up to 320pC



Low range injection (ADC):

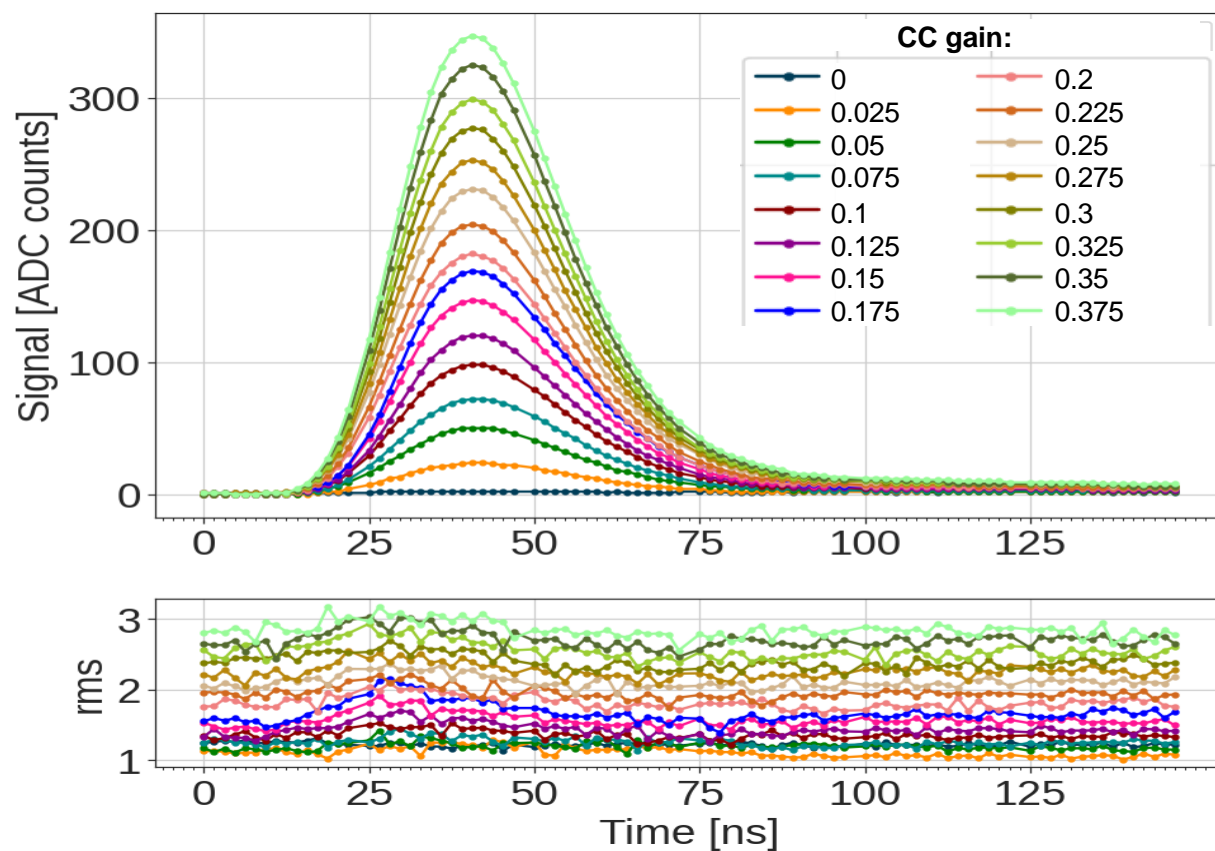


High range injection (TOT):

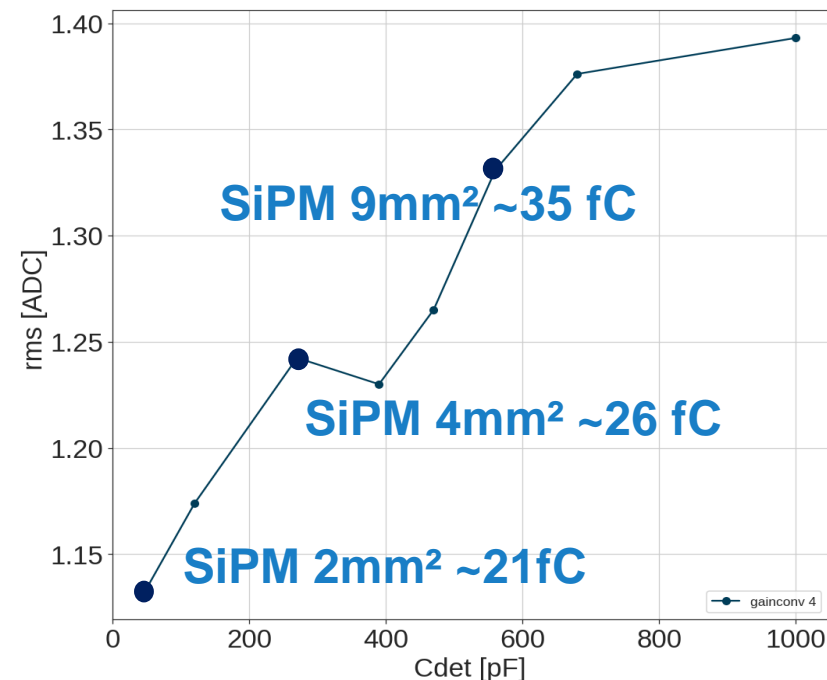


- The CC gain has good performance in linearity.
- The increment in noise is due to the gain configuration and the detector capacitance of the SiPM.

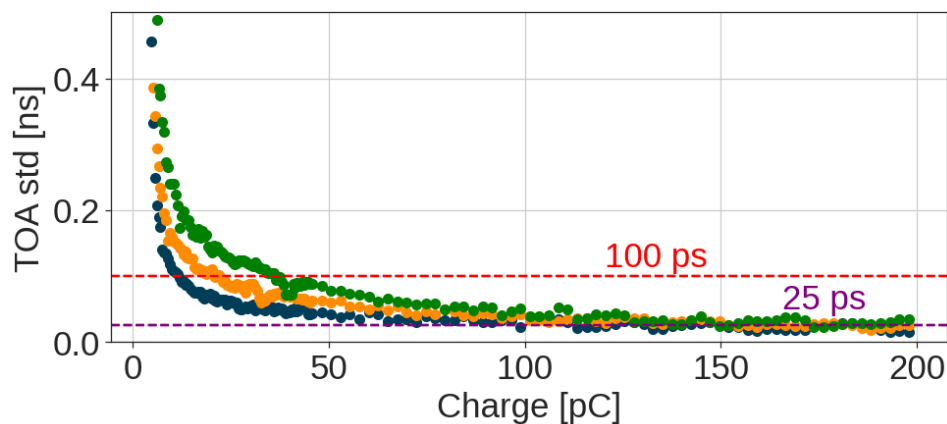
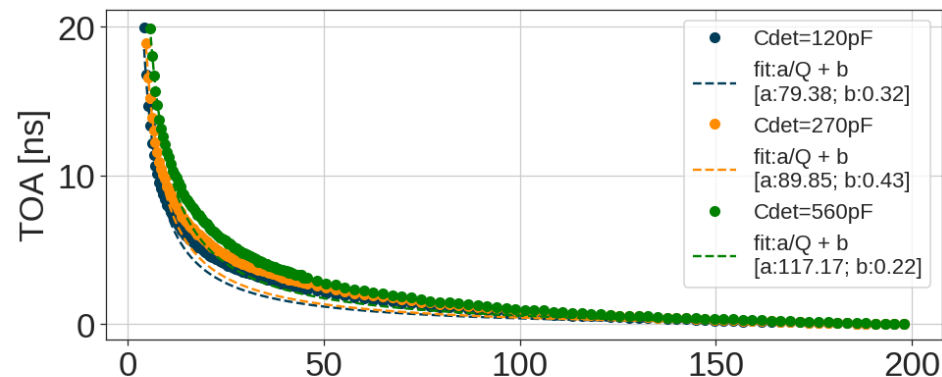
CC gain scan:



Noise vs C_{det} :



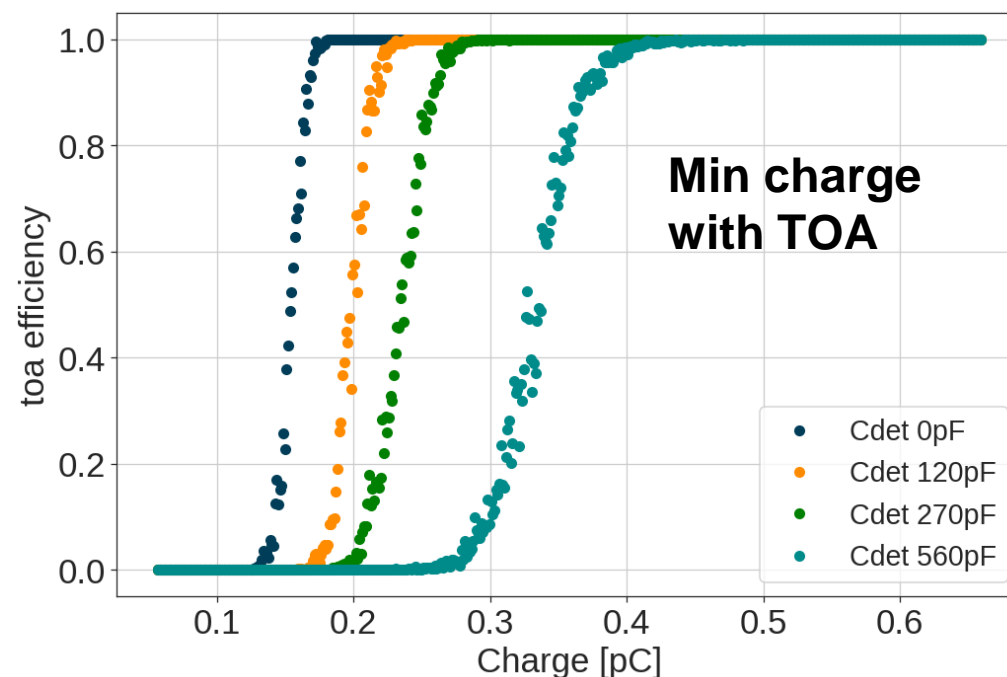
Time of Arrival (TOA) :



- The increase in noise due to larger C_{det} shifts the minimum charge associated with TOA data.
- The thresholds can be adjusted channel-wise for a uniform performance.

Effect of C_{det} on TOA:

- Larger C_{det} produce larger time walk due to the duration of the signal.
- Increasing C_{det} delayed the achievement of a 100ps resolution in charge injection.



Also a different configuration of the ASIC is necessary to increase the SNR.

2mm²:

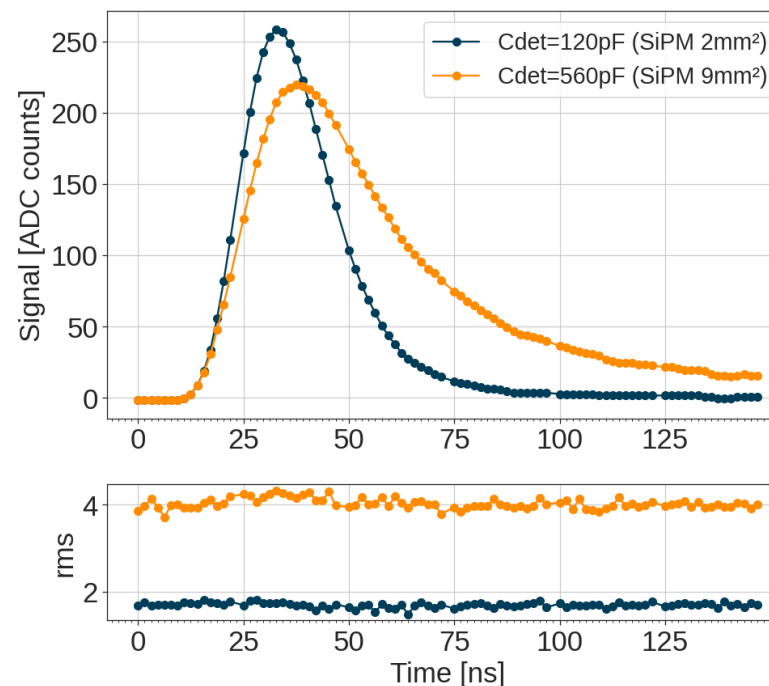
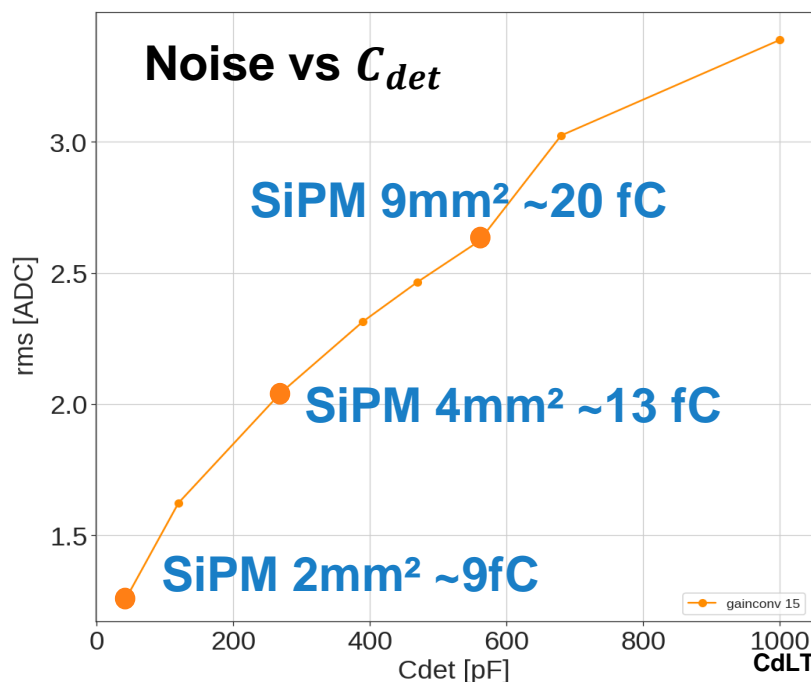


- CC gain attenuation = **0.3**
- $R_f = 16.6 \text{ k}\Omega$
- $C_{f_total} = 600 \text{ fF} (C_f + C_{f_comp})$

9mm²:



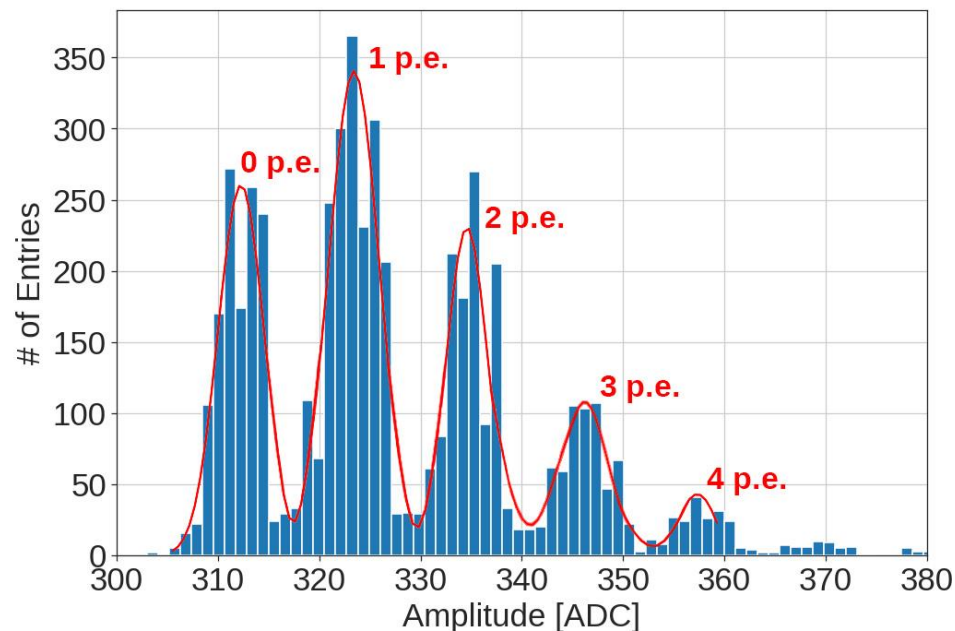
- CC gain attenuation = **0.375**
- $R_f = 16.6 \text{ k}\Omega$
- $C_{f_total} = 300 \text{ fF}$ (To make the pulse shorter)



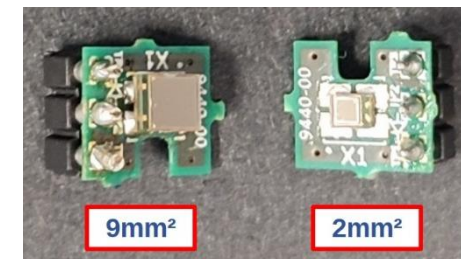
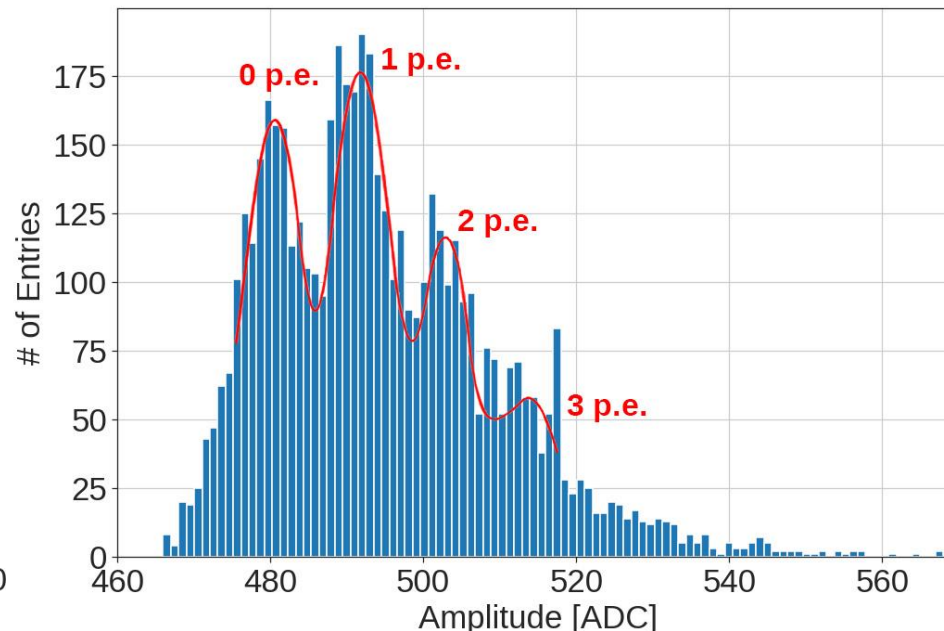
*Noise measured with the same configuration parameters for all C_{det} .

- The increment in noise is due to the detector capacitance of the SiPM.
- SNR can be improved with the gain configuration.

- 2mm²:



- 9mm²:

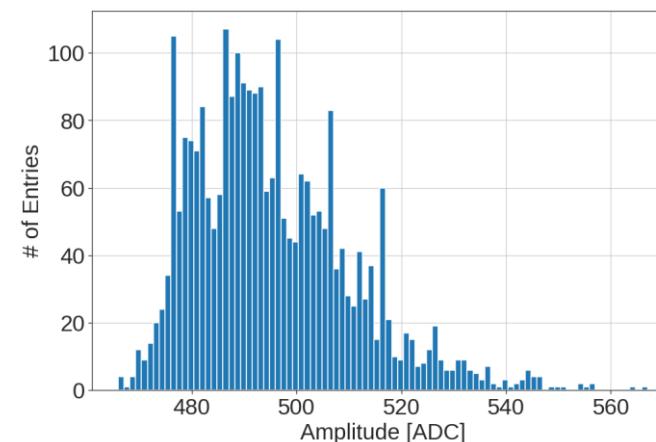


***Extra step for 9mm² SiPM calibration:**

The large C_{det} of the 9mm² SiPM produce an increment of DNL and make it harder to see the photon separation.

The DNL can be mitigated taking data with different pedestal levels using the ASIC to move the pedestals (*Trim_inv* parameter). SPS is clearer after aligning the data.

Without DNL correction:

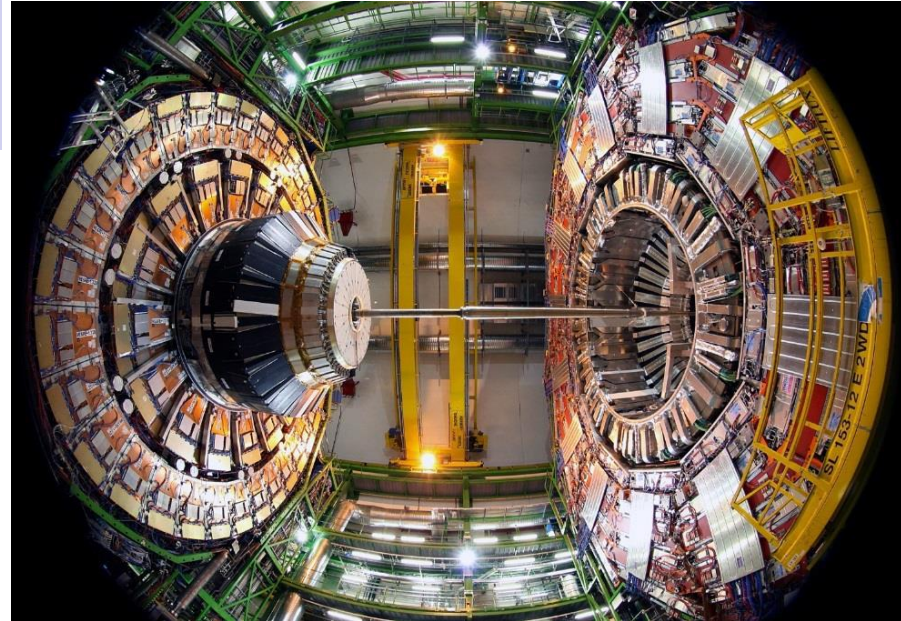


HGCROC for the endcap calorimeter – Phase II

6M of Silicon channels
(+ 240k of SiPM)

Radhard (200 Mrad)
Low Power (15 mW per chn)
Precise timing (25 ps)

Total of 150k ASICs needed
Pre-prod this year
Project started in **2017**



HKROC was developed in
6 months

Same ASIC structure (floorplan)
Same ADC and TDC
Same readout

New preamplifier
New digital processing

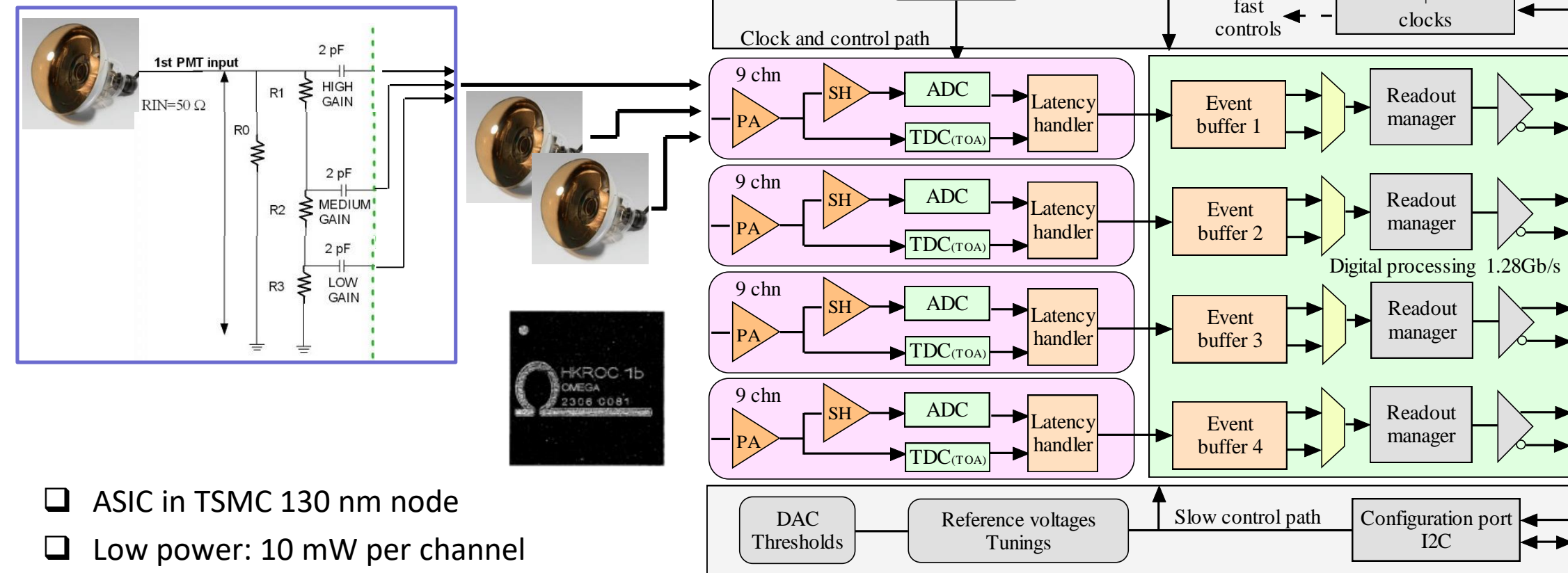
HEP trend => imaging calorimetry

- High number of channels
- Charge and precise timing (<50 ps)
- Low power + System-On-Chip

Based on HGCROC, originally aimed at HK, HKROC-based electronics can provide a versatile, low-power and fully integrated solution for large neutrino experiments

HKROC main features

- HKROC is 36 channels: 12 PMTs with High, Medium and Low gain
 - Or 36 PMTs with one gain

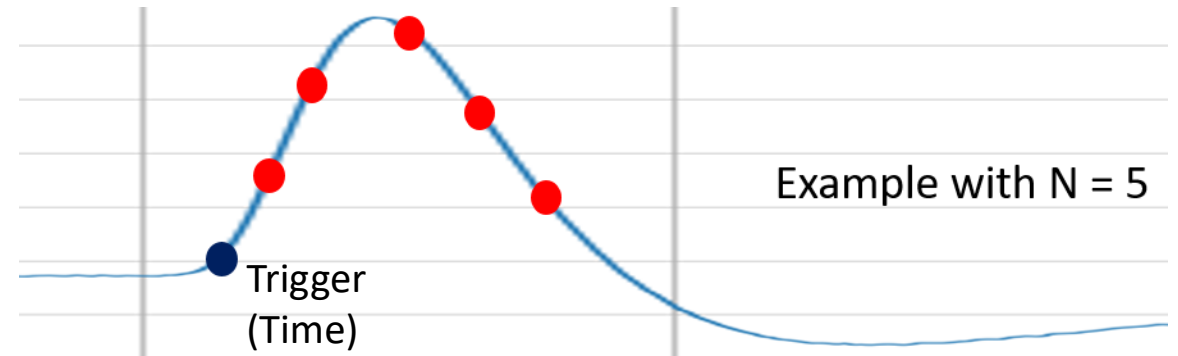


- ASIC in TSMC 130 nm node
- Low power: 10 mW per channel
- Large charge measurement with 3 gains (up to 2500 pC)
- Integrated timing measurements (25 ps binning)
- Readout with high speed links (1,28 Gb/s)
- HKROC is a waveform digitizer with auto-trigger**



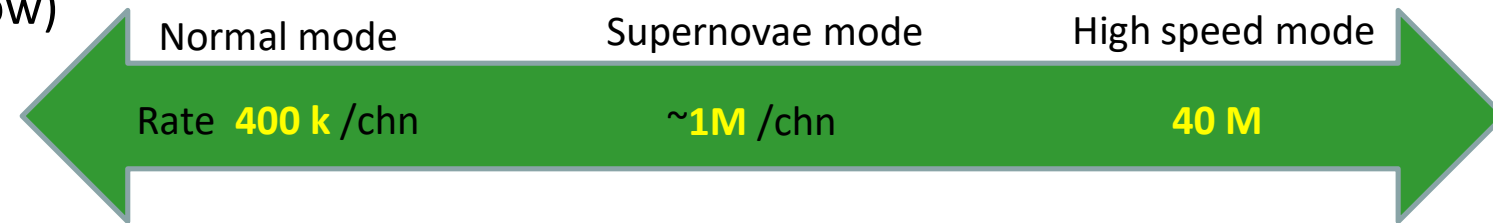
- HKROC is waveform digitizer working @ 40 MHz

- Number of charge sampling points from 1 to 7
- Fast channel for precise timing (25 ps binning)
- Charge reconstruction algorithm in FPGA
 - 5% resources of a modern XILINX FPGA



- When using 3 gains / PMT (high, medium, low)

- Hit rate capability up to 400 kHz / PMT
- Increased up to 1 MHz by focusing on high gain
 - Dynamic selectable by the user
- Average values only limited by readout speed



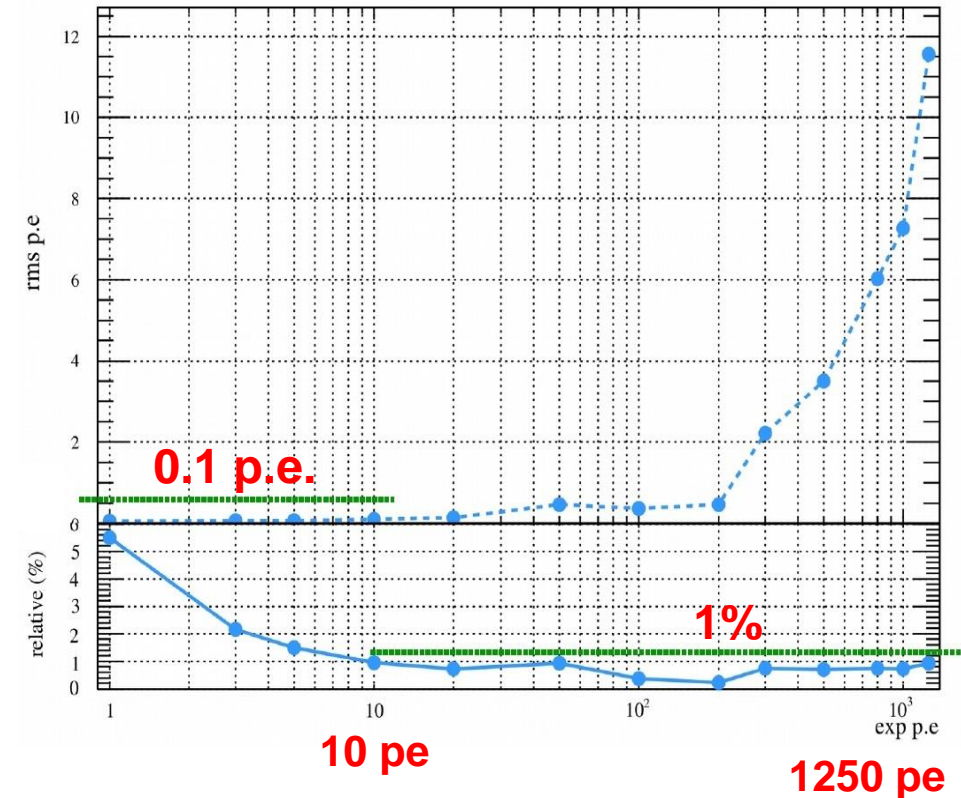
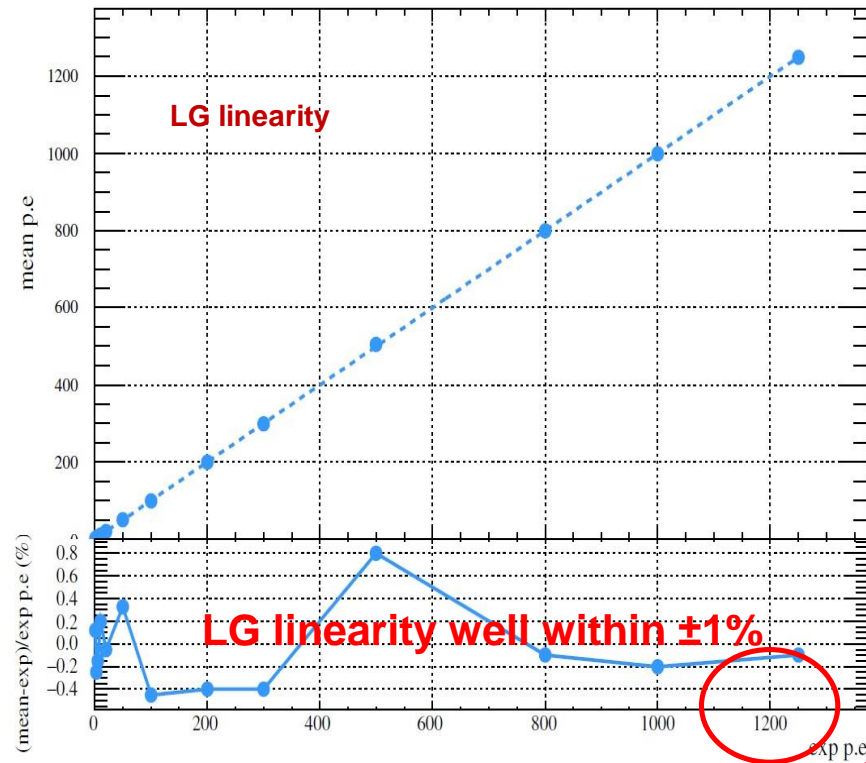
HKROC can accept consecutive events (separated by ~30 ns)

Internal HKROC memory writing is without dead time

Readout speed is only limited by serial link bandwidth (average values above)

The **whole** acquisition **chain** is tested:

The signal is **amplified, auto-triggered** and **converted** by the internal **ADC**.



HG, MG and LG tested!!

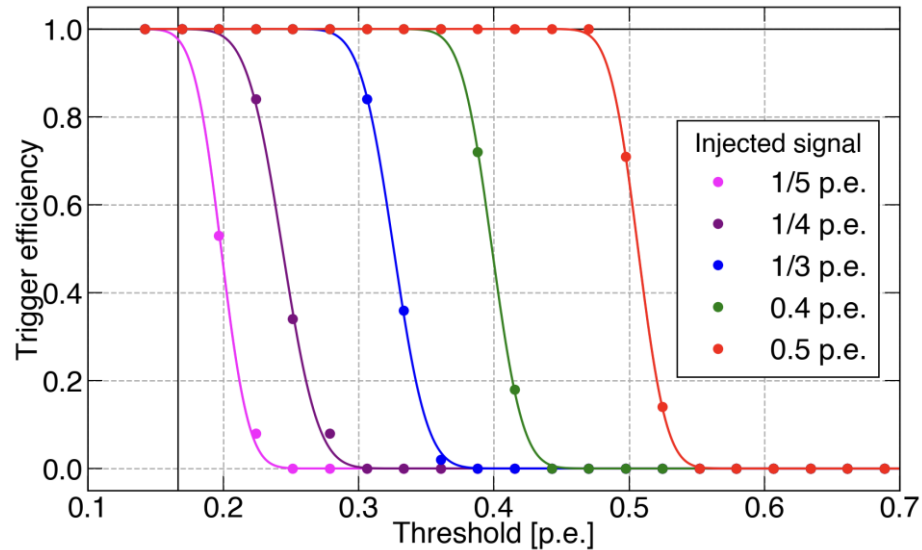
Charge linearity $< \pm 1\%$ from 1 to **1250 p.e. (2500 pC)**

Charge resolution :

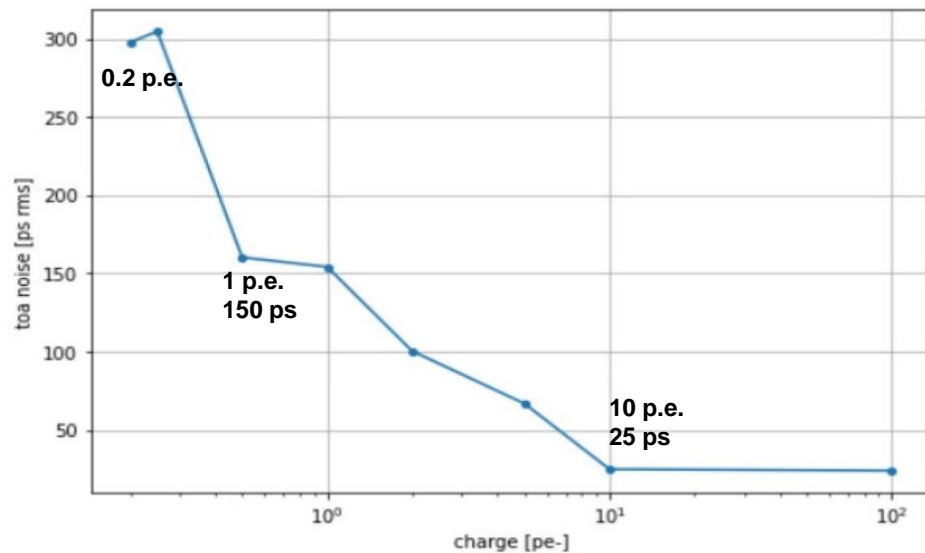
$< 0.1 \text{ p.e. (200 fC)}$ at $\leq 10 \text{ p.e.}$

$< 1\%$ otherwise

The HyperK specifications require the trigger **threshold** to be set at **1/6 p.e (330 fC)**



- **Hit efficiency : 90 % for 1/5 p.e events (400fC)**
~100 % if $\geq 1/4$ p.e
- Extracted **threshold** value corresponding at **1/6 p.e**
- **Very low noise : < 1 Hz (0 noise hit in 10s @ 1/6 of p.e.)**



TDC characterization with **1/6 p.e. threshold**

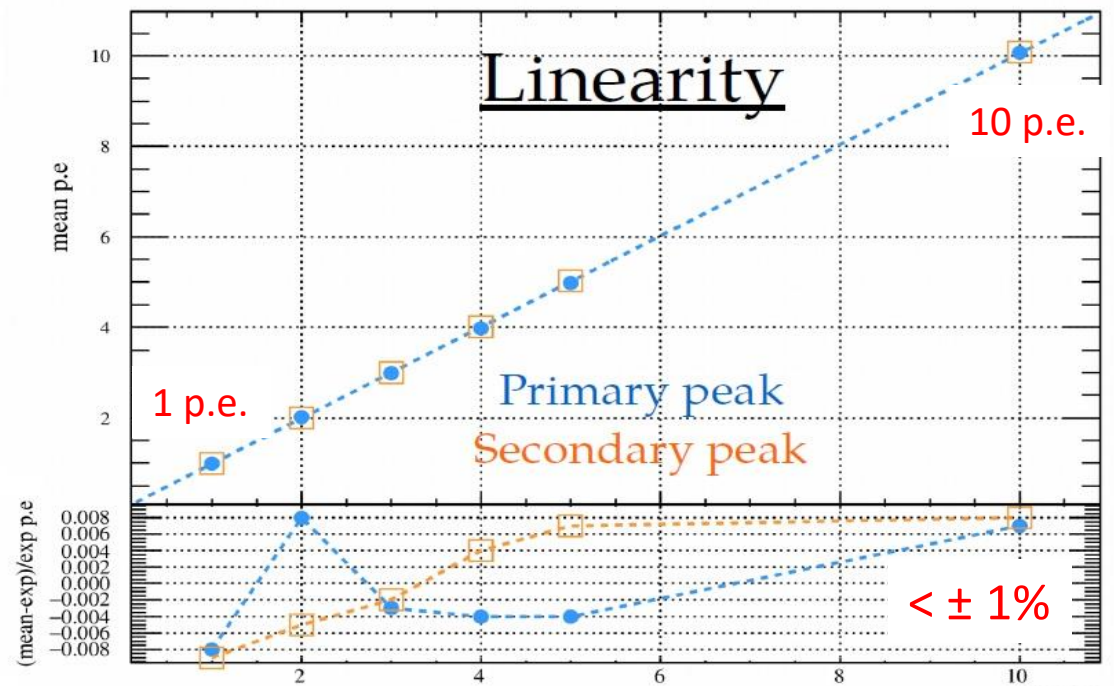
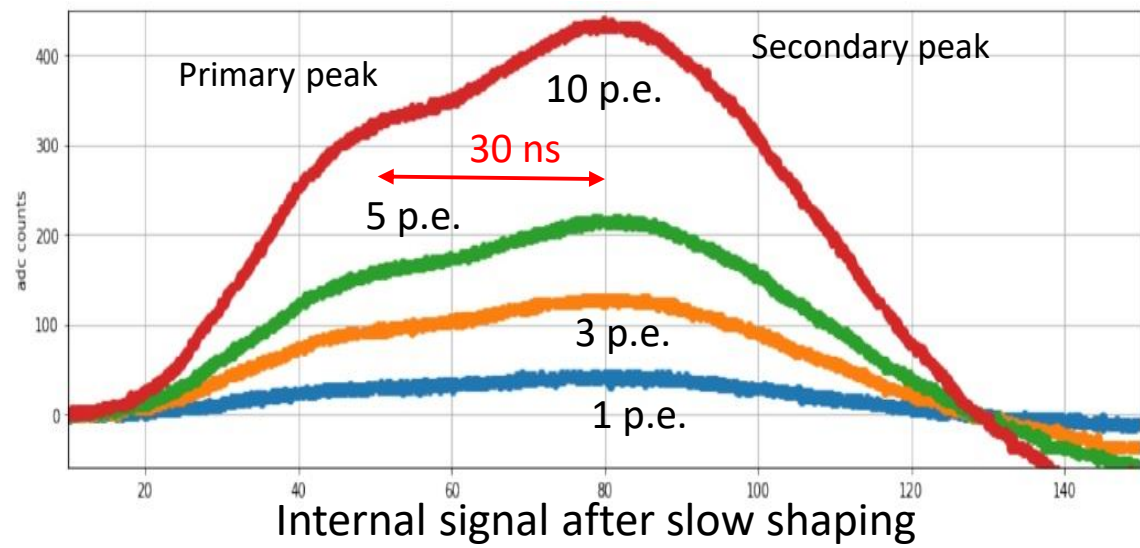
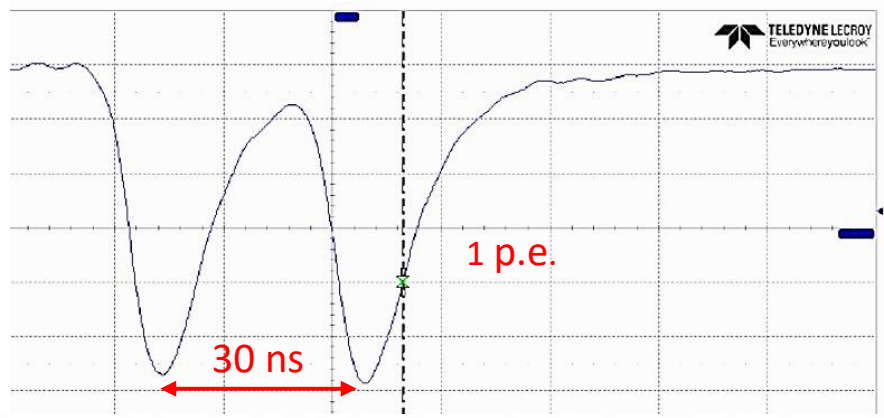
TDC resolution :

150 ps rms @ 1 p.e [300 ps required]

≤ 25 ps rms @ 10 p.e [200 ps required]

Main experimental results with HKROC0 - Pile-up

- Measurement with 2 events separated by ~ 30 ns (full chain: analog, digital and reconstruction)
- Signals auto-triggered (internal programmable threshold)



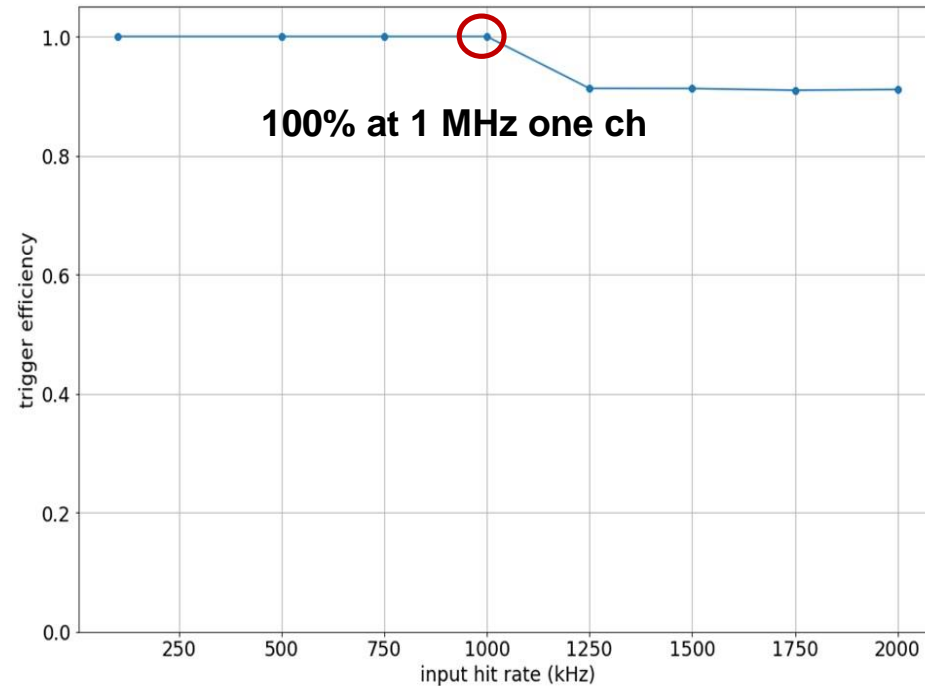
Charge reconstruction algorithm of the two peaks

Good linearity of reconstructed pile-up events

We can reconstruct both peaks properly !

FAST hit rate (~ 1MHz) required for close Supernova signals (~ 1 p.e.)

Normal mode:



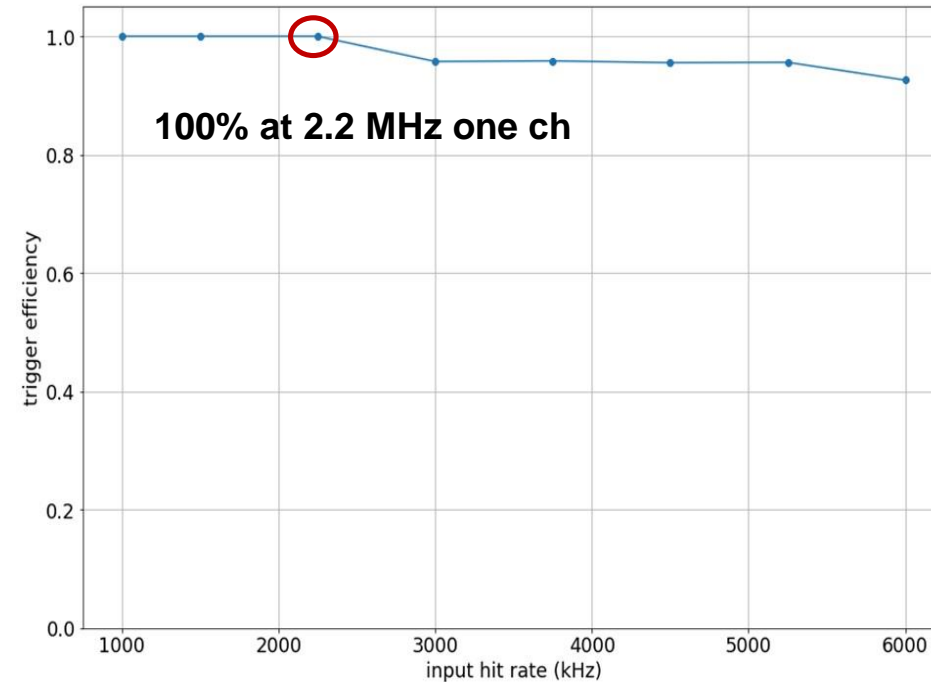
100% at 1 MHz one ch

1 PMT channel →

3 HKROC channels tested in Normal Mode:

100% Trigger efficiency up to **415 kHz 3 chs**

Super Nova mode



100% at 2.2 MHz one ch

1 PMT channel →

3 HKROC channels tested in SuperNova Mode:

100% Trigger efficiency up to **950 kHz 3 chs**

The HKROC saturation naturally appears when the chip internal memory is full. The chip has one independent memory for each read-out link at 1.28 Gb/s, which gather 3 PMTs.

Trigger time distribution for events having charge ≤ 1.5 p.e : FWHM of 2.6 ns

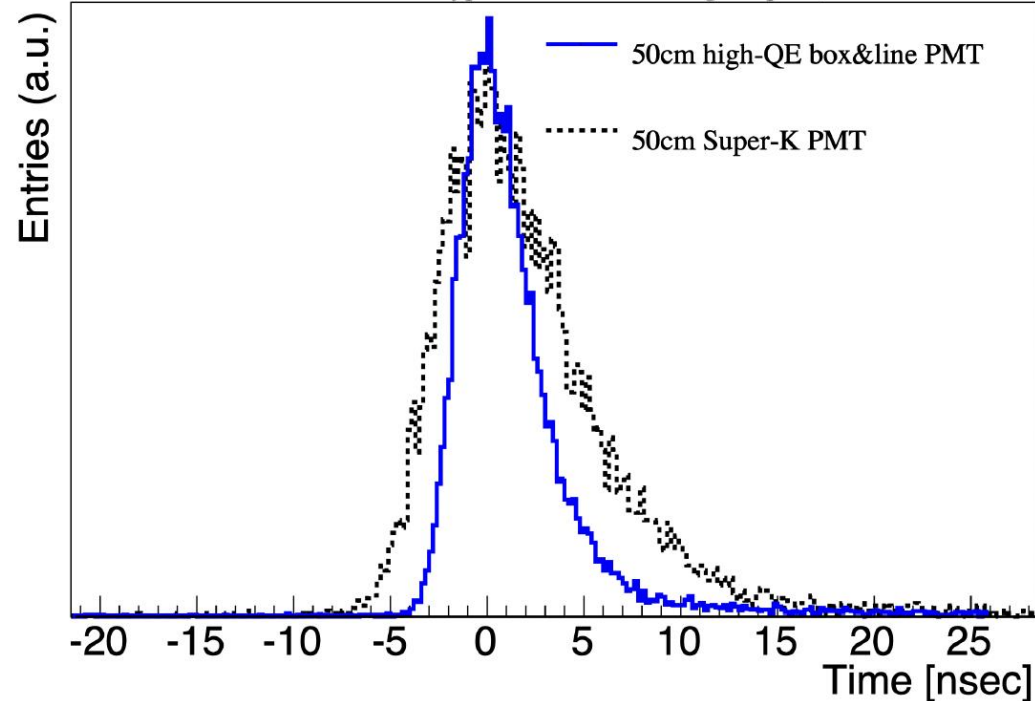
- Excellent agreement with the 2.8 ns found for the PMT only
- Digitizer does not degrade the PMT time resolution !

Time resolution

(TTS for 1 p.e.)

≈ 6.7 ns ($\sigma \approx 3.4$ ns) \rightarrow ≈ 2.6 ns ($\sigma \approx 1.3$ ns)

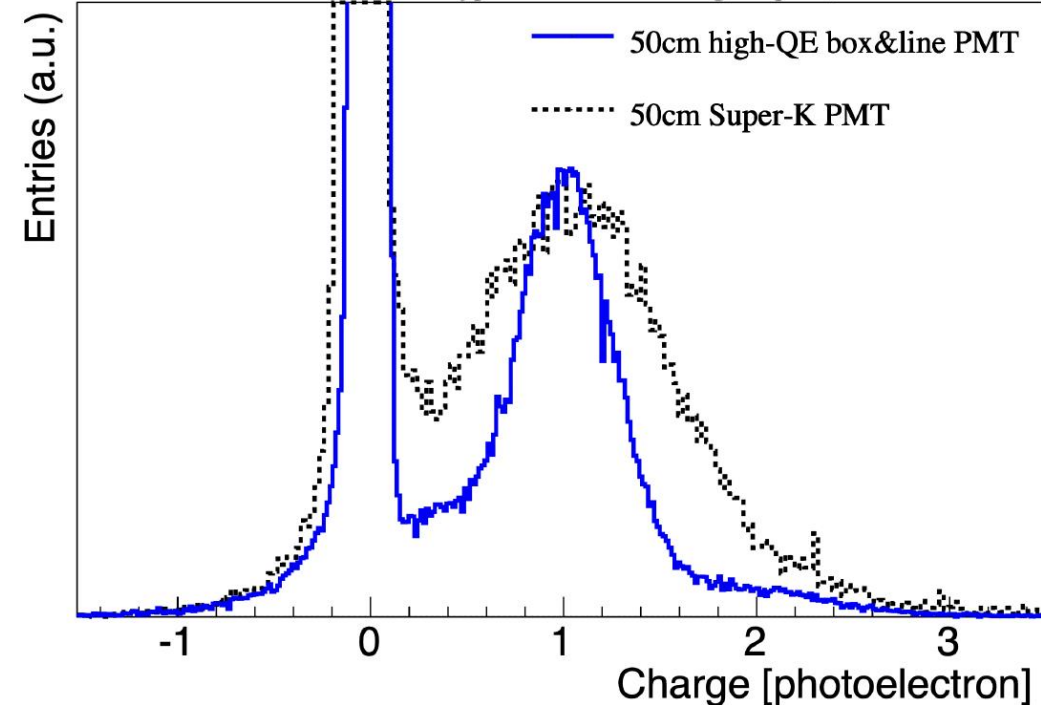
Hyper-Kamiokande Design Report [[arXiv:1805.04163v2](https://arxiv.org/abs/1805.04163v2)]



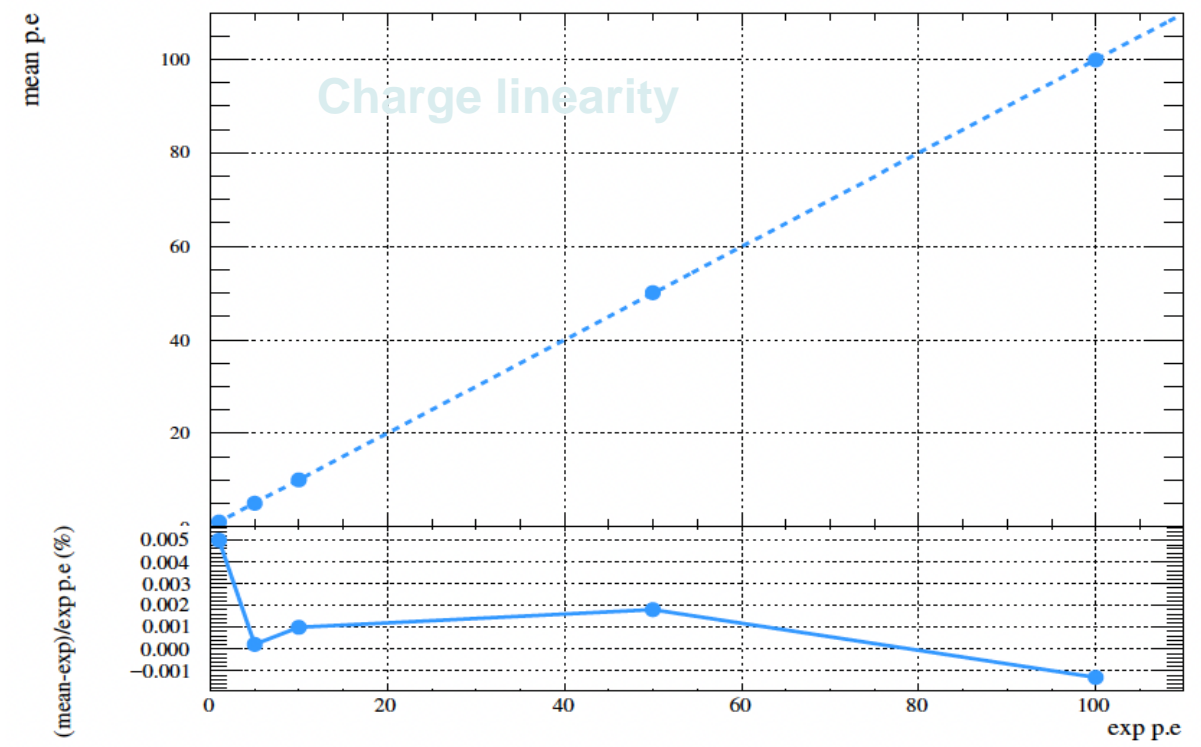
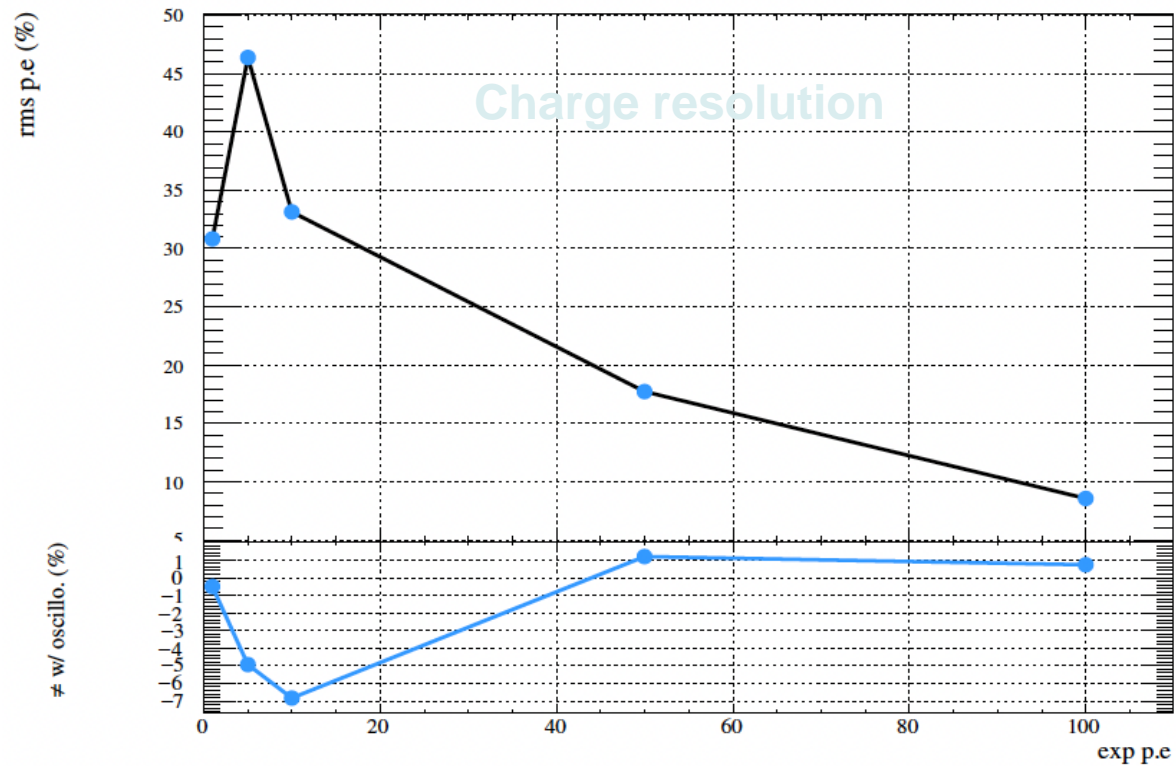
Charge resolution

$\approx 60\%$ \rightarrow $\approx 31\%$

Hyper-Kamiokande Design Report [[arXiv:1805.04163v2](https://arxiv.org/abs/1805.04163v2)]

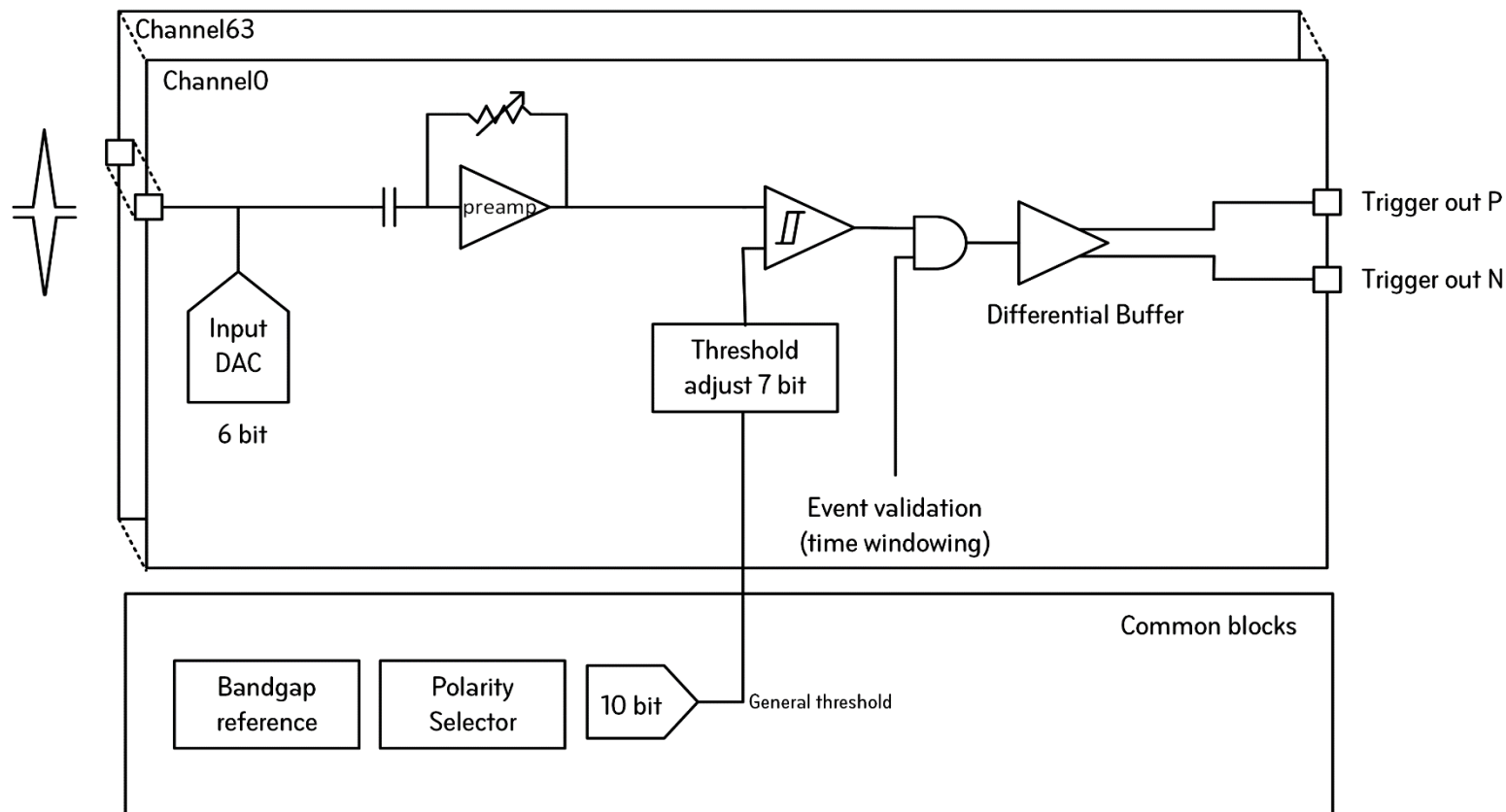


- Charge linearity and resolution
 - Similar with PMT as with pulse generator



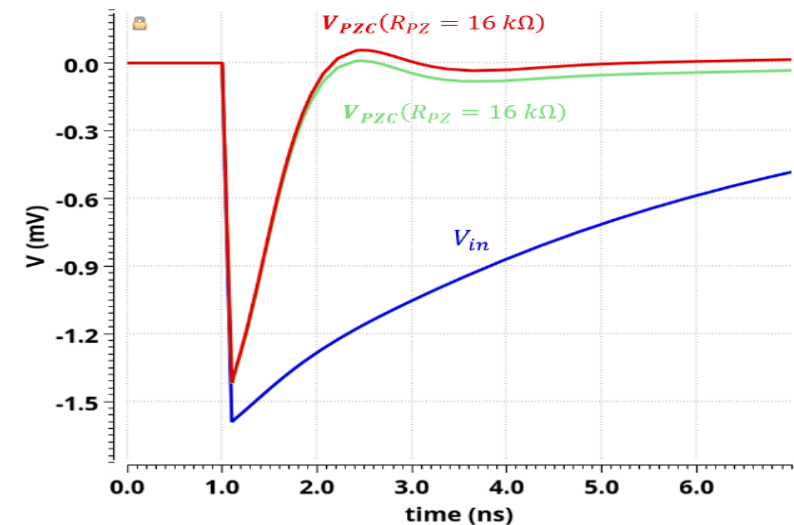
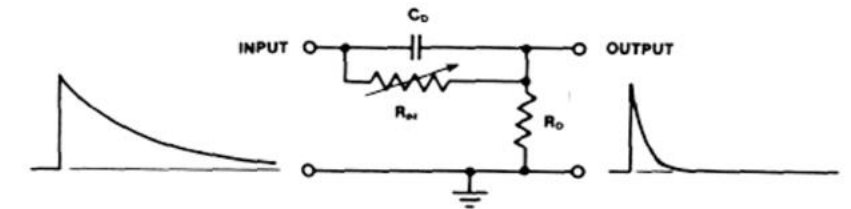
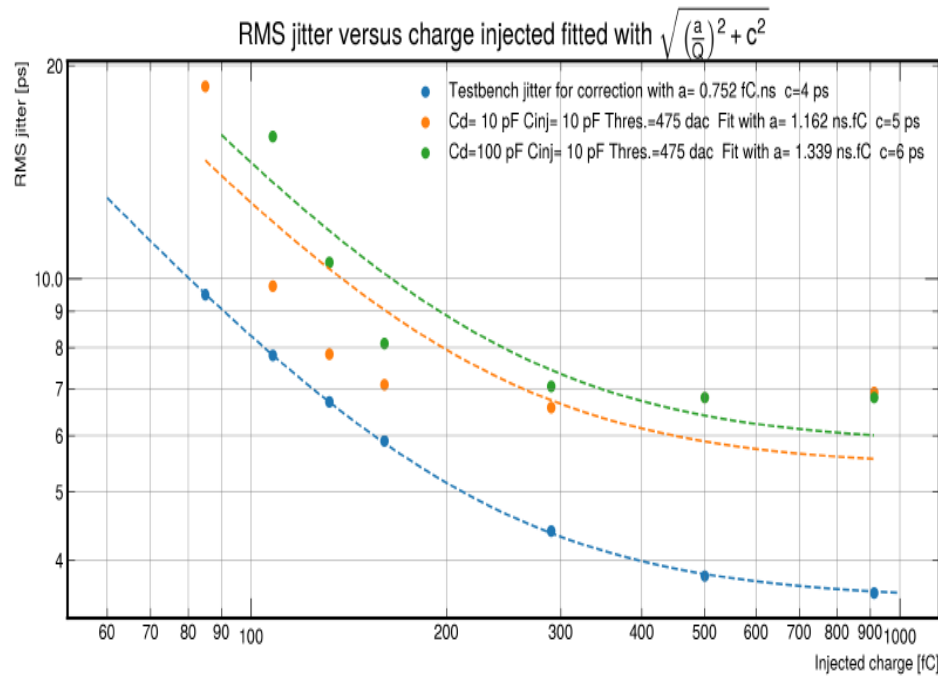
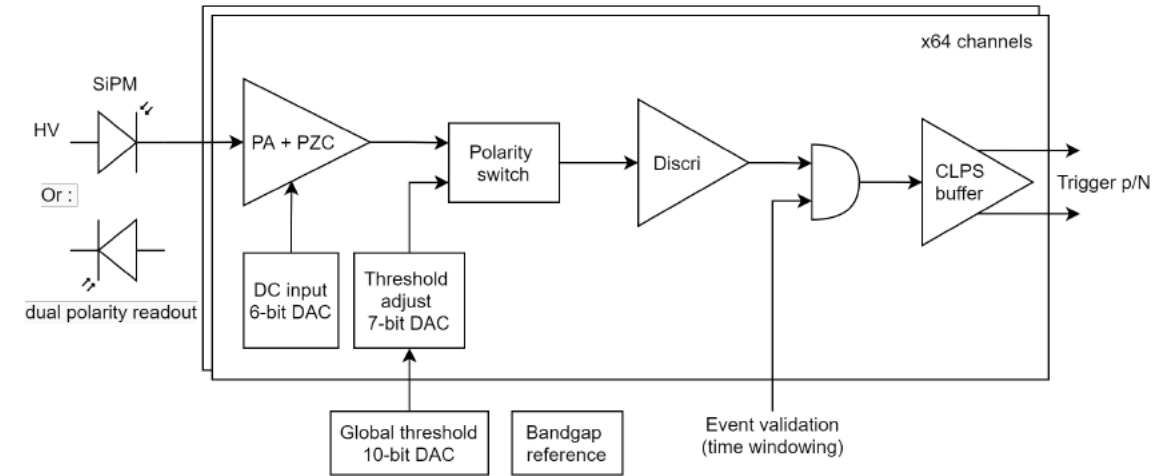
Introducing LIROC : SiPM read-out for Lidar

- Evolution of PETIROC (used in CMS RPCs)
- Can connect directly to CERN picoTDC



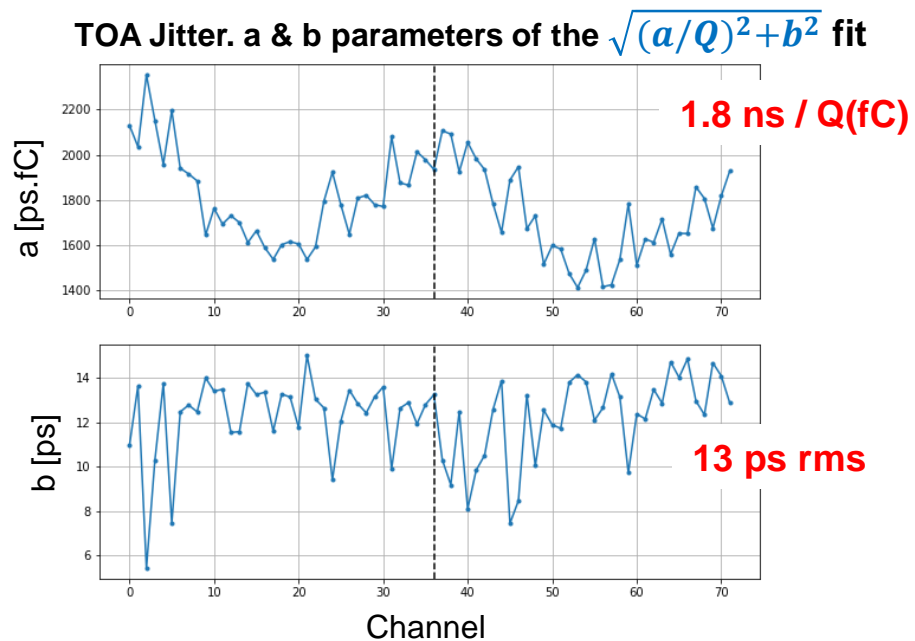
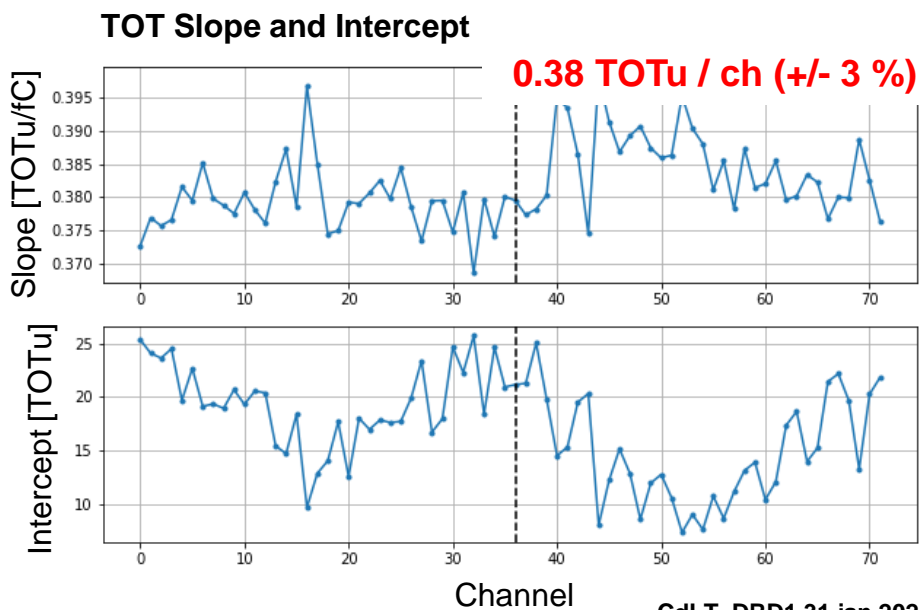
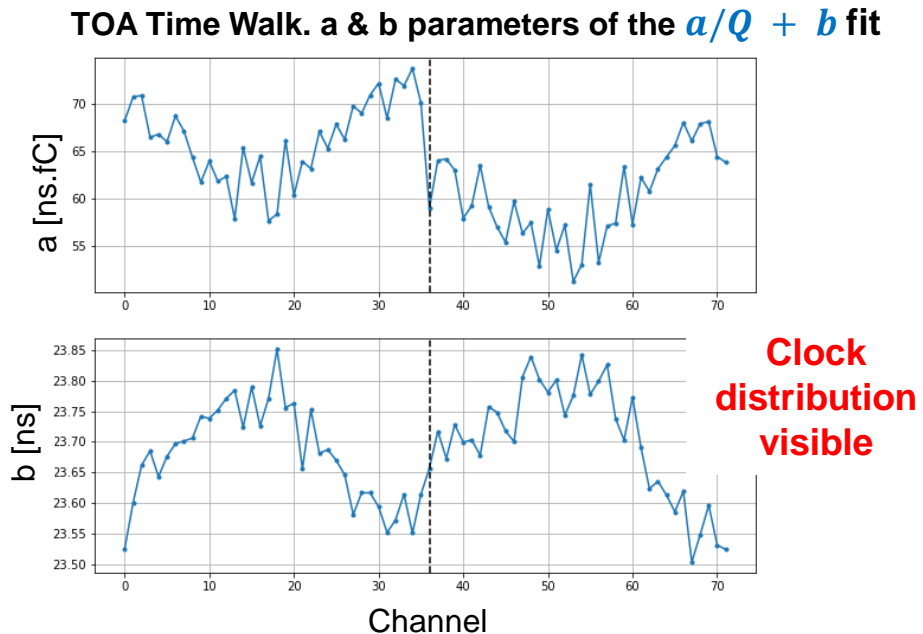
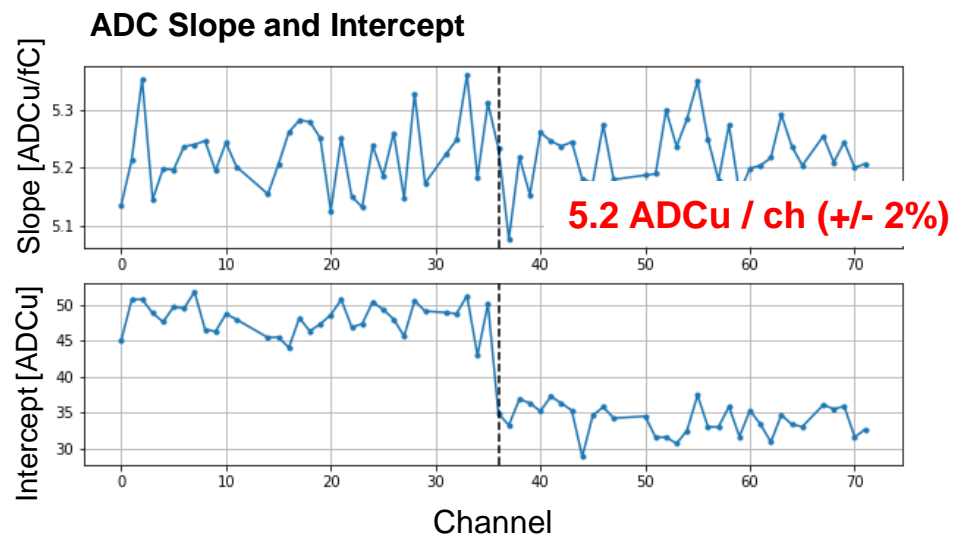
Collaborative design between Weeroc & Omega laboratory that have received Funding from ATTRACT EU H2020 Research & Innovation Program

- LIDAR readout : short double pulse separation
 - 64 channels high speed PA + discri
 - Trigger on 1/3 photoelectron
 - Pole-zero cancellation for 3 ns double pulse separation
 - CLPS discriminator output : couples to picoTDC
 - 3 mW/ch CMOS 130nm



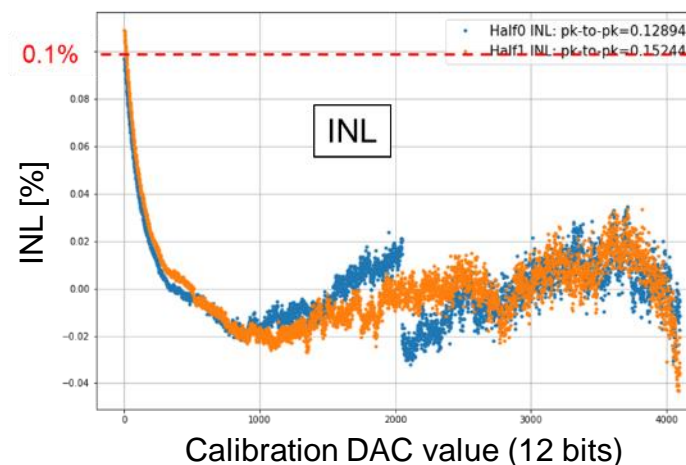
- New generation chips include ADCs and TDCs
- Large dynamic range (15bits)
- Time measurements down to 20 ps
- Low power < 10 mW/ch
- Auto-trigger and streamed data flow
- Radiation tolerant to 100s of Mrad and SEU immune

- H2GCROC, HKROC, LIROC fabricated, used, available !



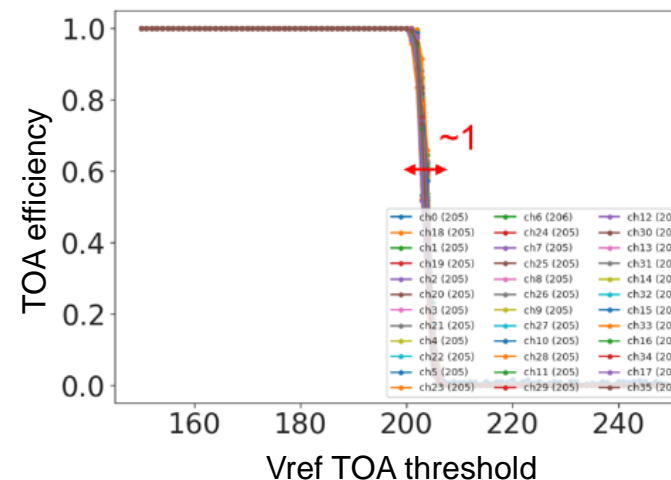
- **12 bits calibration DAC**
 - ~ 2-3 mV offset due to leakage current (1 – 1.5 fC)
 - < 0.1 % linearity, temperature sensitivity: 60 ppm/K, stable after 350 Mrad
- **Four 10-bit DACs** to set pedestals, TOA & TOT thresholds + **3 channel-wise 6-bit DACs** to reduce dispersion per channel
 - Pedestals: ~ 1 ADC counts dispersion after trimming
 - TOA & TOT thresholds: 1-2 DAC counts after trimming
- 8-bit input DAC to compensate for the **leakage current up to 50 μ A**
 - Additional noise as expected from simulation

Calibration DAC:

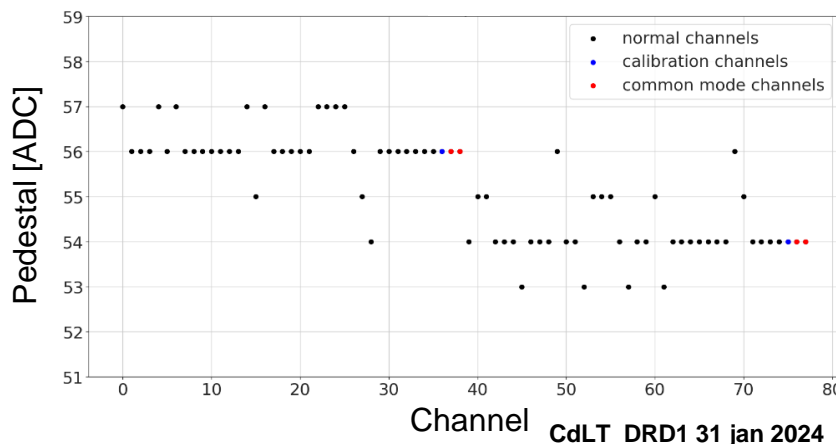


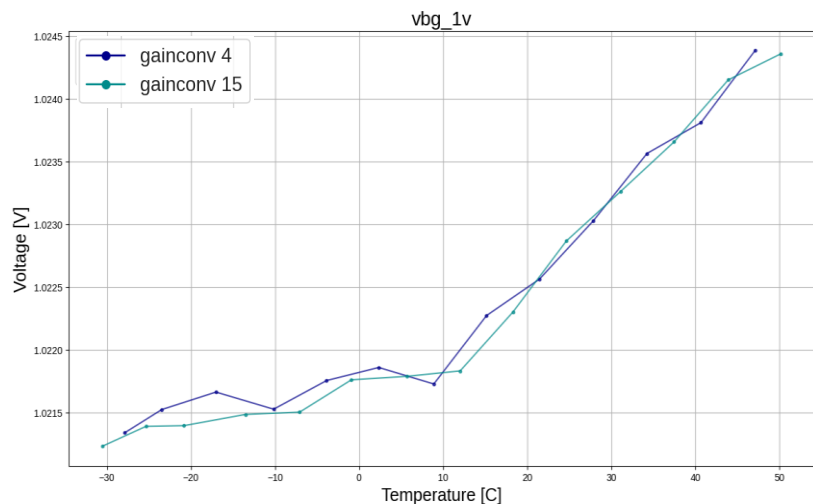
Trimmed TOA thresholds:

10-bit global threshold scan



Trimmed pedestals:





Bandgap (Two slopes):

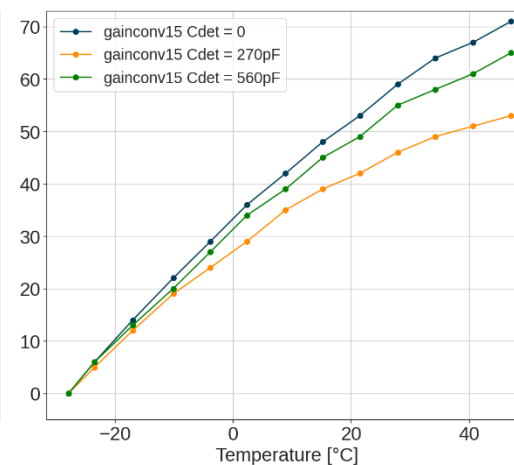
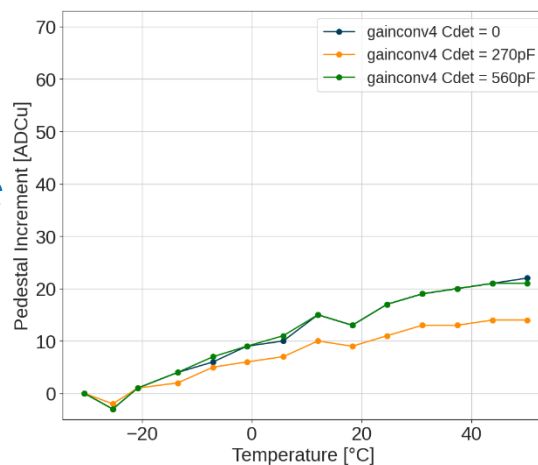
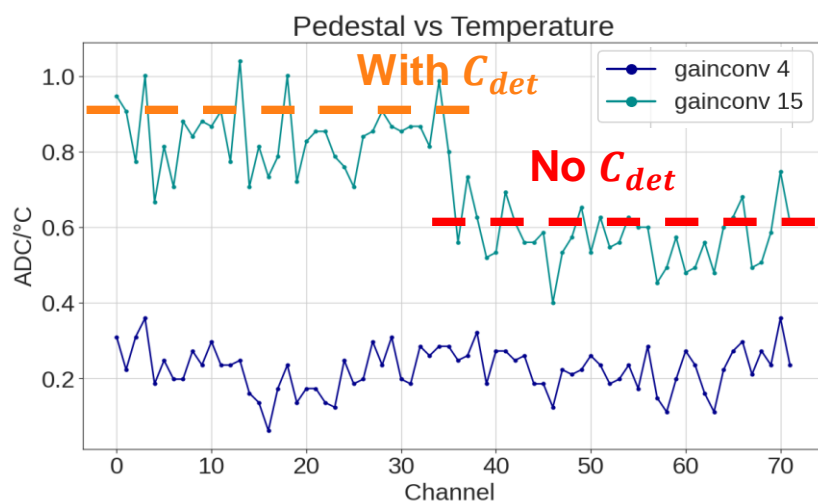
From -30°C to 10°C: **12.5 $\mu\text{V} / ^\circ\text{C}$**

From 10°C to 50°C: **65 $\mu\text{V} / ^\circ\text{C}$**

Pedestals:

Physics mode: **+ 0.3 $\text{ADCu} / ^\circ\text{C}$**

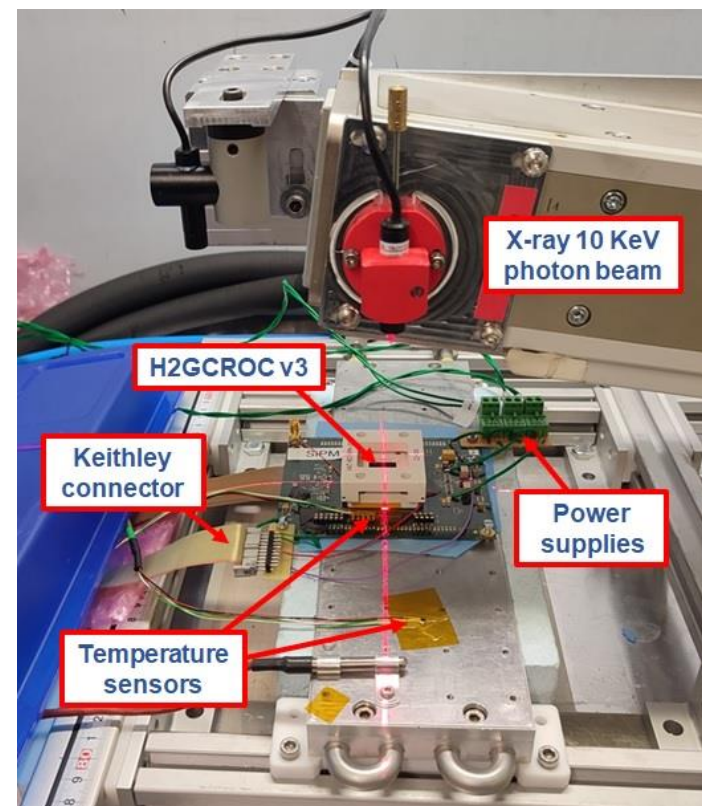
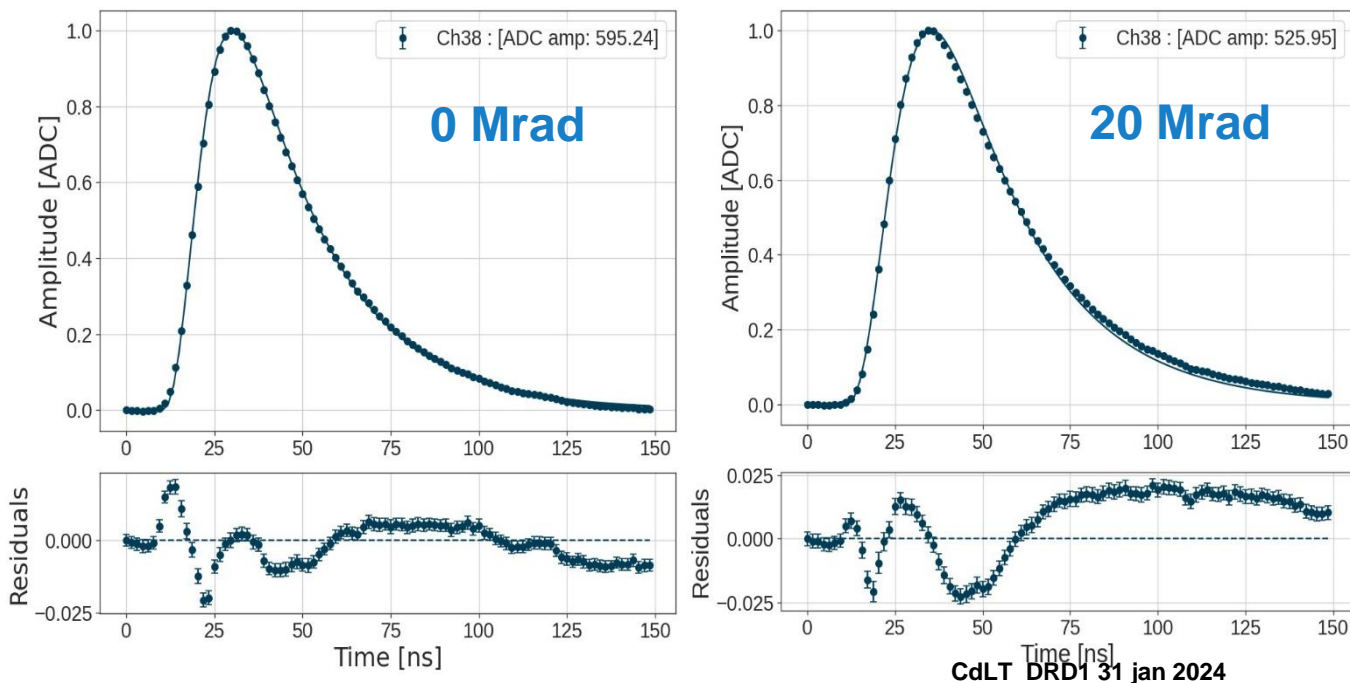
Calibration mode: **+ 0.9 $\text{ADCu} / ^\circ\text{C}$**



*Noise : almost flat

- Power consumption, ADC & TDC performance, noise, links stability, etc. tested during irradiation
- **TID irradiation tests in both ASIC versions.**
- **Heavy ion and Proton irradiation in the Si version of the ASIC**
 - Increase on triplicated parts for HGCROC3b

Stability of ADC measurements after 20Mrad:



- **H2GCROCv3** has proven to be **radiation tolerant up to 20 Mrad** at room and -5°C with good ADC, TDC and PLL measurements.

- Only tested in **HGCROC Si version** for both Protons and Heavy ions.
- Test the radiation damage induced by a single particle to electronic devices and non-cumulative. It can cause a failure at any moment since the beginning of operation.
- **Three types:**
 - Single Event Upset (**SEU**): bit flip (0 -> 1 or 1 -> 0).
 - Single Event Transient (**SET**): bit shift.
 - Single Event Latchup (**SEL**): permanent damage.

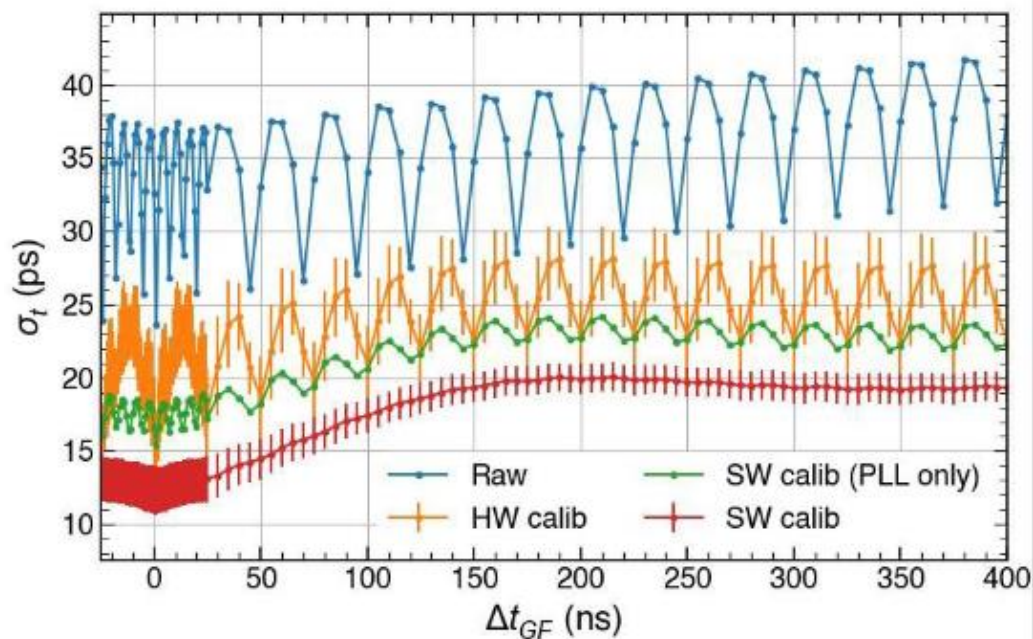
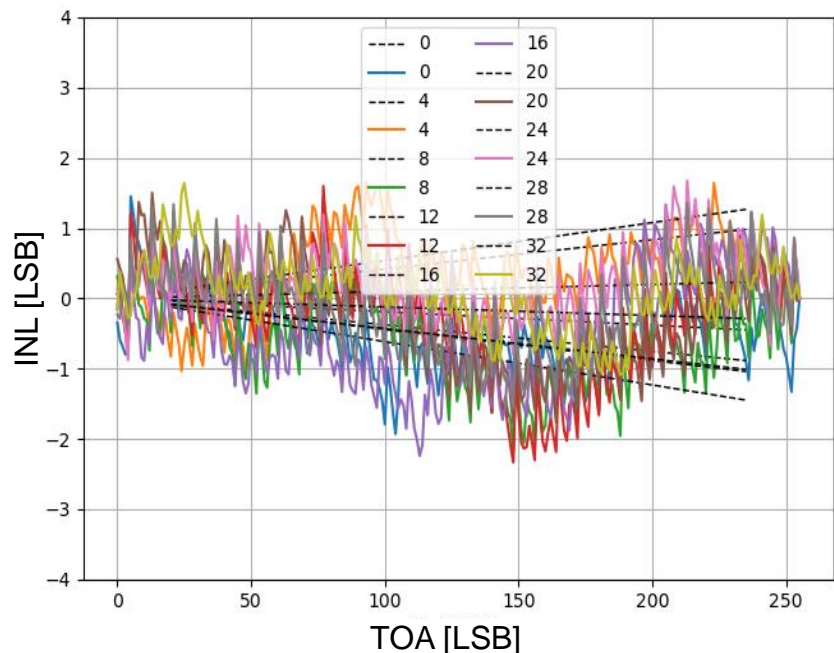
# errors	Counters	Trigger	CRC	Memory	Short SET	Long SET
Heavy ions [12]	0	1	2	3	24	18
Protons [13]	< 1	38	30	127	85	190

1 link loss / 2.5 years (for each chip on average)

- Very few errors in the not triplicated parts of Trigger and CRC.
- Very few errors in the memory, always detected by the hamming.
- Many errors in the not triplicated part (**PLL**).
 - **Increase in the triplication of the new version of PLL (Tested in EICROC).**

**Analysis by Elena Vernazza*

- I2C parameters to tune master and channel-wise DLLs
- Parameters can be optimized thank to the on-chip asynchronous clock generator (ACG) by minimizing the INL.



TDC calibration in 2 steps:

- Master DLL tuning
- Individual channel DLL tuning

After Calibration: INL < ± 2 LSBs, < 16 ps resolution

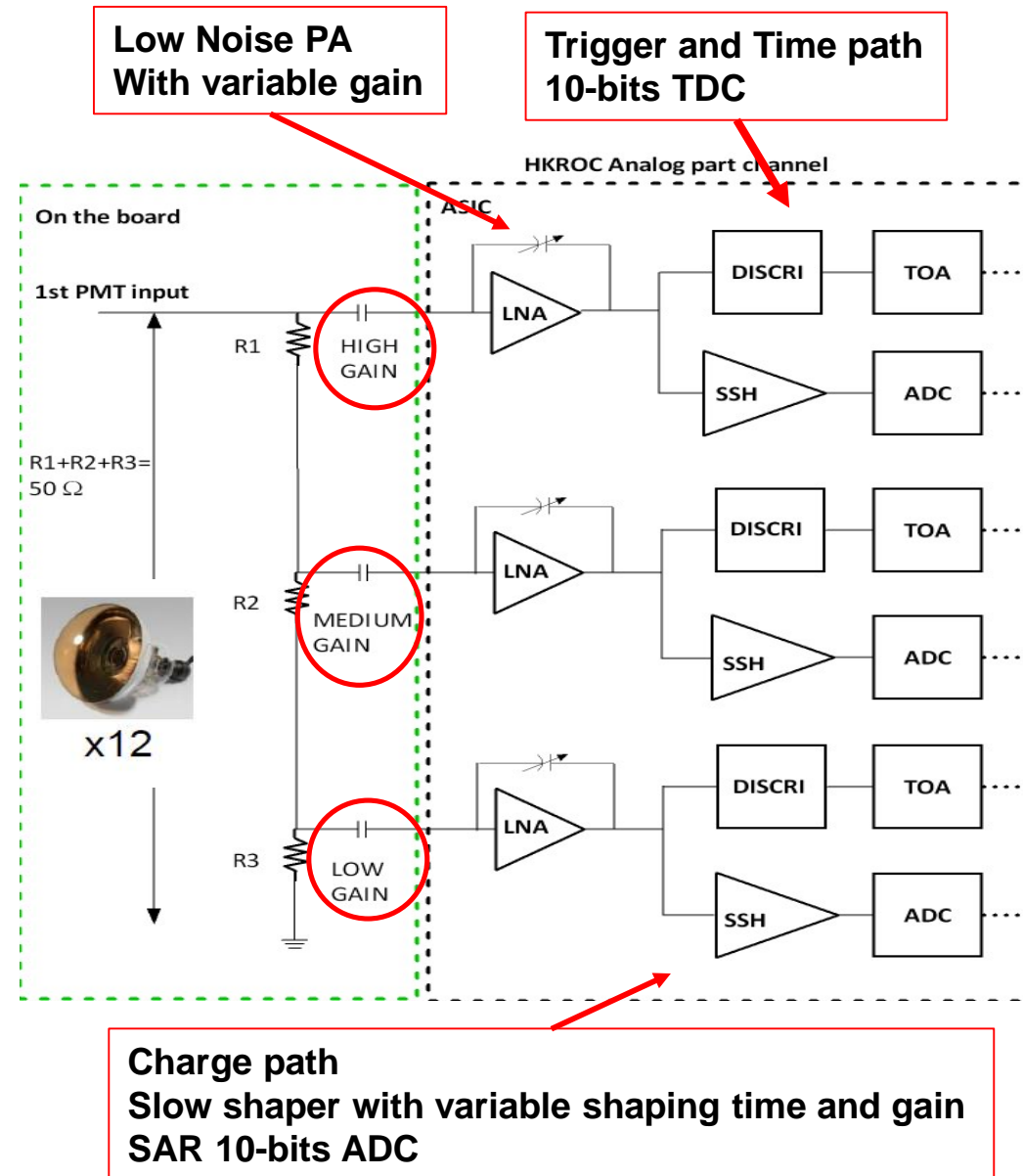
Resolution of 2 uncorrelated chips given by resolution at large T-delays

- Before calibration (blue): ~ 40 ps resolution
- After calibration (orange): < 30 ps resolution
- (After software correction (cancel FPGA clock jitter): **< 20 ps resolution**)

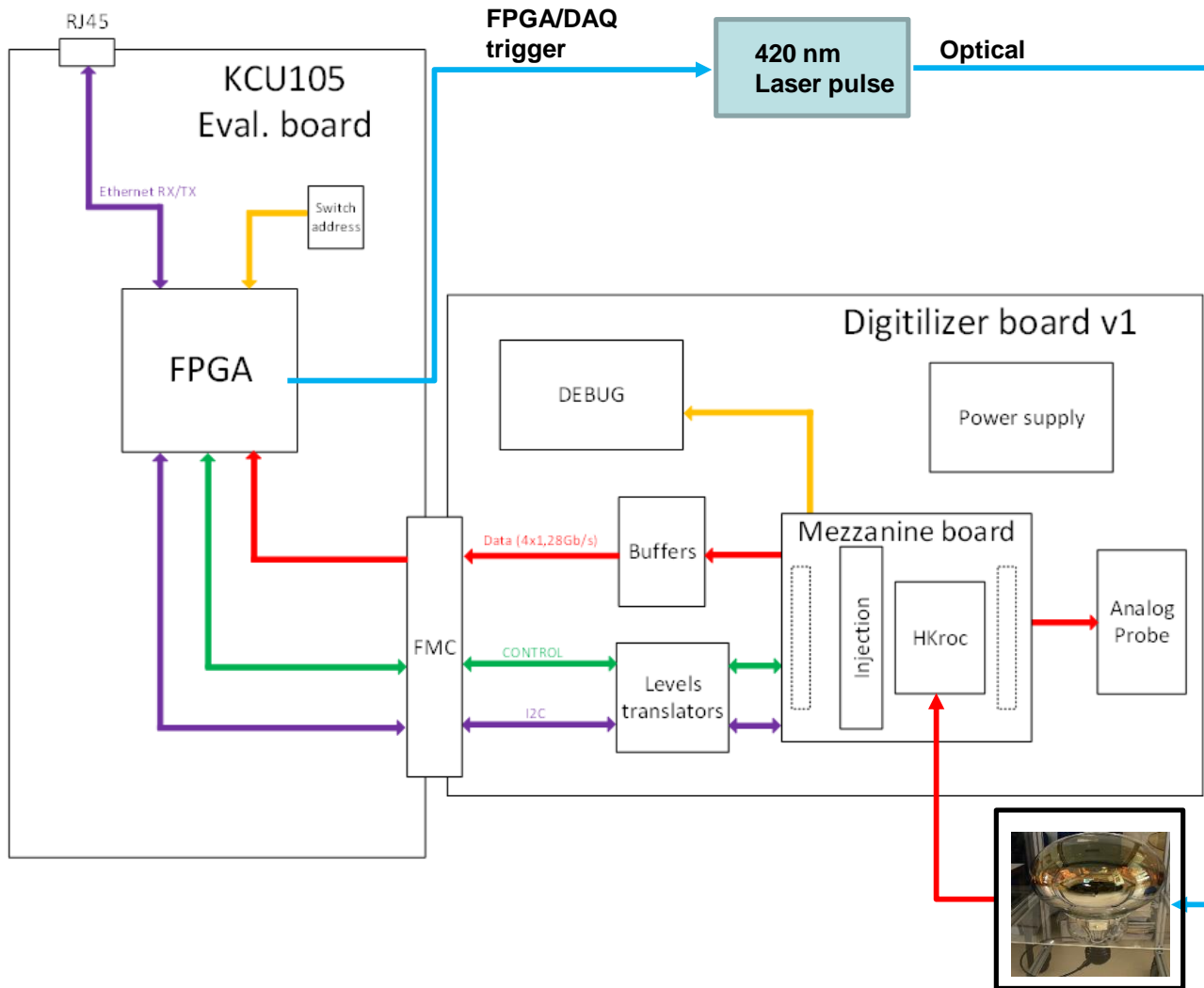
Min requirements	
Discriminator threshold	1/6 p.e. (0.33 pC)
Charge linearity	1% for 1 p.e. to 1250 p.e. (2 pC to 2500 pC)
Charge resolution	0.1 p.e. for < 10 p.e. (0.2 pC for $Q < 20$ pC) Better than 1% for >10 p.e. (1% for 20 pc)
Maximum hit rate	1 MHz/ch For close Supernova
Timing resolution	300 ps for 1 p.e.(2 pc) 200 ps for > 6 p.e. (12 pC)

To extend the charge dynamic range:

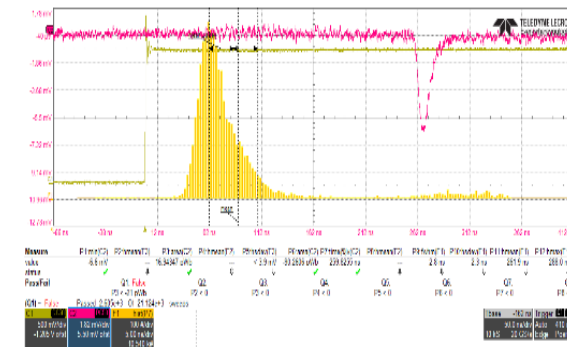
1 PMT channel connected
to **3 HKROC channels**



Connected Hamamatsu R12680 PMT to HKROC illuminated by a PILAS 402 nm laser diode



- PMT HV set to have the 1 p.e peak amplitude at -6 mV
- Charge calibrated
- TTS : FWHM= 2.8 ns, $\sigma = 1.2$ ns

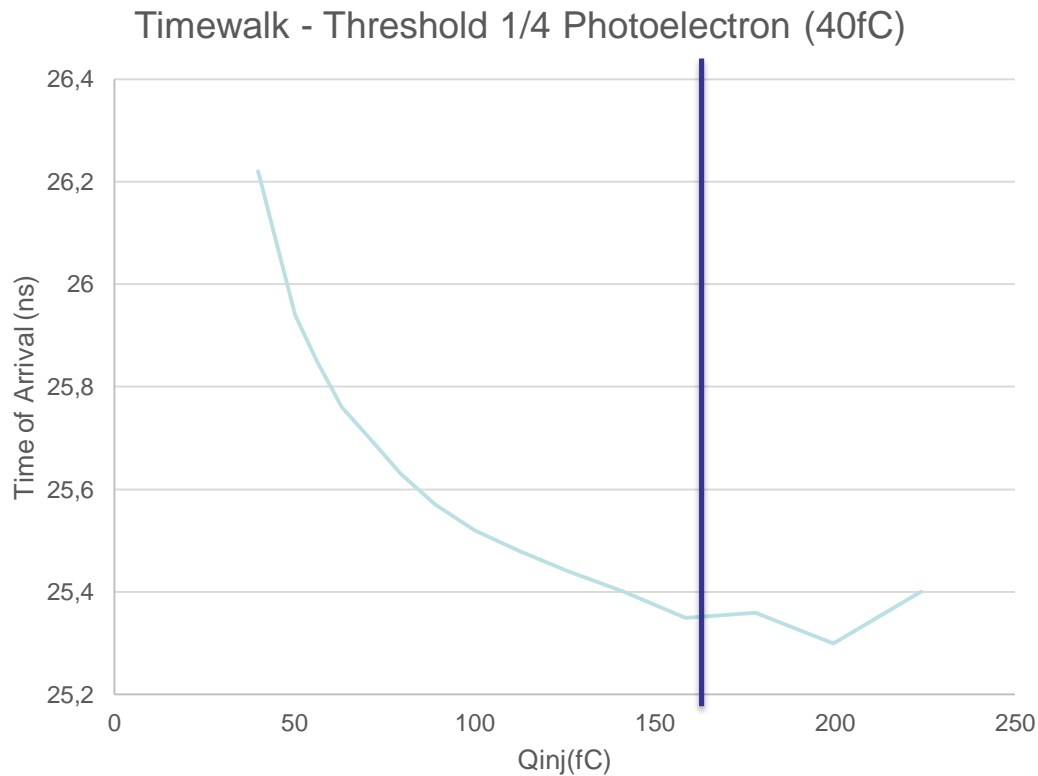


Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive or Negative (selectable ASIC-wise)
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	Better than 20 ps FWHM on single photo-electron Better than 5ns double-peak separation on single photo-electron
Dynamic Range	Over 100MHz photon counting rate
Packaging & Dimension	BGA 20x20 mm ² Flip-Chip low inductance packaging technology
Power Consumption	210mW – Supply voltage : 1.2 V
Inputs	64 analogue inputs with independent SiPM HV adjustments
Outputs	64 low-common-mode LVDS triggers (CLPS) – compatible with CERN picoTDC and all LVDS FPGA I/Os
Internal Programmable Features (I ² C)	64 HV adjustment for SiPM (64 x 6 bit), trigger threshold programming (10bits), 64 x 7 bit channel-wise threshold adjustment, ASIC-wise polarity selector, preamp pole-zero cancellation adjustment, individual trigger masking and cell powering.

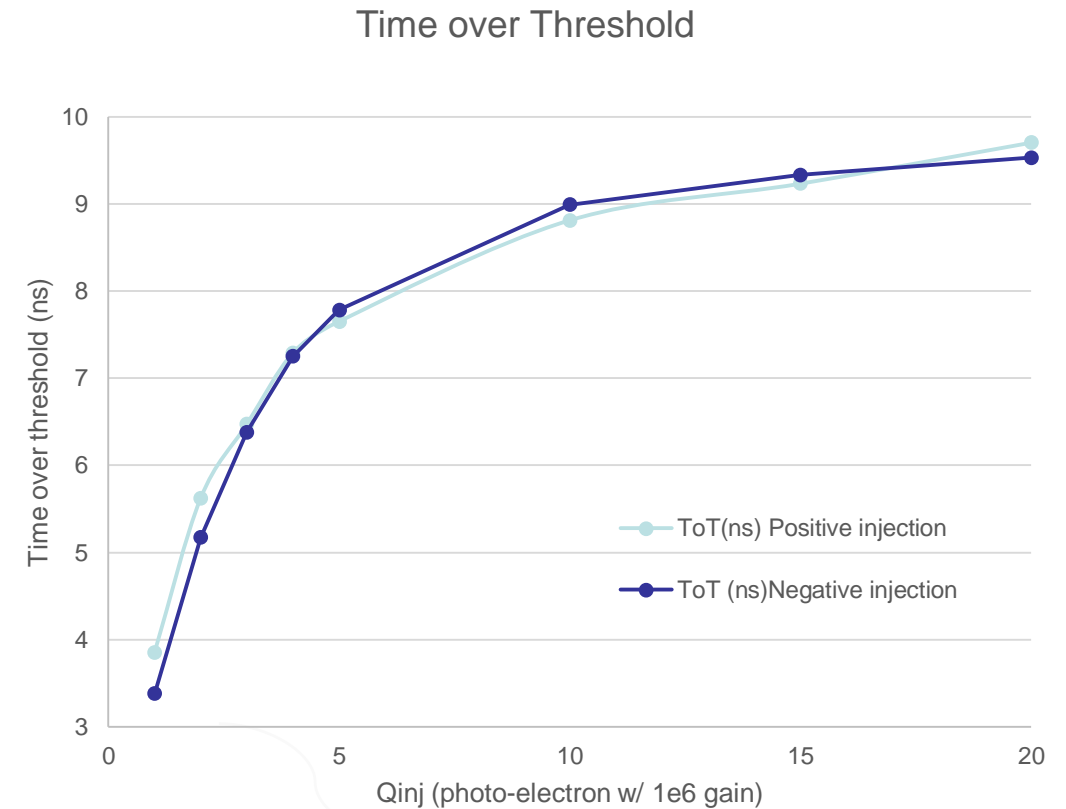
Technology : TSMC 130nm MS-RF
« CERN qualified » for irradiation

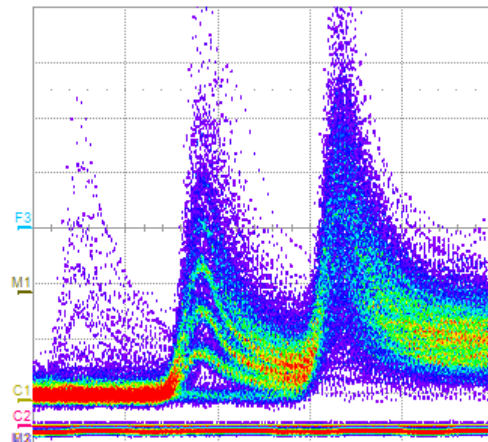
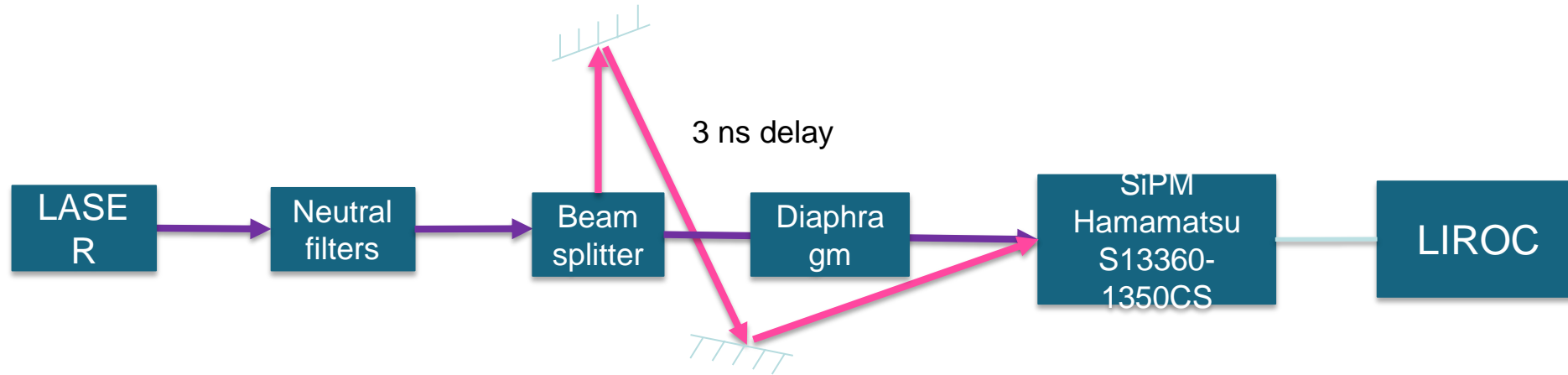


- ToT used to correct timewalk
- Trade-off between double peak separation (see consecutive photons) and time over threshold (tuneable).
- Optimized for double-peak separation in that measurement (3ns separation measured)

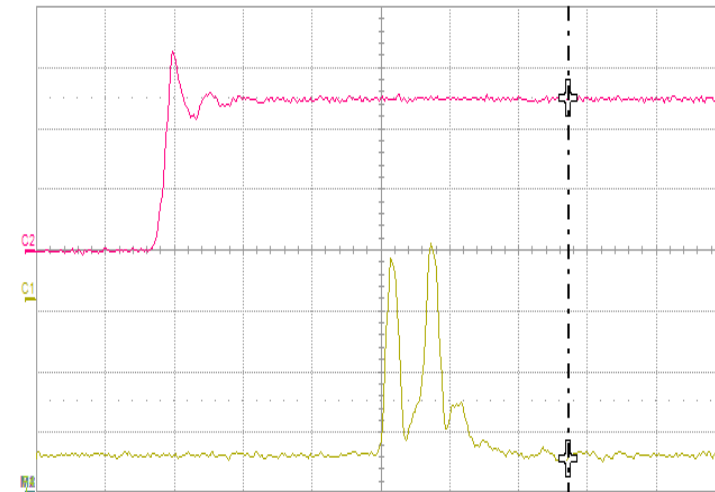
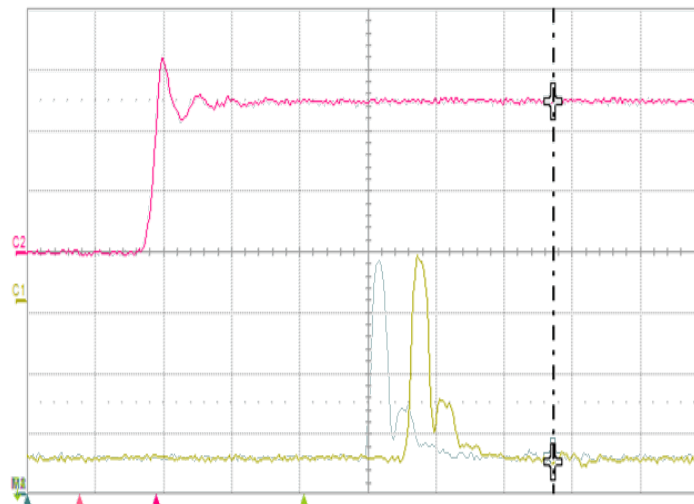


1 photoelectron - Gain 10^6





Direct to oscilloscope, 3 ns interval



50 mV/div
5 ns /div

Conclusion : 3 ns double pulse well separated

