

SRS

Scalable Readout System

Hans Muller

SRS: from RD51 past to DRD1 future

~ 50 x WG5 meetings RD51

1st presentations SRS 2009

.....follow Indico over 14 years

SRS classic status 2023

SRSe new architectures: Last RD51 WG5 Dec 23:

RD51 2009-2023

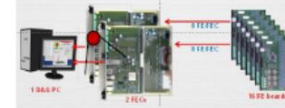
ELECTRONICS: the Scalable Readout System

CERN

SRS & APV25 FE chip

Worldwide use in the RD51 community (>2000 hybrids)

SRS+SiPM (NEXT TPC)



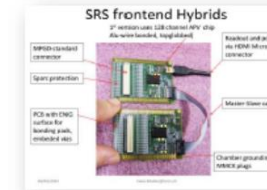
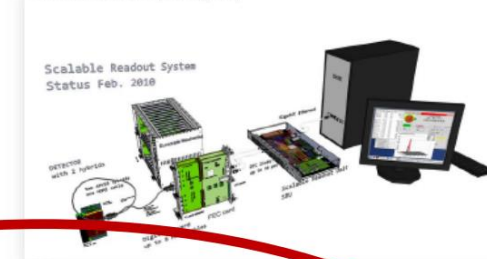
SRS-FEC+TOTEM DAQ



SRS+Timepix (LC-TPC) – Bonn/Desy

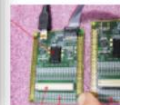


Scalable Readout System (SRS)



SRS: Diff

SRS for R8

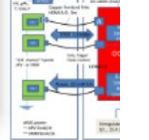


SRS-Classic: FEC and Adap



SRS for e

LHC experiment



Very appealing for the future: VMM (NSW ATLAS FE chip)



Baseline solution for RD51 SRS community.

Interest and support from ESS (European Spallation Source) and ALICE FOCAL

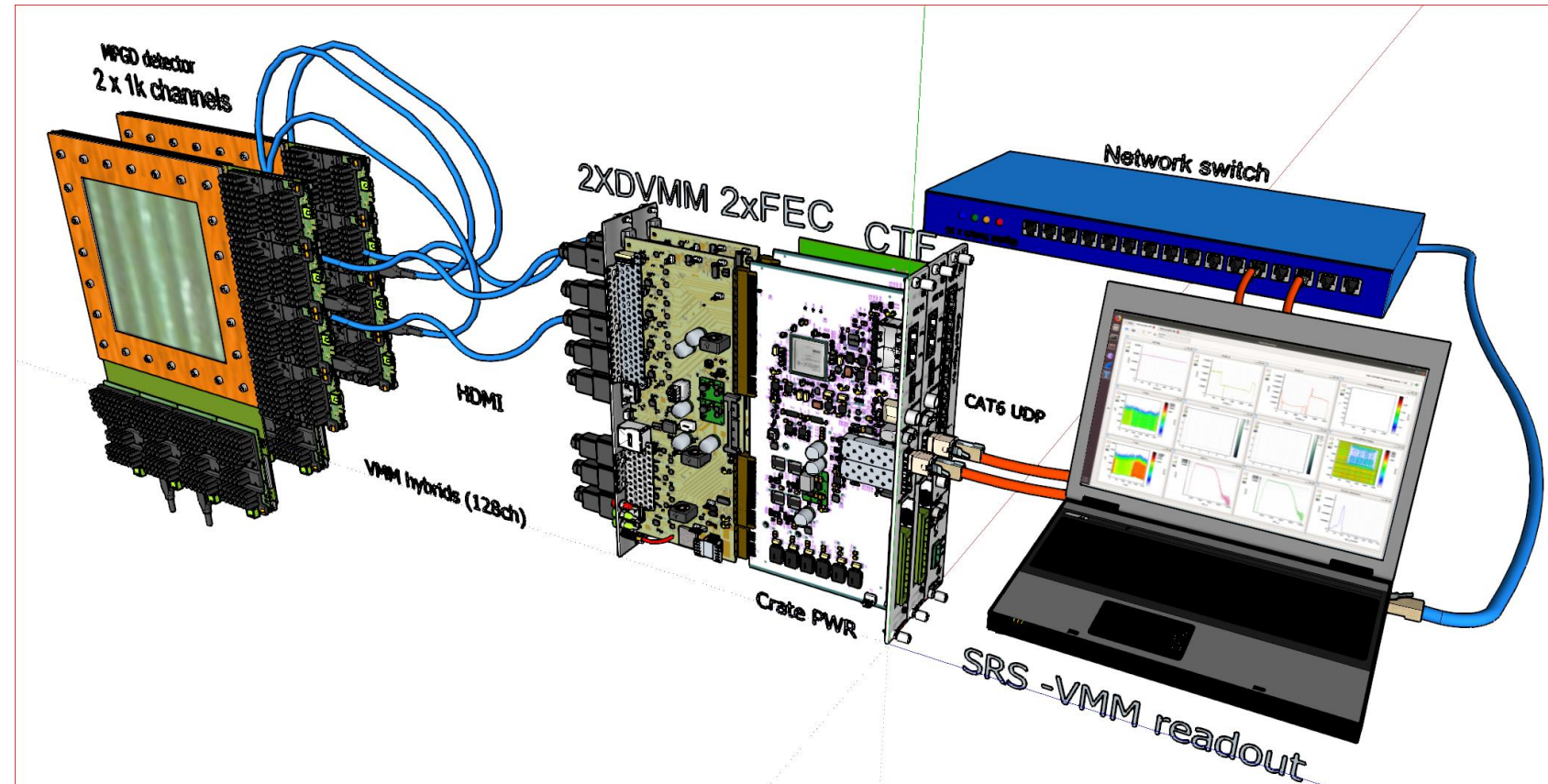
SRS for spatially c



LHCC, 11 September 2019

SRS classic Readout system from detector to Online

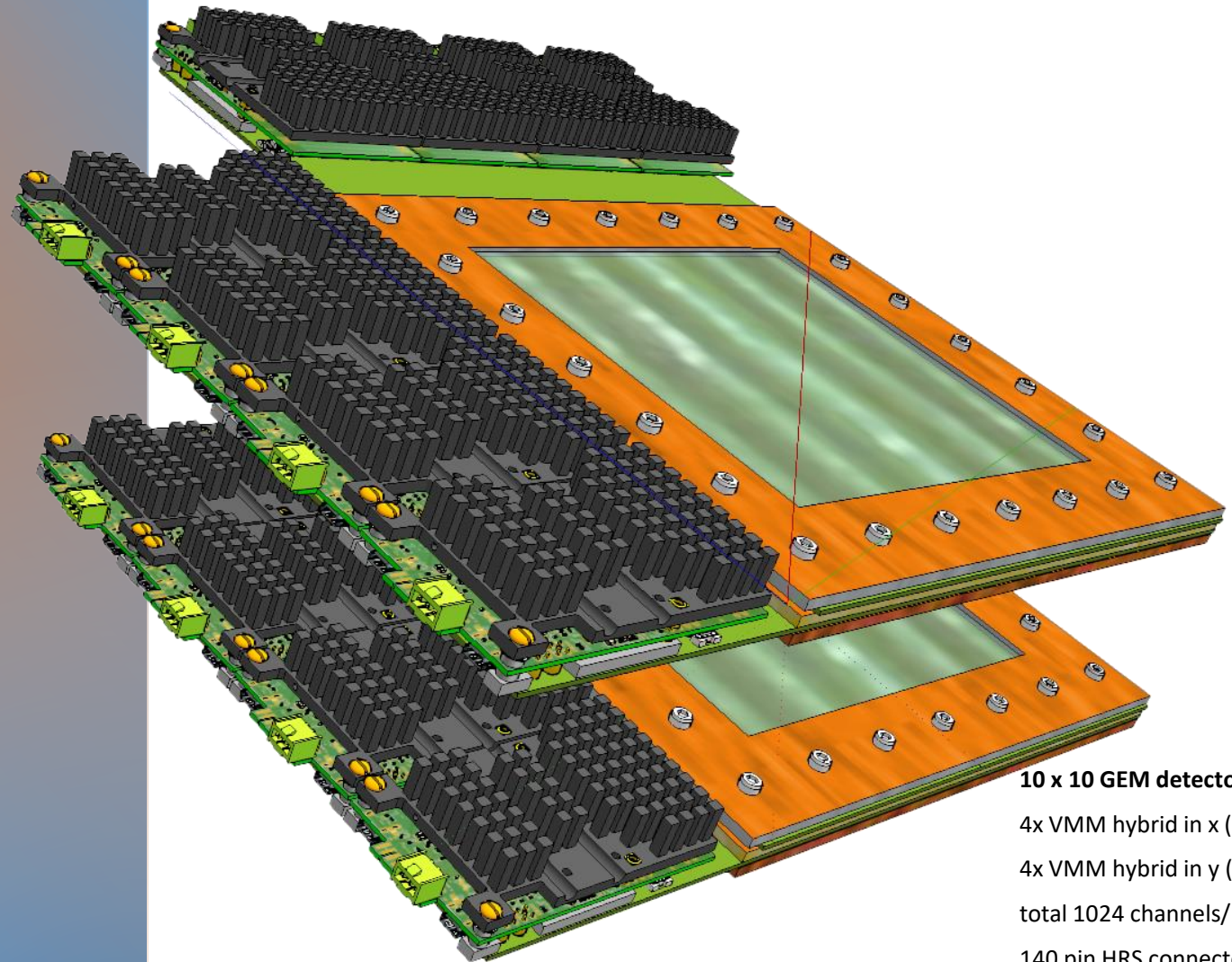
SRS with VMM frontend, so far implemented as a triggerless, scalable multichannel readout system for gas and photon detectors.
Triggered readout added by FRIB team in 2023/24.



1 FEC for 8 VMM hybrids / 1024 detector channels connected via HDMI AD cables to DVMM. 2 FEC's with CTF (common clock) for 16 hybrids, 2048 ch. DVMM cards with octal HDMI connector including 70 W power for 16 VMM hybrids. Power / housing for 2 FECs and CTF via 1 Minicrate (not shown). 1 GB Ethernet /UDP uplink from FEC to Network via SFP+ jack, fiber or optical 1 GBE for network with Jumbo packet support. ESS DAQ Software with Vmm Controls installed under Linux.

Detectors with VMM hybrids

- Since 2019, MPGD detectors are fabricated with 0.5mm pitch, [140 pin HRS connectors](#)* mating with [5mm stackheight](#)
- the HRS connectors of VMM hybrids.



10 x 10 GEM detector

4x VMM hybrid in x (512 ch)

4x VMM hybrid in y (512 ch)

total 1024 channels/ detector

140 pin HRS connectors* on detector

weight 8 VMM hybrids ~ 800 g

heat dissipation 8 hybrids ~ 30W

128 ch. frontend hybrid: VMM3a

[VMM hybrid user manual](#)

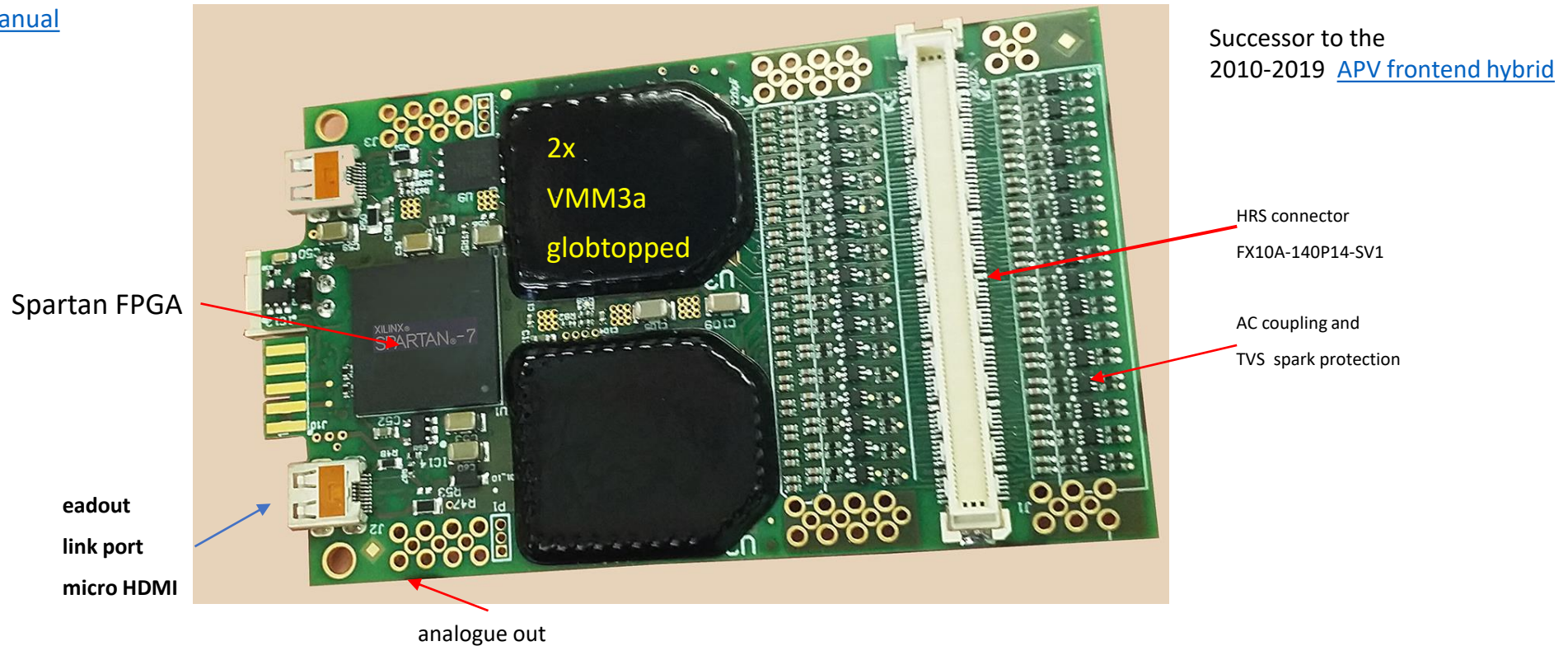


Photo VMM hybrid V5 (2022+) bottom side (cooler plate removed)

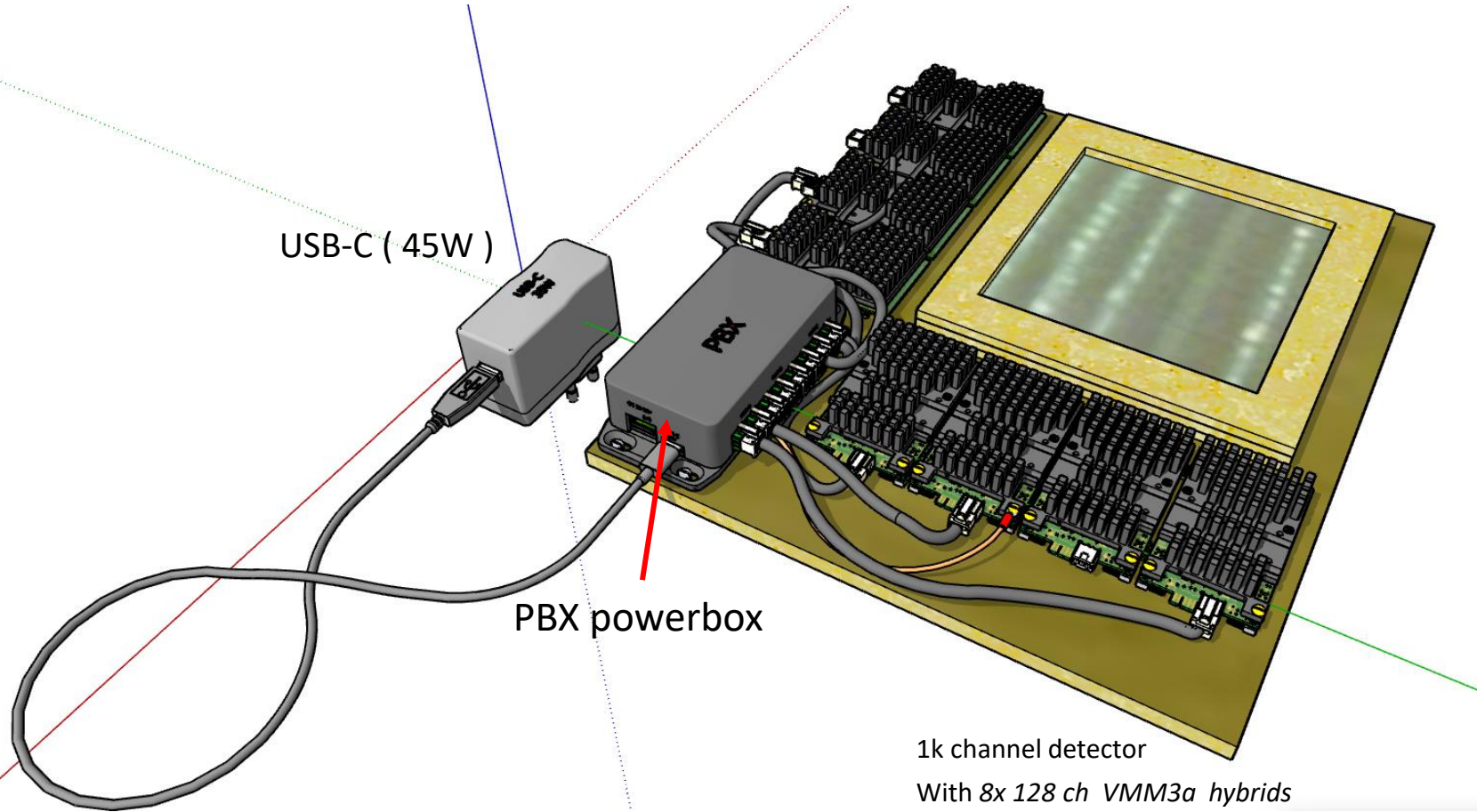
FE links: HDMI

HDMI cables for SRS DTCC links:

- 5 x twisted pairs up 4.95 Gbit/s
- direct power over short cables <5m
- up 30m with PBX power
- SRS links 320(400) + 640(800) Mbit/s
- robust, low-cost and rad-hard

micro HDMI

PBX frontend power

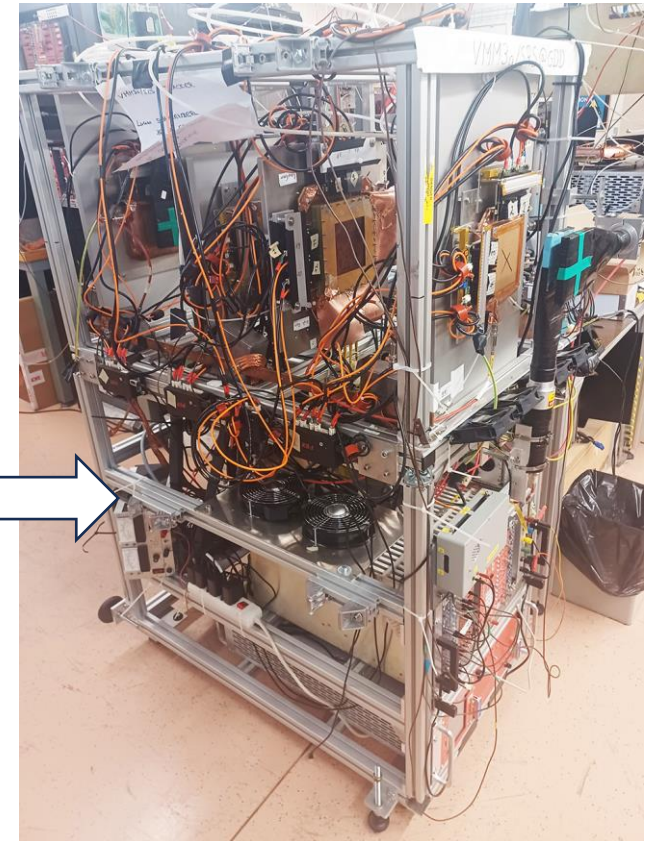


PBX powerbox kit

- 1 PBX box for 1kch VMM3a
- 1 USB-C 45W charger
- 8 x [power cables](#) (default 1m)
- 8 x Ferrite toroids

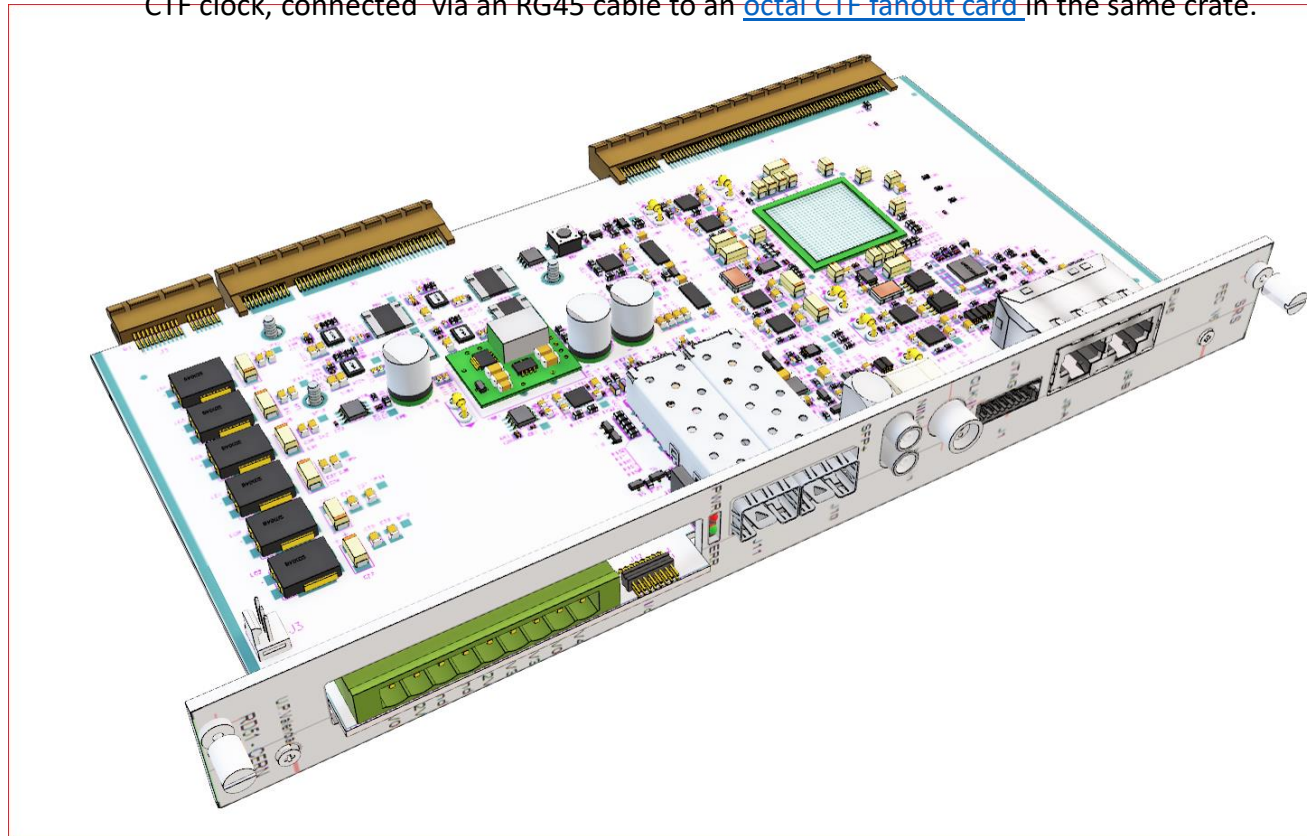


Quad GEM telescope
fully PBX-powered
-> K. Floethner GDD lab



FEC V6 card

The FEC V6 is a [FPGA firmware operated](#) frontend concentrator with an SFP port for Gigabit ethernet uplink to Online. Straddle-mounted frontend adapter like the [DVMM](#) or [ADC cards](#) interface up to 8 HDMI links to its Virtex-6 FPGA*. Single FEC cards can read out up to 8x128 channels from a detector equipped with 8 VMM hybrids. Up to 2 FEC cards can be housed and powered in a 3U Minicrate with a 9-way cable bus powering the FEC via the frontpanel. The FEC has a default a 40 MHz system clock transmitted to the frontend. Several FEC cards require a common, external CTF clock, connected via an RG45 cable to an [octal CTF fanout card](#) in the same crate.



The FEC V6 frontpanel has a rich [set of connectors](#) and 2 status LEDs. Several [configuration jumpers](#) are on the FEC PCB

Default [FEC firmware](#) for the ESS DAQ system for VMM frontend can be [updated via a frontpanel JTAG connector](#)**

Further I/O options require dedicated Firmware: [NIM input](#), [NIM output](#), external LVDS Clock input, [16 pin programmable User I/O](#), RG45 and a second SFP.

A [DDR3 memory plugin](#) can be inserted on the backside of the FEC.

Recommended:
[FEC firmware optimization](#)
2018 student report,
by Yan Huang, CCNU Wuhan

* XC6VLX130T-1FFG784C

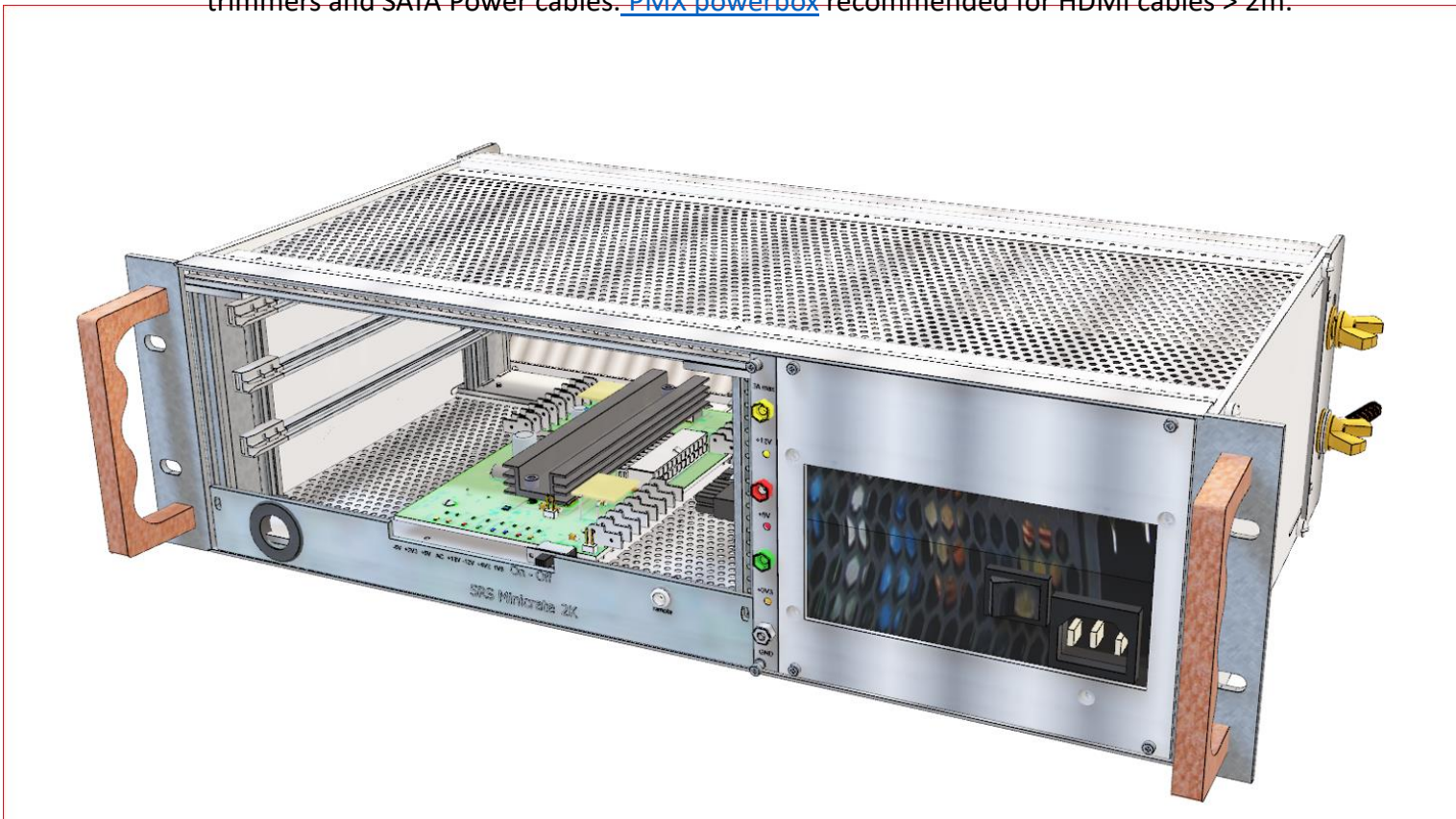
** the correct Flash Chip and Size needs to be determined, [several versions were mounted over time.](#)

SRS Minicrate

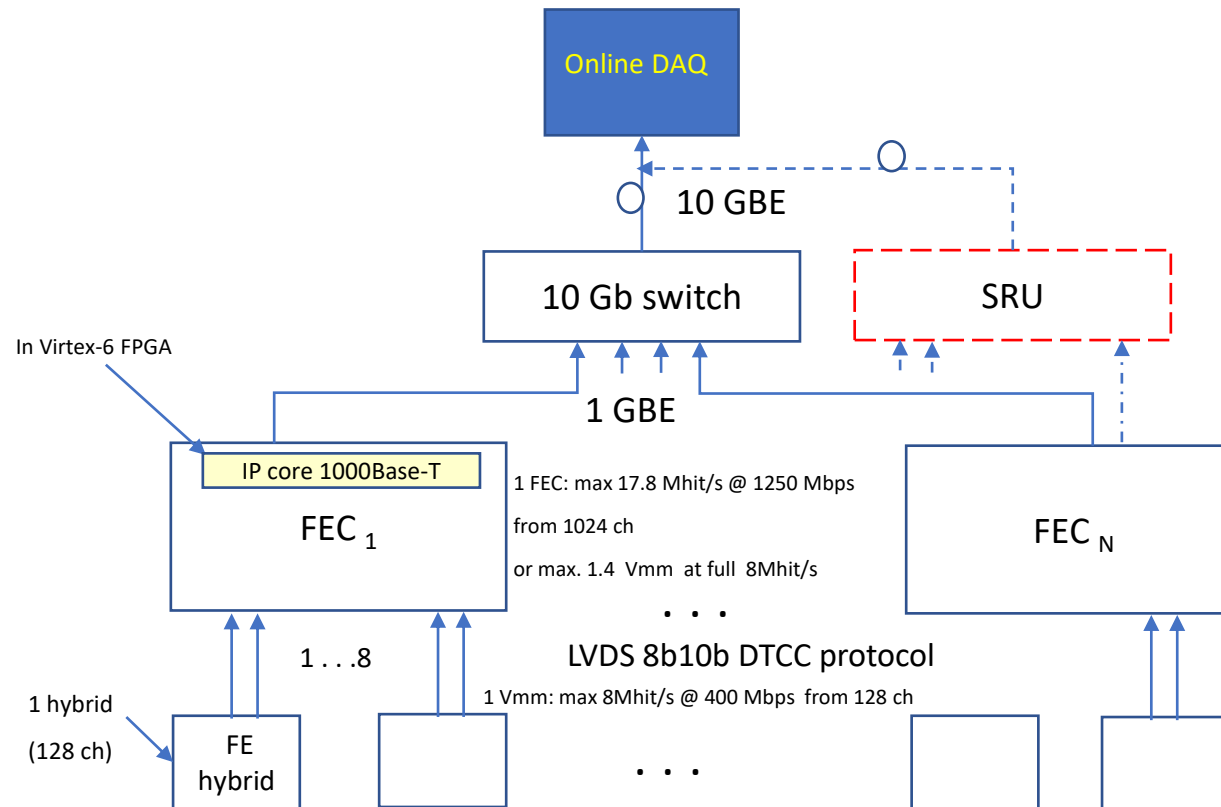
Minicrate for FEC and DVMM cards with [CTF card](#) slot and 2x 65W power for up to 16 VMMhybrids. 3U x 84TE rack-mountable crate 500W AC input, 3 horizontal slots : 2 slot FEC/DVMM, 1 slot CTF card (required for 2 FECs) HDMI links ports on the rear-side DVMMs. AC power inlet 110-240V AC. Octal frontpanel LED status display of ATX adapter voltages. Slide switch for remote on/off via coax cable 50Ω terminator, power panel for direct access +12V,+5V,+3.3V for user service electronics. Rear M8 wing-screws for GND braid attachment to VMM hybrid digital GND. Top cover detachable for access to trimmers and SATA Power cables. [PMX powerbox](#) recommended for HDMI cables > 2m.

[Minicrate user manual](#)
[ATX adapter user manual](#)

The larger 6U x 80TE [SRS Eurocate](#) serves up to 64 VMM hybrids. with 2 x 0.5 kW AC input

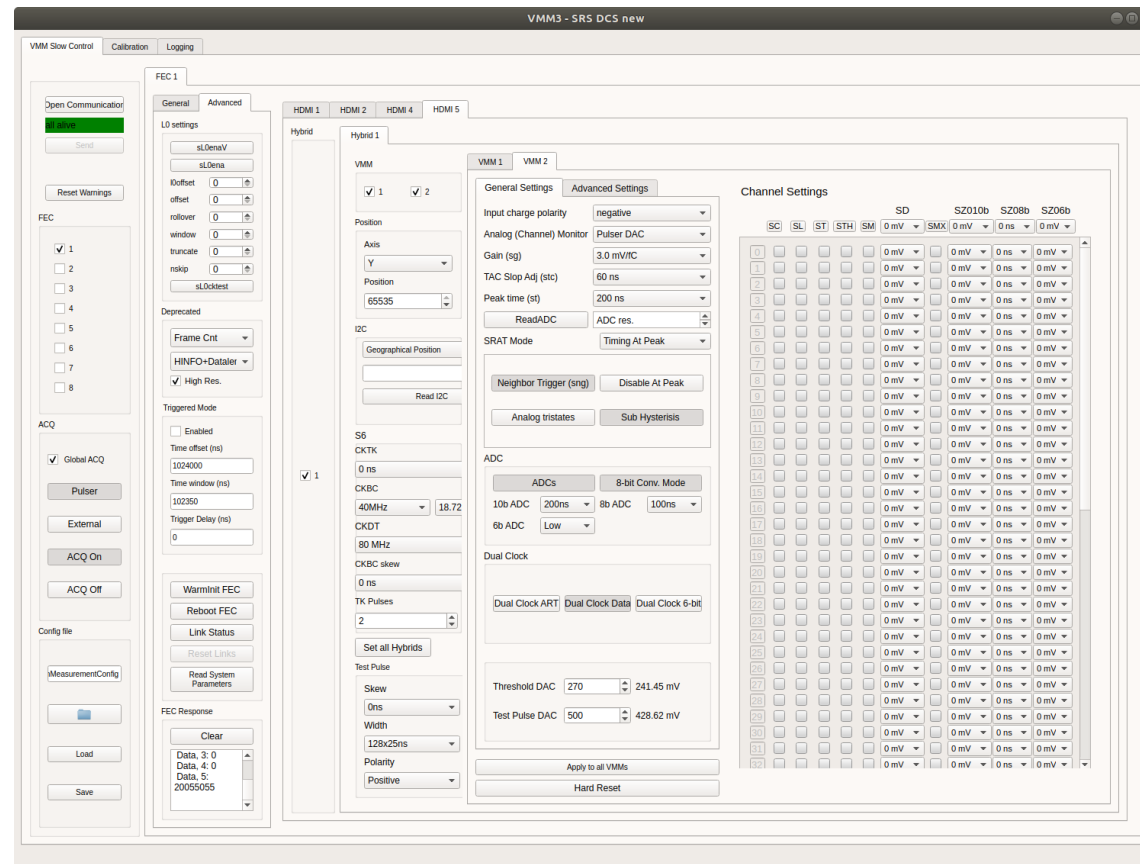


Scalable RO architecture



DAQ and Slow controls

ESS DAQ : <https://github.com/ess-dmsc/essdaq>



Slow Controls GUI for SRS run control with VMM3 frontend connected via [DVMcard](#)

Analysis tool for ESS DAQ data :

<https://github.com/ess-dmsc/vmm-hdf5-to-root>

[VMM3a slow control user manual on gitlab](#)



List of SRS VMM users (since 2018)

GEMs with VMM frontend and SRS readout SW at the NMX Diffractometer ,Multiblade Detector with wire readout using VMM and SRS readout + other ESS instruments considering VMM frontend, ESS European Spallation Source, Lund Sweden

Gaseous Detectors for Preclinical Proton Beam Monitoring, at Dep Physics Medical, LMU Munich

SRS readout with cooled VMM's in a vessel for tracking system for the S800 spectrometer at (FRIB RIB Facility Michigan USA)

New TPC for HYDRA at GSI/TU Darmstadt for measuring pions, SRS readout with VMM frontend @ GSI/TU Darmsatadt

muon tomography for geological applications, SRS VMM readout, LSBB Rustrel, FR

use of GEM telescope with SRS/VMM readout and NIP pattern injector, NA61/Shine CERN

Triple GEM in borehole with VMM readout via VTC, OXY colleague LA ,USA

Cygnus neg. ion TPC in pressure vessel for charge readout VMM/ SRS , Hawai Univ. Honolulu

Micromegas with VMM SRS readout for PANDA-FAIR phase 0 , MAINZ Univ. Physics DE

GripIX TPC with Timepix 3 readout via SRS adapter, BONN Univ. Physics DE

Qualification MM for Atlas NSW, LMU Physics Faculty Munich

readout of Multiplexed MM with VMM SRS for NA64. Plans for addition of external VMM trigger, ETH Zurich, CH

MPGDs for photon detection, VMM, INFN Trieste

VMM trigger readout Controller ROC for ATLAS NSW, IFIN-HH- RO

SRS ATCA readout system for NEXT TPC, UPV Valencia Sect. Gandia

MPGD's for several national research project, SRS with VMM included, JLAB T.Jefferson Natl Accelerator USA

cosmic telescope with VMM readout, Universidad de los Andes, Bogota

GEM beam telescope with SRS VMM for testbeams and VMM qualification , GDD lab CERN

XYU-GEM ambiguity-free readout with VMM/SRS (RD51 -Note -2022-09), GDD lab CERN

TPC with SRS/VMM readout for search of X17 particle at a 5 MV accelerator , Melbourne Univ. AU

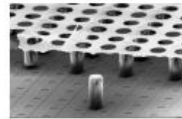
Compass GEM upgrade with SRS VMM3a readout, Univ. Bonn DE

SiPM dual gain readout with VMM/SRS at ALICE FOCAL testbeam

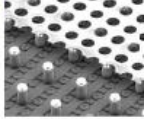
note: this list is not complete

SRS readout Timepix (Univ. Bonn)

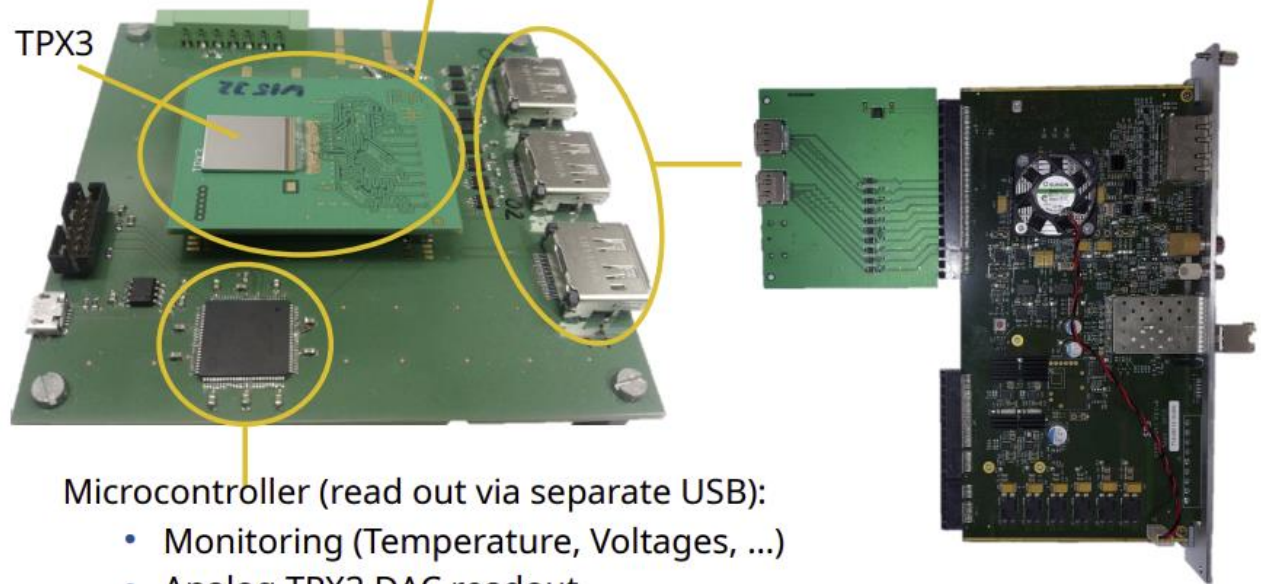
[more information](#) J. Kaminski Dec. 2023



Timepix3 Readout in SRS



Carrier board (plugged into Intermediate board)
Shape and number of chips depending on the detector

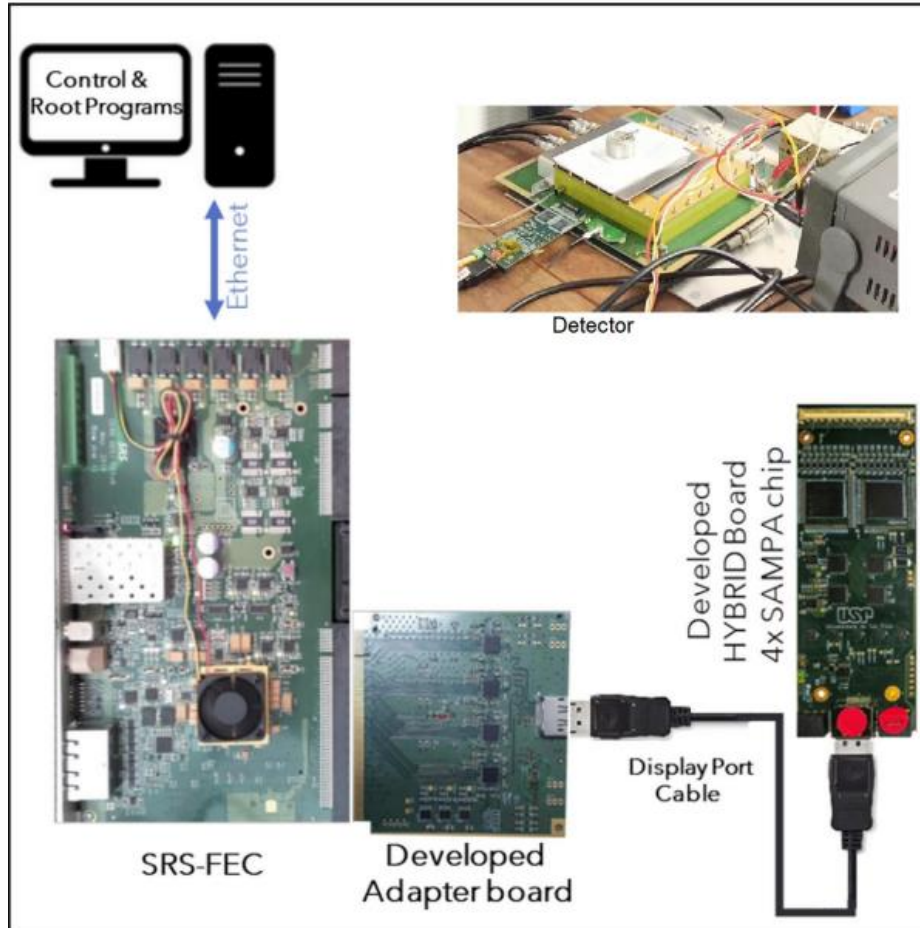


Microcontroller (read out via separate USB):

- Monitoring (Temperature, Voltages, ...)
- Analog TPX3 DAC readout
- External TPX3 DACs

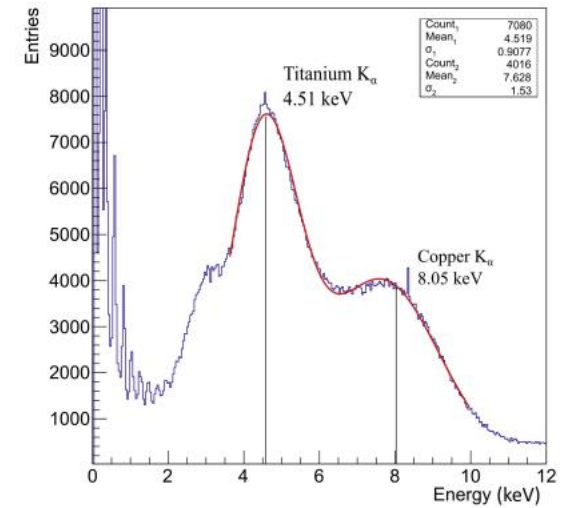
FEC and A-card

SampaSRS



[More information on SampaSRS Dec. 2023](#)

X-ray fluorescence using SAMPA and SRS



SRS production and availability

- CERN store for CERN-registered users (VMM hybrids, FECs, MiniCrates ..) SCEM 07.89.00 - RD51 SRS
- [SRS Technology](#), CH (VMM-hybrids, FECs, DVMM, CTF, + coming: PBX, uROC , SiPM –adapt..)
- Opus Automation, IT (Minicrates) - contact available on request
- SAMWAY, Bucharest, RO (FEC V6 cards) –contact available on request

SRS documentation, FAQ, Repositories

- Google [drive H.M.](#) SRS HW user manuals, [FAQs](#)
- [Software Installation L.Sch.](#) Software overview and mp4 video on SW installation
- [Experience with VMM3a L.Sch](#)
- [Firmware and Software FAQ](#), Firmware DOC
- [Gitlab software repository](#)

Recent & new SRS developments

SiPM adapter for VMM hybrids

SiPM Adapter prototype on on Alice Focal Testbeam 2023 with 4 VMM3a hybrids and SRS DAQ

SiPM adapter



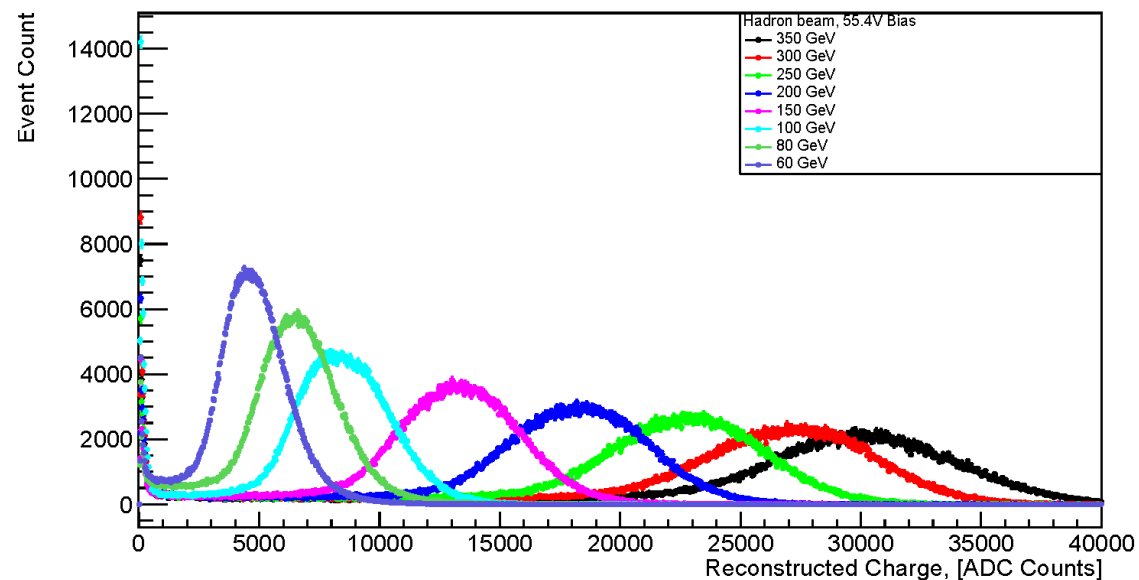
VMM hybrid



64 ch adapter plugs on VMM hybrid
High and low gain
SiPM bias U_{br} 10-80V included
& via Slow Controls

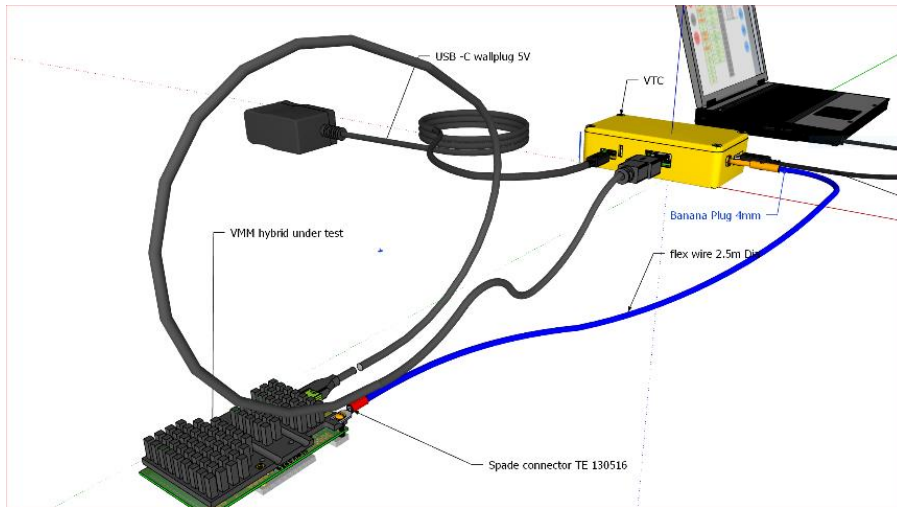
2023 [Alice FOCAL testbeam at SPS with SiPM –VMM adapter](#)
& [Data Analysis](#)

Energy distributions using HG data

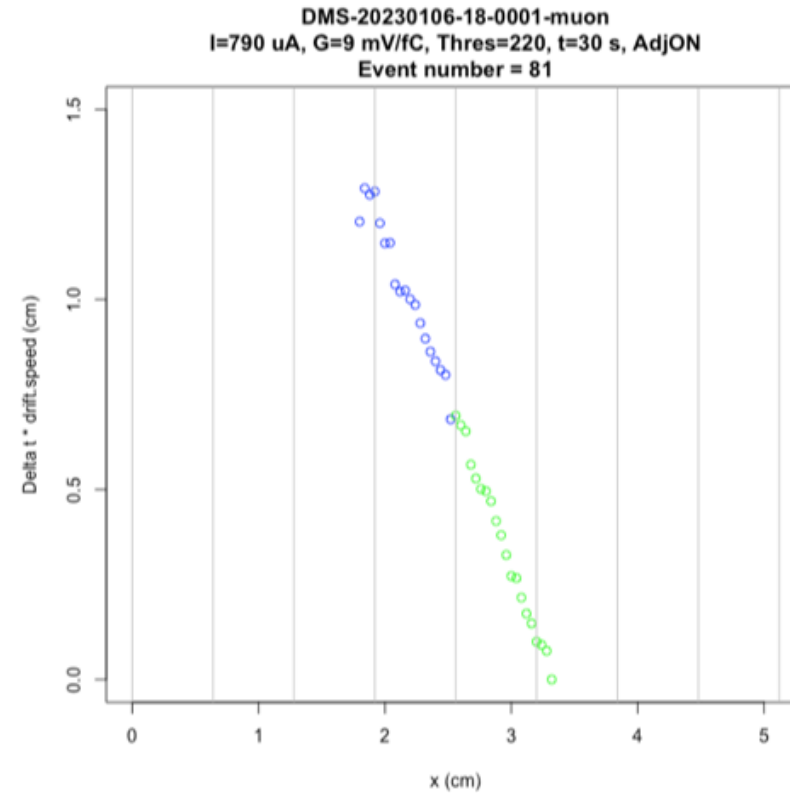


Low- rate, triple GEM readout* with VMM and SoC-based VTC @ OXY Colleague, LA

[more information](#)



“Low Noise Electronics Development at Occidental College for Dark Matter and Muon Research”.



Muon tracks recording

Coming: uROC for 256 ch

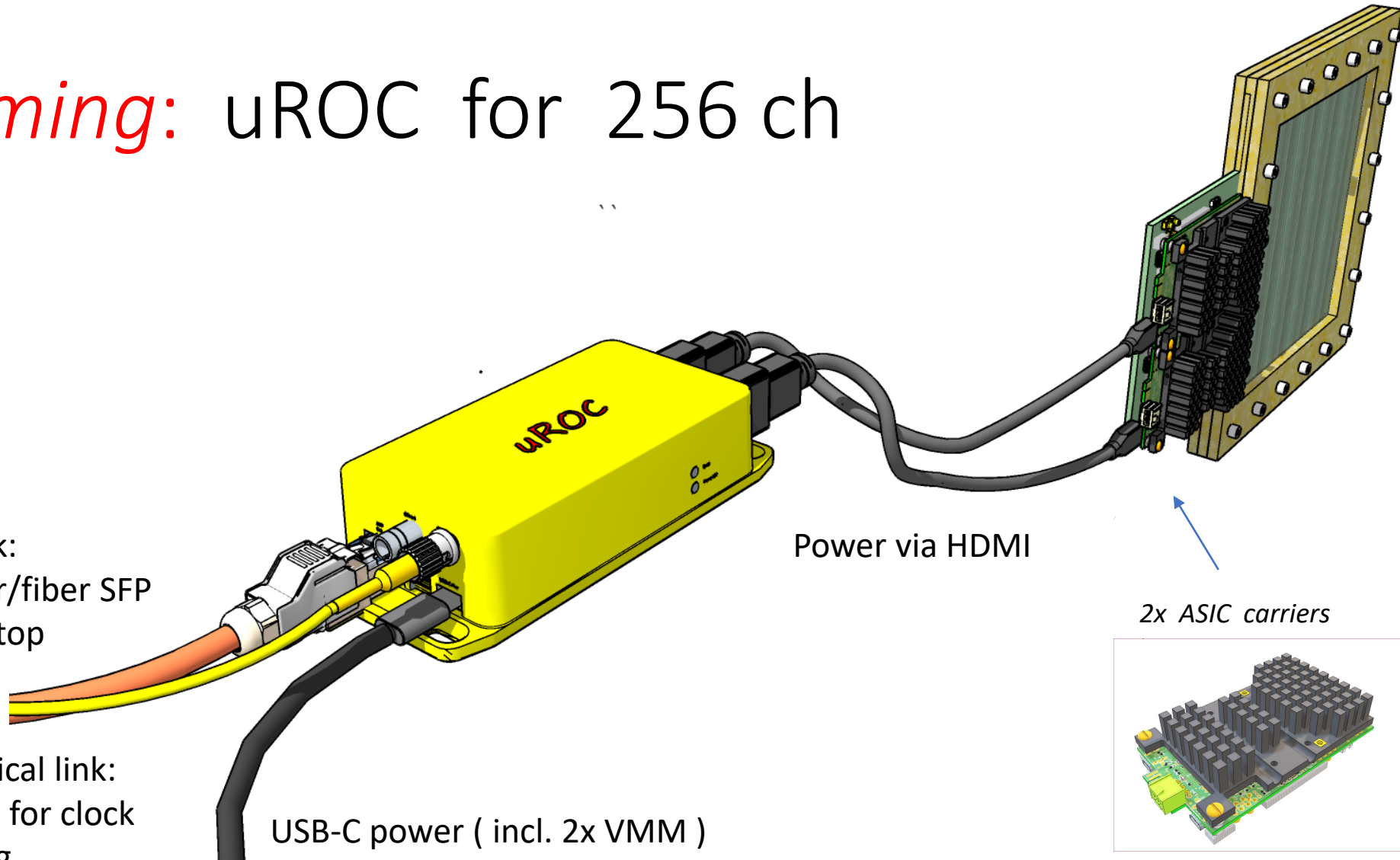
RO link:
copper/fiber SFP
to Laptop

ST optical link:
option for clock
sharing

USB-C power (incl. 2x VMM)

Power via HDMI

2x ASIC carriers

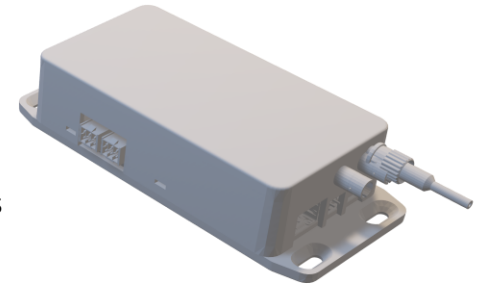


New in 2024: crate-less dFECs

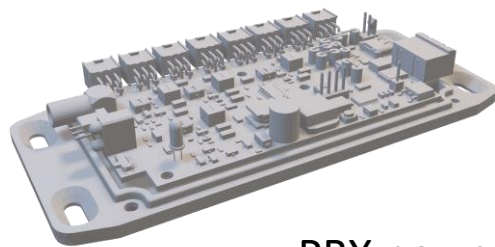
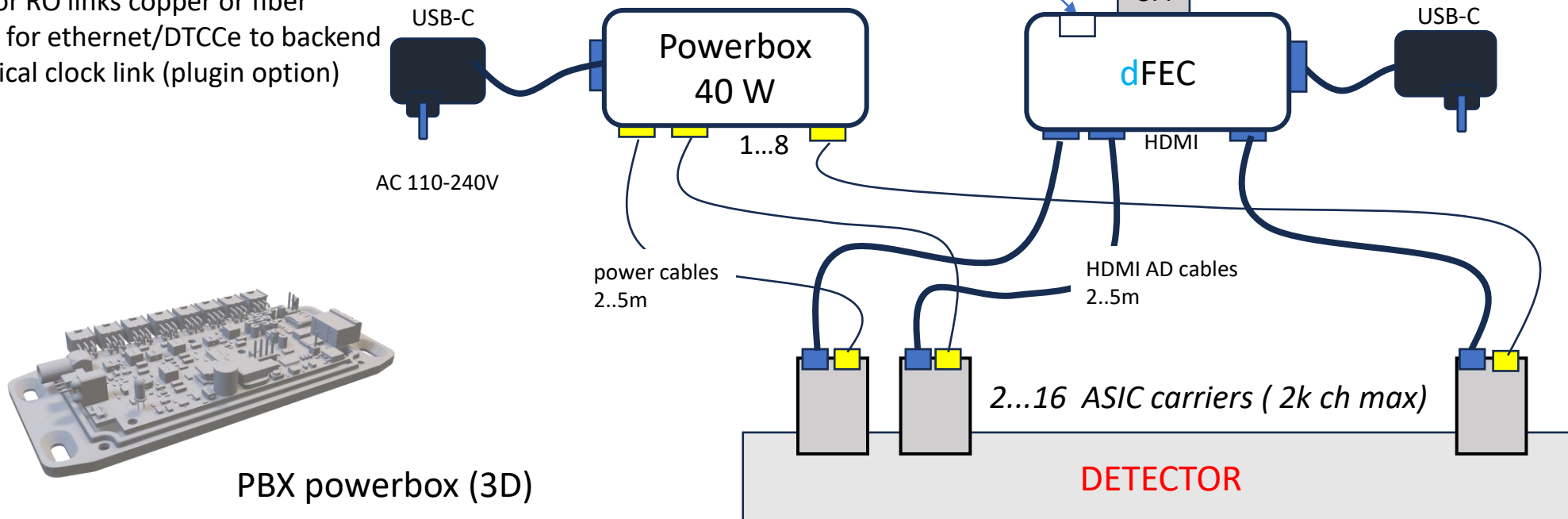
like classic FECs , can directly connect to DAQ on Laptop via ethernet

dFEC's

- portable / hand-sized boxes
- state of art FPGA logic
- 2 ..16 HDMI powered frontend ports
- max. 2k channels/ dFEC
- USB-C powered
- SFP for RO links copper or fiber
- switch for ethernet/DTCce to backend
- ST optical clock link (plugin option)

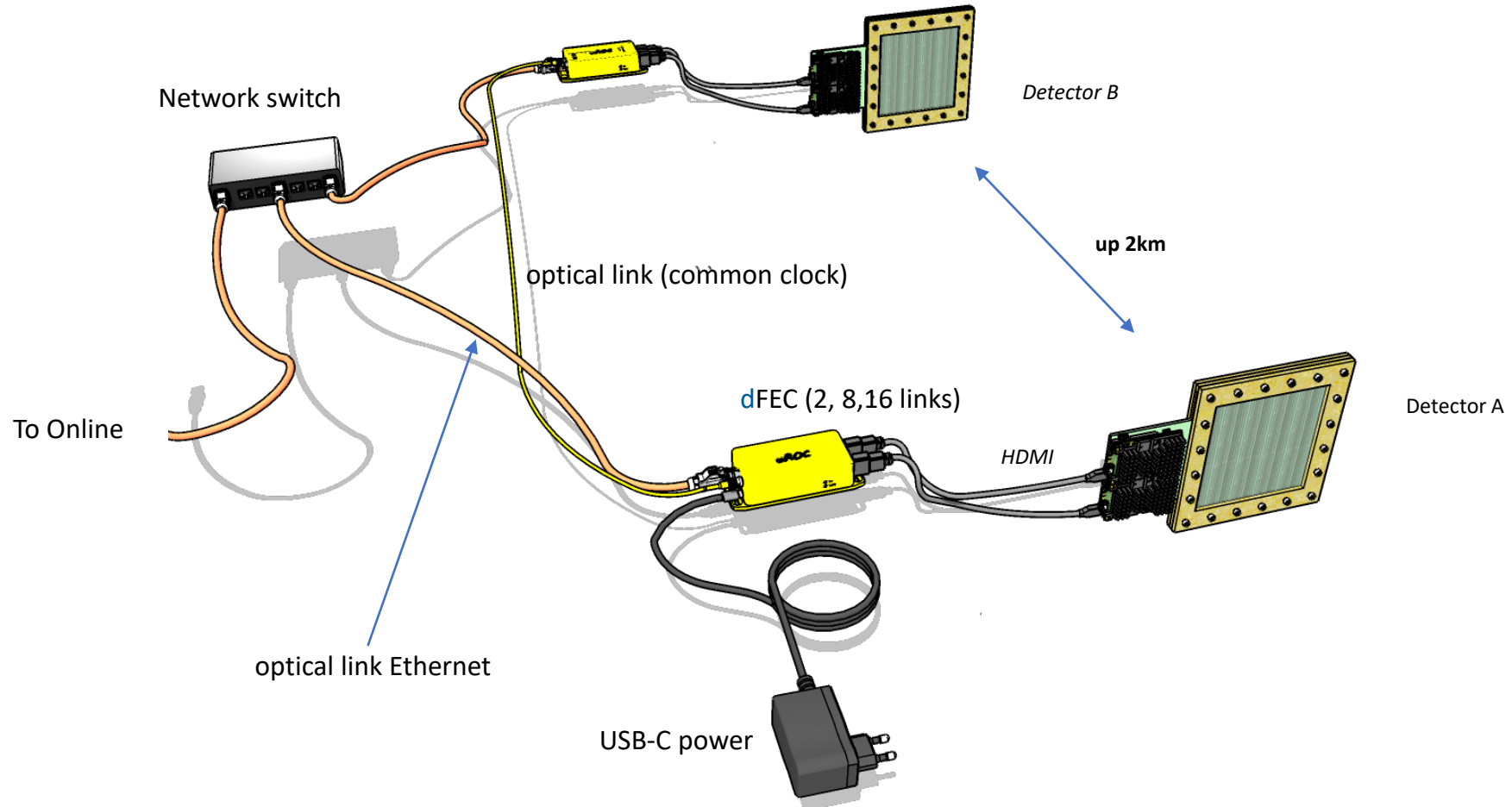


dFEC box (3D)



PBX powerbox (3D)

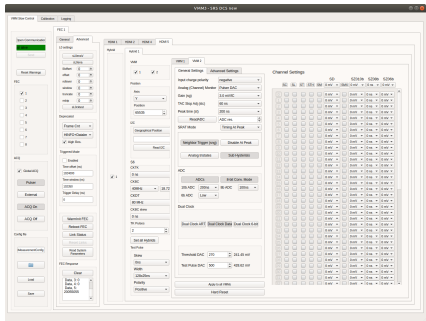
New, distributed, small detectors



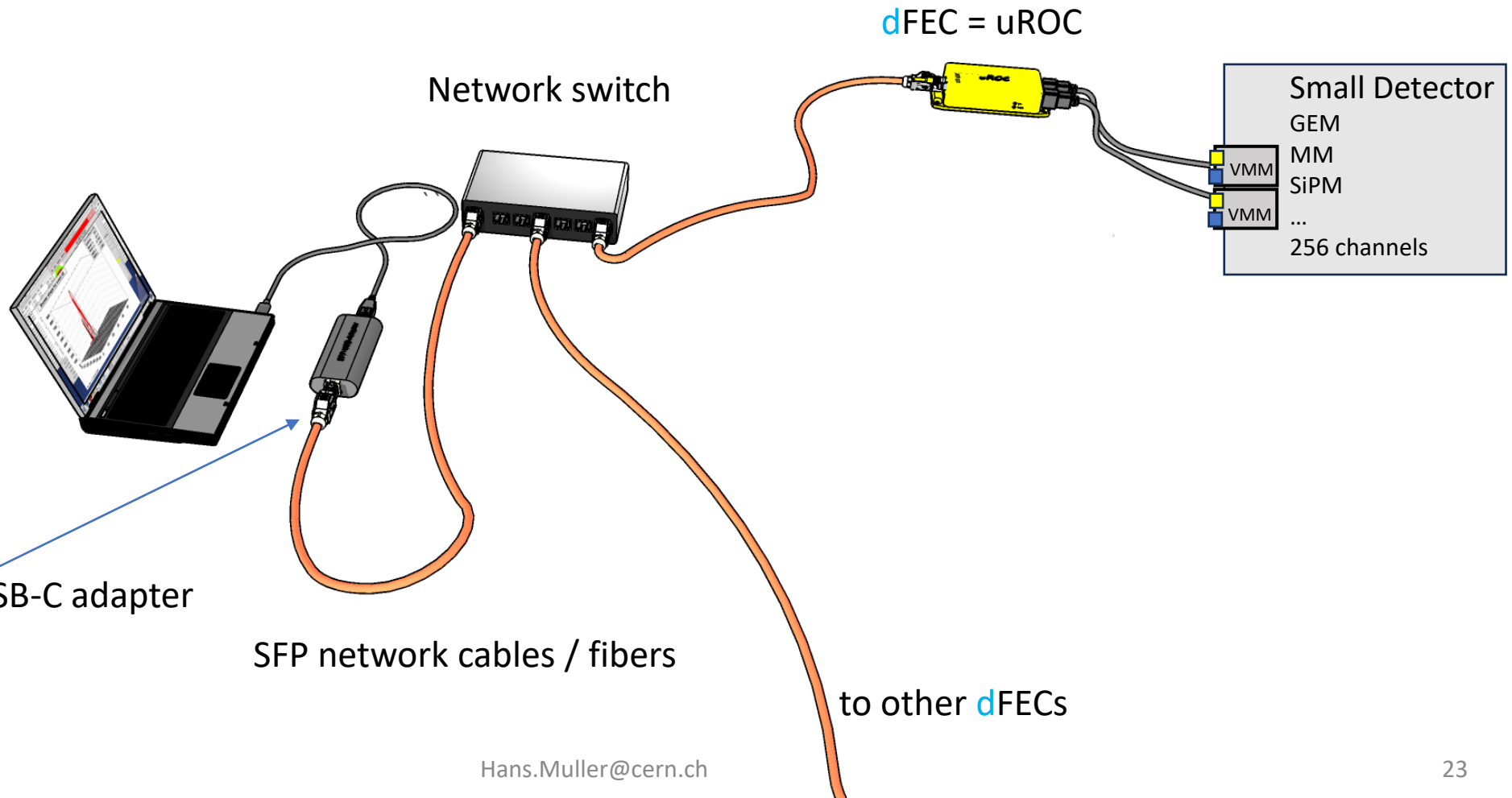
Small systems DAQ

dFEC FW will be adapted to work with ESS-DAQ like classic FEC

ESS DAQ and Controls
on Laptop

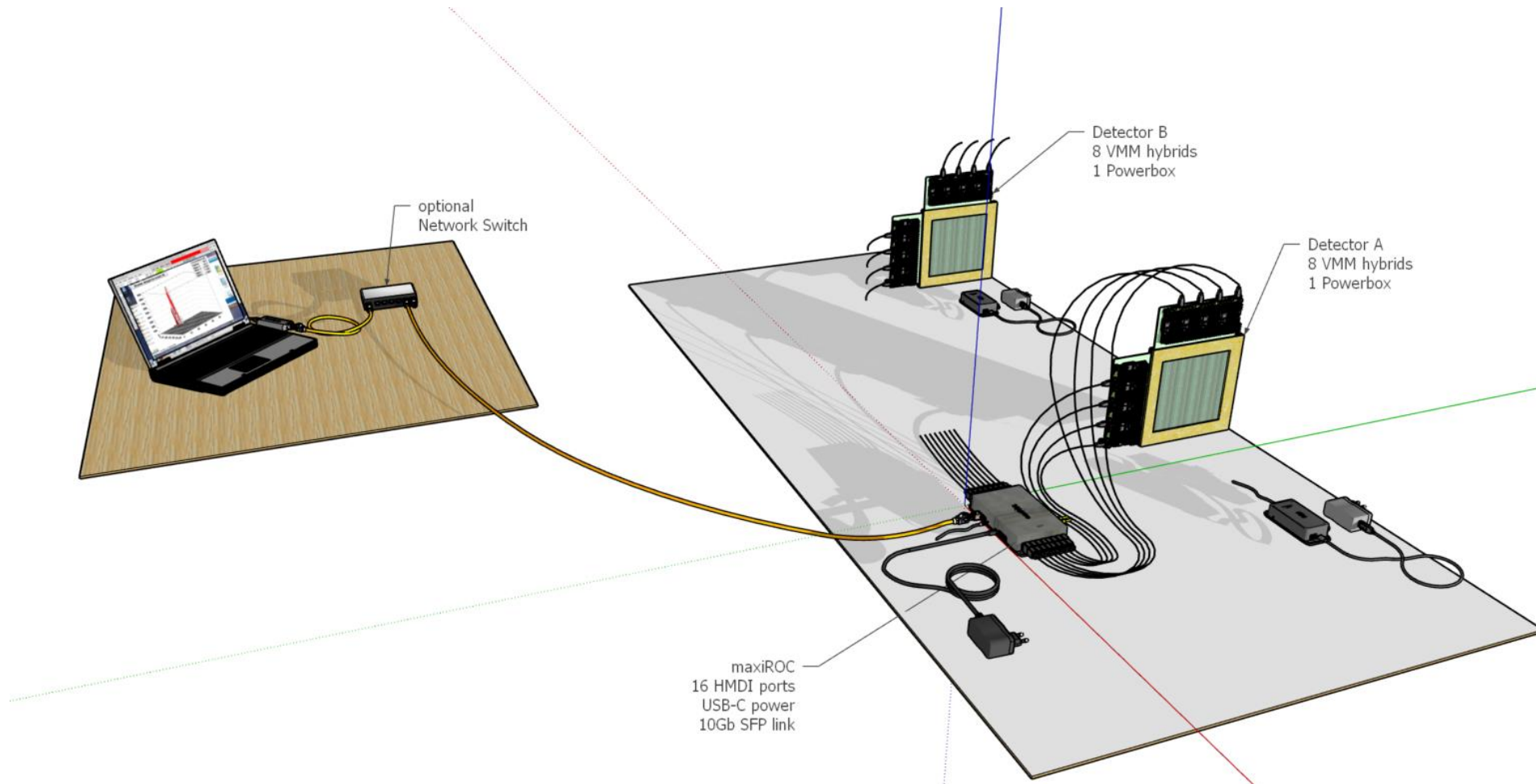


Ethernet / USB-C adapter



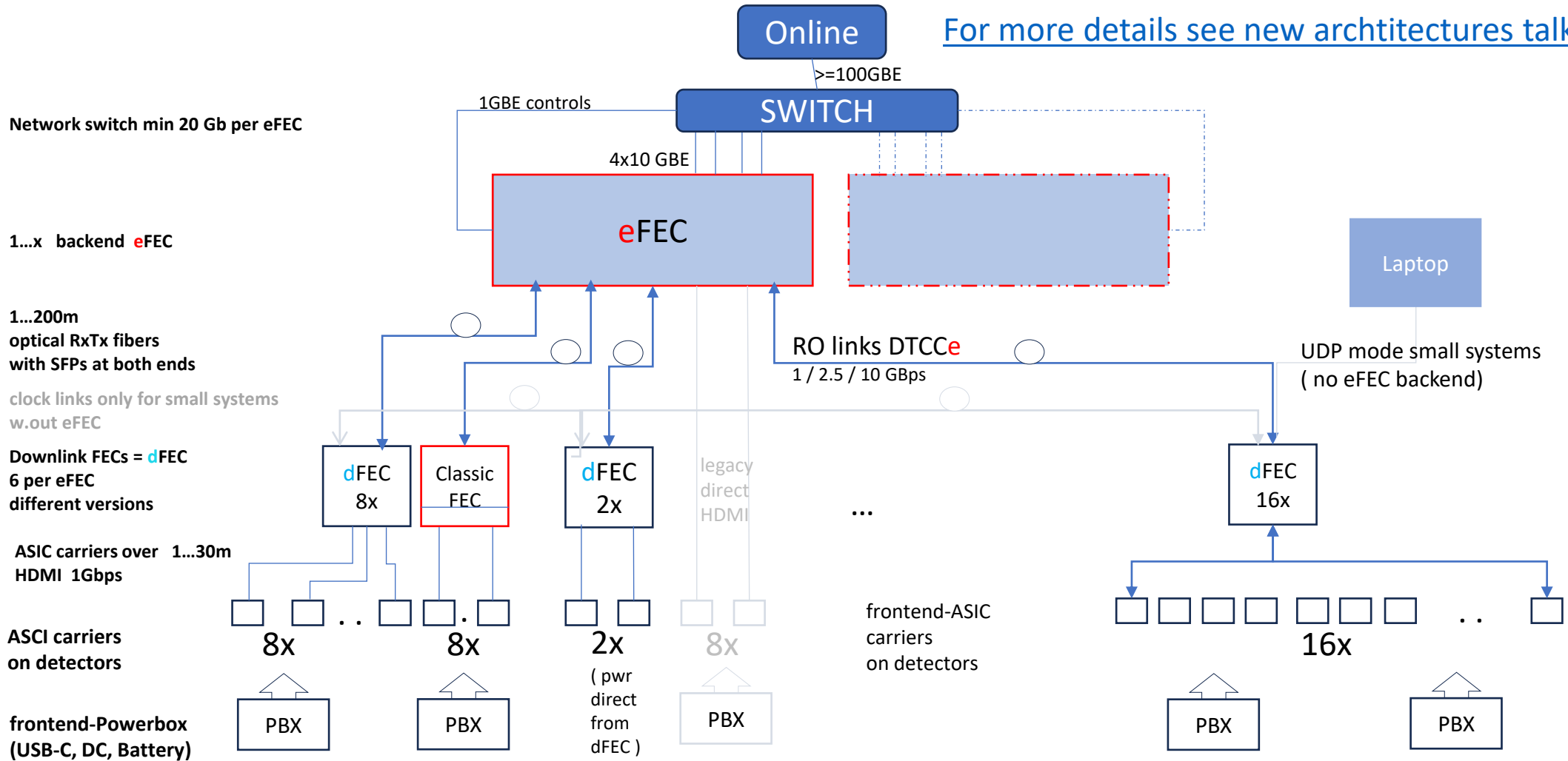
The next step: dFECs for medium-sized detectors

Readout & DAQ of N x 2k detector channels via maxiROC



the full plan: Scalable Readout Architecture

[For more details see new architectures talk Dec 23:](#)



eFEC backend module (to replace 2009 SRU for 2024+)

General

- same physical outlines as FEC + DVMM together 6U x 220mm
- housed and powered (USB-C) in classic SRS crates
- Ultrascale+ Zync FPGA

Connectors rear

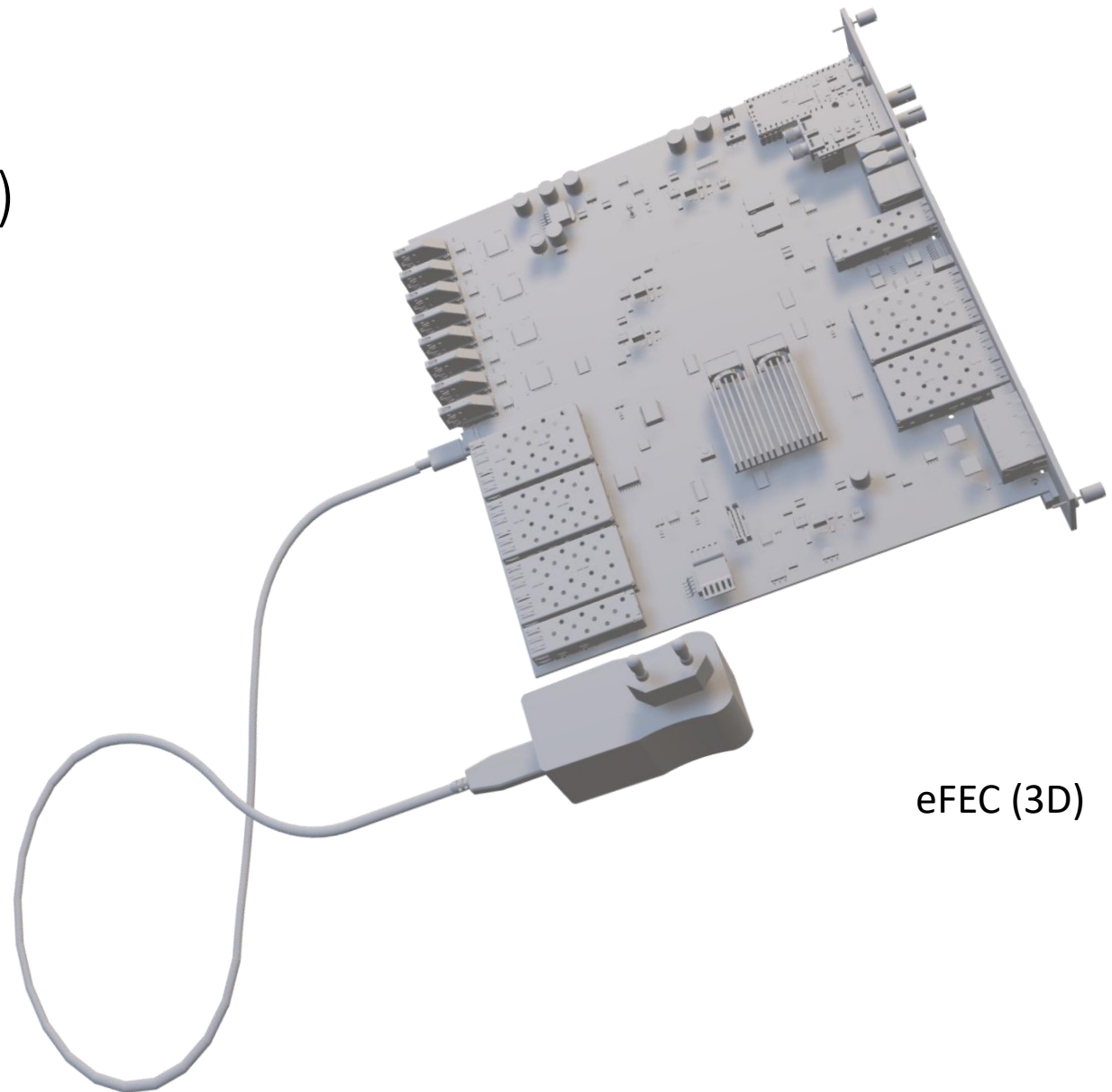
- 8 x legacy, powered HDMI link ports to VMM frontend
- 6x frontend DTCCe link port SFP+ 1 /2.5/ 12.5 Gbps
- 1x 100Base Ethernet for Controls link
- USB-C power connector

Connectors front

- 4 x uplinks SFP+ to Online 10GBE/UDP
- 1 x uplink SFP+ vertical architecture summary link
- 2 coax Trigger Inputs and 2 coax trigger outputs (NIM)
- 1 CTF+ clock and trigger links (RG45)
- 1 x horizontal Xlink Rx Tx horizontal serial link (RG45)
- 1 x horizontal SYNCbus mixed analogue / digital

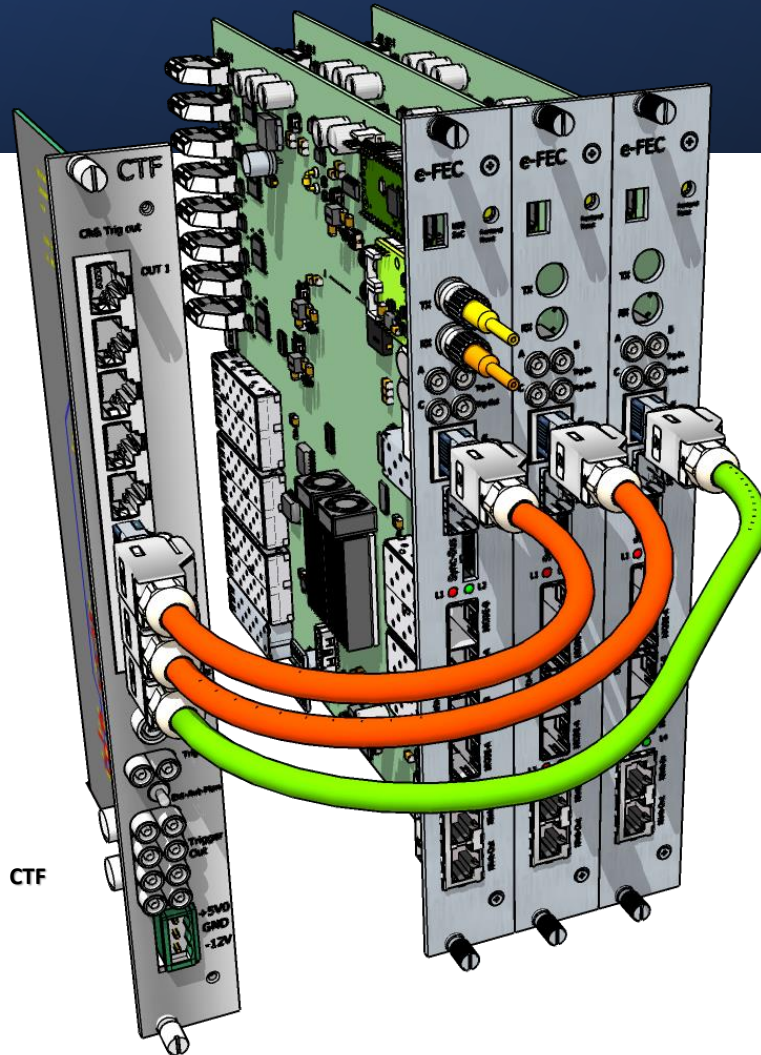
Plugin options

- 1 optical ST RX / TX link mezzanine (serial injector option)
- 32 bit SoC with USB debug port (Raspberry Pi pico)
- DDR4 plugin 64 GB (backside)



eFEC (3D)

New possibilities: online triggers in FPGAs



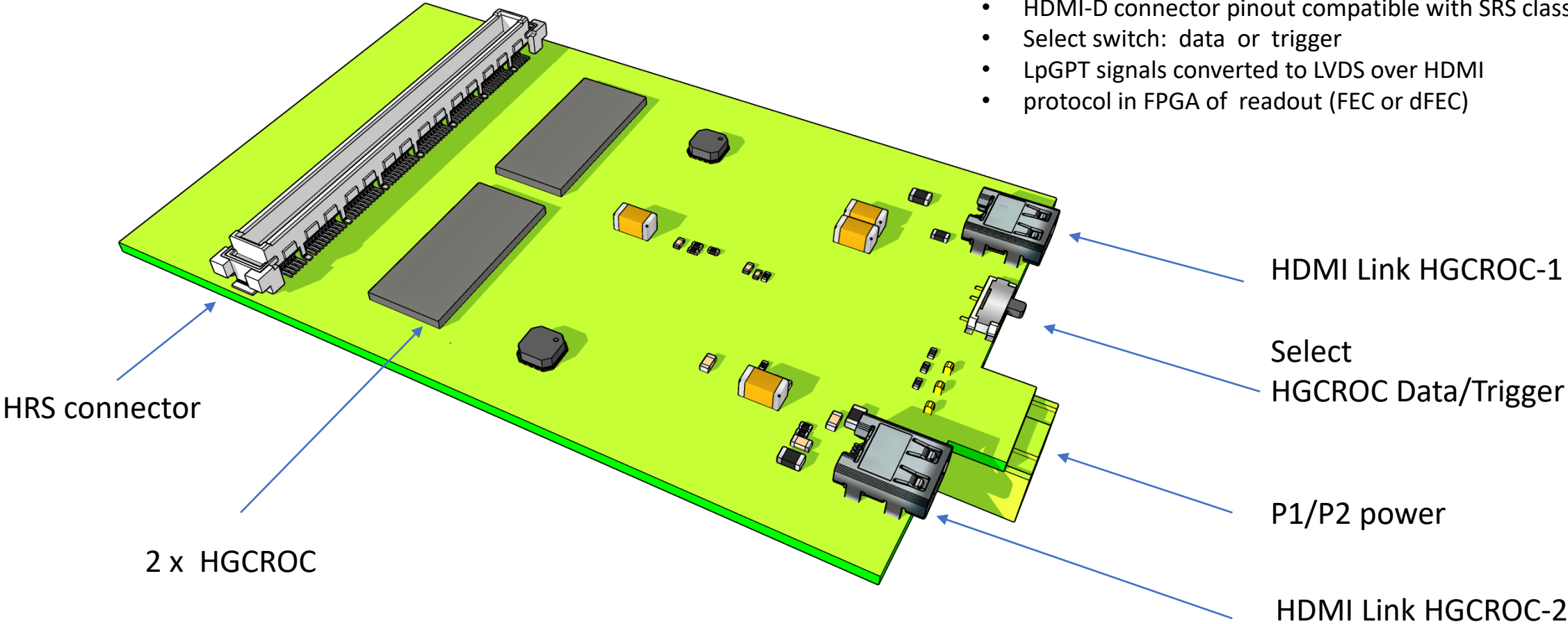
Common clock CTF

- Ultrascale FPGA interconnect cabled via frontpanels

Possible new SRS Frontends (tbd)

example study case: 128 ch HGCROC

- 2x HGCROC per hybrid with 128 ch HRS connector
- 2 x HDMI –Micro connectors , one per HGCROC
- HDMI-D connector pinout compatible with SRS classic
- Select switch: data or trigger
- LpGPT signals converted to LVDS over HDMI
- protocol in FPGA of readout (FEC or dFEC)

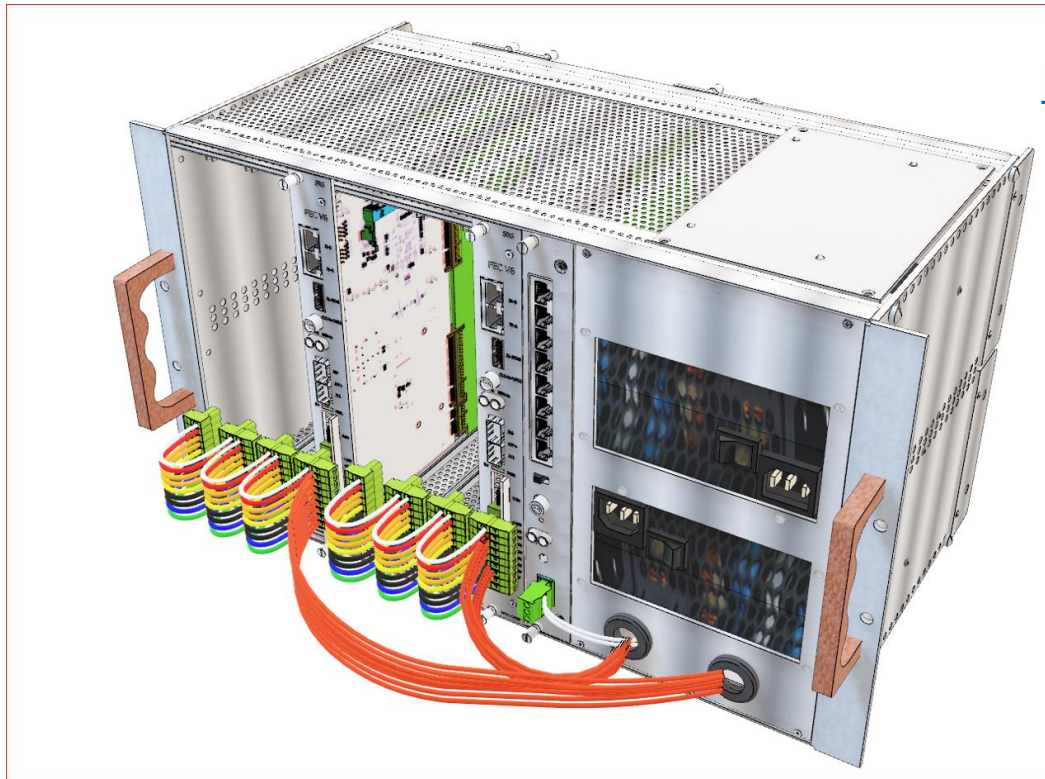


join the SRS user community
and
developer teams / discussions

Backup material

SRS Eurocrate

Eurocrate for FEC and DVMM cards with [CTF card](#) slot and 8x 62W power for up to 64 VMM hybrids. 6U x 80TE rack-mountable crate 2x 500W AC input, 9 vertical slots : 8 slots FEC/DVMM, 1 slot CTF card (required for >1 FECs). HDMI links ports on the rear-side DVMMs. Two AC power inlets 110-240V AC for FECs 1-4 and 5-8. Rear-panel with LED status displays two ATX adapter voltages and 2 slide switches for remote on/off via coax cable 50Ω terminator. Rear power panel for direct access +12V,+5V,+3.3V for user service electronics. Rear M8 wing-screws for GND braid attachment to VMM hybrids, 1 per DVMM. Two frontside powerbuses for FEC1-4 and CTF card, FEC 5-8. 5 x SATA cables each with 3 SATA connectors for DVMM card power. With 500 W ATX supply up to 64W @12 V per SATA cable to DVMM (-> 8 VMM hybrids), [PMX powerbox](#) recommended for HDMI cables > 2m.



[Eurocrate User manual](#)

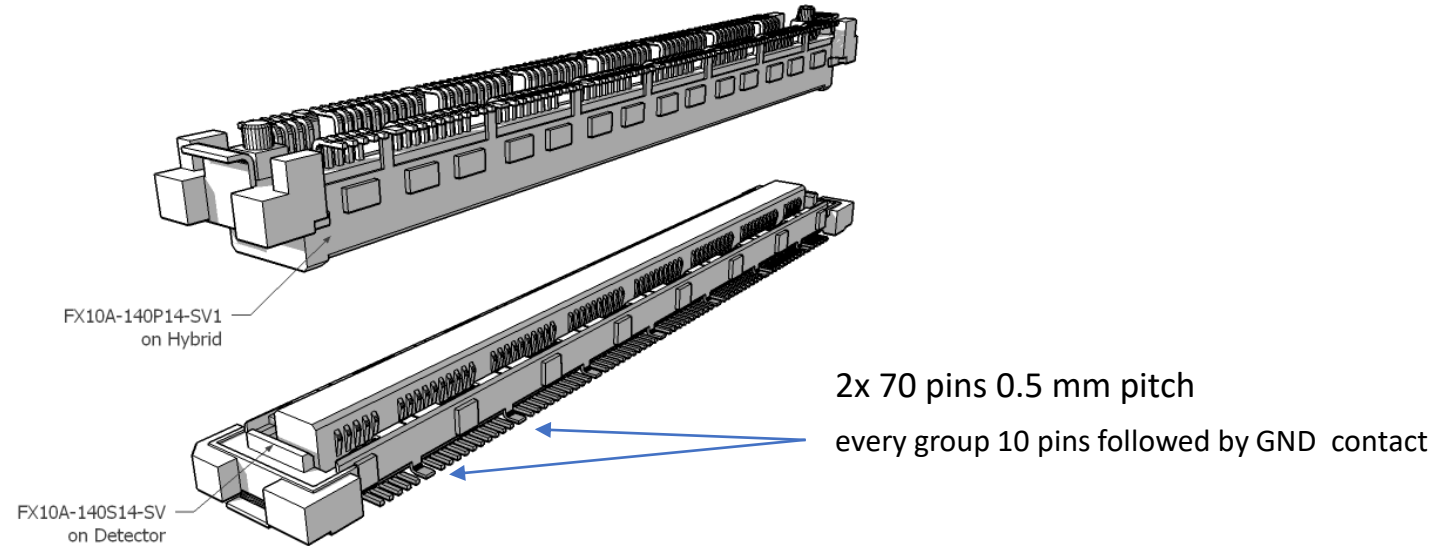
- Note 1: Slot 1 for CTF card only
- Note 2: ventilation from the bottom is mandatory for >2 FECs (any commercial 1U rack-mountable ventilator)
1U air exhaust volume on top of crate
- Note 3: SATA cable routing to DVMMs required
- Note 4: bf default, slide switches on backpanel must be in "ON" position

[3D view download ppt](#)

HRS: MPGD connector standard

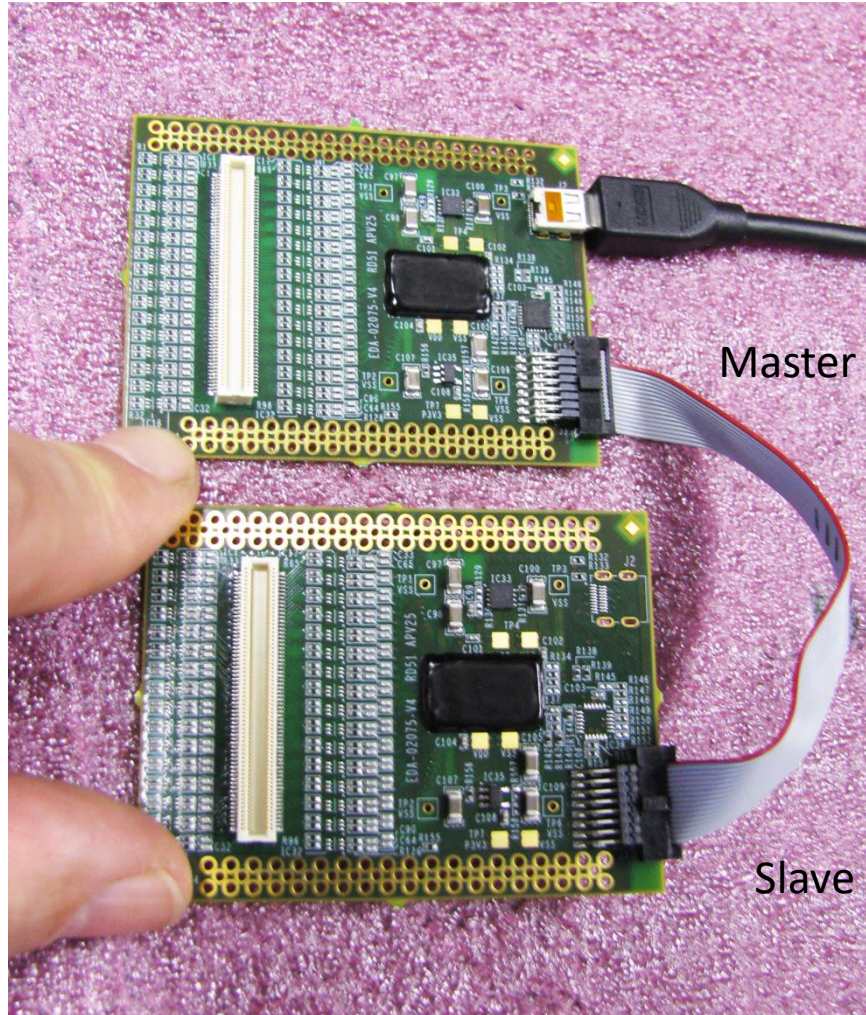
RD51 decided in December 2016 to replace the legacy Panasonic 130 pin connectors [by new 140 pin HRS FX10A connectors](#), starting with the VMM SRS hybrids and progressively implemented on the detector frames.

For a transition time, adapters between Panasonic and HRS are available.



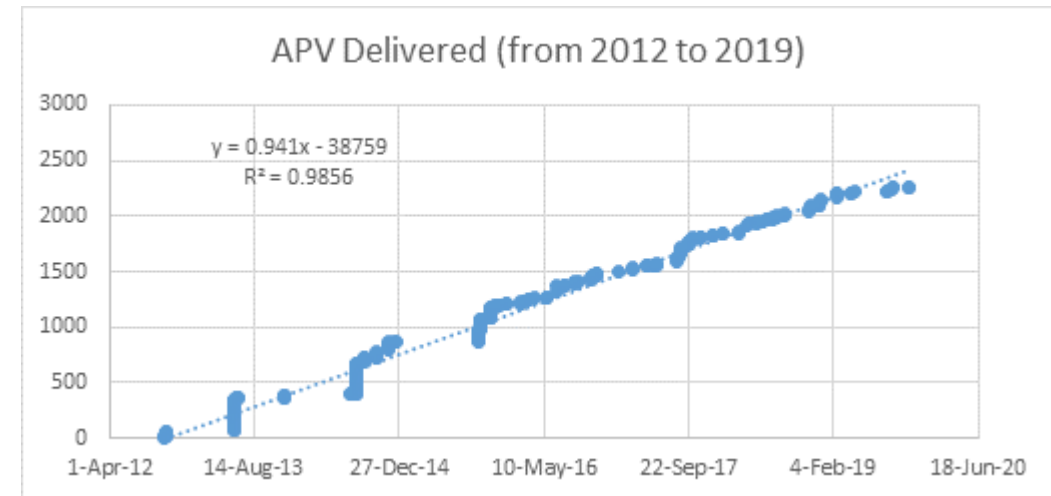
APV 128 ch frontend hybrid

Panasonic connector



SRS working-horse frontend 2011-2019
requires ADC card interface to FEC card

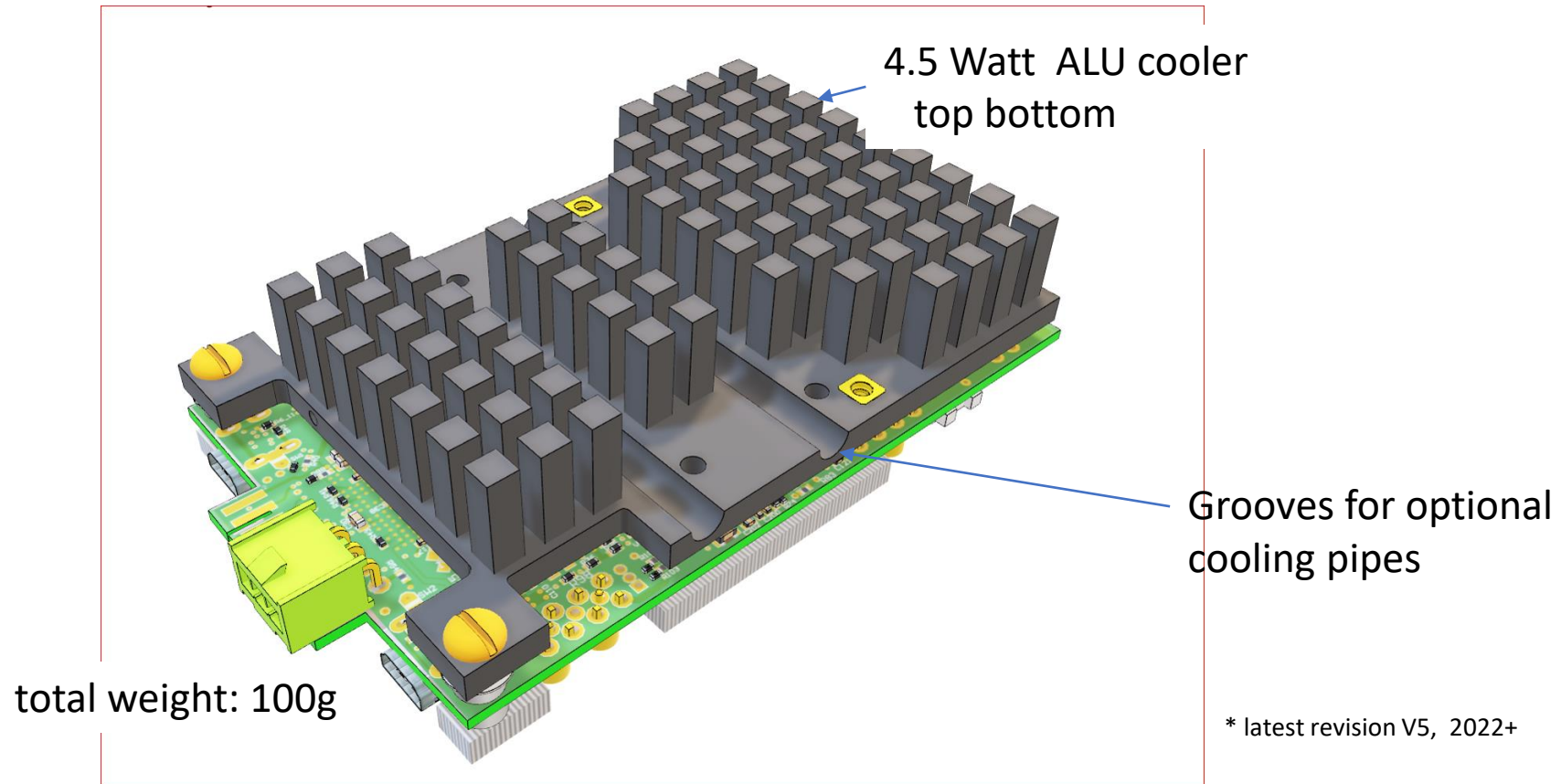
HDMI power and readout link to FEC/ADC card



APV hybrid sales via CERN store 2012-2020

ASIC carriers with cooler

[VMM hybrid for SRS*](#) , 128 channels, 2 VMM3a ASICs, 100g, 4Watt, plugs directly to a MPGD gas or photon detector with 140 pin [HRS connector](#). [Multipurpose ALU cooler](#) (convection / water pipe) to keep die temperatures below 55 C for long lifetime and low noise. HDMI readout link to DVMM card via micro HDMI-AD cable. 3-Pin AUX [power connector](#) for P1 (+3.3V) and P2 (+1.8V). [PCB Edge connector for Jtag and I2C](#). Two 3 pin connectors access to analogue VMM signals (shaper , baseline etc)



eFEC card preview

