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The advanced verification methodology in HEP

A firmware for the Central Trigger Processor (CTP) at ALICE experiment for LHC Run 3 is written in VHDL language. The most of the VHDL code was verified in a simulations using a simple procedures written also in VHDL or by writing data into file and then by checking of a data consistency in a software. In addition to the simulations also a real hardware tests were performed by a test scripts. As a classical verification methods are not providing enough completeness for all possible test cases, a new advanced verification methodology has been tested for the trigger firmware. The selected advanced verification is based on VUnit (a test framework for HDL which simplify a testbenches) and Open Source VHDL Verification Methodology (OSVVM) as it uses well know VHDL language for a hardware designers. A test cases using the Vunit and the OSVVM will be presented.

References:
https://vunit.github.io/
https://osvvm.org/

Author: KRIVDA, Marian (University of Birmingham (GB))

Presenter: KRIVDA, Marian (University of Birmingham (GB))