DRD6 WP4 electronics and DAQ

Ch. de LA TAILLE DRD6 9 April 2024

Organization for Micro-Electronics desiGn and Applications

DRD6 WP4 : Electronics and DAQ

- Goals
  - Produce ASICs and DAQ for prototypes (sizeable quantities…)
  - Avoid parallel developments but encourage communications between groups
  - Optimize commonalities (readout format, interfaces, inter-operability)
  - Organize common ASIC fabrication (share engineering run to minimize costs)

- Close communication with other DRDs
  - DRD3 : MAPS for digital calorimetry
  - DRD4 : photodetectors
  - DRD7 : electronics (ADCs, TDCs…)

- Strong interplay detector/electronics
  - Noise, granularity, timing, power dissipation, data bandwidth….
  - Detector R&D vs/with Electronics R&D

DRD6 (calorimetry) readout schemes

Name	Track	Active media	readout
LAr	2	LAr	cold/warm elx"HGCROC/CALICElike ASICs"
ScintCal	3	several	SiPM
Cryogenic DBD	3	several	TES/KID/NTL
HGCC	3	Crystal	SiPM
MaxInfo	3	Crystals	SIPM
Crilin	3	PbF2	UV-SiPM
DSC	3	PBbGlass+PbW04	SiPM
ADRIANO3	3	Heavy Glass, Plastic Scint, RPC	SIPM
FiberDR	3	Scint+Cher Fibres	PMT/SiPM,timing via CAENFERS, AARDVARC-v3,DRS
SpaCal	3	scint fibres	PMT/SiPMSPIDER ASIC for timing
Radical	3	Lyso:CE, WLS	SiPM
Grainita	3	BGO, ZnWO4	SiPM
TileHCal	3	organic scnt. tiles	SiPM
GlassScintTile	1	SciGlass	SiPM
Scint-Strip	1	Scint.Strips	SiPM
T-SDHCAL	1	GRPC	pad boards
MPGD-Calo	1	muRWELL,MMegas	pad boards(FATIC ASIC/MOSAIC)
Si-W ECAL	1	Silicon sensors	direct withdedicated ASICS (SKIROCN)
Si/GaAS-W ECAL	1	Silicon/GaAS	direct withdedicated ASICS (FLAME, FLAXE)
DECAL	1	CMOS/MAPS	Sensor=ASIC
AHCAL	1	Scint. Tiles	SiPM
MODE	4	-	-
Common RO ASIC	4	-	common R/O ASIC Si/SiPM/Lar

Trends for calorimeter readout

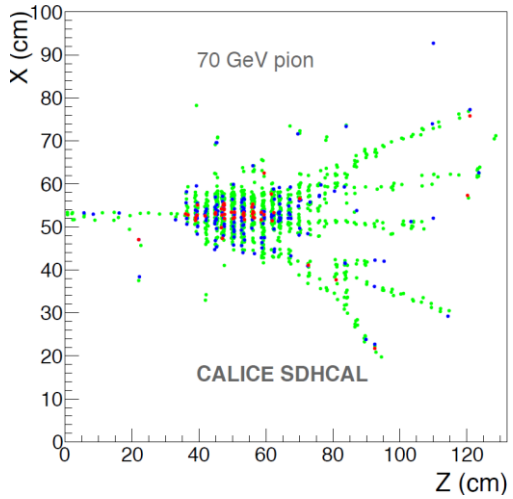
- On-detector embedded electronics, low-power multi-channel ASICs
  - CALICE SKI/SPI/HARDROC, FLAME, CMS HGCROC, FCC LAr, FATIC…
  - Challenges : #channels, low power, digital noise, data reduction
- Off-detector electronics : fiber/crystal readout
  - Wavefrom samplers : DRS, Nalu AARD, LHCb spider…
  - Challenges : low power, data reduction
- Digital calorimetry : MAPs, RPCs…
  - DECAL, ALICE FOCAL, CALICE SDHCAL
  - MAPS for em CAL : eg ALPIDE ASIC for FOCAL, DECAL…
  - Challenges : #channels, low power, data reduction

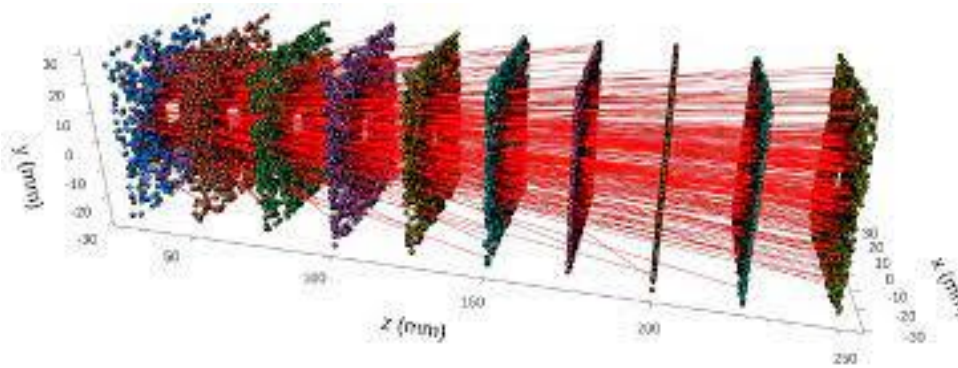
Digital calorimetry

- Hadronic : e.g. CALICE RPCs or µmegas
  - ~1 cm² pixels, low occupancy, ~1 mW/cm² (unpulsed)
  - Performance improvement with semi-digital architecture
  - Timing capability can be added

- Electromagnetic : e.g. DECAL, ALICE FOCAL…
  - Based on ALPIDE : (30µm)² pixels, high occupancy, ~ few 100 mW/cm², slow
  - To be compared with embedded electronics ~10 mW/cm²
  - Most power in digital processing => would benefit a lot from ≤ 28 nm node
  - Semi-digital and/or larger pixels couldl be an interesting study

- Upcoming R&D
  - Power reduction, dead area minimization
  - Coping with high occupancy, managing data bandwidth



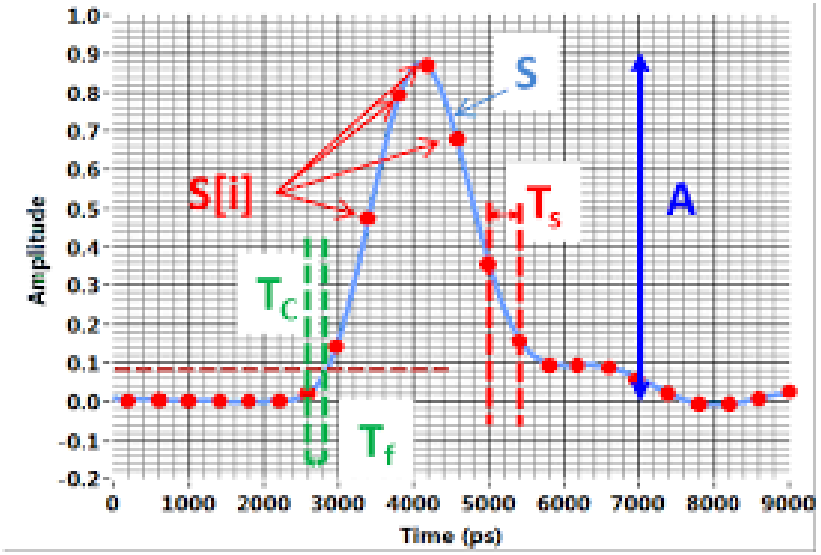


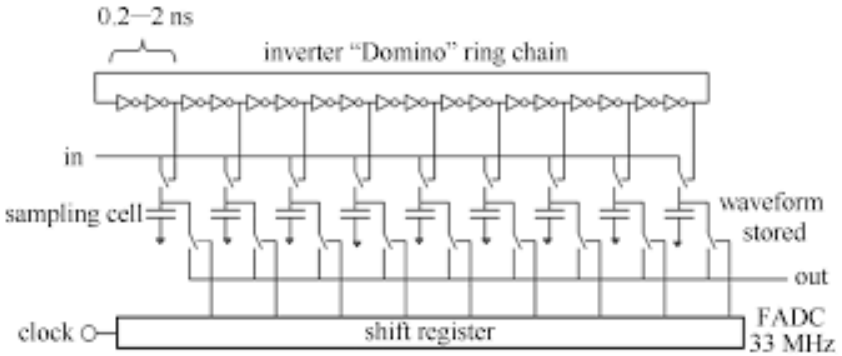
Waveform sampling

- Switched capacitor arrays (DRS4, Nalu, SPIDER…)
  - Pulse shape analysis
  - High accurcay timing, digital CFD
  - Sizeable power to provide GHz BW on large capacitance
  - large data volume

- Often used in off-detector electronics
  - Space and cooling available
  - Small/medium size detector readout and/or characterization
  - See LHCb calorimeter upgrade

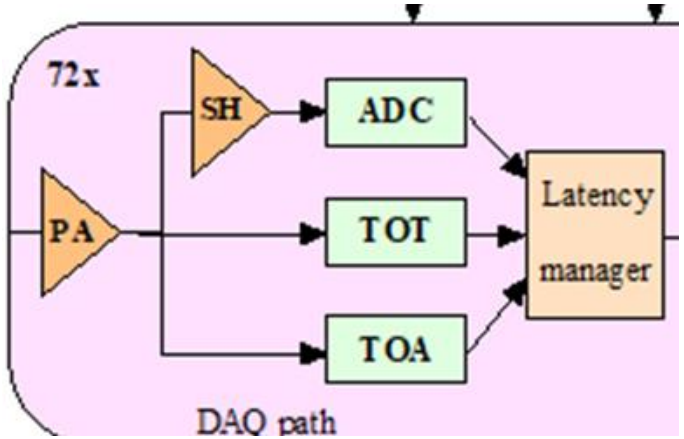
- Upcoming R&D
  - Power reduction, Front-end integration
  - Data bandwitdth
  - Time walk correction, potentially best for ps accuracy



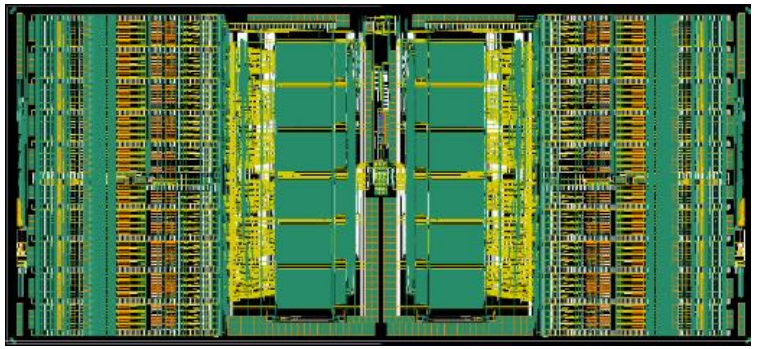


Embedded ASICs

- Pioneered with CALICE R&D (SKIROC, SPIROC..)



- Multi-channel charge/time readout
  - Fast preamp
    - Full dynamic range. Possible extension with ToT
  - Fast path for time measurement (ToA)
    - High speed discriminator and TDC
    - Time walk correction with ADC (or ToT)
  - Slow path for charge measurement
    - ~10 bit ADC ~40 MHz
  - Low power for on-detector implementation (~10 mW/ch) e.g. CMS HGCAL



- Upcoming R&D
  - Power reduction,
  - Auto-trigger, Data-driven readout

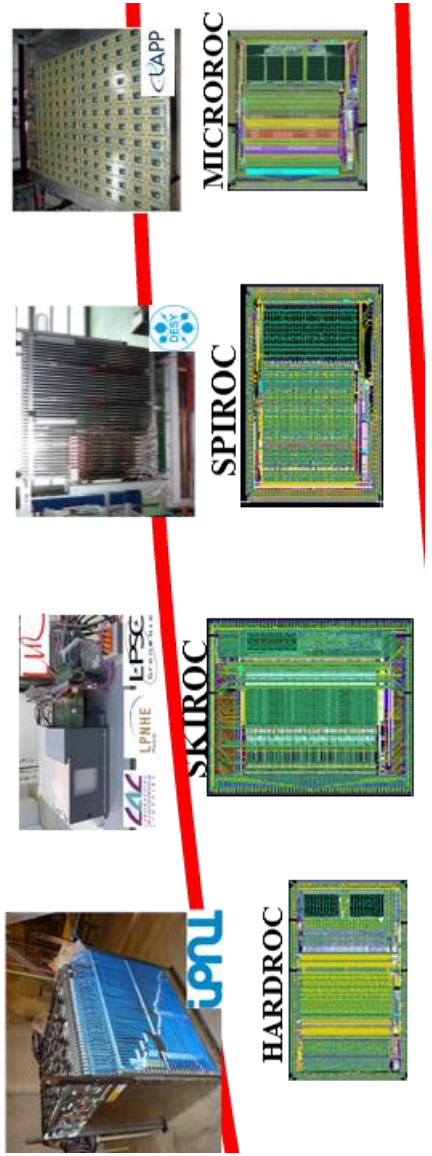
DRD6 Common readout ASICs proposal [AGH, Omega, Saclay]

- Develop readout ASIC family for DRD6 prototype characterization
  - Inspired from CALICE SKIROC/SPIROC/HARDROC/MICROROC family
  - Targeting future experiments as mentionned in ICFA document (EIC, FCC, ILC, CEPC…)
  - Addressing embedded electronics and detector/electronics coexistence
  - Detector specific front-end but common backend

  ⇒ allows common DAQ and facilitates combined testbeam

- Start from HGCROC / HKROC : Si and SiPM
  - Reduce power from 15 mW/ch to few mW/ch. Lower occupancy, slower speed
  - Allows better granularity or LAr operation
  - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
  - Extend to MCPs (PID) or HRPPD. First tests with EIC calo/PID

- Several other ASICs R/Os also developed in DRD6 and it is good !
  - FLAME/FLAXE, FATIC…
  - Waveform samplers : commercial or specific (e.g. SPIDER)
  - DECAL



Next steps

- Go over the electronics and DAQ requirements/wishes from the different participants
  - See what exists and what needs R&D
  - See what's covered internally and what can be provided by DRD6 developments

- Gather the community of « calorimeter electronics developers »
  - Share expertise and experimental results
  - Address specificities of calorimetry
  - Share fabrication (engineering) runs to equip prototypes